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Codesign of *Ka*-Band Integrated GaAs PIN Diodes Limiter and Low Noise Amplifier

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ABSTRACT In this paper, a novel concurrent design of integrated PIN-diode based limiter and low noise amplifier (LNA) is presented for *Ka*-band MMICs fabricated using a combined PIN/0.15-μm-pHEMT technology. To improve the small-signal performance and the power-handling capability of the limiter-LNA, the improvement of the PIN-limiter circuit structure and the survivability of the LNA network are proposed. In addition, the total chip area is 2.5 mm $\times$ 1.2 mm with an equalizer integrated on chip behind the limiter-LNA to improve the bandwidth with a minimum impact on overall NF. The measurements show that the proposed limiter-LNA with only two-stage limiter structure tolerates up to 38 dBm continuous wave (CW) input power without failure, and the average gain and the noise figure for the limiter-LNA are 17 dB and 2.2 – 2.6 dB, respectively, on the 30 – 38 GHz frequency bandwidth.

INDEX TERMS GaAs pHEMT, integrated limiter low noise amplifier (LNA), MMIC, noise figure (NF), PIN diode.

I. INTRODUCTION

The advancement in wireless communication technology has urged the demand of millimeter-wave integrated circuits. Limiters are usually required in the front-end module to protect active devices in the low noise amplifiers from high RF input power levels, and it should have a minimum insertion loss so as to assure the receiver's sensitivity in the receiving period simultaneously [1]. Traditionally, LNAs and limiters are usually connected externally, which not only occupy a large area but also induce high insertion loss, especially in millimeter-waveband applications. Monolithic Microwave Integrated Circuits (MMICs) based on GaAs pHEMT technology can provide the possibility of limiter-LNA integration and achieve a better performance due to the elimination of external connections and wired interconnections [2], in which Schottky diodes are commonly used for the limiter circuits due to an easy monolithic integration. It is reported a 34-36 GHz limiter with a power handling of 28.9 dBm CW power, which achieves an insertion loss of 4 dB [3]. A 20.2-20.9 GHz narrowband limiter is also presented, which has a 3-dB 90° hybrid coupler loaded by Schottky diodes for performance improvement but exhibits a high insertion loss of 5 dB [4]. Active limiters that utilize detectors and FET switches in feedback and feedforward structures are reported in [5], where the existence of detectors and biasing circuits might complicate the limiter design and enlarge the chip size. Literature [6] shows an *X*-band 10W CW broadband balanced limiter-LNA MMIC, and [7] present the integrated limiter-LNAs for *Ku*-band and 2-18 GHz applications with a maximum bearable CW power of 24 dBm and 33 dBm, respectively. A *Ka*-band Schottky-diode based limiter-LNA with the average gain and NF of 21 dB and 2.3 dB is reported in [2], which is capable of handling 2-W CW input power. [2] also reports a *Ka*-band 5-W transistor-based limiter-LNA which utilizes transistors in the limiter topology to increase the power handling of the circuit using the 0.1-μm pHEMT process. The main drawback of the Schottky-diode based limiter focus on the relatively low power-handling capability of the Schottky diodes. To overcome this problem, an effective technique would be the combination of PIN-diode and pHEMT technology in a common GaAs process [7]. It is

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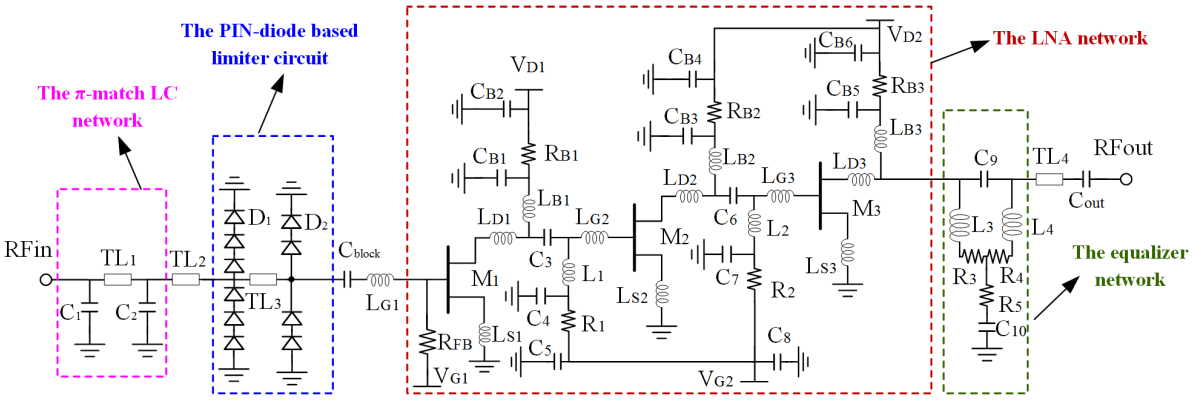

FIGURE 1. Complete schematic of the proposed PIN-diode based limiter-LNA MMIC.

reported a *Ku*-band 20 W PIN-diode based limiter with an insertion loss of 1.3 dB [1]. An *S*-band PIN-diode limiter based on standard 0.25-μm BiCMOS technology is also proposed which can handle up to 58 dBm pulses with 10-μs length and has an insertion loss of 1.0 dB [8]. A 9-16 GHz PIN-diode based limiter-LNA with 30 dBm CW power handling capability is reported in [9], where the limiter-LNA exhibits a 12 dB of gain and less than 2.2 dB of NF across the band. Recently, literature [10] presents an *X*-band balanced PIN-diode based limiter-LNA with a high power handling capability of 20W CW input power, and [11] also shows a 12-22 GHz 10W PIN-diode based limiter-LNA with a small-signal gain of 26 dB.

In this paper, we report a *Ka*-band integrated PIN-diode based limiter-LNA based on the combined PIN/0.15-μm-pHEMT technology. In order to realize both the low NF and the high power-handling capability of the limiter-LNA, the improvements of the PIN-diode limiter structure and the survivability of the LNA network are proposed. Additionally, an equalizer is integrated on chip behind the limiter-LNA to improve the bandwidth of the circuit with a minimum impact on overall NF. The rest of this paper is organized as follows. The improvements of the PIN-diode based limiter structure and the design of LNA & equalizer networks are investigated in Section II. The fabrication of the devices and circuits, the stability analysis and experimental results are demonstrated in Section III. A conclusion of this work is given in Section IV.

II. DESIGN OF THE KA-BAND LIMITER-LNA

A concurrent design of PIN-diode based limiter and LNA is critical for the performance improvement. In this paper, we propose one matching network instead of 50Ω-matching networks between the limiter and the LNA, which aims to achieve an extra loss reduction by merging two matching networks into one. The proposed *Ka*-band limiter-LNA MMIC is composed of four portions including (1) the π-match LC network, (2) the improved PIN-diode based limiter, (3) the robust common source (CS) LNA network and (4) the equalizer network, as shown in Fig. 1. The improvements of the

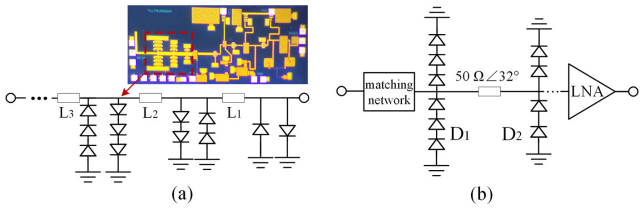

FIGURE 2. (a) Commonly used topology of PIN-diode based limiter and a die of limiter-LNA MMIC fabricated using this topology. (b) Proposed topology of two stage PIN-diode based limiter employed in this work.

Ka-band PIN-diode limiter structure and the survivability of the LNA network and the LNA & equalizer networks are investigated in the following.

A. DESIGN OF THE PIN-DIODE BASED LIMITER

PIN diode limiters exhibit relatively high power-handling capability compared with Schottky-diode counterparts. A commonly used limiter MMIC topology consists of several PIN-diode chains in antiparallel shunt configuration, the number of diodes at the input chains is N times of that at the output chains which usually use the one-PIN-diode chain [8], as shown in Fig.2 (a). It has to be mentioned that $\lambda/4$ transmission lines are widely used in most PIN limiters. However, they are not for MMIC applications due to the chip size limit. In our design, the transmission line is adjusted to be about 32° for a tradeoff between the chip size and the power handling capability. Under the condition of high-power, PIN diodes are turned on in sequence from the output chains to the input chains. As a result, a significant fraction of the input power is reflected back to the source. In addition, these PIN-diodes also absorb part of the input power, therefore reduces the output power of the limiter. Under the condition of small-signal, the off-state diodes load the RF path by their parasitics, thus, the limiter should be designed for a minimum insertion loss so as not to degrade the overall NF of the circuit. Conventionally, a number of diodes are placed in series-connection to reduce the capacitance [12], where more diodes are used at the input than those at the output in order to reduce the capacitance at the cost of increased output power. In this

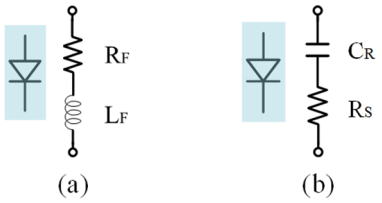

FIGURE 3. (a) The equivalent circuit of PIN diode at high power conducting state. (b) The equivalent circuit of PIN diode at low-level receive state.

paper, two-stage PIN-limiter topology is proposed as shown in Fig. 2(b). Different from conventional ones in Fig. 2(a), we remove one-PIN-diode chain adjacent to the LNA to achieve a lower insert loss and a smaller chip area. In order to deal with the high input power from the limiter to the LNA network, a resistance R_{FB} is employed as a negative feedback in the gate-bias circuit of the first stage of LNA, which can reduce the gate voltage of the transistor M_1 as shown in Fig.1. Fabrications of the limiter-LNA MMIC by using either the PIN-diode topology in Fig.2 (a) or that in Fig. 2(b) have been done and both dies are shown in the insert of Fig.2 (a) and Fig. 6, respectively. Measurements show that the improved limiter-LNA MMIC exhibits the overall NF decreasing by 0.3 dB - 0.35 dB, and the chip area decreasing by 0.4 mm^2, respectively, with the same power-handling capability.

The requirements of the PIN devices are discussed in the following. Under the condition of high-power, the junction capacitance of PIN diode is essentially shorted out and the equivalent circuit of the diode is depicted in Fig. 3 (a). The conducting resistance R_F is as low as one or two ohms due to an increase of the density of charge carriers in the I region of the diode. The turned-on PIN diodes can reflect a significant fraction of the incident power back to the source. However, the resistor R_F and the rectifying action of the ideal diodes also lead to a large current through the diodes. Based on the maximum input power P_{MAX} from a source with a characteristic impedance of Z_0 that the limiter has to be able to withstand, the maximum peak current I_P is derived as [8]

$$I_P = 2\sqrt{2}\frac{\sqrt{P_{MAX}\Re(Z_0)}}{|Z_0|}. \tag{1}$$

Assuming the diodes is an ideal short circuit and $Z_0 = 50\ \Omega$, an upper bound of the maximum peak current I_P through the diodes can be approximated as

$$I_P \approx \frac{2}{5}\sqrt{P_{MAX}}. \tag{2}$$

Under the CW power of 5W, the diodes must be able to draw a peak current of 0.89 A without failing. Therefore, PIN diodes with diameters of 100-μm are adopted in the first stage to handle at least 37 dBm of input power. Additionally, the second stage uses the medium-size PIN diode D_2 with the diameter of 50-μm. The leakage power of the second limiter stage is approximate 22 dBm at 35 GHz, which is obtained through the measurements of the individually manufactured limiter with the same structure.

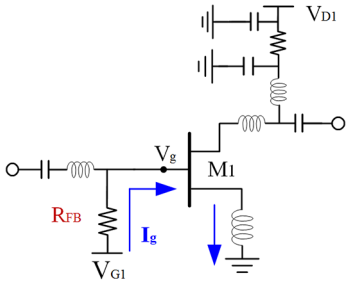

FIGURE 4. Simplified schematic of the first stage of LNA.

At the small-signal level, the equivalent circuit of the PIN diode can be approximated configured by C_R in series with R_S, as shown in Fig.3 (b). The major source of insertion loss in a limiter circuit is the off-state capacitance of the PIN diodes. The parasitic capacitance C_R can be involved in the matching network of limiter-LNA to mitigate the loss.

B. DESIGN OF THE LNA & EQUALIZER NETWORKS

Survivability, NF, bandwidth, gain and gain-flatness are the most important characteristics to be considered in the design of limiter-LNAs. In order to achieve a total gain of higher than 16 dB, a three-stage CS LNA topology with inductive degeneration is introduced in this design. For GaAs-based LNA, the maximum of RF CW power it can withstand is typically 18 - 20 dBm. Among all the factors causing stress to the device, such as the total dissipated power, the dc forward gate current, the gate and drain breakdown, it is demonstrated that the dc forward gate current is the most severe threat to device lifetime [13]. When the excess forward gate current flows to the gate to source junction, the pHEMT device is damaged in the Schottky contact region [14]. It has been reported that large size transistors and the topology of stacked transistors have been employed in the first stage of LNAs to realize a high survivability [14], [15]. However, these approaches inevitably introduce more noise, especially for LNAs operating in millimeter-waveband. Besides, these approaches also result in an increase of power consumption. In this limiter-LNA, a series resistance R_{FB} is employed in the gate-bias circuit to improve the ruggedness of LNA network, as shown in Fig. 4. It makes the LNA network to withstand the leakage power of ~22 dBm from the last stage of limiter. Under the condition of high-power, as the input power of the LNA increases up to a certain point, a dc gate current caused by turn-on of the gate diode will be drawn from the gate bias supply [13]. The series resistance R_{FB} (see Fig. 4) is employed as a negative feedback, which aims to reduce the gate bias voltage (V_g) by a voltage drop of $R_{FB} \times I_g$, where I_g is the forward gate current. Simulation in Fig. 5(a) shows that an increased R_{FB} leads to a decrease in the slope of I_g. Therefore, this feedback in turn reduces the positive peak voltage to values below threshold. It has to be mentioned that for the ~22 dBm leakage power from the PIN limiter, the gate voltage decrease little as R_{FB} increases (when $R_{FB} > 1$ kΩ from simulations). Additionally, NFs of the

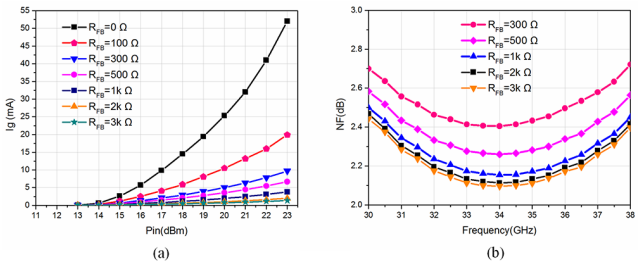

FIGURE 5. (a) Simulated gate current of the first stage of LNA as a function of the input power at 35 GHz. (b) Simulated NF of the limiter-LNA as a function of the series resistance R_{FB} at 35 GHz.

circuits with different R_{FB} are simulated at the schematic level, because R_{FB} is located in the gate bias circuit of the first stage of the LNA network. The simulation result in Fig.5(b) indicates that NF decreases from 2.7 dB to 2.4 dB when R_{FB} changes from 300 Ω to 3 kΩ, where it decreases very little when R_{FB} changes from 1 kΩ to 3 kΩ. Therefore, it is hoped to set R_{FB} to be more than 1 kΩ in the design.

To improve the overall NF, several methods have been applied to the LNA network. Firstly, the gate-width of the first-stage transistor M_1 and the source degeneration inductance L_{S1} are optimized to 4×38 μm and 76 pH, respectively, to improve both the noise performance and the input matching. The leakage power of the limiter cannot cause stress to the first-stage transistor with such a small size due to the improved survivability of the LNA network. This technique makes it possible to optimize the gate-width of the first-stage transistor to improve the noise performance. The gate voltages of M_2 - M_3 are set to be -0.4 V, while that of M_1 is modified from -0.4 V to -0.35 V to increase the gain of this stage and reduce the noise contribution of subsequent stages in overall NF [16]. For multi-stage amplifiers, shunt feedback is usually adopted to enhance the bandwidth and the gain flatness by decreasing low-frequency gain response [17]–[20]. Unlike the commonly used method, in our design, an equalizer is integrated behind the LNA network to improve the gain flatness and the bandwidth of the limiter-LNA with the advantage of adding rarely noise to the total circuit, as illustrated in Fig. 1 enclosed by dash line.

The gate breakdown of M_1 should be considered due to the large negative peak voltage caused by the resistance R_{FB}. It is known that the gate-source diode of M_1 is considered as a conventional Schottky-diode [21]. And the gate voltage of M_1 was estimated to be a safe value through both the simulations and the measurements. Table 1 shows the measured bias voltage (V_{gs}) of M_1, where V_{gs} is about -3.7 V when R_{FB} is 1 kΩ for 38 dBm-input-power at 35 GHz. It also indicates that V_{gs} decreases little while the R_{FB} alters rapidly from 1 kΩ to 6 kΩ. As indicated by Table 1, the whole gate-voltage swing is almost kept at negative values for R_{FB} of 6 kΩ, hence, the maximum negative voltage swing at the gate does not exceed about -8 V (instantaneous value). And the dc measurement of the gate-current as a function of gate-source voltage shows that the dc gate breakdown occurs at

TABLE 1. The measured V_{gs} for different R_{FB}.

R_{FB}	1 kΩ	2 kΩ	4 kΩ	6 kΩ
V_{gs}	-3.7 V	-3.8 V	-3.9 V	-3.9 V

V_{gs} is measured at the input power of 38 dBm at 35 GHz.

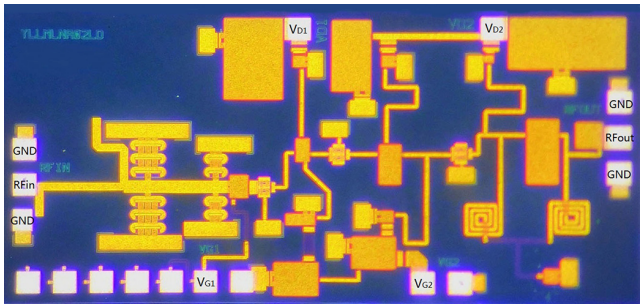

FIGURE 6. Die photograph of the proposed limiter-LNA.

$V_{GS} = -11$ V (gate-current is 1mA/mm). Therefore, the maximum negative voltage swing at the gate cannot cause stress to the device. Besides, R_{FB} and the gate capacitor C_{gs} of M_1 compose an R-C time constant, thus, the value of R_{FB} is set to be 1 kΩ to obtain a short recovery time with decreased I_g.

III. CIRCUIT FABRICATION AND EXPERIMENT RESULTS

A. FABRICATION OF DEVICE AND CIRCUIT

The fabrication for the PIN/pHEMT devices is performed using a selective epitaxial growth technique on 4-inch GaAs substrates. The epitaxial structure for PIN diode is first grown and followed by process definition of the PIN diode and pHEMT active regions. A second epitaxial growth of pHEMT material is done and the complete PIN/pHEMT process follows using the merged process which consists of the 0.15-μm pHEMT process, the base mesa and the ohmic-contact steps necessary to create the limiters. For PIN-diodes, both the insertion loss and the maximum working frequency are a function of the parasitic capacitance that is proportional to the diode area. Meanwhile, it has been reported that the power-handling capability of a GaAs PIN-diode is proportional to its perimeter [12]. In order to reduce the insertion loss and increase the bandwidth of the limiter, we adopt an oval-shape diode geometry for the larger sized PIN diode, which can reduce the diode area of more than 50% compared with the round diode of equivalent perimeter [22].The integrated two-stage PIN-diode based limiter, three-stage LNA and an equalizer is designed and implemented by using the combined PIN/0.15-μm-pHEMT technology. Fig. 6 shows the die photograph of the fabricated limiter-LNA with chip area of 2.5 mm×1.2 mm including input/output pads. PIN-diodes D_1 and D_2 have the diameters of 100 - μm and 50 - μm, respectively. Transistors M_1-M_3 have equal size of 4×38 μm. The optimization of all component parameters is

TABLE 2. Values of components used in the limiter-LNA.

Capacitors(pF)	Capacitors(pF)	Inductors(pH)	Inductors(pH)	Resistors(Ω)	T-Lines(Z/θ°)
C_1=0.02	C_{10}=0.67	L_{G1}=73	L_{B1}=249	R_{FB}=1000	TL_1=60 Ω ∠38°
C_2=0.07	C_{block}=2.8	L_{G2}=68	L_{B2}=720	R_{B1}=8.5	TL_2=50 Ω ∠10°
C_3=1.26	C_{out}=4.80	L_{G3}=71	L_{B3}=577	R_{B2}=8.5	TL_3=50 Ω ∠32°
C_4=0.68	C_{B1}=0.64	L_{S1}=76	L_1=225	R_{B3}=8.5	TL_4=80 Ω ∠12°
C_5=5.79	C_{B2}=5.79	L_{S2}=24	L_2=390	R_1=70	
C_6=1.80	C_{B3}=0.44	L_{S3}=11	L_3=910	R_2=54	
C_7=0.66	C_{B4}=5.79	L_{D1}=180	L_4=910	R_3=445	
C_8=5.79	C_{B5}=0.66	L_{D2}=92		R_4=445	
C_9=4.08	C_{B6}=5.79	L_{D3}=94		R_5=1056	

θ is reported at 35 GHz

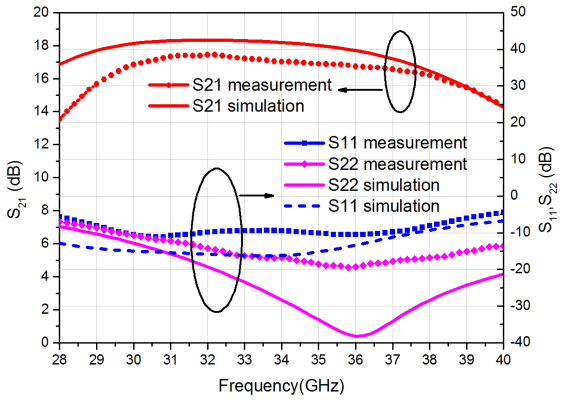

FIGURE 7. Simulated and measured S-parameters of the limiter-LNA.

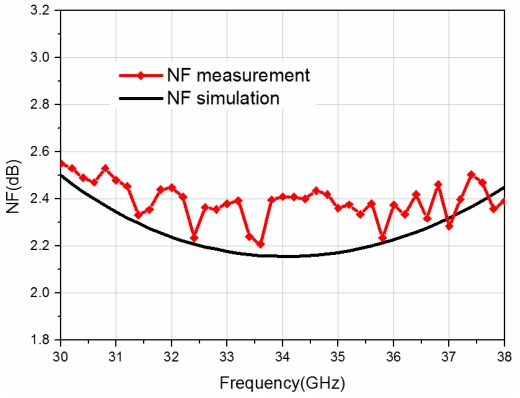

FIGURE 8. Simulated and measured NF of the limiter-LNA.

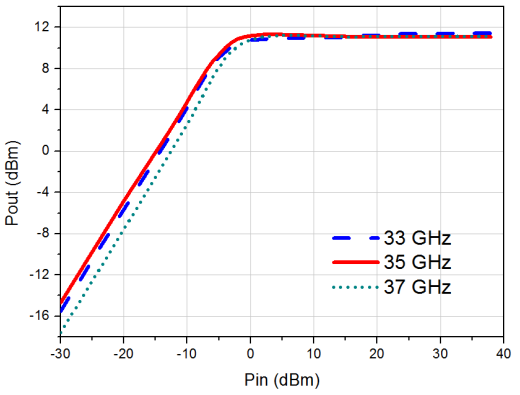

FIGURE 9. Output power of the limiter-LNA in terms of input power.

targeted to get optimized overall circuit performance and the final design parameters are listed in Table 2.

B. STABILITY ANALYSIS

To enhance the circuit stability, several methods are adopted. The source degeneration inductors $L_{S1} \sim L_{S3}$ are employed into each stage to further enhance the stability [23], as illustrated in Fig. 1. Additionally, the equalizer which is employed behind the LNA can significantly enhance the circuit stability, as illustrated in Fig. 1 enclosed by dash line. Moreover, resistors $R_{B1} \sim R_{B3}$ are introduced into the drain bias circuits of each stage to reduce the Q factor of the matching circuit, avoiding unwanted resonances caused by the microstrip lines, parasitic inductance of the VIA holes and the MIM capacitor. And the circuit stability is also improved by the resistors $R_1 \sim R_3$ and R_{FB} which are added in the gate bias circuits of the LNA. Meanwhile, the simulation results indicate that both the coefficients k and μ are larger than 1 from dc to the cut-off frequency, which proves that unconditional stability is achieved both within and outside the bandwidth.

C. EXPERIMENT RESULTS

The on-wafer S-parameters and noise performance was measured with a KEYSIGHT N5245A PNA-X at room temperature. The LNA is biased at $V_{G1} = -0.35$ V, $V_{G2} = -0.4$ V and $V_{D1} = V_{D2} = 2$ V. The whole chip draws 38 mA from the power supply, resulting in a power consumption of 76 mW. The measured and simulated S-parameters of the limiter-LNA are shown in Fig. 7, while NF results are shown in Fig. 8. Over the 30-38 GHz band, the measured average small-signal gain is 17 dB with gain flatness of ± 0.6 dB. And the input and output return losses better than −8 dB and −10 dB, respectively. The Rollet stability factor calculated from the measured-parameters shows that the limiter-LNA is unconditionally stable both within and outside the bandwidth. The measured NF ranges from 2.2 dB to 2.6 dB across the bandwidth. To characterize the power-handling capability of

TABLE 3. Performance comparison.

Ref.	Technology	Topology	Frequency (GHz)	CW Power(dBm)	Gain (dB)	NF (dB)	Chip size(mm^2)
[1]	PIN Diode	Diode-limiter	*Ku-band*	40[a]	-1.3	1.3	-
[2]	0.1-μm GaAs pHEMT	Schottky-Diode-Limiter/LNA	28-38	33	21	<2.9	2.6×1.3
		Transistor-Limiter/LNA	30-38	37	18	<2.9	2.6×1.3
[3]	Schottky Diode	Diode-Limiter	34-36	28.9	-4	4	-
[4]	Alumina	90° Hybrid Coupler	20.2-20.9	15	-5	5	-
[6]	MESFET process	Schottky-Diode balanced limiter/LNA	8.5-11.5	40	>14	<2.7	3.6×4.0
[9]	PIN/HEMT process	Balanced amplifier	9-16	30	12	<2.2	3.8×3.2
[10]	PIN/pHEMT process	PIN-Diode balanced Limiter/LNA	8-12	43	>24	<1.8	3.2×2.4
[11]	PIN/pHEMT process	PIN-Diode-Limiter/LNA	12-22	40	26	<2.7	3.0×1.1
[24]	GaN	Diode-Limiter/LNA	8-12	36	14	1.6-1.8	3.0×2.0
		Transistor-Limiter/LNA	7-11	40	18	2.0	3.0×2.0
This work	PIN/0.15-μm pHEMT process	PIN-Diode-Limiter/LNA	30-38	38	17	<2.6	2.5×1.2

[a] pulse input power.

the limiter-LNA, the die was attached using gold-tin (AuSn) solder on a Copper-Molly carrier plate for maximum heat conduction. The plate is inserted into a copper carrier with high-frequency SMA connectors. The signal and bias bond pads were bonded to printed circuit board traces using 25-μm diameter gold bond wires. The insert loss introduced by each high-frequency SMA connector is 0.6 dB in the input and output RF path, which is considered and extracted in the final power- handing results of the limiter-LNA. In order to measure the survivability of the circuit, a power amplifier was used before the limiter-LNA under test and a −10 dB coupler is adopted behind the power amplifier to ensure accurate input-power to the limiter-LNA. The output-power of the limiter-LNA is measured by an Agilent N1912A power meter. The input power was increased from low powers (−30 dBm) to high powers, the S-parameters and NF are measured before and after 30-minutes exposure. The limiter-LNA is able to handle at least 38 dBm of CW input power at 35 GHz without failing. The input power versus output power data is shown in Fig.9. The performance comparison between this limiter-LNA and similar works is summarized in Table 3. Compared with reported Ka-band limiter/LNAs this limiter-LNA demonstrates excellent performance including lower NF, higher tolerable power, comparable gain and smaller chip area. Moreover, the power-handling capability of the limiter-LNA can be further improved by using larger size PIN-diodes in the first stage of the limiter and the design techniques proposed in this paper can be further applied in the limiter-LNA circuits.

IV. CONCLUSION

Design procedures for codesign of integrated PIN-diode based limiter-LNAs are presented in a PIN/0.15-μm pHEMT technology. The improvements of the PIN-diode limiter structure and the survivability of the LNA network are proposed to realize both the low NF and the high power-handling capability of the circuit. The measurement results show that the limiter-LNA tolerates the CW input power of 38 dBm with only two PIN limiter stages. The overall NF of the limiter-LNA is <2.6 dB over the 30 GHz - 38 GHz bandwidth, while the average small-signal gain is 17 dB. This proposed PIN-diode based limiter-LNA can be further applied to millimeter-wave frond-end systems due to its excellent performance.

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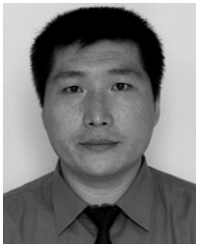

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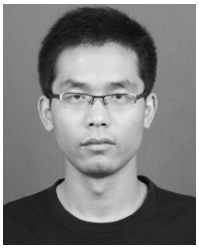

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