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Power Loss Model and Efficiency Analysis of Three-Phase Inverter Based on SiC MOSFETs for PV Applications

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ABSTRACT This paper presents the power loss model analysis and efficiency of three-level neutral-point-clamped (3L-NPC) inverter that is widely employed in solar photovoltaic energy conversion system. A silicon carbide (SiC) 3L-NPC inverter is developed in this paper by employing wide bandgap semiconductor power devices, such as SiC MOSFET and SiC diode (SiC D). These devices are used due to their superior characteristics over silicon (Si) semiconductor devices for the reduction of inverter power losses, and as a result, an improving efficiency at the high switching frequency. Accurate and detailed power loss calculation formula and power loss distribution over switching devices of the SiC 3L-NPC inverter are derived according to the modulation technique and inverter operation. The switching energy loss of SiC MOSFET is then measured and determined experimentally via inductive clamp double pulse test (DPT) at the real working condition of the circuit. Afterward, this experimental data is used in the thermal description file of the device's library of PLECS simulation software to determine the total power loss of SiC 3L-NPC inverter. The developed simulation model replicates the real operating conditions of the 3L-NPC inverter. This method gives results close to the practical test. Finally, the power loss of SiC 3L-NPC inverter is measured and compared with the theoretical results. Furthermore, SiC MOSFET and SiC D are employed to achieve high system efficiency at the high switching frequency. The results verify the features of SiC 3L-NPC inverter, the corresponding modulation technique used and their effects on reducing and improving power loss in solar SiC photovoltaic inverters.

INDEX TERMS Three-level neutral-point clamped inverter (3L-NPC), SiC MOSFET, power loss, DPT-double pulse test, PLECS.

I. INTRODUCTION

The penetration of solar photovoltaic (PV) energy has led to massive research in the areas of solar energy harvesting. To increase the efficient generation of solar energy, silicon carbide semiconductors power devices are playing an essential role in power electronics technology because of its excellent material properties when compared to traditional silicon semiconductors power devices. The PV inverter is one of the main components of solar photovoltaic conversion system, whose performance depends on the efficient topology and modulation technique applied. The power loss in the conversion system should be minimized as much as possible by selecting proper semiconductor devices of advanced high-voltage, high-operating frequency and high-temperature semiconductor materials, such as SiC. This is to achieve a high-efficiency and maximum power from the solar photovoltaic generation. The performance improvements are based on superior material properties of SiC such as thermal conductivity, wide band gap, saturated drift velocity and critical breakdown field [1], [2].

The SiC-technology is considered as a promising new solution for fabricating power switching devices. This is due to the capability of the SiC MOSFET to push up the maximum

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junction-temperature and breakdown-voltage levels over the normal Si limits. The SiC material also sustains higher temperature levels than the traditional Si. This features make the equipment designed using SiC work at high temperature [3]. Moreover, the SiC has smaller size and width of space charge compared to the Si switching devices.

In addition to the previous benefits, the SiC switching devices are superior in terms of thermal conductivity, which is higher than that of their rivals. This feature of SiC leads to a scaling down of the cooling system size. However, SiC devices has several challenges, such as high cost, low voltage and current ratings as compared to Si devices and the oscillation behavior challenges. SiC switching devices are, however, expected to become less expensive in the forthcoming decade.

The aforementioned properties and benefits of SiC indicate the importance, benefits and impact of using silicon carbide semiconductor technology in a solar photovoltaic generation application. In recent years, renewable energy sources such as photovoltaic systems and wind turbines have become increasingly used. That is why the multilevel converters are growing fast nowadays, which are needed in industry and solar energy conversion system [4].

These multilevel converters can be classified according to voltage operation as high voltage, medium voltage, and low voltage converters. The medium voltage converters could operate with high efficiency under lower switching frequency in order to reduce the switching losses [2]. The calculation and analysis of power losses in multilevel converters are very important in determining and improving the efficiency of power converter. Every year, the prices of SiC semiconductor devices, including SiC diode and SiC MOSFET are becoming lower than the previous year. This feature and other technical features which previously mentioned, made SiC semiconductor devices to replace Si semiconductor devices for the PV inverter conversion system [5]. The Voltage Oscillations in SiC MOSFET is studied in [6] based on half bridge converter to achieve high power density for converter. A 60-KW T-type SiC photovoltaic inverter is presented in [7], and it is found that the SiC devices have achieved better utilization than traditional three-level T-type LCL topology when operating at a higher switching frequency. The LCL filter components are calculated to design the filter and reduce the noise of SiC devices in [8]. Comparison of SiC MOSFET and Si IGBT power modules in photovoltaic DC/AC inverters based on the electro-thermal have been studied in [9]. By comparing and analyzing various types of PV inverter system, it is simply noted that the application of SiC power semiconductor devices is very useful in eliminating power loss and improving efficiency. This is due to the superior material of silicon carbide compared to silicon. At higher switching frequency applications, the multilevel converter topologies have a lower total harmonic distortion (THD) factor than two-level converters [10]. Furthermore, a simple technique is developed in [11] to reduce THD and improve efficiency based on SIC semiconductor power devices.

The main advantage of multilevel inverters is that, the semiconductor switching devices are commutating with only the part of DC link voltage. For instance, in the three-level inverter, each switching device can switch only half the DC link voltage, whereas, in a conventional two-level inverter, each switching device switches the full DC link voltage. This directly leads to reduced switching power losses for the three-level inverter at high or any given switching frequency. Nevertheless, total semiconductor power losses in a two-level inverter can still be lower compared to a three-level inverter if the switching frequency is low enough. Hence, the operating condition becomes a crucial aspect when comparing topologies.

For instance, in [12], the two-level and the three-level NPC converter is compared in terms of semiconductor power losses, reliability, filter aspects and cost. It is found that the staircase voltage at the NPC converter output terminals and hence the reduced harmonic contents directly leads to a smaller AC filter size. The size reduction of the AC filter and the lower heat sink required for a three-level inverter (because of the reduced switching losses) lead to an expensive or a cheaper PV inverter despite the fact that the power semiconductor count is higher.

A similar comparison is carried out in [13], in which a two-level inverter is evaluated with the three-level NPC and the three-level T-Type inverters. The T-Type structure is a derivation of the NPC, achieving the same output performance at reduced semiconductor count [13].

As described in [12], the three-level inverters can outperform the two-level inverter at increased switching frequencies, not only in power losses but also in prices. For residential PV systems, the switching frequency is usually set between 16 kHz and 48 kHz with around 20 kHz as a good compromise between switching power losses and the filter size [14]. In [15], two-level and three-level inverter constellations is evaluated based on their leakage currents, which is a major concern in transformer-less PV systems, and found out that the Common Mode (CM) voltage is larger for the Full-Bridge structure in comparison with NPC.

Within the three-level inverter topologies, as shown in [13], the three-level T-Type structure can achieve lower semiconductor power losses compared to its NPC alternative at low and medium switching frequencies. This is due to the fact that NPC inverter has relatively large conduction power losses as always two semiconductor devices conduct the load current [16]. This also can lead to an uneven power loss distribution among the semiconductor devices [17]. While this can be solved in an Active Neutral-Point-Clamped (ANPC) [18], which the clamping diodes can be replaced by using switching elements. The T-Type inverter shows higher total semiconductor power losses above a certain switching frequency compared to the NPC because of the relatively large switching power losses in the outer DC bus connecting switches.

The transformer-less photovoltaic systems nowadays are becoming proffered for use in the low voltage applications such as the residential sector, due to their low cost, high

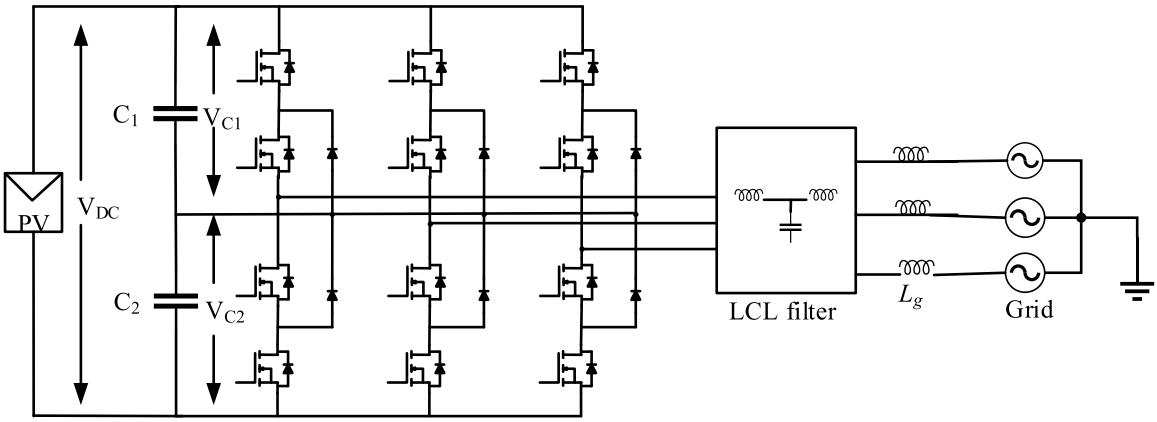


FIGURE 1. Circuit topology of three-phase SiC 3L-NPC PV inverter.

efficiency, and small size [15]. For improved efficiency and lower cost for PV inverter systems, previous researches have studied and investigated the tradeoffs between three- and two-level PV inverters. By increasing the switching frequency, it is found that the three-level PV inverters have lower total semiconductor power loss compared to the two-level inverters, as well as allowing a significant size reduction in AC filter design [12], [13]. The high efficiency of a simulation-based three-level inverter using SiC MOSFET is discussed in [19], but the device losses are not validated through experimentation. Thermal loss of low voltage-SiC-IGBT device-based power inverter is presented in the literature [20], [21].

This paper focuses on the efficiency and extensive power loss analysis in a three-level neutral-point clamped inverter based on 1.2 kV/19A SiC MOSFET at a high switching frequency of 100 kHz, which can be used for solar photovoltaic application. The losses derivation of SiC MOSFET and SiC diode semiconductor devices used in the three-phase SiC 3L-NPC inverter are presented in details. These losses are used in simulating the power losses, which are switching and conduction losses. Additionally, a SiC 3L-NPC inverter is developed to achieve high-efficiency work by using SiC-MOSFET based power electronics new technology in the PV energy conversion system. Experimental results of SiC MOSFET switching energies are obtained using clamped inductive switching waveform test circuit for silicon carbide power MOSFET C2M0160120D manufactured by CREE, which is used in the developed model of SiC 3L-NPC inverter. The thermal modeling description of the semiconductor device is obtained using the extracted parameters from their datasheets and those of the measured power losses from experiment and simulation results of the presented models.

The main contributions of this work could be summarized as:

- Comprehensive power loss analysis and identification of major loss contributors within 3L-NPC inverter topology.
- Evaluation of the use benefits of SiC switching devices in 3L-NPC structure.
- A thorough investigation of the 3L-Neutral-Point-Clamped (3L-NPC) topology based on Silicon Carbide. semiconductor switching devices.
- The alternative methodology of SiC MOSFET power loss model validation by experimental results.
- Operation of SiC MOSFET at high switching frequency and low power losses.
- Development SiC 3L-NPC inverter by employing wide bandgap semiconductor power devices such as SiC MOSFET.

This kind of power loss simulation model can be suggested for research as an applicable replacement for measuring devices which are very expensive.

II. POWER LOSSES MODELING OF SiC 3L-NPC INVERTER

This section describes the modeling and calculation of SiC 3L-NPC inverter according to the clamped inductive switching waveform test. The power loss is the most important calculation in any converter efficiency calculation. The highest power loss in this converter happens in the MOSFET. The high-power dissipation in the MOSFET occurs because it handles the switching processes. Besides inverter efficiency, it is important to know the power loss and dissipated heat in order to design the proper heat sink or ventilation fan if needed.

A. OVERVIEW OF SiC 3L-NPC INVERTER

A SiC 3L-NPC inverter topology is built in this paper. LCL filter is often used to interconnect inverter to the utility grid as an interface device to filter the harmonics produced by the inverter. The complete system block diagram of SiC 3L-NPC inverter for PV application is shown in Figure 1 and the parameters of the system are shown in Table 1. This paper mainly focuses on the modeling and calculation of total power loss of the SiC 3L-NPC inverter that can be used for PV application.

By using SiC MOSFET in this inverter, the efficiency is improved. This is due to the superior characteristics of the SiC MOSFET.

TABLE 1. System parameters.

Unit	Quantity	value
V	Input DC voltage	800
kW	Output power	12
kHz	Switching frequency of the inverter	100
V	Grid voltage ($V_{g\text{-}rms}$)	230
mH	Grid inductance (L_g)	1
Hz	system frequency	50
SPWM	Modulation	

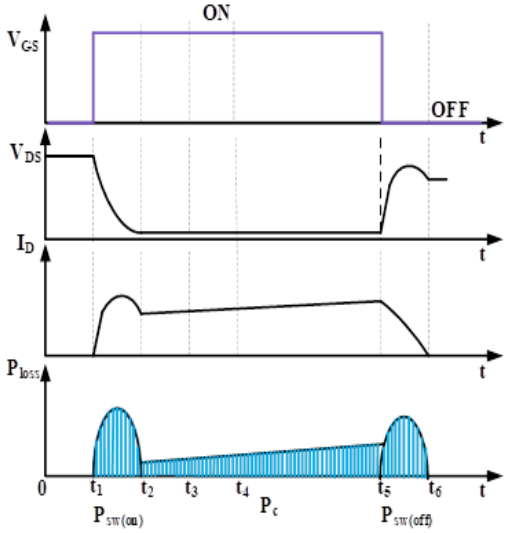


FIGURE 2. Power losses transition waveforms of SiC -MOSFET.

B. SiC SEMICONDUCTOR DEVICE POWER LOSS ANALYSIS

Generally, power losses in power semiconductor switches are divided into two groups, namely; static loss, and dynamic loss. The static loss includes conduction loss (On-state power losses) and cut-off loss, while the dynamic loss includes turn-on and turn-off loss. The most essential losses that must be calculated in the SiC MOSFET are the switching loss and conductions loss. However, the cut-off loss is neglected due to SiC device leakage current being negligible. Figure 2 shows the power losses transition waveforms of SiC -MOSFET, including conduction loss (P_c), turn-on loss ($P_{sw(on)}$) and turn-off loss ($P_{sw(off)}$).

1) CONDUCTION POWER LOSS

The conduction loss happens due to SiC MOSFET's resistive parameters when it is ON. When the current flows through dynamic on-resistance $R_{DS(on)}$, the power is dissipated as heat from the MOSFET. The physical size also plays a role in the conduction loss. This is because, increasing the physical size will decrease the $R_{DS(on)}$, and hence, it will decrease the loss.

Thus, the conduction loss of the SiC MOSFET $P_{c(MOSFET)}$ can be expressed mathematically as:

$$P_{c(MOSFET)} = \int_{t_2}^{t_5} I_{rms}^2 \cdot R_{DS(\text{on})} dt \tag{1}$$

However, the frequency affects the conduction loss, thus the conduction loss can be multiplied by frequency:

$$P_{c(\text{MOSFET})} = f_{sw} \int_{t_2}^{t_5} I_{rms}^2 \cdot R_{DS(\text{on})} dt \tag{2}$$

The conduction loss of a SiC power Schottky diode $P_{c(diode)}$ can be also calculated based on their dynamic on resistance ($R_{on(Diode)}$) as follows:

$$P_{c(\text{Diode})} = f_{sw} \int_{t_2}^{t_5} I_{rms}^2 \cdot R_{\text{on,(Diode)}} dt \tag{3}$$

where I_{rms} is the SiC MOSFET conduction current root mean square (RMS) value; f_{sw} is the switching frequency. For SiC MOSFET and SiC Diode, only their on-resistance $R_{DS(on)}$ and $R_{on(Diode)}$ are needed to find conduction losses.

2) SWITCHING ENERGIES LOSS

The switching loss of the SiC semiconductor devices represent the energy losses and it is classified as a dynamic loss. The switching loss occurs when the switch of SiC device turn-on and off (switching transient). These losses depend on the switching frequency, the current through switch and voltage across it [22]. Switching energy loss reduction in SiC devices using a novel series hybrid switching technique is presented in [23]. Switching energy loss reduction in SiC devices using a novel series hybrid switching technique is presented in [23]. The physical size of the MOSFET plays a role in switching loss. The increase MOSFET size will increase its intrinsic parasitic capacitance and this will cause an increase in switching loss. The switching energies for SiC MOSFET can be found by a summation of both turn on and turn-off switching energies as in (4).

$$P_{sw(MOSFET)} = E_{on(MOSFET)} + E_{off(MOSFET)} \tag{4}$$

where the formulas $E_{off(MOSFET)}$ and $E_{on(MOSFET)}$ represent turn-off and turn-on energies of SiC MOSFET, respectively

$$E_{on(MOSFET)} = f_{sw} \int_{t_1}^{t_2} V_{DS(\text{on})} I_{D(\text{on})} \cdot dt \tag{5}$$

$$E_{off(MOSFET)} = f_{sw} \int_{t_5}^{t_6} V_{DS(off)} I_{D(off)} \cdot dt \tag{6}$$

Then by substituting equation (5) and (6) in equation (4), The mathematical equation used to evaluate the SiC MOSFET's total switching losses can be expressed as:

$$P_{sw(MOSFET)} = f_{sw} \left(\int_{t_1}^{t_2} V_{DS(\text{on})} I_{D(\text{on})} \cdot dt + \int_{t_5}^{t_6} V_{DS(off)} I_{D(off)} \cdot dt \right) \tag{7}$$

The $I_{D(on)}$ and $I_{D(off)}$ are currents flowing through SiC MOSFET during turn-on and turn-off stages; $V_{DS(on)}$ and $V_{DS(off)}$ are SiC MOSFET drain-source voltage applied in case of turn-on and turn-off, respectively; t_1, t_2, t_5, and t_6 can be denoted as the start and terminal turn-on and turn-off times.

The total power loss model of a SiC MOSFET $P_{loss(MOSFET)}$ can be calculated as:

$$P_{loss(MOSFET)} = P_{c(MOSFET)} + P_{sw(MOSFET)} \tag{8}$$

Substituting equations (2) and (7) into (8), the total power loss is obtained as in equation (9)

$$\begin{aligned} P_{loss(MOSFET)} &= f_{sw} \int_{t_2}^{t_5} I_{rms}^2 \cdot R_{DS(\text{on})} dt \\ &+ f_{sw} \left(\int_{t_1}^{t_2} V_{DS(\text{on})} I_{D(\text{on})} \cdot dt \right. \\ &+ \left. \int_{t_5}^{t_6} V_{DS(off)} I_{D(off)} \right) \end{aligned} \tag{9}$$

Normally, the switching energies of the SiC diodes used in a power converter are not considered during power loss calculation. This is because of the SiC diode switching energy is very small in comparison with SiC MOSFET switching energies, it is thus neglected in total loss model of a SiC power Schottky diode as follows

$$\begin{aligned} P_{loss(\text{Diode})} &= P_{c(\text{Diode})} + P_{sw(\text{Diode})} \\ P_{\text{loss(Diode)}} &= f_{sw} \int_{t_2}^{t_5} I_{rms}^2 \cdot R_{\text{on,(Diode)}} dt \end{aligned} \tag{10}$$

C. TOTAL POWER LOSS MODEL ANALYSIS OF SiC 3L-NPC INVERTER

In this section, the power loss model of the SiC MOSFETs and SiC power diodes are used to calculate switching energies and conduction losses in a high switching frequency three phases SiC 3L-NPC inverter. These losses affect the overall performance of the conversion system.

There are different modulation techniques that have been subjected to three-level inverters. These techniques are aimed at obtaining current and voltage waveforms with minimal losses as well as reduced harmonics distortion and common medium voltage. Mainly, two types of modulation strategies exist, namely; sinusoidal pulse width modulation (SPWM) and space vector pulse modulation (SVPWM), are used for three level inverters. In this paper, SiC 3L NPC inverter power loss in the SPWM modulation technique is analyzed. On the SPWM modulation technique, m is the amplitude modulation index.

Considering the SPWM modulation technique and positive half-wave of the output voltage, the voltage drops across SiC MOSFETs, SiC Diodes and the load current function during a conduction period can be expressed as follows:

$$u_{c(MOSFET)} = u_{DS} = i(t) R_{DS} \tag{11}$$

$$u_{c(Diode)} = u_{ak} = V_f \tag{12}$$

$$i(t) = I_m \sin(\omega t) \tag{13}$$

where u_{ak} is the diode anode-cathode voltage drop; V_f is the diode equivalent voltage drop under zero-current condition; I_m is the peak of inverter output current and ω is the current angular frequency.

The conduction power losses $P_{c(MOSFET)}$ over a single SiC MOSFET device are given by:

$$P_{c(MOSFET)} = \frac{1}{2\pi} \cdot \frac{1}{T_s} \int_0^{\pi} u_c i(t) \cdot t_{(MOSFET)} d(\omega t) \tag{14}$$

The reverse recovery time of SiC MOSFETs antiparallel diode is neglected due to its high switching frequency characteristics, thus, the diode can effectively carry the current during the dead time intervals. According to the switching cycle T_s, $t_{(MOSFET)}$ and $t_{(Diode)}$ are expressed as follows:

$$t_{(MOSFET)} = \frac{T_s}{2} [1 + m \sin(\omega t + \theta)] \tag{15}$$

$$t_{(\text{Diode})} = T_s - t_{(MOSFET)} \tag{16}$$

Then

$$t_{(Diode)} = T_s - \frac{T_s}{2} [1 + m \sin(\omega t + \theta)] \tag{17}$$

where θ is the phase displacement angle between the grid current and voltage.

By substituting equations (11), (13) and (15) in (14), the SiC MOSFET conduction loss is calculated as:

$$\begin{aligned} P_{c(MOSFET)} = &\frac{1}{2\pi} \cdot \frac{1}{T_s} \int_0^{\pi} I_m \sin(\omega t) \cdot R_{DS} \\ &\cdot I_m \sin(\omega t) \cdot \frac{T_s}{2} [1 + m \sin(\omega t + \theta)] \, d(\omega t) \end{aligned} \tag{18}$$

$$P_{c(MOSFET)} = I_m^2 R_{DS} \left(\frac{1}{8} + \frac{m \cos\theta}{3\pi} \right) \tag{19}$$

The conduction loss of the diode is as follow:

$$P_{c(\text{Diode})} = \frac{1}{2\pi} \cdot \frac{1}{T_s} \int_0^{\pi} u_{c(Diode)} \cdot i(t) \cdot t_{(\text{Diode})} d(\omega t) \tag{20}$$

The switching energy loss of SiC MOSFET expressed as follows:

$$\begin{aligned} P_{sw(MOSFET)} = &\frac{f_{sw}}{2\pi} \int_0^{\pi} (V_{DS(\text{on})} I_{D(\text{on})} \\ &+ V_{DS(off)} I_{D(off)}) dt \end{aligned} \tag{21}$$

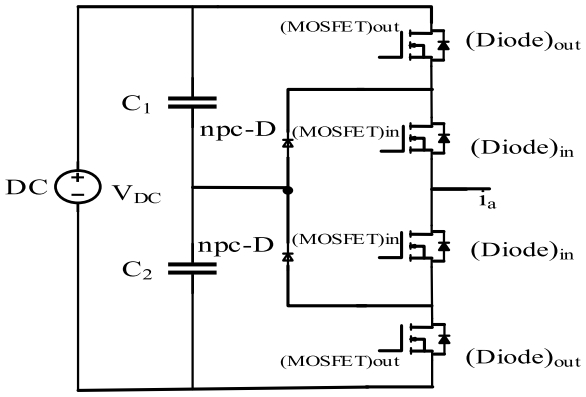


FIGURE 3. Represents leg a of the three-phase SiC 3L- NPC inverter topology.

By substituting equations (12),(13) and (17) in (20), the SiC diode conduction loss is calculated as:

$$P_{c(\text{Diode})} = \frac{1}{2\pi} \cdot \frac{1}{T_s} \int_0^{\pi} V_f \cdot I_m \sin(\omega t) \cdot T_s - \frac{T_s}{2}[1 + m\sin(\omega t + \theta)]d(\omega t) \quad (22)$$

$$P_{c(\text{Diode})} = \frac{1}{2\pi} \int_0^{\pi} V_f \cdot I_m \sin(\omega t) \cdot \frac{[1 - m\sin(\omega t + \theta)]}{2} d(\omega t) \quad (23)$$

$$P_{c(\text{Diode})} = I_m V_f \left(\frac{1}{2\pi} - \frac{m\cos\theta}{8}\right) \quad (24)$$

D. POWER LOSSES DISTRIBUTION AMONG THE DEVICES OF THE 3L-NPC INVERTER

The main disadvantage of 3L-NPC topology is the unequal power losses distribution through its semiconductor devices, especially in the case of medium and high-power applications, where its effects are particularly severe [24]. The power loss of each device for 3L-NPC inverter is determined at the high switching frequency. The SiC 3L-NPC inverter has three legs as shown in Figure1. Each leg contains four SiC -MOSFET devices with antiparallel diodes and two clamping diodes as in Figure 3 shows leg a (phase a) of the three-phase SiC 3L- NPC inverter topology. In this model, the antiparallel diodes of the SiC MOSFET device have been used as clamping diodes.

Generally, 3L-NPC inverter contains three phase (legs), known as phase a, phase b and phase c, with each leg having the same and equal semiconductor devices. Figure 3, represents phase a of the 3L-NPC inverter. This phase (leg) contains two outer MOSFETs $(MOSFET)_{out}$, two inner MOSFETs $(MOSFET)_{in}$, two outer diodes $(Diode)_{out}$, two inner diodes $(Diode)_{in}$, and two clamping diodes *npc-D*. In SiC 3L- NPC inverter, the inner devices have higher loss compared to the outer device.

The power loss of all the outer devices for all 3 legs of a SiC 3L-NPC inverter are the same. Similarly, the inner device's power loss is the same for all 3 legs of a SiC 3L-NPC inverter. Thus, the conduction loss of SiC 3L-NPC inverter in SPWM modulation is obtained as follow:

$$P_c = 3(2P_{c(MOSFET)\text{out}} + 2P_{c(MOSFET)\text{in}} + 2P_{c(\text{Diode})\text{out}} + 2P_{c(\text{Diode})\text{in}} + 2P_{c(\text{npc-D})}) \quad (25)$$

The total switching loss of 3L-NPC inverter is:

$$P_{sw} = 3(2P_{sw}(\text{MOSFET})\text{out} + 2P_{sw}(\text{MOSFET})\text{in}) \quad (26)$$

III. POWER LOSS CALCULATION USING PLECS SIMULATOR AND EXPERIMENTAL RESULT

The conduction loss and switching energies of both SiC -MOSFET and SiC diode are calculated according to Equations (2), (3) and (7), and the current and voltage waveforms measured during a commuted interval by clamped inductive switching waveform test. To improve inverter efficiency, it is necessary to select suitable and convenient devices which have an effective loss model, from which the total losses of these devices are then calculated. This method makes it easy to determine the total loss of the inverter.

A. SIMULATION RESULTS AND SWITCHING ENERGIES ANALYSIS OF SiC MOSFET

The 3L-NPC inverters can attain improved efficiency and reduced power loss by replacing all the normal silicon semiconductor devices by silicon carbide semiconductor devices. In order to achieve this, it is necessary to study and investigate the performance and establish an effective power loss model for the new selected devices.

1) THE ADVANTAGE OF SiC MOSFET

The semiconductor devices that are made from Silicon carbide have several features that make it preferable as compared to normal silicon material, such as a wide band gap. This feature of wider energy band-gap allows the SiC devices to continue operating under high temperatures of more than 400 degrees Centigrade. Also, the SiC MOSFET has capability to offer high switching frequencies as high as 20MHz. The SiC devices have the ability to operate with high junction temperature. This offers the potential to reduce weight and size of heat sink, which can also lead to cost saving. The SiC devices can be operating at 2500V breakdown voltages [25].

The switching energies reduction by using SiC MOSFET enables the SiC 3L NPC inverter to operate at higher switching frequency. Hence, the ac output filter size of SiC-3L-NPC inverter is reduced. SiC semiconductor devices have lower switching energy than Si semiconductor devices; up to five times with the same operating conditions.

2) DYNAMIC CHARACTERISTIC OF SiC MOSFET

The parameters of any device can be found according to datasheet given by the manufacturer. However, the manufacturer's testing environment and the device working state are

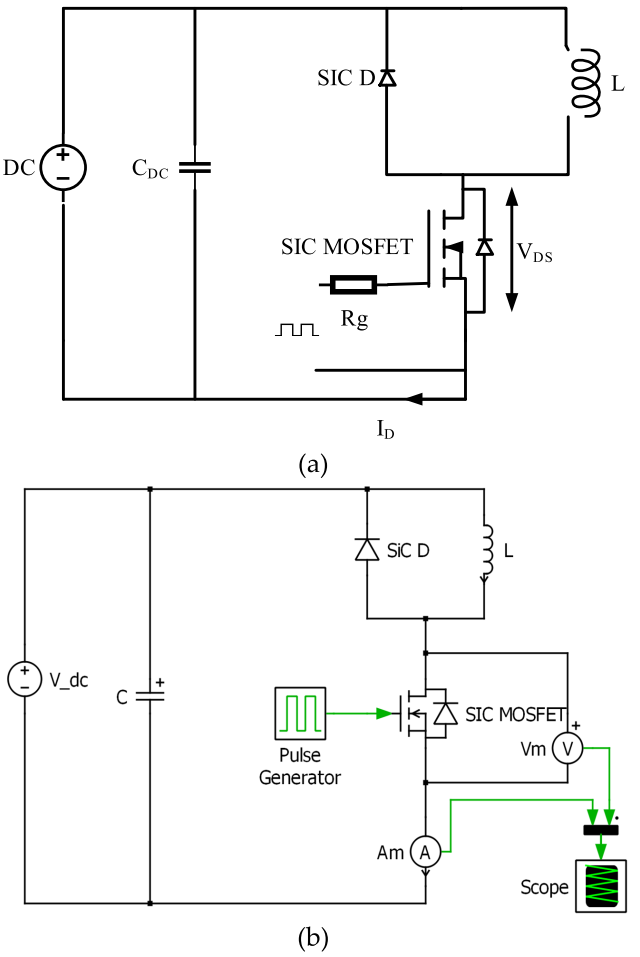


FIGURE 4. Inductive clamp double pulse test. (a) Inductive clamp double pulse test circuit. (b) Double pulse inductive clamp test circuit in PLECS.

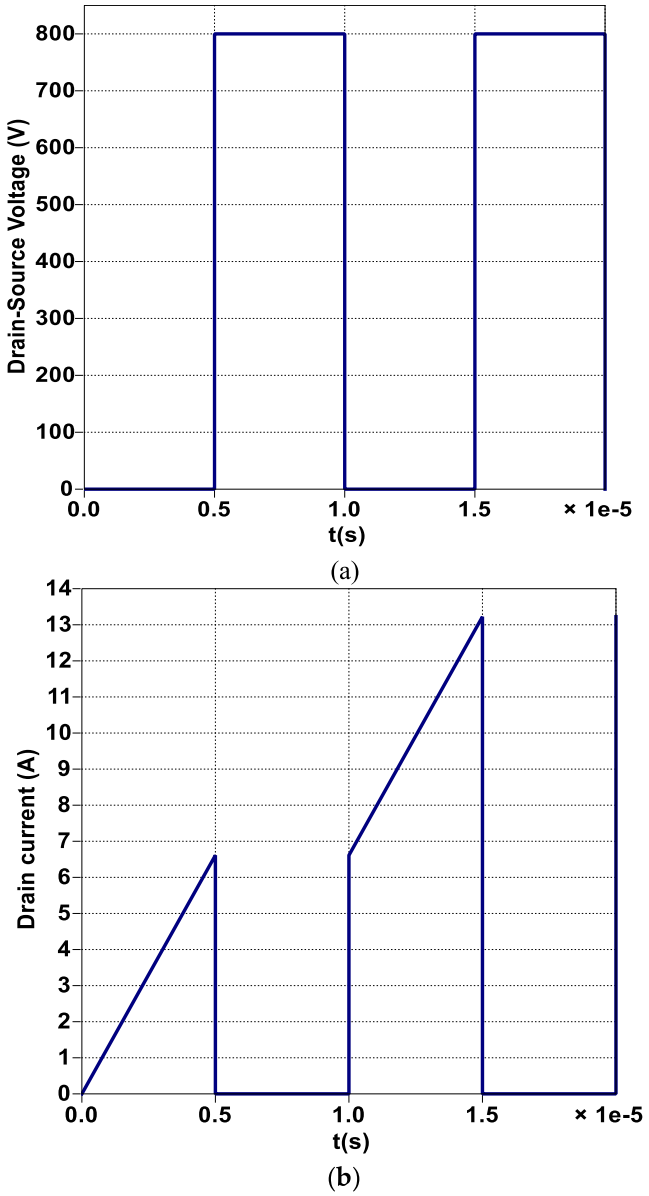


FIGURE 5. Double pulse test circuit results: (a) Drain-source voltage (VDS). (b) Drain current (ID).

different from real application. Thus, there is a degree of error between real dynamic characteristics of the SiC semiconductor device and the characteristics given by datasheet. Therefore, some parameters of the SiC semiconductor devices must be tested to ensure the accuracy of loss which is calculated by using the simulation model [26], [27]. Figure 4 (a) shows the inductive clamp double pulse test circuit. This circuit can be simulated in PLECS software as shown in Figure 4 (b), and results of the simulation model are investigated using hardware realization of inductive clamp double pulse test as shown in Figure 6.

3) SIMULATION MODEL AND RESULTS OF DOUBLE PULSE TEST FOR SiC MOSFET

The clamped inductive switching waveform test circuit shown in Figure 4 is simulated in PLECS simulation platform environment. The circuit in Figure 4 (b) is developed for the simulation study. This test is carried out with freewheeling diode and inductor as its basic components in order to evaluate the C2M0160120D SiC MOSFET semiconductor devices switching energy performance. The device parameters used in this simulation model are given in Table 2. Here, inductive switching waveform test by using SiC MOSFET is built in PLECS simulator to simulate the behavior of the device. This simulation is to support the hardware circuit design before carrying out the experiment to validate the simulation results. The switching energies are simulated for DC bus voltages of 800 V.

The switching losses simulation setup is shown in Figure 5. From the values of drain-source voltage (V_{DS}) and current flow through device (I_D) during turn-off and turn-on periods, turn-off and turn-on energy can be calculated easily for 1.2KV, 19A SiC MOSFET by using the equivalent circuit with 10 gate resistance (R_g) and ambient temperature (T_a) of 25 °C. The switching losses are based on multiple of the source to drain voltage and the drain current. These switching

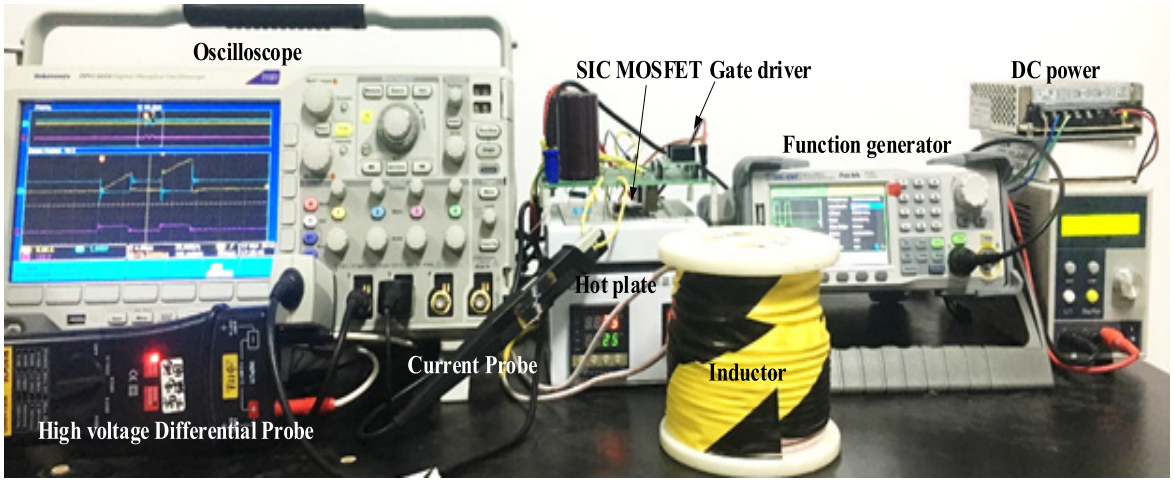


FIGURE 6. Hardware realization of inductive clamp double pulse test.

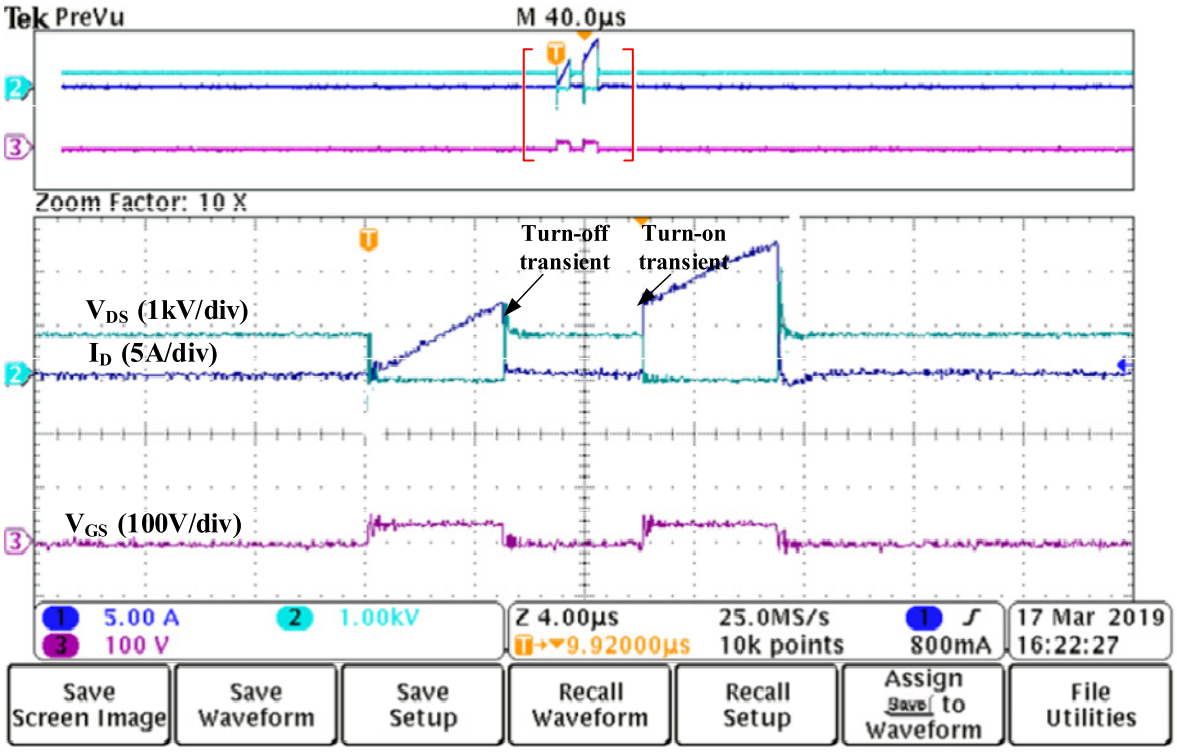


FIGURE 7. Dynamic characteristics at 800V with $R_g = 10\ \Omega$.

energies are also dependent on the switching frequency which is set as 100 kHz in the developed model.

B. EXPERIMENTAL SWITCHING ENERGIES LOSS EVALUATION OF 1.2 kV/19A SiC MOSFET

In this section, the 1.2 kV/19 A SiC MOSFET power loss evaluation is explained. The dynamic switching energy loss is measured using the inductive clamp double pulse test circuit. The schematic of the double pulse test circuit used is shown in Figure 4 and the hardware realization of inductive clamp double pulse test is shown in Figure 6. The junction temperature of the SiC MOSFET C2M0160120D device has the same value as hot plate temperature. Figure 7 shows the overall recorded results during inductive clamp double pulse test for 800 V.

The simulation results of SIC MOSFET as shown in Figure 5 is validated experimentally as shown in Figure 7. During the first pulse, the desired current for device under test is set according to width of the first pulse, and at the end of this pulse, the SiC MOSFET is turned off. The current and

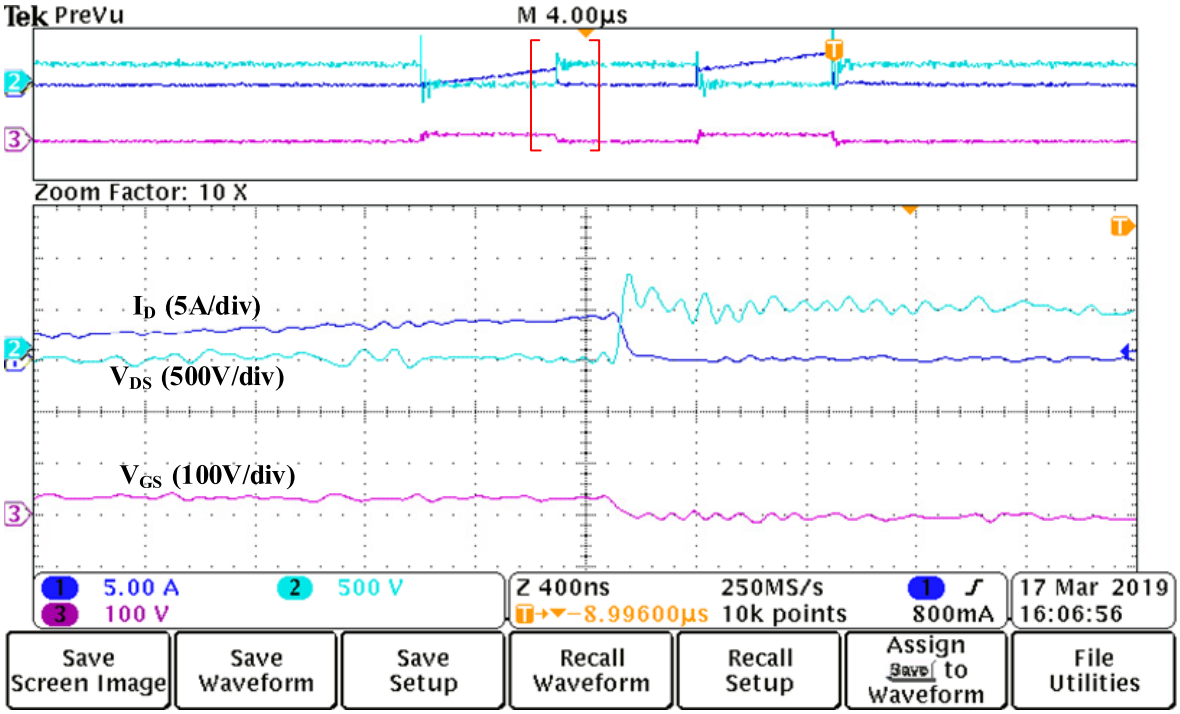


FIGURE 8. Turn-off characteristics switching characteristics at 800V with $R_g = 10\ \Omega$.

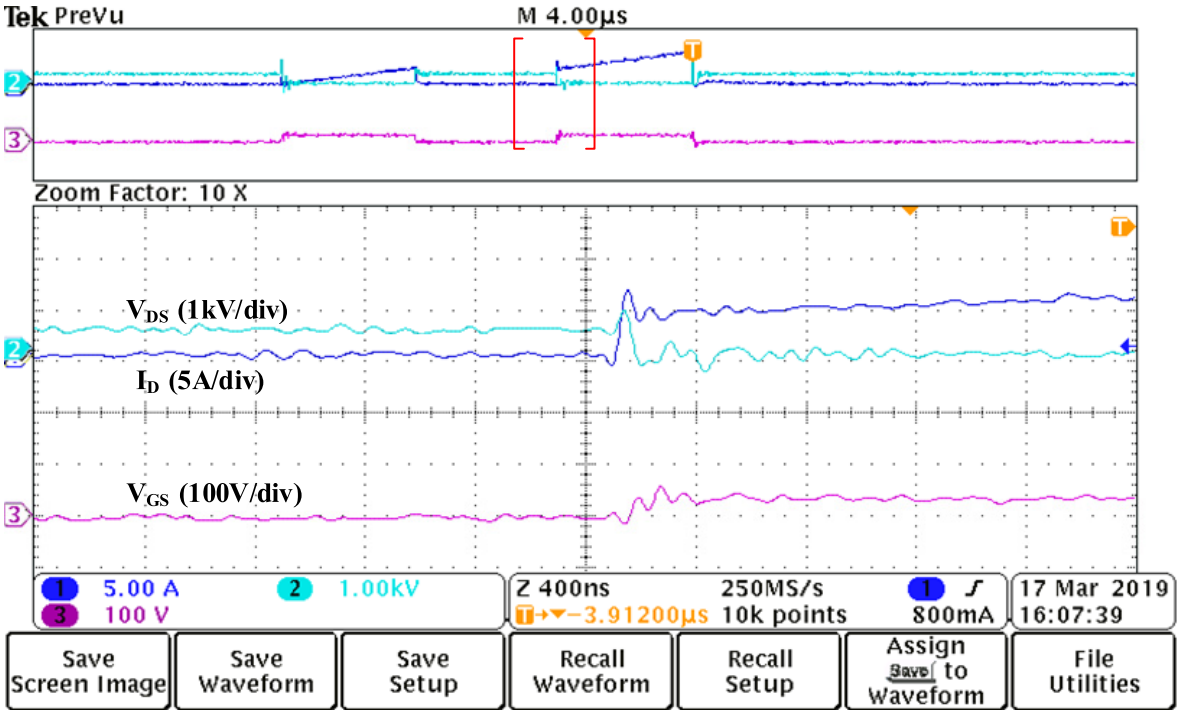
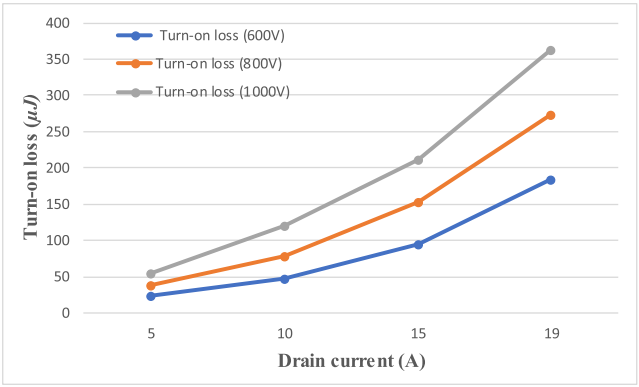


FIGURE 9. Turn-on characteristics switching characteristics at 800V with $R_g = 10\ \Omega$.

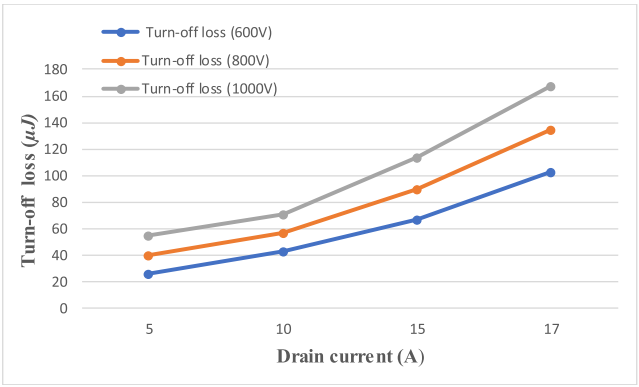
voltage of the device during turn-off period are then measured as shown in Figure 8. The device is then turned on, and the device's voltage and current during turn-on transient are measured at 800 V, with gate resistance R_g value for the device as 10 Ω. Figure 9 shows the device switching characteristics during turn-on transient. The overlap regions between voltage and current during turn-on and turn-off periods are the turn-on and turn-off energies power loss of the SiC MOSFET

TABLE 2. Parameters of MOSFET SiC C2M0160120D and SiC diode C4D05120A.

Unit	Quantity	value
V	SiC MOSFET -Drain-source voltage (V_{DS})	1200
A	SiC MOSFET Drain-source current (I_{DS})	19
$m\Omega$	SiC MOSFET Drain-source resistor (R_{DS})	160
$^{\circ}C$	SiC MOSFET Ambient temperature (T_a)	25
V	SiC diode Repetitive peak reverse voltage	1200
A	SiC diode Forward current (I_F)	19
nC	SiC diode relative permeability	27



(a)



(b)

FIGURE 10. 1.2-kV/19 A SiC MOSFET switching energy loss. (a) Turn-on loss and (b) turn-off loss with $R_g = 10\ \Omega$ and $T_a = 25^{\circ}C$ at different voltages and currents.

respectively. During turn-off transient, the current falls, and the voltage rises. During turn-on transient, the current rises, while voltage falls.

The switching energy losses corresponding to C2M0160120D SiC MOSFET device are measured Experimentally and plotted at different device voltages and currents as shown in Figure 10. (a) the turn-on losses and (b) turn-off losses. The temperature of hot-plate is set at 25°C and the gate resistance is 10 Ω. From these Figures, it is shown that turn-on and turn-off power losses are increasing gradually linearly with the current values. The DC voltage affects the switching energy losses of the switch proportionally.

IV. SIMULATION MODEL OF SiC 3L-NPC INVERTER BASED ON EXPERIMENTAL DATA

The high-frequency three-phase SiC 3L-NPC inverter simulation model used for PV application is shown in Figure 11. The power losses of these devices are determined by real working condition of the circuit. The average switching loss and average on state loss (conduction loss) are calculated by using the device's library of PLECS. The experimental results data of the SiC device (Section III.B) are used in thermal description file of the devices as shown in Figure 12 and Figure 13. This method of substitution dynamic and static characteristics for the switching semiconductor device gives results close to practical test data in practical application.

The switching energies loss is defined as a function of the ambient temperature of the device, current through the device, gate driver and voltage across the device (V_{block}) in a 3D look-up table, as shown in Figure 12. The switching energy loss is measured and recorded during the double pulse test at different voltage and currents. Figure 13 shows the 1.2 kV/19 A SiC MOSFET forward V–I characteristics from forward Conduction loss.

The instructions for implementing the conduction and switching loss into the switching device model used for the simulation of the inverter model are as follow:

- Double-click on the switching device and create a new thermal description to define the conduction and switching losses
- use the switching losses measurements as in figure 12 and conduction losses as shown in figure 13. The 'Energy scale' must be set to 'mJ' when defining the turn-off and turn-on losses. Save the model as switching device name.
- input the conduction loss the same way as with the switching losses.
- To add multiple rows or columns in the power loss lookup table, enter the new voltage or current values using vector format. For example, to enter the current values for the diode turn-off loss description, right-click on the '0 A' column header, select 'New current values'. Then enter the following values in the dialog box: 5,10,15,19 manually, otherwise, by inputting the switching losses formulas in the switching losses box which automatically calculate and plot the values.

These steps explain how to use the thermal modeling features of PLECS to create a combined electrical-thermal simulation of the inverter. By using the data in the thermal description file of the switching device, the power loss of the switching device can be determined by actual working conditions of the inverter circuit.

Figure 14 shows the waveforms of the transition conduction loss in watts (W) and the switching energies power losses in joules (J) for the SiC 3L-NPC inverter during real operation. Figure 15 shows the output three-phase voltage and current of SiC 3L NPC inverter. The switching losses caused by the three-phase SiC 3L NPC inverter devices switching affects the three output voltages and current.

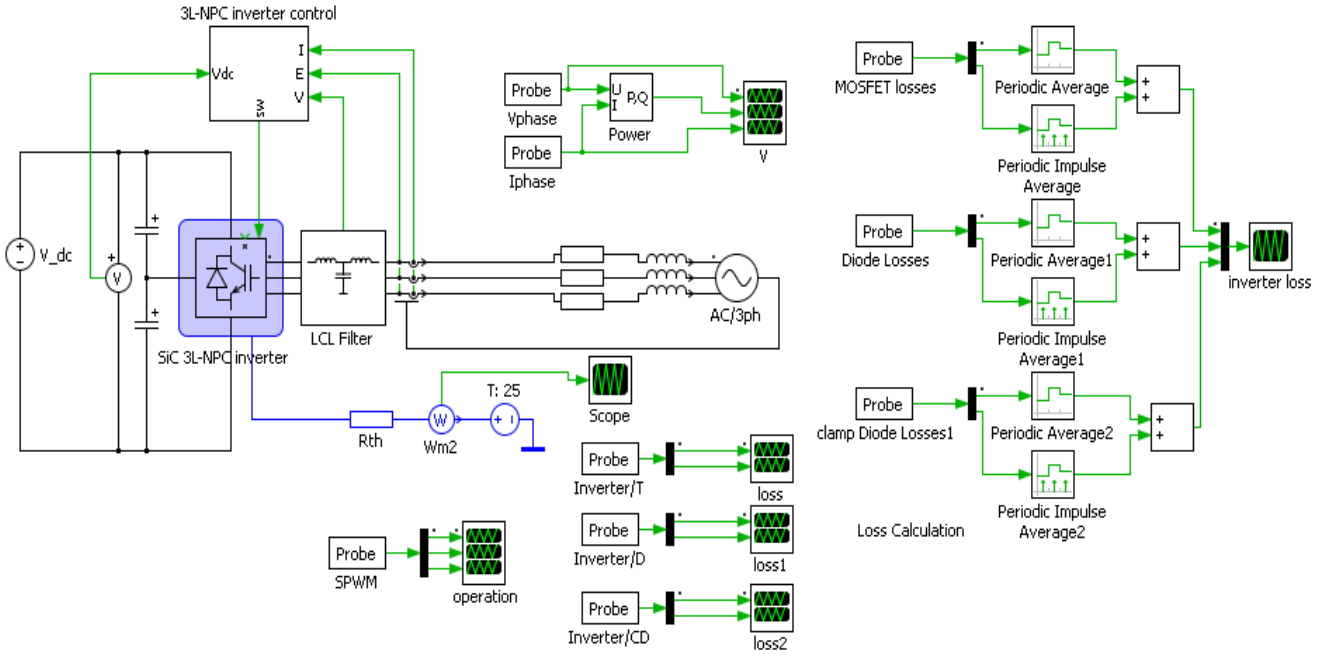


FIGURE 11. The PLECS loss simulation model of the three-phase 3L-NPC inverter for PV application.

TABLE 3. The parameters used for theoretical calculation.

Quantity	Value
V_{DS}	800 V
R_{DS}	160 mΩ
f_{sw}	100 kHz
T_s	10μs
$cos\theta$	0.995
m	0.95
I_m	14.12 A

TABLE 4. Power loss comparison of theoretical calculation and simulation based on experimental data.

Module	Theoretical Calculation Values		Simulation Based on Experimental Data Values	
	Conduction Loss (W)	Switching loss (W)	Conduction Loss (W)	Switching loss (W)
SiC 3L-NPC inverter	42.25	34.5	62.15	40.26
Total Power loss ($\sum Pl_{osses}$)	76.75		102.41	

However, the LCL filter is used to filter the three-phase output voltage and current to be sinusoidal, and then fed to the grid, where 12 kW of active power is delivered.

A. RESULTS OF THE THEORETICAL CALCULATION MODEL AND SIMULATION MODEL BASED ON EXPERIMENTAL DATA

By using the parameters shown in Table 3 and the formulas derived in Sections II.B and II.C, the theoretical calculation results of the total conduction loss and switching loss of SiC semiconductor devices used in SiC 3L-NPC inverter are calculated. Moreover, the total power loss of the SiC 3L-NPC inverter simulation model based on Experimental data is obtained. Table 4 shows the comparison of power losses values between the theoretical calculation and the PLECS power loss simulation model based on Experimental data.

Table 4 shows the comparison values of the theoretical calculation and simulation values based on experimental data. According to this table, the total power loss values of the simulation values based on experimental data are generally greater than those of the theoretical calculation values. This is because, the data of semiconductor device used in the simulation model are tested under real conditions operation of the devolved inverter, and it is slightly higher than the given datasheet values. Thus, the total power losses in the simulation results based on experiment data are all higher than the theoretical calculation values. However, the values obtained by theoretical calculation are different from the simulation based on experiment data due to unequal distribution loss among the semiconductor devices of the 3L-NPC inverter.

B. EFFICIENCY

SiC 3L-NPC Inverter efficiency is obtained using total power loss at 800 V input voltage, Efficiency of the inverter is calculated with Expression (26):

$$\eta = \frac{P_{out}}{P_{out} + \sum P_{losses}} \tag{27}$$

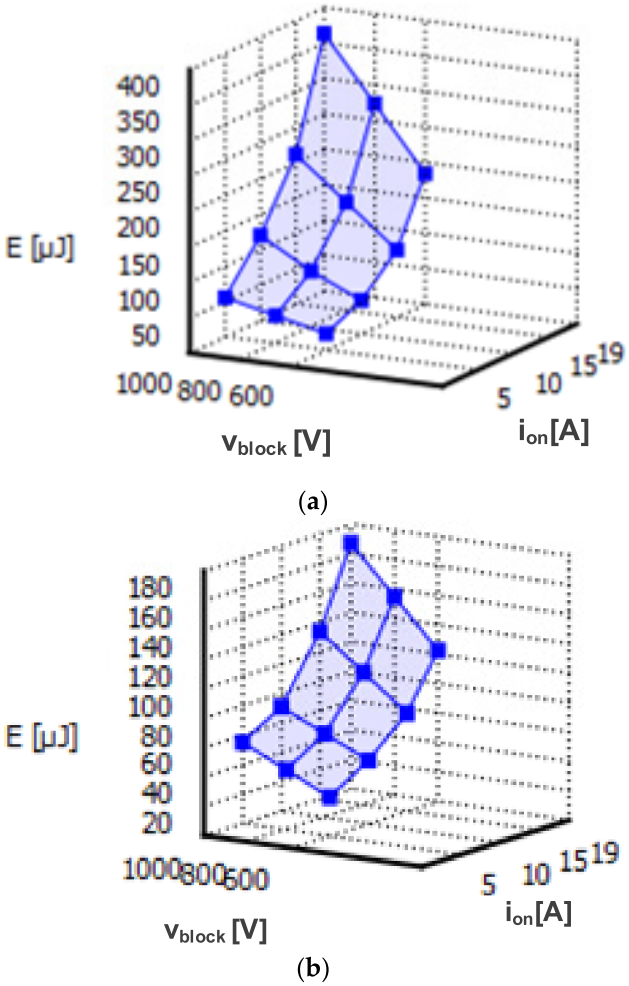


FIGURE 12. 1.2 kV/19 A SiC MOSFET thermal description file. (a) Turn-on loss and; (b) turn-off loss distributions (from DPT experiments for different voltages and currents).

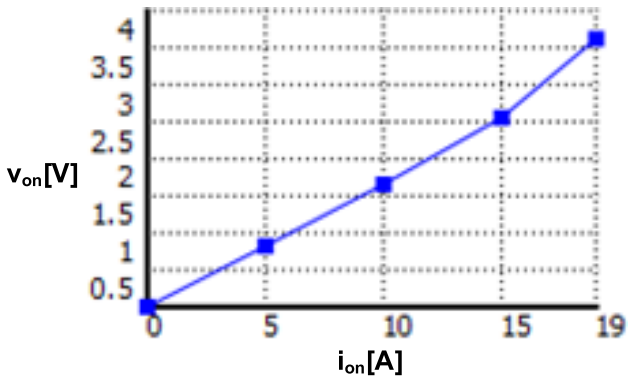


FIGURE 13. 1.2 kV/19 A SiC MOSFET forward V–I characteristics (from forward Conduction loss for different voltages and currents).

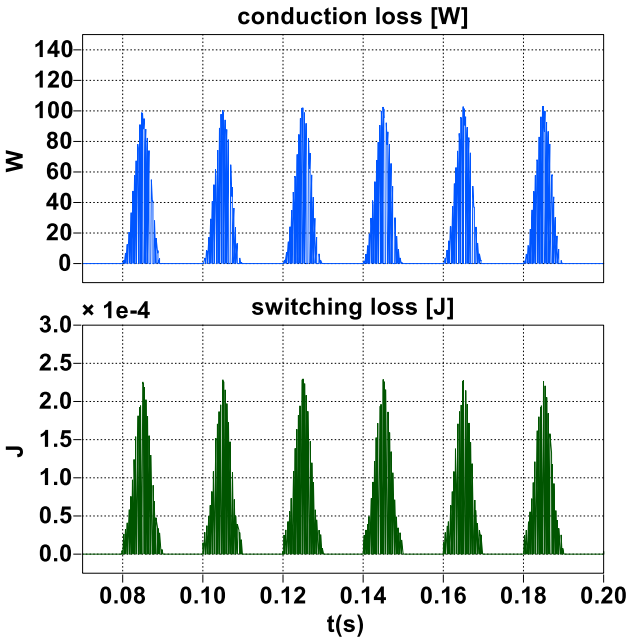


FIGURE 14. 1.2 kV/19 A SiC MOSFET transition conduction loss (W) and switching loss(J) in SiC 3L-NPC inverter.

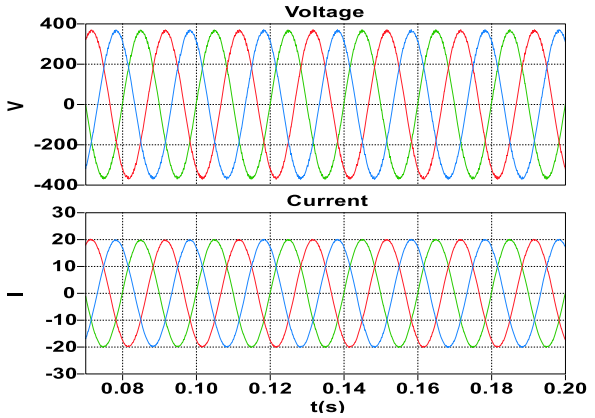


FIGURE 15. Output voltages and currents of the 3L-NPC inverter.

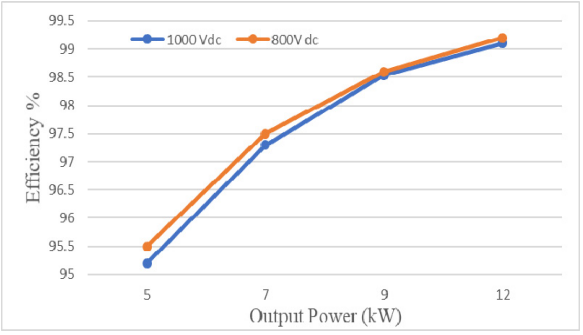


FIGURE 16. Efficiency of the SiC 3L-NPC inverter versus output power at 800 V and 1000 V DC input voltages.

Inverter efficiency is derived according to expression (26). Calculated efficiencies are shown in Figure 16. At 800 V and 1000 V DC input voltages. The highest efficiency is obtained at 800 V input voltage with peak efficiency of 99.2%. This is because of DC-link voltage of 800 V input is lower than that of 1000 V input. Therefor the conduction loss and switching loss are smaller in case of DC input voltage is 800 V. When the input voltage is less than 700 V, the system needs boost stage.

The peak efficiency obtained for input voltage of 800 V and 1000 V and output power in the range of 5–12 kW. The total power loss of the SiC 3L-NPC inverter obtained shows that the conversion system achieved high efficiency.

V. CONCLUSIONS

This paper presents power loss analysis of a developed SiC 3L-NPC inverter and its efficiency based on SiC MOSFETs switches. An accurate and detailed power loss calculation formula for the semiconductor switches used in the inverter is derived. Furthermore, a power losses theoretical calculation of SiC 3L-NPC inverter based on datasheet parameters is calculated. The switching loss and conduction loss of SiC semiconductor devices used in the inverter are also obtained. Based on the experimental results of SiC MOSFET, a comparison between theoretical analysis and simulation analysis based on experimental data of SiC 3L-NPC inverter is given. The SiC MOSFET power losses are obtained at various voltages and currents at high switching frequency. The theoretical calculation and simulation based on experimental data of SiC 3L-NPC inverter using SPWM strategy show that, the total power loss of the two methods are different, and the simulation values based on experimental data values are higher than the theoretical calculation values. This difference is due to the real operating conditions of the inverter used in the developed model.

In addition, high efficiency of the inverter is observed by using SiC. According to efficiency calculation, the results show that the efficiency increases from 95.2% to 99.2% at a different output power of the inverter, and the highest efficiency is obtained when the DC input voltage is 800 V.

Conclusively, it is obtained that the total power loss and output power of 3L NPC inverters can be improved by using SiC semiconductor device. Therefore, operating the 3L-NPC inverters using SiC MOSFET and high switching frequency SPWM strategy is a very efficient solution for grid-connected SiC PV inverter applications. The paper mainly focuses on developing the SiC 3L-NPC inverter power loss model based on experimental data, to achieve high efficiency of SiC 3L-NPC inverter used for PV application.

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