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Ultra-Compact and Wideband V(U)HF 3-dB Power Dividers Consisting of Novel Asymmetric Impedance Transformers

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ABSTRACT Novel asymmetric impedance transformer (NAIT) containing most of symmetric and asymmetric impedance transformers' properties is proposed for ultra-compact and wideband 3-dB power dividers. All the simulated frequency responses of the NAITs are about the same, regardless of sizes, which is regarded as one of the distinct and unique properties not only for the size reduction with design flexibility but also for the wide bandwidths, considering that the bandwidths of the general passive components are proportional to the sizes. The advantage of the NAITs can also be confirmed by another example that even if the NAIT is three times shorter than the previous one, slightly wider bandwidth can be achieved. To verify the suggested theory, one NAIT power divider is tested at 100 MHz. The total transmission-line sections (TLs) of the power divider are only 14.6° long, and the measured bandwidth is about 58 %, leading to 99.3 % size reduction, compared to the conventional typical ones with 90° TLs. In terms of sizes versus bandwidths, the fabricated NAIT power divider may be regarded as the smallest among those ever recorded, based on the low-cost microstrip technology.

INDEX TERMS Novel asymmetric impedance transformers (NAITs), compact V(U)HF three-port 3-dB power dividers, Wilkinson power dividers, compact asymmetric impedance transformers.

I. INTRODUCTION

The impedance transformers have been used for various applications such as three-port power dividers (PDs) [1]–[14], ring and branch-line hybrids [15]–[18], baluns [19] and antenna arrays. As wireless communication systems require substantial reduction in mass and volume, the miniaturization of the impedance transformers has been of high interest, especially for V(U)HF applications. Transformation of a real impedance into another one necessitates the impedance transformers, which may be classified into symmetric and asymmetric structures. The representative symmetric impedance transformers are quarter wave impedance transformers whose compact forms are Π-types [16], [19], [21], T- types [2], [12], [19], [21] and $L_{s1}-$ types [17], while the asymmetric impedance transformers (AITs) are CCTs (constant conductance-type transmission-line impedance transformers), CVTs (constant VSWR-type transmission-line impedance transformers) [1], [4], [8], [18], MCCTs (modified CCTs), MCVTs (modified CVTs) [3], [5] and L-sections with lumped elements [20, Sec. 5.1]. As well known, the AITs contain all the attribute of the symmetric impedance transformers and have more advantages such as wider bandwidths with smaller sizes, arbitrary phase delays and more design flexibilities. Therefore they can be used not only for the impedance transformers but also for phase shifters [4], [8], [18]. However, there are still restrictions on reducing the sizes, due to unfeasible high values of characteristic impedances of the transmission-line sections (TLs) and smaller bandwidths [1], [3]–[5], [8], lack of the design flexibility of the L-sections [20] due to the limited values of chip inductors and capacitors, or difficulties for the fabrication of Y-junctions in the three-port PDs [21].

To overcome the problems, solutions are suggested in [5], [6], and [13]. The AITs treated in [5] are inherently MCCTs in [3], fabricating high impedance TLs with $L_{s1}-$types [17]. However, even though the way [5] can alleviate the fabrication difficulties somehow, it cannot be a fundamental solution to the size reduction and wide bandwidth, because the

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bandwidths of the MCCTs in [5] are proportional to the sizes just like the typical passive components. Furthermore, there is no way to reduce the number of TLs. The impedance transformers in [6] each consist of two TLs and a series inductance in between and can be asymmetric and symmetric. However, the frequency responses of symmetric and asymmetric impedance transformers are about the same, and the phase delays have only one value of 90°. That is, the asymmetric impedance transformers in [6] have no AIT property, and the symmetric impedance transformers [6] are the same as the L_{S1}−type with $N = 1$ in [17], Fig. 6(d)], thereby leading to smaller bandwidths, limited design flexibility, restriction on the size reduction which will be discussed further. Since the AIT [13] consists of shunt open/short stubs at both ends, the phase delays are very small, but the bandwidths are very small.

To solve the conventional problems in [5], [6], and [13], a novel asymmetric impedance transformer (NAIT) is suggested for the ultra-compact sizes and wide bandwidths. The NAIT consists of two different TLs, one open stub and one series inductance and contains most of conventional asymmetric and symmetric impedance transformer topologies and properties. Frequency responses are generated, varying different sizes, but about the same, regardless of the sizes, which can be considered the unusual and distinct characteristics, compared to the fact that the bandwidths of the general passive components are proportional to the sizes. The reason for the about same frequency performance even with the different sizes is because one TL can be designed for the best performance.

As an application, the NAIT PD is fabricated at the design frequency of 100 MHz and tested. The total TLs of the NAIT PD are 14.6° long, leading the 99.3 % size reduction, compared to the conventional typical PD with 90° TLs, and the measured 15-dB return loss bandwidth is about 58 %. In terms of sizes versus bandwidths, the NAIT PD can be considered the smallest among those ever recorded.

II. NOVEL ASYMMETRIC IMPEDANCE TRANSFORMERS (NAITs)

Before treating the NAIT PDs, the NAIT needs to be discussed in more detail. The NAIT is depicted in Fig. 1, transforming a real impedance of R_S into another one of R_L. The NAIT is asymmetric, and therefore the termination impedances of R_S and R_L cannot be interchangeable, and R_S is always greater than R_L. The NAIT in Fig. 1 consists of two TLs, one open stub and a series inductance of L. One TL located close to the termination impedance of R_S has the characteristic impedance of Z_T and the electrical length of Θ_T, while the other one connected to R_L has Z_{Ta} and Θ_{Ta}. The characteristic impedance and the electrical length of the open stub are Z_o and Θ_o, respectively.

A. DESIGN FORMULAS

Design formulas can be derived based on the scattering parameters [13], but available conditions are

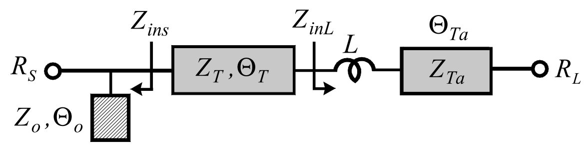

FIGURE 1. Novel asymmetric impedance transformer.

$|\boldsymbol{S_{11}}| = |\boldsymbol{S_{22}}| = 0$ and $\boldsymbol{S_{12}} = \boldsymbol{S_{21}} = \mathbf{e}^{-j\boldsymbol{\Phi}}$ where $\boldsymbol{\Phi}$ is the phase delay. Therefore the method [13], [14] can be extremely difficult and complicated for seven variables of the NAIT. An easy way for the design formulas will be introduced.

Two input impedances of $\boldsymbol{Z_{inS}}$ and $\boldsymbol{Z_{inL}}$ are indicated in Fig. 1, which are

$$Z_{inS} = \left(j\frac{1}{Z_o}\tan\Theta_o + \frac{1}{R_S}\right)^{-1} \tag{1a}$$

$$Z_{inL} = j\omega L + Z_{Ta}\frac{R_L + jZ_{Ta}tan\Theta_{Ta}}{Z_{Ta} + jR_L tan\Theta_{Ta}} \tag{1b}$$

The reflection coefficients related with the two input impedances are

$$\Gamma_S = \frac{Z_{inS} - Z_T}{Z_{inS} + Z_T}, \quad \Gamma_L = \frac{Z_{inL} - Z_T}{Z_{inL} + Z_T} \tag{2}$$

For the perfect matching at both ports, $|\Gamma_S| = |\Gamma_L|$ should be [22]. The relation for Θ_T is $\Gamma_L^* = e^{-j2\Theta_T}\Gamma_S$ where Γ_L^* is the complex conjugate of Γ_L. Applying the two conditions to both Z_{inS} and Z_{inL} gives the design formulas for Z_T and Θ_T as

$$Z_T = \sqrt{\frac{R_e\left(Z_{inL}\right)\left|Z_{inS}\right|^2 - R_e\left(Z_{inS}\right)\left|Z_{inL}\right|^2}{R_e\left(Z_{inS}\right) - R_e\left(Z_{inL}\right)}} \tag{3a}$$

$$\tan\Theta_T = Z_T\frac{I_m\left(Z_{inS}\right) - I_m\left(Z_{inL}\right)}{R_e\left(Z_{inS}\right)R_e\left(Z_{inS}\right) + I_m\left(Z_{inS}\right)I_m\left(Z_{inS}\right) - Z_T^2} \tag{3b}$$

where Z_T should be of real values.

The *ABCD* parameters of the NAIT are

$$A = A_T\left(A_{Ta} + j\omega LC_{Ta}\right) + B_T C_{Ta} \tag{4a}$$

$$B = A_T\left(B_{Ta} + j\omega LD_{Ta}\right) + B_T D_{Ta} \tag{4b}$$

$$C = \left(jA_T S + C_T\right)\left(A_{Ta} + j\omega LC_{Ta}\right) + \left(jB_T S + D_T\right)C_{Ta} \tag{4c}$$

$$D = \left(jA_T S + C_T\right)\left(B_{Ta} + j\omega LD_{Ta}\right) + \left(jB_T S + D_T\right)D_{Ta} \tag{4d}$$

where $S = Z_o^{-1}tan\Theta_o$,

$$\begin{bmatrix} A_T & B_T \\ C_T & D_T \end{bmatrix} = \begin{bmatrix} cos\Theta_T & jZ_T sin\Theta_T \\ j\dfrac{sin\Theta_T}{Z_T} & cos\Theta_T \end{bmatrix} \tag{4e}$$

$$\begin{bmatrix} A_{Ta} & B_{Ta} \\ C_{Ta} & D_{Ta} \end{bmatrix} = \begin{bmatrix} cos\Theta_{Ta} & jZ_{Ta}sin\Theta_{Ta} \\ j\dfrac{sin\Theta_{Ta}}{Z_{Ta}} & cos\Theta_{Ta} \end{bmatrix} \tag{4f}$$

The phase delay Φ of the NAIT [8], [18] is

$$\Phi = tan^{-1}\left\{-j\left(\frac{B + CR_S R_L}{AR_L + DR_S}\right)\right\} \tag{5}$$

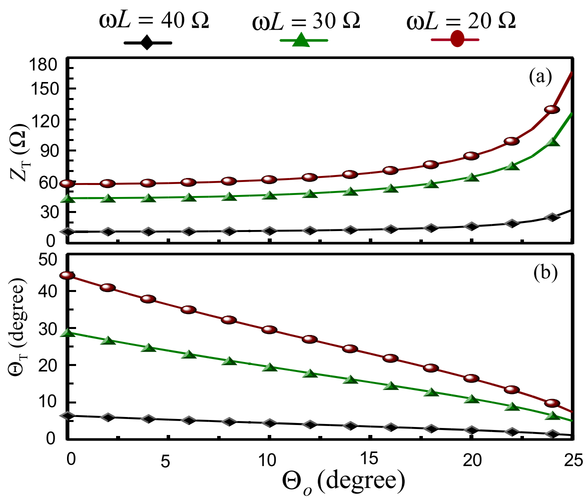

FIGURE 2. Calculation results for different values of ω_L (a) Z_T (b) Θ_T.

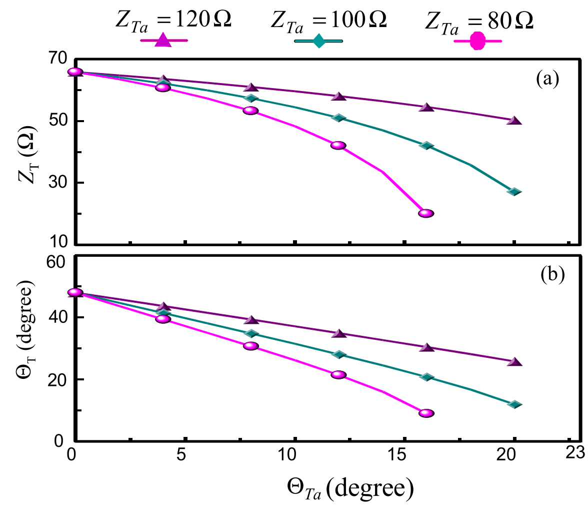

FIGURE 3. Calculation results for different values of Z_{Ta} (a) Z_T (b) Θ_T.

B. DESIGN PARAMETERS AND FREQUENCY RESPONSES

Since the design formulas (3) are only for the characteristic impedances of Z_T and the electrical lengths of Θ_T, other parameters should be determined arbitrarily. For the short phase delays between R_S and R_L, the characteristic impedances of Z_T should be lower than those of Z_{Ta}, and bigger differences between Z_T and Z_{Ta} give shorter total TLs, based on designs [3], [8]. Fixing at $Z_{Ta} = 127\ \Omega$, $\Theta_{Ta} = 5^o$ and $Z_o = 50\ \Omega$ arbitrarily, the calculations for Z_T and Θ_T were carried out for $R_S = 100\ \Omega$ and $R_L = 50\ \Omega$, varying ωL and Θ_o, and the calculation results are plotted in Fig. 2.

The characteristic impedances of Z_T in Fig. 2(a) increase gradually with the electrical lengths of Θ_o, while the electrical lengths of Θ_T decrease gradually with Θ_o. The plots in Fig. 2 find that lower values of Z_T and Θ_T can be obtained with higher values of ωL, in any case.

Other calculations were carried out, varying Z_{Ta} and Θ_{Ta} and fixing at $\omega L = 20\ \Omega$, $Z_o = 50\ \Omega$ and $\Theta_o = 5^o$ arbitrarily, and the calculation results for Z_T and Θ_T are plotted in Fig. 3(a) and (b), respectively. The plots in Fig. 3 show that the lower values for Z_T and Θ_T can be obtained with higher values of Z_{Ta} and Θ_{Ta}.

Several NAITs listed in Table 1 were simulated, and the frequency responses are plotted for $\Theta_T = 6.4^o$, $\Theta_T = 7.77^o$, $\Theta_T = 11.0^o$ and $\Theta_T = 13.8^o$ in Fig. 4 where f_0 and f are design and operating frequencies, respectively, and frequency responses of $|S_{11}|$ and phase responses of S_{21} are in Fig. 4(a) and (b), respectively. All the matching responses in Fig. 4(a) are about the same, even with the different design parameters (sizes). The phase delay of the NAIT for $\Theta_T = 6.4^o$ is $\Phi = 47.2^o$ at f_0, far less than 90^o of the conventional ones, and other ones for $\Theta_T = 7.77^o$, $\Theta_T = 11.0^o$ and $\Theta_T = 13.8^o$ are about the same. The main reason for the about same frequency responses is that the Z_T and Θ_T in Fig. 1 can be changed at the same time for the best performance, which can be regarded as a big advantage for the design flexibilities and size reduction.

TABLE 1. Design parameters of NAITs.

$R_S = 100\ \Omega$ and $R_L = 50\ \Omega$; $Z_{Ta} = 127\ \Omega$, $\Theta_{Ta} = 5^o$, $Z_o = 50\ \Omega$			
Z_T	Θ_T	Θ_o	ωL
11.14 Ω	6.4°	0°	40 Ω
48.0 Ω	7.77°	20°	35 Ω
64.2 Ω	11.0°	20°	30 Ω
75.7 Ω	13.8°	20°	25 Ω

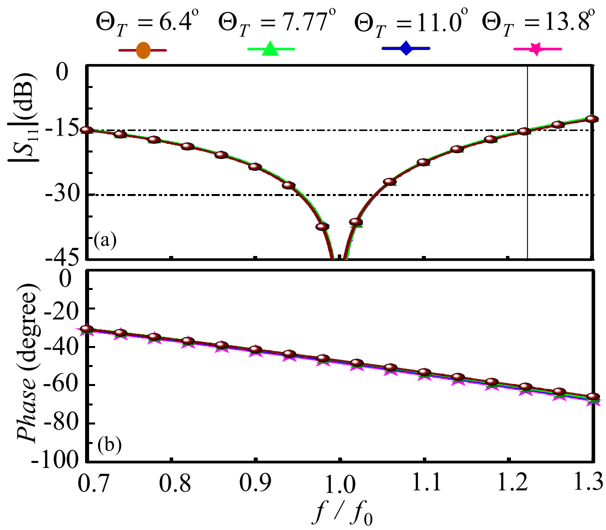

FIGURE 4. Frequency responses of NAITs. (a) $|S_{11}|$. (b) Phase responses of S_{21}.

III. VERIFICATION AND CMPARISONS

When $\Theta_o = 0^o$, the NAIT is the same as the AITs in [6]. When $Z_T = Z_{Ta}$ and $\Theta_T = \Theta_{Ta}$ with $\Theta_o = 0^o$, the NAIT is the same as the symmetric impedance transformers in [6] and also the same as symmetric $L_{S1}-$ type in [17] with $N = 1$. When $L = 0$, the NAIT is the same as MCCT in [3] and [5].

TABLE 2. Design and fabrication parameters for two NAITs.

$R_s = 100\ \Omega$, $R_L = 50\ \Omega$, $L = 18\ nH$	
$\Theta_{Ta} = 0^o$	$Z_o = 50\ \Omega$, $\Theta_o = 20^o$, $Z_T = 75.75\ \Omega$, $\Theta_T = 14.2^o$. open stub: $w = 2.33\ mm$, $\ell = 39.56$ mm. $TL: w = 1.17\ mm$, $\ell = 28.67\ mm$
$\Theta_o = 0^o$	$Z_T = 38.3\ \Omega$, $\Theta_T = 24.3^o$; $Z_{Ta} = 124\ \Omega$, $\Theta_{Ta} = 4.5^o$. TL with $Z_T: w = 3.4\ mm$, $\ell = 47.4\ mm$; TL with $Z_{Ta}: w = 0.38\ mm$, $\ell = 9.3\ mm$.

When $\Theta_o = 0^o$ and $L = 0$, the NAIT is the same as the CVT in [1] and [8]. When $L = 0$ and $\Theta_{Ta} = 0^o$, the NAIT is the same as the CCT in [1] and [8]. When $\Theta_T = \Theta_{Ta} = 0^o$, the NAIT is the same as that of L-section in [20].

That is, the NAIT in Fig. 1 contains most of the conventional asymmetric and symmetric impedance transformers. For the verification, two NAITs with $\Theta_{Ta} = 0^o$ and $\Theta_o = 0^o$ will be measured, and the impedance transformers [6] will be discussed and compared to highlight the advantages of the NAITs for $R_S = 100\ \Omega$ and $R_L = 50\ \Omega$.

A. MEASUREMENTS FOR VERIFICATION

Two NAITs with $\Theta_{Ta} = 0^o$ and $\Theta_o = 0^o$ were designed at a design frequency of 300 MHz, and fabricated on a substrate (RT/duriod 5870, $\varepsilon_r = 2.33$, $H = 31\ mil$). For both NAITs, $L = 18\ nH$ is fixed. For the first design with $\Theta_{Ta} = 0^o$, $Z_o = 50\ \Omega$ and $\Theta_o = 20^o$ are determined arbitrarily. Then the final values for Z_T and Θ_T can be calculated using (3) as $Z_T = 75.75\ \Omega$ and $\Theta_T = 14.2^o$. For the second NAIT with $\Theta_o = 0^o$, if the values for Z_{Ta} and Θ_{Ta} are selected arbitrarily as $Z_{Ta} = 124\ \Omega$ and $\Theta_{Ta} = 4.5^o$, the values for Z_T and Θ_T can be obtained as $Z_T = 38.3\ \Omega$ and $\Theta_T = 24.3^o$. The open stub with Z_o can be replaced with a chip capacitor, and therefore the total TL for the first NAIT is only 14.2^o long to transform $R_s = 100\ \Omega$ into $R_L = 50\ \Omega$. Comparing a conventional 90^o impedance transformer, the length of 14.2^o is very tiny and can be reduced further using T- and $\Pi-$ types with N in [21], because the characteristic impedance of Z_T is still 75.75 Ω.

Design and fabrication parameters are collected in Table 2 where w and ℓ are width and length of a TL, respectively, and the fabricated NAITs are depicted in Fig. 5(a). Even though the termination impedance of R_s is not 50 Ω, the two NAITs can be measured without any additional impedance transformer.

Each fabricated NAIT in Fig. 5(a) was measured in the form in Fig. 5(b) where ports ① and ② are terminated in 50 Ω, and the physical lengths of the feeding lines are L. Then, the measured data are saved in ADS (Advanced Design System, a circuit simulator) data item as shown in Fig. 5(c) [23, Fig. 11]. Removing the feeding line effect at ports ① and ② by connecting the physical lengths of -L in Fig. 5(c), and simulating them once more with terminating ports ① and ② in 100 Ω and 50 Ω, respectively, the measured data with $R_s = 100\ \Omega$ and $R_L = 50\ \Omega$ can be obtained.

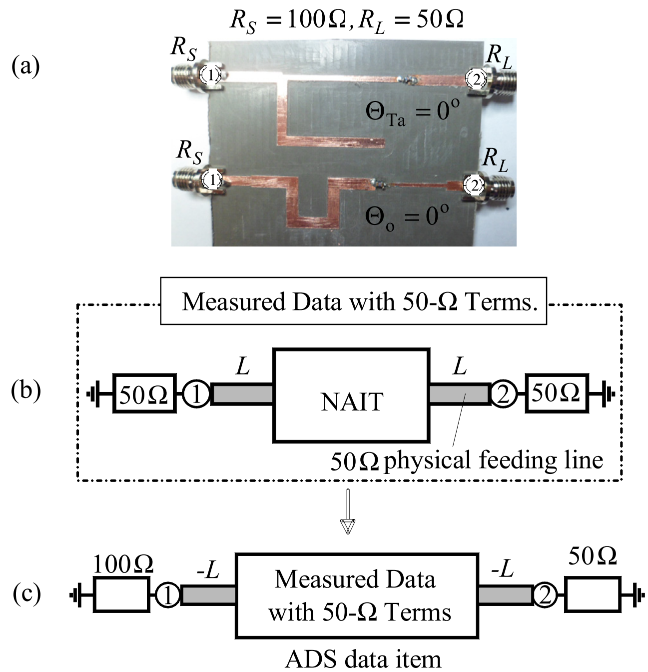

FIGURE 5. Fabricated NAITs and measuring method without use of any impedance transformer. (a) NAITs. (b) and (c) Measuring method.

TABLE 3. Design parameters of NAITs with $\Theta_o = 0^o$.

Z_T	Θ_T	Z_{Ta}	Θ_{Ta}	ωL
15.3 Ω	8.67^o	127 Ω	10^o	30 Ω
22.1 Ω	13.1^o	127 Ω	4^o	40 Ω
26.9 Ω	16.1^o	127 Ω	6^o	35 Ω
30.9 Ω	18.7^o	127 Ω	8^o	30 Ω

The predicted and measured frequency responses are compared in Fig. 6 where solid and dotted lines are measured and predicted ones, and the responses of $|S_{21}|$ and $|S_{11}|$ are in Fig. 6(a) and (b), respectively. As far as the matching properties are verified, the phase performance is also verified. So, the phase responses are not treated.

The measured bandwidths with 15-dB return loss in Fig. 6(b) are 53.3 % (200-360 MHz) for both. At 300 MHz, measured $|S_{21}|$ and $|S_{11}|$ are −0.14 dB and −26.86 dB, respectively for the NAIT with $\Theta_{Ta} = 0^o$, while those for the NAIT with $\Theta_o = 0^o$ are −0.11 dB and −32.75 dB, respectively. Quite good agreement between measured and predicted results is achieved.

B. COMPARISONS WITH IMPEDANCE TRANSFORMERS IN [6]

As mentioned above, when $\Theta_o = 0^o$, the NAITs in Fig. 1 are the same as those in [6]. Four NAITs with $\Theta_o = 0^o$ were designed in Table 3 and simulated. The frequency responses for $|S_{11}|$ and phase responses of S_{21} are plotted in Fig. 7(a) and (b), respectively where they are expressed as $\Theta_T = 8.67^o$, 13.1^o, 16.1^o and 18.7^o. All the responses

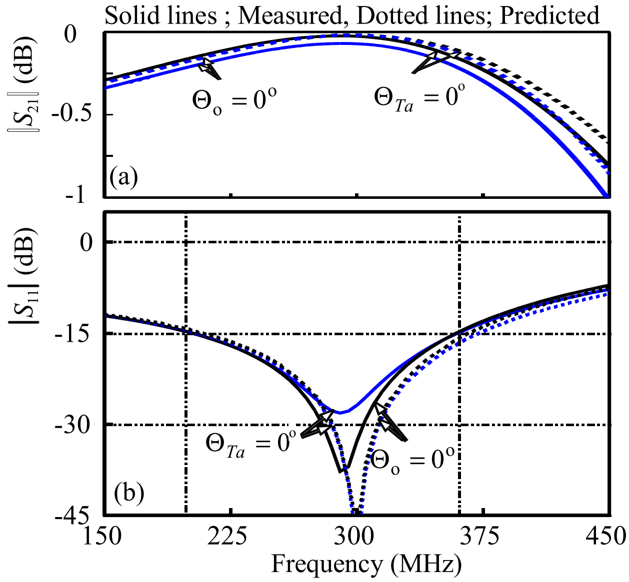

FIGURE 6. Measured frequency responses. (a) $|S_{21}|$. (b) $|S_{11}|$.

TABLE 4. Design parameters of conventional impedance transformers [6].

Symmetric	Asymmetric	
$Z_T = Z_{Ta}$, $\Theta_T = \Theta_{Ta}$	Z_T, Θ_T	Z_{Ta}, Θ_{Ta}
64.8 Ω, 85/2°	65.2 , 45°	64.3, 40°
ωL = 11.34 Ω	ωL = 11.33 Ω	
45.0 Ω, (65/2)°	46.8, 35 °	43.2, 30 °
ωL = 42.0 Ω	ωL = 41.96 Ω	
11.7 Ω, (18.7/2)°	10.8, 8.67°	12.4, 10°
ωL = 68.77 Ω	ωL = 68.79 Ω	

for $\Theta_T = 8.67^o$, 13.1^o, 16.1^o and 18.7^o in 7(a) are about the same like those in Fig. 4(a), regardless of total TLs of Θ_{Tot}, or, $\Theta_{Tot} = \Theta_T + \Theta_{Ta}$, while the phase delay Φ for $\Theta_T = 8.67^o$ in Fig. 7(b) is 48.9° at f_0.

To compare the NAITs with the impedance transformers [6], the design parameters in [6] are, based on [6, eqs. (19)-(24)], written in Table 4 for symmetric and asymmetric cases. For the symmetric ones, the design parameters are the same as those of $L_{s1}-$ types with $N = 1$ in [17, Fig. 7(d)]. The frequency responses [6] are plotted in Fig. 8 where the frequency responses of $|S_{11}|$ are in Fig. 8(a), while the phase responses of S_{21} are in Fig. 8(b). The frequency responses for symmetric and asymmetric impedance transformers are about the same in Fig. 8 for the same values of Θ_{Tot}, and the bandwidths are proportional to Θ_{Tot} in Fig. 8(a) just like the typical passive components. All the phase delays of Φ are 90° at f_0 in Fig. 8(b).

To highlight the advantages of the NAITs further, one NAIT with $\Theta_{Tot} = 18.67^o$ or $\Theta_T = 8.67^o$ in Table 3, the smallest, is compared with two AITs in [6] with $\Theta_{Tot} = 18.67^o$ and 65° in Fig. 9 where blue solid response is for the NAIT, while two dotted lines are for the AITs in [6]. The bandwidth of the NAIT for $\Theta_{Tot} = 18.67^o$ is 54 %, while

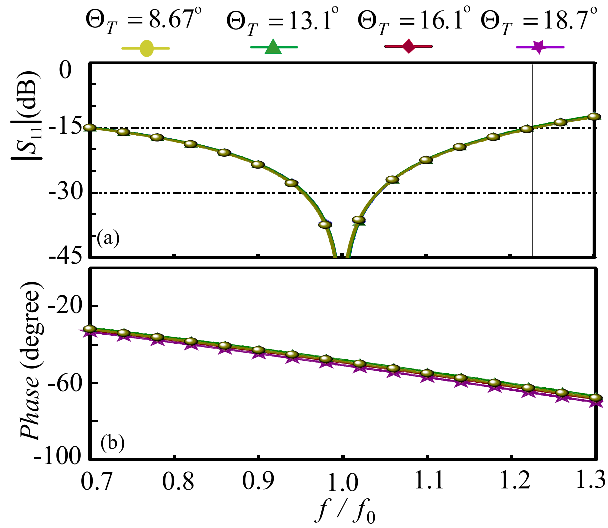

FIGURE 7. Frequency response of NAITs with $\Theta_o = 0^o$. (a) $|S_{11}|$. (b) Phase responses of S_{21}.

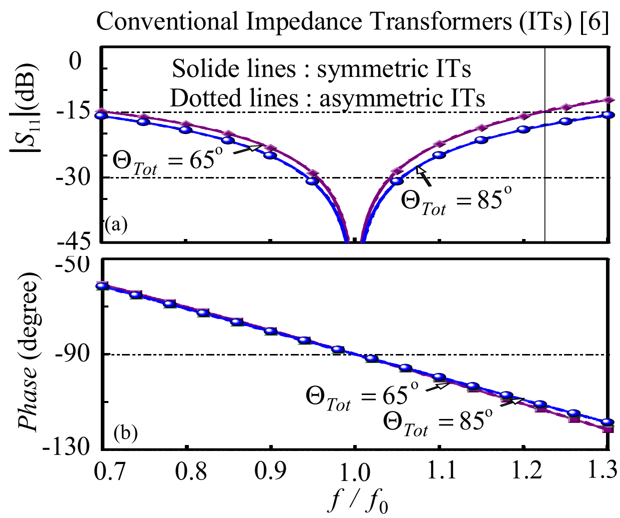

FIGURE 8. Frequency response of symmetric and asymmetric impedance transformers in [6]. (a) $|S_{11}|$. (b) Phase responses of S_{21}.

the AIT with $\Theta_{Tot} = 18.67^o$ [6] is only 32.5 %. On the other hand, the bandwidth of the AIT for $\Theta_{Tot} = 65^o$ [6] is slightly smaller than that of the NAIT with $\Theta_{Tot} = 18.67^o$, even if the NAIT is three times shorter. In other words, the AITs in [6] have no additional property which the typical AITs possess inherently (wider bandwidths with smaller sizes and arbitrary phase delays).

IV. APPLICATION TO NAIT 3-dB POWER DIVIDERS

The NAITs in Fig. 1 can be utilized for various applications, and one of them is for three-port 3-dB PDs which will be treated further in this section. Since the two outputs of the PDs are in-phase, the phase delay responses of the NAITs do not need to be treated.

A. NAIT POWER DIVIDERS

The NAIT PD with equal termination impedances of R_L is depicted in Fig. 10 where two identical NAITs are connected in parallel at port ①, and an isolation circuit with

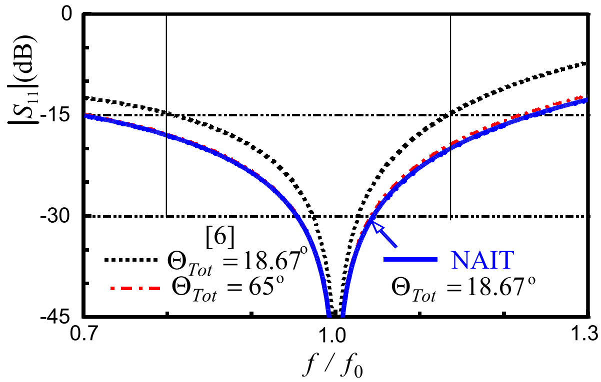

FIGURE 9. One NAIT is compared with two AITs in [6].

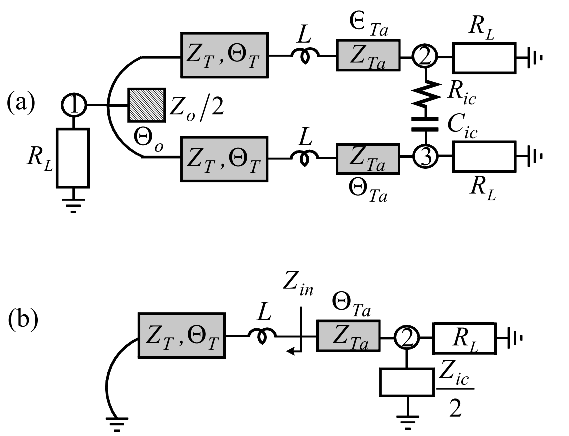

FIGURE 10. NAIT PD and its odd-mode equivalent circuit. (a) NAIT PD. (b) Odd-mode equivalent circuit.

a resistance of R_{ic} and a capacitance of C_{ic} is connected between ports ② and ③. Due to the available symmetry, the even- and odd-mode excitation analyses are possible. The even-mode equivalent circuit is the NAIT in Fig. 1 with $R_S = 2R_L$, and the odd-mode equivalent circuit is in Fig. 10(b) where half of the isolation impedance of $Z_{ic}/2$ is connected to the ground, and an input impedance looking into the inductance of L is expressed as Z_{in}.

For the isolation impedance of Z_{ic}, the following relation holds;

$$Y_{Ta}\frac{Y_{in} + jY_{Ta}tan\Theta_{Ta}}{Y_{Ta} + jY_{in}tan\Theta_{Ta}} + \frac{2}{Z_{ic}} = \frac{1}{R_L} \tag{6}$$

where $Y_{Ta} = Z_{Ta}^{-1}$, $Y_{in} = Z_{in}^{-1} = (j\omega L + jZ_T tan\Theta_T)^{-1}$.

The isolation impedance of Z_{ic} from (6) is expressed as

$$Z_{ic} = 2\left(\frac{1}{R_L} - Y_{Ta}\frac{Y_{in} + jY_{Ta}tan\Theta_{Ta}}{Y_{Ta} + jY_{in}tan\Theta_{Ta}}\right)^{-1} \tag{7}$$

and can also be expressed with the phase delay Φ as

$$Z_{ic} = 2R_L \sin\Phi\,(\sin\Phi - j\cos\Phi) \tag{8}$$

The isolation impedances were, based on (7), calculated, varying ωL and Θ_o and fixing $R_L = Z_o = 50\ \Omega$, $Z_{Ta} = 105\ \Omega$ and $\Theta_{Ta} = 4°$. The calculation results are plotted in Fig. 11 where the resistances of R_{ic} are

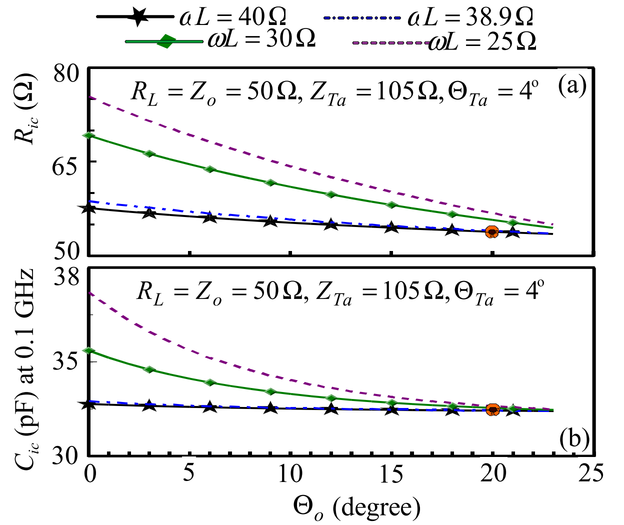

FIGURE 11. Isolation impedances. (a) R_{ic}. (b) C_{ic} at 0.1 GHz.

in Fig. 11(a),while the capacitance values of C_{ic} at 0.1 GHz in Fig. 11(b). Both values decrease with Θ_o.

B. DESIGN AND MEASUREMENTS OF NAIT PD

The NAIT PD was designed at 100 MHz and fabricated on the substrate (RT/duroid 5880, $\varepsilon_r = 2.2$, $H = 62\ mil$). The conventional PD consists of two 90° TLs with the characteristic impedances of 70.71Ω. At 100 MHz and 1 GHz, the physical lengths of the 90° TL on the substrate are 555.4 mm and 55.5 mm, respectively, requiring a large occupied area even at 1 GHz. Thus, the design of NAIT PD at 100 MHz should focus on the compact size, and any sophisticate design method is demanded. For this, the final values for Z_T and Θ_T should be as low as possible to reduce the TLs with Z_T and Θ_T further, keeping the inherent bandwidths. Referring to the calculation results for Z_T and Θ_T in Figs. 2 and 3, higher values of ωL, Z_{Ta} and Θ_{Ta} give lower values for Z_T and Θ_T. However, since the TL with Z_{Ta} cannot be reduced further due to high value of Z_{Ta}, it does not need to be too long. The isolation impedances should be soldered with the available chip resistors and capacitors with discrete values.

Considering all the relations for the compact sizes, $Z_{Ta} = 105\ \Omega$ and $\Theta_{Ta} = 4°$ along with $Z_o = 50\ \Omega$ were selected arbitrarily. With available chip resistors, capacitors and inductors, the suitable solutions for ωL and Θ_o can be found by sweeping the values in Fig. 11 as $\omega L = 38.9\ \Omega$ ($L = 62$ nH) and $\Theta_o = 20°$ (see red dots in Fig. 11). Then, the final values for Z_T and Θ_T can be calculated as $Z_T = 46.8\ \Omega$ and $\Theta_T = 7.6°$ using (3).

The design parameters for the NAIT are written in Fig. 12 (a). The open stub with $Z_o = 50\ \Omega$ and $\Theta_o = 20°$ can be replaced with a chip capacitor with 11.58 pF at $f_o = 100$ MHz. However, there is no such value of chip capacitor and soldering is also of a problem. The general open stub with Z_{op} and Θ_{op} in Fig. 12(b) can be converted into the stepped impedance open stub consisting of two different TLs and an available chip capacitor with C_{av}. One TL with Z_{th} and Θ_{th}

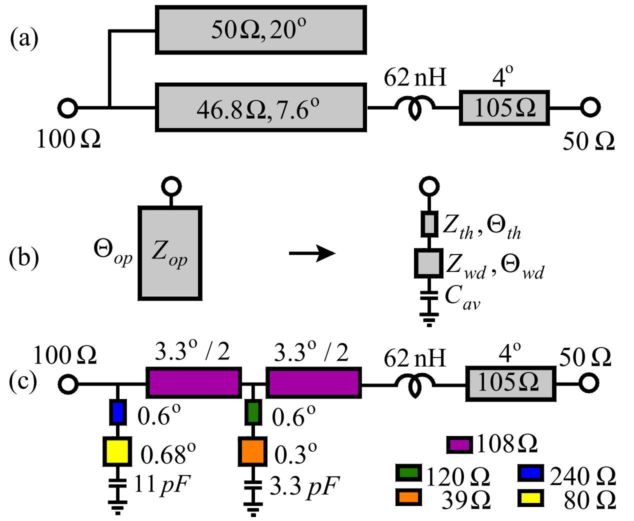

FIGURE 12. Designed NAIT and its compact form. (a) NAIT. (b) Transformation of an open stub into compact stepped impedance open stub with an available chip capacitor. (c) Compact NAIT.

should be very thin to minimize the soldering problem, and another TL with Z_{wd} and Θ_{wd} should be as wide as possible to shorten the open stub. The relations in Fig. 12(b) are

$$Y_{op} \tan \Theta_{op} = Y_{th} \frac{\xi_{+} Y_{wd} + \xi_{-} Y_{th} \tan \Theta_{th}}{\xi_{-} Y_{th} - \xi_{+} Y_{wd} \tan \Theta_{th}} \tag{9}$$

where $Y_{op} = Z_{op}^{-1}$, $Y_{th} = Z_{th}^{-1}$, $Y_{wd} = Z_{wd}^{-1}$ and

$$\xi_{+} = \omega C_{av} + Y_{wd} \tan \Theta_{wd} \tag{9a}$$

$$\xi_{-} = Y_{wd} - \omega C_{av} \tan \Theta_{wd} \tag{9b}$$

For the single open stub with $Z_{op} = Z_o = 50\ \Omega$ and $\Theta_{op} = \Theta_o = 20^{o}$ in Fig. 12(a), the value for the thin-line characteristic impedance of Z_{th} was determined as $Z_{th} = 240\ \Omega$, as high as possible. The value for the wider-line characteristic impedance of Z_{wd} was selected as low value as possible as $Z_{th} = 80\ \Omega$. The available chip capacitance value C_{av} should be less than 11.58 pF and was selected as $C_{av} = 11$ pF. Then only two unknown variables for Θ_{th} and Θ_{wd} are left in the right term with the given value of the left term in (9). The two values for Θ_{th} and Θ_{wd} were calculated as $\Theta_{th} = 0.6^{o}$ and $\Theta_{wd} = 0.68^{o}$ to have the small difference between them. For the fabrication, since two identical stepped impedance open stubs are connected in parallel, the characteristic impedances of 240 and 80 Ω become to be of half values, and the capacitance of 11 pF to be doubled.

Since the characteristic impedance of Z_T is still 46.8 Ω, the TL with Z_T and Θ_T can be reduced further to a T-type consisting of two identical TLs with the characteristic impedance of 108 Ω and the electrical lengths of 3.3°/2 and one open stub as shown in Fig. 12(c) [19]. Similarly, the open stub of the T-type is also reduced and realized as the stepped impedance open stub with an available chip capacitor with 3.3 pF. The TL with Z_T is 7.6° long, while the total TLs of the T-type are only 3.3° long. Nevertheless, the bandwidth of the T-type does not shrink, referring to [21, Fig. 9], which is the reason that the targeting values for Z_T and Θ_T should be as low as possible.

TABLE 5. Design and fabrication parameters for NAIT PD.

Design Parameters ($R_L = 50\ \Omega$)
$Z_o = 50\ \Omega$, $\Theta_o = 20^{o}$, $Z_T = 46.8\ \Omega$, $\Theta_T = 7.6^{o}$, $Z_{Ta} = 105\ \Omega$, $\Theta_{Ta} = 4^{o}$ and $L = 62\ nH$. One TL with Z_T → T-type with $N = 1$ in Fig. 12(c). $Z_{ic} = (54.0\text{-}j49.8)\ \Omega$.
Fabrication Parameters ($R_{ic} = 54.2\ \Omega$, $C_{ic} = 32\ pF$)
TL with 105 Ω : $w = 1.25$ mm, $\ell = 25.2$ mm; TL with 108 Ω : $w = 1.16$ mm, $\ell = 10.4$ mm ; TL with 120 Ω and 0.6° : $w = 0.9$ mm, $\ell = 3.79$ mm ; TL with 39 Ω and 0.3° : $w = 6.9$ mm, $\ell = 1.8$ mm. Two parallel open stubs (TL with 120 Ω and 0.6° : $w = 0.9$ mm, $\ell = 3.8$ mm ; TL with 40 Ω and 0.68° : $w = 6.67$ mm, $\ell = 4.0.9$ mm

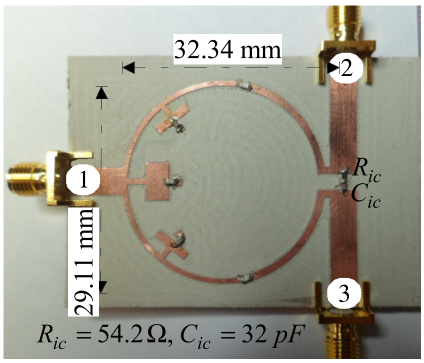

FIGURE 13. Fabricated NAIT PD.

The final design parameters are illustrated in Fig. 12(c), and design and fabricated parameters are collected in Table 5 where the isolation impedance was calculated as $Z_{ic} = (54.0\text{-}j49.8)\ \Omega$ and realized with available chip resistor ($R_{ic} = 54.2\ \Omega$) and capacitor ($C_{ic} = 32\ pF$). The fabricated NAIT PD is illustrated in Fig. 13, and the measured frequency responses are compared with the predicted ones in Fig. 14. The measured bandwidth of $|S_{11}|$ with 15-dB return loss is 58 % (130-72 MHz = 58 MHz). The measured power division of $|S_{21}| = -3.22$ dB and $|S_{31}| = -3.33$ dB, $|S_{11}| = -34.7$ dB and the isolation of $|S_{23}| = -22.6$ dB are achieved at 100 MHz.

C. COMPARISONS WITH CONVENTIONAL POWER DIVIDERS

The NAIT PD is compared to the conventional compact ones in Table 6. The total TLs of each fabricated NAIT is 7.3° long in Fig. 12(c), leading to 14.6° long for the PD in Fig. 13. In this case, the size can be reduced by 99.3 %, compared to the conventional typical ones with 90° TLs. In [5], two MCCTs are employed, but the total TLs are 39.68° long, leading to 95.1 % size reduction. In [6], two different $L_{S1}-$ types with $N = 1$ are employed, but the total

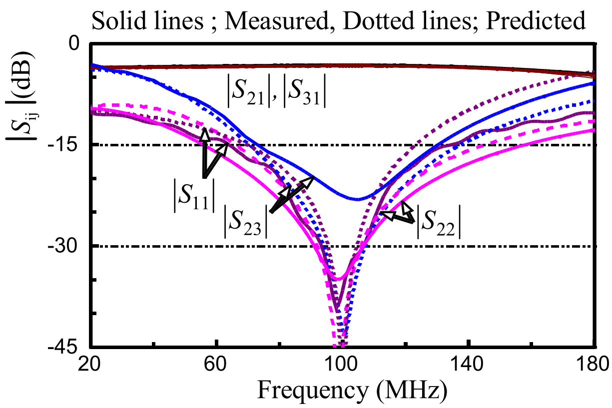

FIGURE 14. Measured and predicted frequency responses of NAIT PD.

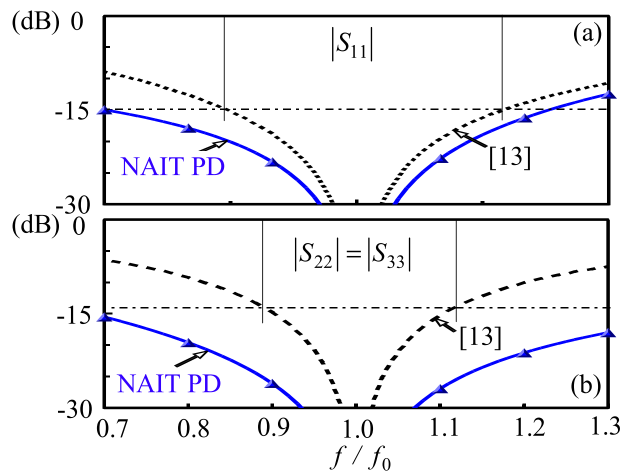

FIGURE 15. Compared frequency responses. (a) $|S_{11}|$. (b) $|S_{22}| = |S_{33}|$.

TABLE 6. Comparisons with conventional compact PDs.

	Miniaturization methods	15-dB BW ($|S_{11}|$)	Total TL lengths
This work	NAITs	58 %	14.6°
[5]	MCCTs	68 %	39.68°
[6]	L_{S1} −type	38 %	81.46°
[9]	CRLH TLs	< 26 %	76°
[10]	DGS	~43%	~54.2°
[11]	SIW	~27 %	~ 90°
[12]	T-type	82.7 %	415.5°
[13]	Small phase delay	14.18 %	25.4°

TLs are 81.46° long. Occupied area is reduced by 79.5 %. Nevertheless, the bandwidth is only 38 %, much smaller than that of the measured NAIT PD in this paper.

In [9], lumped-element equivalent circuits (CRLH TLs) are implemented for the compact size. However, the bandwidths are less than 26 % [9, Table 3], and the total TLs are 76° long at the first design frequency, 82.1 % size reduction. In [10], an etched pattern on ground plane should be involved, and the required total TLs are 54.2° long. In [11], the PD is fabricated with SIW (substrate integrated waveguide) structure, and 75 % size reduction is written, leading to the total TLs of 90°. Nevertheless, the bandwidth is much smaller than that of the proposed NAIT PD. In [12], to reduce the size of a TL, T-types with two additional 180° TLs are applied, leading to the total TL length of 415.5° which can be calculated based on the given dimensions, substrate with the dielectric constant and design frequency of 2.45 GHz.

The total TLs of [13] are 25.4° long, about 1.8 times longer than those of the NAIT PD but the smallest among the conventional compact PDs in Table 6. Based on the ideal design parameters, the frequency responses of the NAIT PD and [13] are compared in Fig. 15 where blue solid and black dotted lines are those of the NAIT PD and [13], respectively. The design frequencies of f_0 are different as 100 MHz and 500 MHz, respectively, but for the fair comparisons, the frequency responses are normalized. The measured 15-dB return loss bandwidth of $|S_{11}|$ is 14.18 % [13], far smaller than that of the NAIT PD as shown in Fig. 15(a). The simulated $|S_{22}| = |S_{33}|$ bandwidths in Fig. 15 (b) are 77 % and 20 % for the NAIT PD and [13], respectively. The open stub [13] at port ① contributes to the size reduction, but the short stubs at ports ② and ③ can cause the small bandwidths even with any advantage to lower characteristic impedances of TLs.

The compared results in Table 6 and Fig. 15 demonstrate that the NAIT PD has a definite advantage in terms sizes and bandwidths.

V. CONCLUSION

In this paper, the NAIT is suggested for V(U)HF compact PDs, and design formulas are derived. The NAIT consists of one series inductance, by which lower characteristic impedances of the TLs can be generated, which is a big advantage to reduce the sizes more. As demonstrated, the frequency responses are about the same, regardless of the sizes, which is also another advantage for the design flexibility and further size reductions.

Since the suggested NAITs can have arbitrary phase shifts, they can be used for not only impedance transformers but also phase shifters, as the AITs possess inherently. In this paper, the application of the NAITs is verified only for the compact V(U)HF PDs, but they can be utilized for other applications diversely.

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