IEEE Access
Multidisciplinary : Rapid Review : Open Access Journal

Received May 21, 2019, accepted June 3, 2019, date of publication June 5, 2019, date of current version June 26, 2019.
Digital Object Identifier 10.1109/ACCESS.2019.2921233

Electrical Stability and Flicker Noise of Thin-Film Heterojunction FETs on Poly-Si Substrates

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ABSTRACT Electrical stability and flicker (1/f) noise of thin-film heterojunction field-effect transistors (HJFETs) comprised of hydrogenated amorphous Si (a-Si:H) gate and hydrogenated crystalline Si (c-Si:H) source and drain regions on small-grain poly-Si substrates are investigated and benchmarked against conventional thin-film transistors (TFTs). Despite the low growth temperature of a-Si:H and c-Si:H (~200 °C), HJFETs are found to have higher stability and lower flicker noise than conventional TFTs. These results may be attributed partly to the device structure and partly to the high-quality gate heterojunction of the HJFETs.

INDEX TERMS 1/f noise, heterojunctions, silicon devices, stability, thin film transistors.

I. INTRODUCTION

Thin-film Si heterojunction FETs (HJFETs) combine the low-cost large-area capability of hydrogenated amorphous Si (a-Si:H) with the high quality of crystalline Si (c-Si) [1]–[3]. The gate and source/drain regions of the HJFETs are formed by low-temperature (~200 °C) plasma-enhanced chemical vapor deposition (PECVD) of a-Si:H and hydrogenated crystalline Si (c-Si:H), respectively. The c-Si substrate may be polycrystalline [4], in which case the c-Si:H source/drain regions are also polycrystalline, due to the epitaxial growth of c-Si:H [5], [6]. Provided that the starting poly-Si substrates are also prepared by a low-temperature technique, such as excimer laser annealing (ELA) of doped a-Si:H, the HJFET process is compatible with low-cost flexible plastic substrates.

In this paper, the electrical stability and flicker noise of HJFET devices fabricated on small-grain poly-Si substrates [4] are investigated and benchmarked against conventional TFTs. High TFT stability is critical for applications such as active-matrix organic LED (AMOLED) displays [7]–[15], while low TFT flicker noise is critical for applications such as image sensors, amplifiers, and biosensors [16]–[20]. These results suggest that the higher stability and lower flicker noise observed in HJFETs may be attributed partly to the device structure and partly to the high quality of the a-Si:H/c-Si gate heterojunction.

The associate editor coordinating the review of this manuscript and approving it for publication was Ludovico Minati.

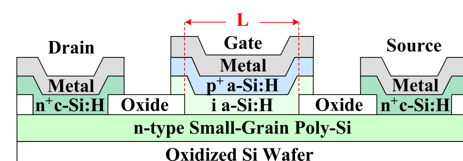

FIGURE 1. Schematic cross-section of fabricated HJFET devices [4].

II. DEVICE CHARACTERISTICS

The schematic cross-section of the fabricated HJFETs is given in Fig. 1. The small-grain poly-Si film has a thickness of ~55 nm, a grain size of ~50 nm, and a sheet resistance of ~500 KΩ/□. The a-Si:H and c-Si:H layers are grown in the same PECVD reactor at 200 °C. The c-Si:H layer has a resistivity of $\sim 5\times10^{-4}\Omega$.cm. The ~50 nm-thick etch-stop oxide layer is also grown by PECVD at ~200 °C. Further details regarding the fabrication process are available in [4].

The basic device structure and therefore the operation principles of the HJFETs are similar to junction FETs (JFETs), whereas conventional TFTs are similar to MOSFETs. The transfer and output characteristics of an HJFET with a channel width-to-length ratio of $W/L = 15\ \mu$m/7.5 μm are plotted in Figs. 2(a) and (b), respectively. The HJFET has a pinch-off voltage of $V_p \approx -0.35$ V and a subthreshold swing of 90 mV/dec. Larger pinch-off voltages (and therefore wider operation ranges) can be obtained by increasing the doping and/or thickness of the starting substrate [3]. For applications with large dynamic range requirements, larger swings can be obtained with circuit techniques [21]. The ON/OFF ratio

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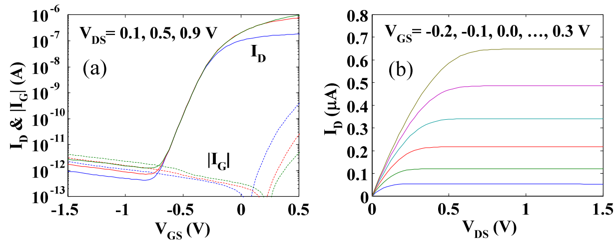

FIGURE 2. The measured (a) transfer and (b) output characteristics of an HJFET with poly-Si thickness of ~55 nm, and $W/L = 15$ μm/7.5 μm (© [2018] IEEE [4]).

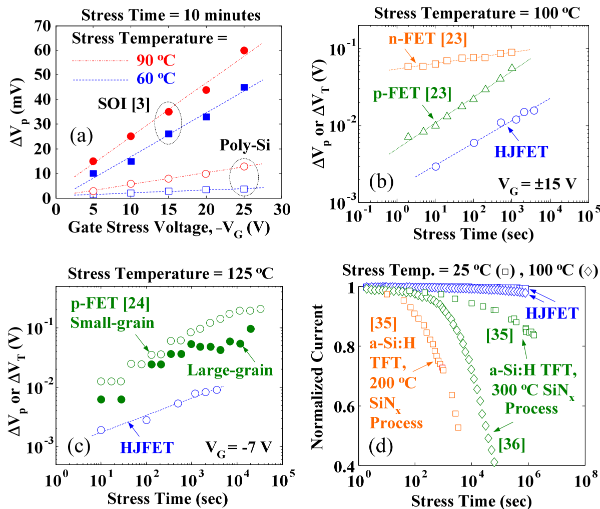

FIGURE 3. (a) Pinch-off voltage shift (ΔV_p) of HJFETs fabricated on small-grain poly-Si (this work) compared to (a) ΔV_p of HJFETs fabricated on SOI [3], (b) threshold voltage shift (ΔV_T) of large-grain n-channel and p-channel poly-Si TFTs reported in [23] (© [2018] IEEE [4]), and (c) ΔV_T of p-channel large-grain and small-grain poly-Si TFTs reported in [24], with drain and source terminals grounded during bias stress. (d) Stability of normalized drain current in saturation for small-grain poly-Si HJFETs (this work) and a-Si:H TFTs with gate nitride deposition temperature of 200°C [35] and 300°C [35], [36] at typical drive conditions for 1000 Cd/m^2 OLED brightness (starting $I_D \approx 5$ μA).

is expected to increase by at least 10X by using large-grain poly-Si prepared by excimer laser annealing of in-situ doped amorphous Si. Since the OFF current is proportional to the HJFET gate area ($W.L$), scaling down the device dimensions is also expected to increase the ON/OFF ratio [3]. The fabricated HJFETs are normally-ON devices and must be operated at negative or small positive gate voltages to avoid forward-biasing the gate heterojunction. Normally-OFF HJFETs can be obtained by incorporating a blocking layer in the gate stack [22].

III. ELECTRICAL STABILITY

The pinch-off voltage shift (ΔV_p) of the fabricated HJFETs subjected to negative bias temperature instability (NBTI) tests are plotted in Fig. 3(a), along with that of reference HJFETs fabricated on <100> single-crystalline Si-on-insulator (SOI) substrates [3]. The fabricated HJFETs exhibit a very low ΔV_p, interestingly lower than that of

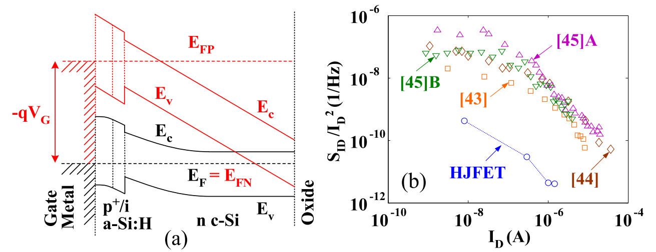

FIGURE 4. (a) Schematic energy band diagrams of the HJFET gate heterojunction in equilibrium ($V_G = 0$) and under negative bias tress ($V_G < 0$). Band-bending at the gate metal/p$^+$ a-Si:H and n c-Si/oxide interfaces is neglected for simplicity. The conduction and valence band offsets between a-Si:H and c-Si are ~0.1 eV and ~0.4 eV, respectively. (b) Normalized drain-current noise spectral density (S_{ID}/I_D^2) of the HJFETs (this work) with $W/L = 50$ μm/7.5 μm vs. I_D, at $V_{DS} = 0.1$ V, $f = 20$ Hz, compared to conventional poly-Si TFTs: $W/L = 40$ μm/20 μm, $V_{DS} = 0.2$ V, $f = 20$ Hz [43], $W/L = 50\mu$m/4 μm, $V_{DS} = 0.1$ V, $f = 20$Hz [44], $W/L = 80$ μm/60 μm, $V_{DS} = 0.3$ V, $f = 20$ Hz [45] (type A), and $W/L = 50$ μm/20 μm, $V_{DS} = 0.3$ V, $f = 20$ Hz [3] (type B). The reported substrates are large-grain poly-Si prepared by excimer laser crystallization, except for solid-phase-crystallized poly-Si in [45] (type B) (© [2018] IEEE [4]).

SOI HJFETs. The stability of conventional poly-Si TFTs has been widely reported in the literature [23]–[27]. While stability has improved considerably in other TFT technologies, and particularly for oxide TFTs, poly-Si TFTs largely remain the most stable devices [28]−[34]. As seen from Figs. 3(b) and 3(c), the fabricated HJFETs have a higher stability than the most stable poly-Si TFTs [23], [24], despite their much lower gate stack process temperature (~200°C) compared to conventional poly-Si TFTs (450−700 °C). As seen from Fig. 3(d), the fabricated HJFETs also have a higher stability than the most stable a-Si:H TFTs [35], [36].

The schematic energy band diagrams of the HJFET gate heterojunction in equilibrium (no bias) and under bias stress are given in Fig. 4(a). The defects associated with a-Si:H/c-Si interfaces are comprised of Si-Si dangling bonds with similar energy distribution and thermal equilibration kinetics to that of bulk a-Si:H [37], [38]. According to the defect pool model [39]–[41], raising the quasi-Fermi level for holes (E_{FP}) during the bias stress reduces the density of acceptor defects, resulting in the equilibrium Fermi-level (E_F) to move closer to the valence-band mobility-edge (E_V) in a-Si:H after the removal of the bias stress. This results in a larger built-in potential and therefore a less negative V_p which is observed experimentally. In contrast to a-Si:H TFTs where threshold voltage (V_T) has a linear dependence on defect density, the dependence of built-in potential and therefore V_p of HJFETs on defect density is logarithmic (i.e. sublinear). Therefore, the high stability of the HJFETs may be attributed to (i) a high-quality a-Si:H/c-Si interface and therefore a low density of metastable states (i.e. weak Si-Si bonds that may break or reconstruct), and (ii) the sublinear dependence of V_p on the density of charged defects (i.e. broken Si-Si bonds). The higher stability of the HJFETs fabricated on poly-Si substrates compared to the SOI references (Fig. 3(a)) may be attributed to a larger number of allowed Si-Si bonding

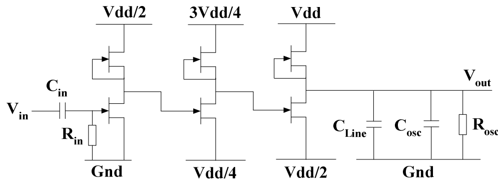

FIGURE 5. Schematic circuit diagram of the 3-stage HJFET amplifier, input bias network (R_{in} = 1 MΩ, C_{in} = 1 μF) and equivalent output circuit (line capacitance $C_{Line} \approx$ 100 pF, oscilloscope capacitance C_{osc} = 8 pF and resistance R_{osc} = 1 MΩ). HJFET dimensions are W/L = 60 μm/7.5 μm [4].

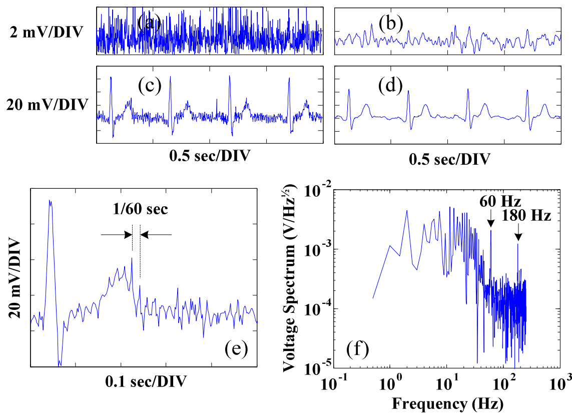

FIGURE 6. Output signal of an ECG simulator as acquired on an oscilloscope (a) with no amplification and (c) after amplification with the 3-stage HJFET amplifier [4]. (b) and (d) are the signals resulting from filtering the acquisition noise from (a) and (c), respectively. (e) is a higher magnification of a portion of (c), and (f) is the Fourier transform of (c).

reconstructions between a-Si:H and c-Si <100> than other orientations such as <111> [42].

IV. FLICKER NOISE

As reported in [4], HJFETs produce a substantially lower flicker noise than conventional poly-Si TFTs [43]–[45] (Fig. 4(b)). Flicker noise has a direct impact on applications such as acquisition and amplification of weak biological signals. The circuit diagram of a 3-stage amplifier suitable for capacitive reading of electrocardiogram (ECG) signals is given in Fig. 5. For simplicity, the HJFETs have the same dimensions, $W/L = 60\ \mu$m/7.5 μm, and DC bias ($V_{GS} = 0$ V and therefore $I_D \approx$ 0.6 μA). There are no DC-blocking capacitors between the stages to allow the routing of very low frequencies. Further details regarding the amplifier are available in [4]. At this bias condition, the input-referred noise voltage of the HJFETs (and therefore the amplifier) is $V_{n,in} \approx 2.1(1/\mathrm{f})^{1/2}\mu\mathrm{V/Hz}^{1/2}$, and the integrated $V_{n,in}$ in the range of 1 Hz-1 KHz is $\sim$5 $\mu\mathrm{V_{rms}}$. Therefore, the HJFET amplifier is suitable for acquisition of ECG signals ($\sim$200 $\mu\mathrm{V_{rms}}$). Without amplification, the ECG signal is not discernable on an oscilloscope (Fig. 6(a)), and cannot be reconstructed by signal processing (Fig. 6(b)). In contrast, the amplified signal is clearly discernable (Fig. 6(c)), and can be smoothed by filtering the acquisition noise (Fig. 6(d)). As seen from Figs. 6(e) and 6(f), the acquisition noise is mainly due to the harmonics of 60 Hz (picked up from the power line) and is not related to the HJFET flicker noise.

The physical origin of flicker noise has been discussed for over half a century but still remains unresolved and subject of active research. Nonetheless, Hooge's empirical model provides a simple approach for describing the experimentally observed flicker noise and it is particularly useful for comparing the devices fabricated in different technologies [46]–[48]. To this end, Hooge's model has been widely used for characterizing and benchmarking TFTs [44], [45], [49]–[54]. The well-known expressions for flicker noise in long-channel MOSFETs [46]–[57] (Table 1) are applicable to conventional TFTs as well, at least to the first order. However, HJFETs are rather analogous to JFETs. In contrast to MOSFETs, JFETs have been rarely studied, but it is known that the flicker noise behavior of JFETs is generally the same as MOSFETs [58]. It is also known that properly designed JFETs can achieve extremely low flicker noise [59]–[62]. For appropriate bench-marking, first-order expressions for HJFET flicker noise are derived in a form suitable for direct comparison with conventional TFTs, as described below.

A. MODEL

According to Hooge's empirical model [63], normalized current flicker noise (S_I/I^2) is inversely proportional to the total number of charge carriers (N) involved in conduction,

$$S_I/I^2 = \alpha_H/fN \tag{1}$$

where I is the current, S_I is the noise current spectral density, f is the frequency, and α_H is a dimensionless parameter known as the Hooge's parameter. For a homogenous sample, $1/N = q\mu_b R/l^2$, where q is the electric charge, R is the sample resistance, l is the sample length, and μ_b is the bulk mobility. For HJFETs, the dependence of channel resistance on the gate and drain bias must be taken into account. The depletion region width, $w_d(x)$, at a point x along the channel of an n-channel HJFET (Fig. 7(a)), is given by

$$\begin{aligned} w_d(x) &= \left(\frac{V_{bi}-V_G+v_{ch}(x)}{qN_D/2\varepsilon_{Si}}\right)^{1/2} \\ &= t_{Si}\left(\frac{V_{bi}-V_G+v_{ch}(x)}{V_{bi}-V_p}\right)^{1/2} \end{aligned} \tag{2}$$

where ε_{Si} is the dielectric constant of Si, $v_{ch}(x)$ is the channel potential, N_D is the concentration of active donors in the channel, V_{bi} is the built-in potential of the gate heterojunction, t_{Si} is the channel thickness, and $V_p = V_{bi} - qN_D t_{Si}^2/2\varepsilon_{Si}$ is the pinch-off voltage. For HJFETs, $V_{bi} = 1.0 - 1.1$ V for $N_D = 10^{17}-5\times10^{18}\mathrm{cm}^{-3}$, as estimated analytically [1] and also extracted from C-V characteristics [3]. The depletion region width at the source-side of the gate ($x = 0$) is given by

$$W_D = t_{Si}\left(\frac{V_{bi}-V_{GS}}{V_{bi}-V_p}\right)^{1/2} = t_{Si}\left(1-\frac{V_{GS}-V_P}{V_{bi}-V_p}\right)^{1/2} \tag{3}$$

In the linear regime ($V_{DS} << V_{GS} - V_P$), the depletion region width is nearly constant along the channel, and

TABLE 1. First-order flicker noise expressions for HJFETs and conventional TFTs.

HJFET (and long-channel JFET or MESFET)	Conventional TFT (and long-channel MOSFET)
Linear Regime ($V_{DS} << V_{GS}-V_p$) $\frac{S_{ID}}{I_D^2}=\frac{\alpha_H q}{WLC_{Si}(V_{GS}-V_P)f}\left[\left(1+\frac{W_D}{t_{Si}}\right)/2\right]$	Linear Regime ($V_{DS} << V_{GS}-V_T$) $\frac{S_{ID}}{I_D^2}=\frac{\alpha_H q}{WLC_{ox}(V_{GS}-V_T)f}$
Saturation Regime ($V_{DS} \geq V_{GS}-V_p$) $\frac{S_{ID}}{I_D^2}=\frac{2\alpha_H q}{WLC_{Si}(V_{GS}-V_P)f}\left[\frac{3}{4}\frac{\left(1+\frac{W_D}{t_{Si}}\right)^2}{1+2\left(\frac{W_D}{t_{Si}}\right)}\right]$ $\frac{S_{ID}}{g_m^2}=\frac{\alpha_H q}{2WLC_{Si}f}(V_{GS}-V_P)\left[\left(1+2\frac{W_D}{t_{Si}}\right)/3\right]$	Saturation Regime ($V_{DS} \geq V_{GS}-V_T$) $\frac{S_{ID}}{I_D^2}=\frac{2\alpha_H q}{WLC_{ox}(V_{GS}-V_T)f}$ $\frac{S_{ID}}{g_m^2}=\frac{\alpha_H q}{2WLC_{ox}f}(V_{GS}-V_T)$

the channel resistance, $R_{lin} = L/[q\mu_b N_D(t_{Si} - W_D)W]$, where L and W are the channel length and width, respectively. From (3), $t_{Si}^2 - W_D^2 = (t_{Si} - W_D)(t_{Si} + W_D) = 2\varepsilon_{Si}(V_{GS} - V_P)/qN_D$. Therefore,

$$R_{lin} = \frac{L}{\mu_b C_{Si} W(V_{GS} - V_P)}\left[\left(1 + \frac{W_D}{t_{Si}}\right)/2\right] \tag{4}$$

where $C_{Si} = \varepsilon_{Si}/t_{Si}$ is the dielectric capacitance of the channel. Inserting $1/N = q\mu_b R_{lin}/L^2$ in (1) yields

$$\left(\frac{S_{ID}}{I_D^2}\right)_{lin} = \frac{\alpha_H q}{WLC_{Si}(V_{GS} - V_P)f}\left[\left(1 + \frac{W_D}{t_{Si}}\right)/2\right] \tag{5}$$

At higher V_{DS} values, I_D can be determined by solving

$$\int_{v_{ch}=V_S}^{v_{ch}=V_D} [q\mu N_D (t_{Si} - w_d) W]\, dv_{ch} = \frac{1}{I_D}\int_{x=0}^{x=L} dx \tag{6}$$

where w_d is given as a function of v_{ch} in (2). At $V_{DS} = V_{GS} - V_p$, the drain saturation current is found as

$$I_{D,\,sat} = \frac{1}{3}G_0(V_{bi} - V_p)\left[1 - 3\left(\frac{V_{bi} - V_{GS}}{V_{bi} - V_p}\right) + 2\left(\frac{V_{bi} - V_{GS}}{V_{bi} - V_p}\right)^{3/2}\right] \tag{7}$$

where $G_0 = q\mu_b N_D t_{Si} W/L$ is the "metallurgical" channel conductance, i.e. the conductance of the channel material in the absence of a gate structure. Eq. (7) is widely used to describe long-channel JFETs (and MESFETs with Schottky gate junctions), with minor variations in notation [64]–[67]. The term inside the brackets in (7) is equal to $1-3u^2+2u^3 = (1 - u)^2(1 + 2u) = (1 - u^2)^2(1 + 2u)/(1 + u)^2$, where $u = W_D/t_{Si}$, based on (3). Therefore, (7) may be re-written as

$$I_{D,\,sat} = \frac{1}{2}\mu_b C_{Si}\frac{W}{L}(V_{GS} - V_p)^2\left[\frac{4}{3}\frac{1 + 2\left(\frac{W_D}{t_{Si}}\right)}{\left(1 + \frac{W_D}{t_{Si}}\right)^2}\right] \tag{8}$$

Inserting $1/N = [(V_{GS} - V_P)/I_{D,sat}](q\mu_b/L^2)$ in (1) yields

$$\left(\frac{S_{ID}}{I_D^2}\right)_{sat} = \frac{2\alpha_H q}{WLC_{Si}(V_{GS} - V_P)f}\left[\frac{3}{4}\frac{\left(1 + \frac{W_D}{t_{Si}}\right)^2}{1 + 2\left(\frac{W_D}{t_{Si}}\right)}\right] \tag{9}$$

The transconductance of the HJFET is given by

$$g_{m,\,sat} = \frac{\partial I_{D,\,sat}}{\partial V_{GS}} = G_0\left[1 - \frac{V_{bi} - V_{GS}}{V_{bi} - V_p}\right]^{1/2} = G_0\left[1 - \left(\frac{W_D}{t_{Si}}\right)^2\right]^{1/2} \tag{10}$$

The input-referred noise voltage is therefore

$$\left(\frac{S_{ID}}{g_m^2}\right)_{sat} = \frac{\alpha_H q}{2WLC_{Si}f}(V_{GS} - V_P)\left[\left(1 + 2\frac{W_D}{t_{Si}}\right)/3\right] \tag{11}$$

It should be noted that source/drain series resistance is not included in above expressions. Treatment of series resistance, when significant, is the same as conventional TFTs.

B. DISCUSSION

The flicker noise expressions derived for HJFETs are summarized in Table 1, along with the well-known expressions for conventional TFTs [46]–[57] (V_T is the threshold voltage and C_{ox} is the gate dielectric capacitance of conventional TFTs). Apart from the terms inside the brackets, the HJFET expressions are the same as the conventional TFT expressions if V_p and C_{Si} are replaced with V_T and C_{ox}, respectively. The terms inside the brackets, $\alpha_1(u) = (1 + u)/2$, $\alpha_2(u) = 3(1+u)^2/4(1+2u)$ and $\alpha_3(u) = (1+2u)/3$, where $u = W_D/t_{Si}$, are plotted in Fig. 7(b). Since $0 < W_D \leq t_{Si}$, the corresponding values of $1/2 < \alpha_1 \leq 1$, $3/4 < \alpha_2 \leq 1$ and $1/3 < \alpha_3 \leq 1$ result in a somewhat lower flicker noise (up to 3X lower input-referred noise voltage) for HJFETs compared to conventional TFTs under equal conditions. In addition, the typically used t_{Si} of ~40−50 nm and ~50 nm-thick oxide gate dielectrics (standard for low-temperature poly-Si TFTs in production), result in $C_{Si} \approx 3C_{ox}$ and therefore ~3X lower flicker noise in HJFET. Since the HJFET structure and typical parameters can explain only up to ~10X lower flicker noise

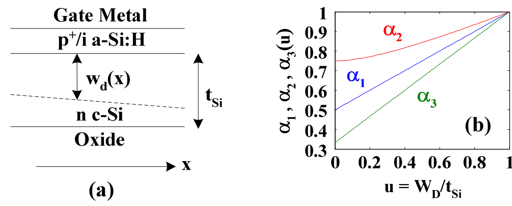

FIGURE 7. (a) Schematic diagram of a portion of an n-channel HJFET showing the a-Si:H/c-Si gate heterojunction and the depletion region width $w_d\ (x)$ at point x along the channel, and (b) plots of $\alpha_1(u) = (1+u)/2$, $\alpha_2(u) = 3(1+u)^2/4(1+2u)$, and $\alpha_3(u) = (1+2u)/3$, where $u = W_D/t_{Si}$ and $W_D = w_d\ (x = 0)$.

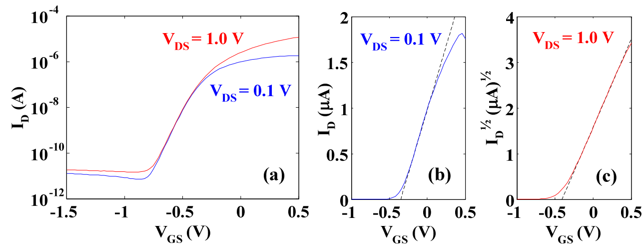

FIGURE 8. (a) Transfer characteristics of an HJFET with $W/L = 100\ \mu$m /5 μm; and extrapolation of pinch-off voltage V_P in (b) linear regime ($V_P = -0.35$ V), and (c) saturation regime ($V_P = -0.41$ V).

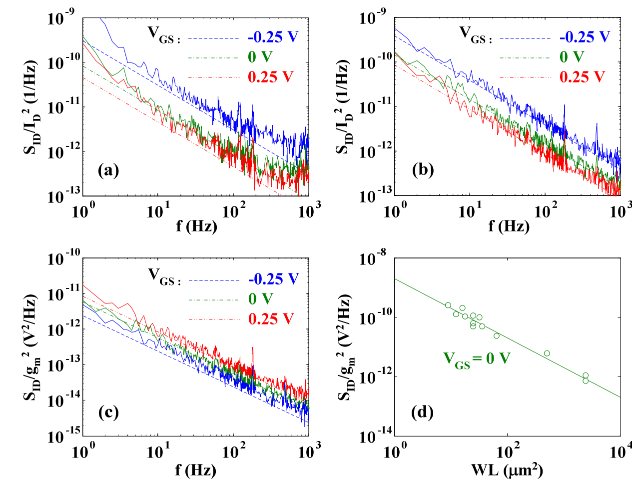

FIGURE 9. Measured noise characteristics of the HJFET of Fig. 8, (a) in the linear regime ($V_{DS} = 0.1$ V) and (b), (c) in saturation ($V_{DS} = 1.0$ V); and (d) input-referred noise voltage at 20 Hz measured for various HJFETs with different gate areas ($W.L$). The lines represent the expressions for HJFET flicker noise summarized in Table 1, with $\alpha_H = 0.0002$.

than conventional TFTs, the substantially (~100X) lower flicker noise observed in HJFETs is expected to be primarily due to a lower α_H for HJFETs.

The transfer characteristics of a fabricated HJFET and extrapolation of V_p in the linear and saturation regimes are shown in Figs. 8(a), 8(b) and 8(c), respectively. The measured noise current spectrum in the linear and saturation regimes and the input-referred noise voltage of the HJFET are given in Figs. 9(a), 9(b) and 9(c), respectively. The described flicker noise expressions with $\alpha_H = 2.0 \times 10^{-4}$ are also

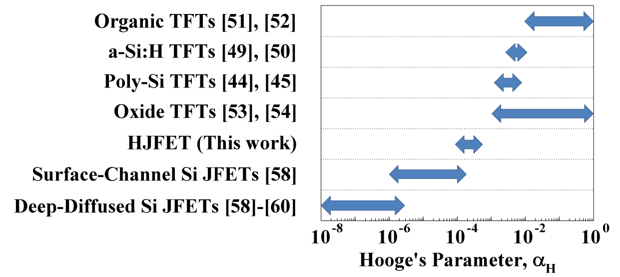

FIGURE 10. Extracted values of Hooge's parameter α_H for HJFETs (this work) along with reported values for various TFT technologies and Si JFETs.

plotted in the figures. Despite the simplicity of the model, the described expressions provide a reasonably good estimate of α_H. The measured flicker noise is inversely proportional to $W.L$ (Fig. 9(d)), as expected from the described expressions. This suggests that source/drain series resistance (including that of underlapped regions between gate and source/drain) has a negligible effect on the overall flicker noise. This is expected given the low α_H values of the order of 10^{-6} reported for passivated Si resistors [48], [58].

The Hooge's parameter, α_H, is known to have a strong dependence on fabrication process [48]. For a-Si:H [49], [50], organic [51], [52], metal-oxide [53], [54] and poly-Si [44], [45] TFTs, the reported α_H is in the range of $0.001-1$ or even higher. In devices with substantially defect-free materials and interfaces such as epitaxial layers, α_H is typically in the range of $10^{-4}-10^{-6}$ [48]. In single-crystalline Si JFETs with deep diffused gate p-n junctions, very low α_H in the range of $10^{-8}-10^{-6}$ has been achieved [58]–[60]; however, α_H increases to up to 2×10^{-4} in implanted-channel JFETs with shallow gate p-n junctions [58]. The reason for the very low α_H in deep diffused JFETs is believed to be a combination of negligible surface effects and substantially damage-free crystalline lattice. The α_H of 2×10^{-4} extracted for HJFETs is lower than conventional TFTs, of the same order as surface-channel Si JFETs, and higher than deep diffused Si JFETs (Fig. 10). This suggests that despite the low deposition temperature, the HJFET gate heterojunction has a reasonably good quality comparable with the gate junction of surface-channel Si JFETs fabricated at much higher temperatures.

V. SUMMARY AND CONCLUSION

Electrical stability and flicker noise of thin-film Si HJFETs were investigated and benchmarked against conventional TFTs. Despite their low fabrication temperature, the HJFETs were found to have higher stability and lower flicker noise than conventional TFTs. While these results do not provide direct evidence for establishing the physical origins of bias instability and flicker noise, they suggest that the high stability and low flicker noise observed in HJFETs may be attributed partly to the device structure and partly to the high-quality a-Si:H/c-Si gate heterojunction of the HJFETs. As for the HJFET device structure, these results suggest that

the sublinear dependence of pinch-off voltage on charged defect density in a-Si:H (as opposed to linear dependence in conventional a-Si:H TFTs) benefits high stability, and bulk conduction (as opposed to surface conduction in conventional poly-Si TFTs) benefits low flicker noise.

ACKNOWLEDGMENT

The author gratefully acknowledges Dr. Ghavam G. Shahidi, Dr. T-C. Chen and Dr. Devendra K. Sadana of IBM Research for helpful discussions and managerial support. The author is also grateful to Prof. James C. Sturm and Prof. Sigurd Wagner of Princeton University for allowing the usage of their PECVD facility for this work.

REFERENCES

[1] B. Hekmatshoar, "Thin-film heterojunction field-effect transistors with crystalline Si channels and low-temperature PECVD contacts," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 81–83, Jan. 2014. doi: 10.1109/LED.2013.2289920.

[2] B. Hekmatshoar and A. Afzali-Ardakani, "Thin-film heterojunction field-effect transistors for ultimate voltage scaling and low-temperature large-area fabrication of active-matrix backplanes," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2014, pp. 26.2.1–26.2.4. doi: 10.1109/IEDM.2014.7047111.

[3] B. Hekmatshoar, "Thin-film silicon heterojunction FETs for large area and flexible electronics: Design parameters and reliability," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3524–3529, Oct. 2015. doi: 10.1109/TED.2015.2463721.

[4] B. Hekmatshoar, "Thin-film heterojunction FETs on poly-Si substrates for high-stability driving and low-power amplification," *IEEE Electron Device Lett.*, vol. 39, no. 10, pp. 1528–1531, Oct. 2018. doi: 10.1109/LED.2018.2868176.

[5] D. Sharjerdi, B. Hekmatshoar, S. W. Bedell, M. Hopstaken, and D. K. Sadana, "Low-temperature epitaxy of compressively strained silicon directly on silicon substrates," *J. Electron. Mater.*, vol. 41, no. 3, pp. 494–497, Mar. 2012. doi: 10.1007/s11664-011-1807-6.

[6] B. Hekmatshoar, D. Shahrjerdi, M. Hopstaken, J. A. Ott, and D. K. Sadana, "Characterization of thin epitaxial emitters for high efficiency silicon heterojunction solar cells," *Appl. Phys. Lett.*, vol. 101, no. 10, pp. 103906-1–103906-4, Sep. 2012. doi: 10.1063/1.4751339.

[7] R. Ma, "Active matrix for OLED displays," in *Handbook of Visual Display Technology*, J. Chen, W. Cranton, and M. Fihn, Eds., 2nd ed. Cham, Switzerland: Springer, 2016, pp. 1821–1841. doi: 10.1007/978-3-319-14346-0_80.

[8] C. Kim, "TFT backplane and issues for OLED," in *Flat Panel Display Manufacturing*, J. Souk, S. Morozumi, F.-C. Luo, and I. Bita, Eds. Hoboken, NJ, USA: Wiley, 2018, pp. 115–127. doi: 10.1002/9781119161387.ch7.

[9] T. Tsujimura *et al.*, "4.1: A 20-inch OLED display driven by super-amorphous-silicon technology," in *SID Symp. Dig. Tech. Papers*, 2003, vol. 34, no. 1, pp. 6–9. doi: 10.1889/1.1832193.

[10] B. Hekmatshoar, A. Z. Kattamis, K. H. Cherenack, K. Long, J.-Z. Chen, S. Wagner, J. C. Sturm, K. Rajan, and M. Hack, "Reliability of active-matrix organic light-emitting-diode arrays with amorphous silicon thin-film transistor backplanes on clear plastic," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 63–66, Jan. 2008. doi: 10.1109/LED.2007.910800.

[11] H. Sirringhaus, "25th anniversary article: Organic field-effect transistors: The path beyond amorphous silicon," *Adv. Mater.*, vol. 26, no. 9, pp. 1319–1335, Jan. 2014. doi: 10.1002/adma.201304346.

[12] N. A. Morrison, T. Stolley, U. Hermanns, A. Reus, T. Deppisch, H. Bolandi, Y. Melnik, V. Singh, and J. G. Cruz, "An overview of process and product requirements for next generation thin film electronics, advanced touch panel devices, and ultra high barriers," *Proc. IEEE*, vol. 103, no. 4, pp. 518–534, Apr. 2015. doi: 10.1109/JPROC.2015.2408052.

[13] S. Lee, S. Jeon, R. Chaji, and A. Nathan, "Transparent semiconducting oxide technology for touch free interactive flexible displays," *Proc. IEEE*, vol. 103, no. 4, pp. 644–664, Apr. 2015. doi: 10.1109/JPROC.2015.2405767.

[14] J. Y. Noh, D. M. Han, W. C. Jeong, J. W. Kim, and S. Y. Cha, "Development of 55' 4 K UHD OLED TV employing the internal gate IC with high reliability and short channel IGZO TFTs," *J. Soc. Inf. Display*, vol. 26, no. 1, pp. 36–41, Jan. 2018. doi: 10.1002/sdtp.11605.

[15] H. Hayashi, A. Murai, M. Miura, T. Imada, Y. Terai, Y. Oshima, T. Saitoh, Y. Hiromasu, and T. Arai, "AlO sputtered self-aligned source/drain formation technology for highly reliable oxide thin film transistor backplane," *J. Soc. Inf. Display*, vol. 26, no. 10, pp. 583–594, Oct. 2018. doi: 10.1002/jsid.683.

[16] K. S. Karim, A. Nathan, and J. A. Rowlands, "Amorphous silicon active pixel sensor readout circuit for digital imaging," *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 200–208, Jan. 2003. doi: 10.1109/TED.2002.806968.

[17] J. P. Lu, K. Van Schuylenbergh, J. Ho, Y. Wang, J. B. Boyce, and R. A. Street, "Flat panel imagers with pixel level amplifiers based on polycrystalline silicon thin-film transistor technology," *Appl. Phys. Lett.*, vol. 80, no. 24, pp. 4656–4658, Jun. 2002. doi: 10.1063/1.1481788.

[18] C. Zhao and J. Kanicki, "Amorphous In-Ga-Zn-O thin-film transistor active pixel sensor X-ray imager for digital breast tomosynthesis," *Med. Phys.*, vol. 41, no. 9, pp. 091902-1–091902-14, Sep. 2014. doi: 10.1118/1.4892382.

[19] T. Moy, L. Huang, W. Rieutort-Louis, C. Wu, P. Cuff, S. Wagner, J. C. Sturm, and N. Verma, "An EEG acquisition and biomarker-extraction system using low-noise-amplifier and compressive-sensing circuits based on flexible, thin-film electronics," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 309–321, Jan. 2017. doi: 10.1109/JSSC.2016.2598295.

[20] W. Lee, D. Kim, N. Matsuhisa, M. Nagase, M. Sekino, G. G. Malliaras, T. Yokota, and T. Someya, "Transparent, conformable, active multielectrode array using organic electrochemical transistors," *Proc. Nat. Acad. Sci. USA*, vol. 114, no. 40, pp. 10554–10559, Oct. 2017. doi: 10.1073/pnas.1703886114.

[21] B. Hekmatshoar, "Thin-film heterojunction field-effect transistors with multiple subthreshold swings for large-area/flexible electronics and displays," *Electron. Lett.*, vol. 53, no. 8, pp. 570–571, Apr. 2017. doi: 10.1049/el.2016.4597.

[22] B. Hekmatshoar, "Normally-off thin-film silicon heterojunction field-effect transistors and application to complementary circuits," *IEEE Electron Device Lett.*, vol. 35, no. 5, pp. 545–547, May 2014. doi: 10.1109/LED.2014.2309113.

[23] C.-Y. Chen, J.-W. Lee, S.-D. Wang, M.-S. Shieh, P.-H. Lee, W.-C. Chen, H.-Y. Lin, K.-L. Yeh, and T.-F. Lei, "Negative bias temperature instability in low-temperature polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2993–3000, Dec. 2006. doi: 10.1109/TED.2006.885543.

[24] S. Maeda, S. Maegawa, T. Ipposhi, H. Nishimura, T. Ichiki, J. Mitsuhashi, M. Ashida, T. Muragishi, Y. Inoue, and T. Nishimura, "Mechanism of negative-bias temperature instability in polycrystalline-silicon thin film transistors," *J. Appl. Phys.*, vol. 76, no. 12, pp. 8160–8166, Dec. 1994. doi: 10.1063/1.358430.

[25] M.-K. Han and I. H. Song, "56.2: Invited paper: Low temperature poly-Si TFTs with advanced device structures," in *SID Symp. Dig. Tech. Papers*, 2003, vol. 34, no. 1, pp. 1490–1493. doi: 10.1889/1.1832567.

[26] M. Cuscunà, L. Mariucci, G. Fortunato, A. Bonfiglietti, A. Pecora, and A. Valletta, "Improved electrical stability in asymmetric fingered polysilicon thin film transistors," *Appl. Phys. Lett.*, vol. 89, no. 12, pp. 123506-1–123506-3, Sep. 2006. doi: 10.1063/1.2354420.

[27] C.-F. Weng, T.-C. Chang, F.-Y. Jian, S.-C. Chen, J. Lua, and I.-C. Lua, "Asymmetric negative bias temperature instability degradation of poly-Si TFTs under static stress," *J. Electrochem. Soc.*, vol. 157, no. 1, pp. H22–H26, Jan. 2010. doi: 10.1149/1.3244596.

[28] T. Arai, "Oxide-TFT technologies for next-generation AMOLED displays," *J. Soc. Inf. Display*, vol. 20, no. 3, pp. 156–161, Mar. 2012. doi: 10.1889/JSID20.3.156.

[29] R. Chaji and A. Nathan, "13.2: Invited paper: LTPS vs oxide backplanes for AMOLED displays: System design considerations and compensation techniques," in *SID Symp. Dig. Tech. Papers*, 2014, vol. 45, no. 1, pp. 153–156. doi: 10.1002/j.2168-0159.2014.tb00042.x.

[30] A. Nathan, S. Lee, S. Jeon, and J. Robertson, "Amorphous oxide semiconductor TFTs for displays and imaging," *J. Display Technol.*, vol. 10, no. 11, pp. 917–927, Nov. 2014. doi: 10.1109/JDT.2013.2292580.

[31] K.-S. Park, S. Oh, P. Yun, J. U. Bae, and I. B. Kang, "Prospects of oxide TFTs approaching LTPS," in *Proc. AM-FPD*, Kyoto, Japan, Jul. 2015, pp. 241–244. doi: 10.1109/AM-FPD.2015.7173254.

[32] J. U. Bae, J. H. Baeck, P. Yun, D. H. Kim, Y. H. Jang, K.-S. Park, S. Y. Yoon, and I. B. Kang, "High mobility oxide TFT for OLED pixel circuits," in *Proc. AM-FPD*, Kyoto, Japan, Jul. 2017, pp. 309–311.

[33] Y. Hara, T. Kikuchi, H. Kitagawa, J. Morinaga, H. Ohgami, H. Imai, T. Daitoh, and T. Matsuo, "IGZO-TFT technology for large-screen 8 K display," *J. Soc. Inf. Display*, vol. 26, no. 3, pp. 169–177, Mar. 2018. doi: 10.1002/jsid.648.

[34] S. H. Park, J. Y. Park, P. S. Yun, J. U. Bae, K.-S. Park, S. Y. Yoon, and I. Kang, "P-18: Improvement of reliability in coplanar a-IGZO TFTs by multilayer SiO_2 gate insulator," in *SID Symp. Dig. Tech. Papers*, 2018, vol. 49, no. 1, pp. 1246–1248. doi: 10.1002/sdtp.12136.

[35] B. Hekmatshoar, K. H. Cherenack, A. Z. Kattamis, K. Long, S. Wagner, and J. C. Sturm, "Highly stable amorphous-silicon thin-film transistors on clear plastic," *Appl. Phys. Lett.*, vol. 93, no. 3, Jul. 2008, Art. no. 032103. doi: 10.1063/1.2963481.

[36] T. Liu, L. E. Aygun, S. Wagner, and J. C. Sturm, "Reliability of highly stable amorphous-silicon thin-film transistors under low gate-field stress—Part I: Two-stage model for lifetime prediction," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 2, pp. 243–254, Jun. 2016. doi: 10.1109/TDMR.2016.2526498.

[37] M. Schmidt, L. Korte, A. Laades, R. Stangl, C. Schubert, H. Angermann, E. Conrad, and K. V. Maydell, "Physical aspects of a-Si:H/c-Si hetero-junction solar cells," *Thin Solid Films*, vol. 515, no. 19, pp. 7475–7480, Jul. 2007. doi: 10.1016/j.tsf.2006.11.087.

[38] S. D. Wolf, C. Ballif, and M. Kondo, "Kinetics of *a*-Si:H bulk defect and *a*-Si:H/*c*-Si interface-state reduction," *Phys. Rev. B, Condens. Matter*, vol. 85, no. 11, pp. 113302-1–113302-4, Mar. 2012. doi: 10.1103/PhysRevB.85.113302.

[39] Y. Bar-Yam and J. D. Joannopoulos, "Theories of defects in amorphous semiconductors," *J. Non-Crystal. Solids*, vols. 97–98, no. 1, pp. 467–474, Dec. 1987. doi: 10.1016/0022-3093(87)90110-4.

[40] K. Winer, "Defect formation in *a*-Si:H," *Phys. Rev. B, Condens. Matter*, vol. 41, no. 17, pp. 12150–12161, Jun. 1990. doi: 10.1103/PhysRevB.41.12150.

[41] M. J. Powell and S. C. Deane, "Improved defect-pool model for charged defects in amorphous silicon," *Phys. Rev. B, Condens. Matter*, vol. 48, no. 15, pp. 10815–10827, Oct. 1993. doi: 10.1103/PhysRevB.48.10815.

[42] S. De Wolf, B. Demaurex, A. Descoeudres, and C. Ballif, "Very fast light-induced degradation of *a*-Si:H/*c*-Si(100) interfaces," *Phys. Rev. B, Condens. Matter*, vol. 83, no. 23, pp. 233301-1–233301-4, Jun. 2011. doi: 10.1103/PhysRevB.83.233301.

[43] A. Corradetti, R. Leoni, R. Carluccio, and G. Fortunato, "Evidence of carrier number fluctuation as origin of 1/f noise in polycrystalline silicon thin film transistors," *Appl. Phys. Lett.*, vol. 67, no. 12, pp. 1730–1732, Sep. 1995. doi: 10.1063/1.115031.

[44] A. Bonfiglietti, A. Valletta, L. Mariucci, A. Pecora, and G. Fortunato, "Noise performance of polycrystalline silicon thin-film transistors made by sequential lateral solidification," *Appl. Phys. Lett.*, vol. 82, no. 16, pp. 2709–2711, Apr. 2003. doi: 10.1063/1.1568820.

[45] L. Pichon, A. Boukhenoufa, C. Cordier, and B. Cretu, "Numerical simulation of low-frequency noise in polysilicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 716–718, Aug. 2007. doi: 10.1109/LED.2007.900849.

[46] L. K. J. Vandamme, X. Li, and D. Rigaud, "1/f noise in MOS devices, mobility or number fluctuations?" *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1936–1945, Nov. 1994. doi: 10.1109/16.333809.

[47] L. K. J. Vandamme, "How useful is Hooge's empirical relation," in *Proc. ICNF*, Montpellier, France, Jun. 2013, pp. 1–6. doi: 10.1109/ICNF.2013.6578875.

[48] L. K. J. Vandamme and F. N. Hooge, "What do we certainly know about 1/f noise in MOSTs?" *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 3070–3085, Nov. 2008. doi: 10.1109/TED.2008.2005167.

[49] J. M. Boudry and L. E. Antonuk, "Current-noise-power spectra of amorphous silicon thin-film transistors," *J. Appl. Phys.*, vol. 76, no. 4, pp. 2529–2534, Aug. 1994. doi: 10.1063/1.357614.

[50] J. Rhayem, D. Rigaud, M. Valenza, N. Szydlo, and H. Lebrun, "1/f noise modeling in long channel amorphous silicon thin film transistors," *J. Appl. Phys.*, vol. 87, no. 4, pp. 1983–1989, Feb. 2000. doi: 10.1063/1.372124.

[51] P. V. Necliudov, S. L. Rumyantsev, M. S. Shur, D. J. Gundlach, and T. N. Jackson, "1/f noise in pentacene organic thin film transistors," *J. Appl. Phys.*, vol. 88, no. 9, pp. 5395–5399, Nov. 2000. doi: 10.1063/1.1314618.

[52] L. K. J. Vandamme, R. Feyaerts, and G. Trefán, "1/f noise in pentacene and poly-thienylene vinylene thin film transistors," *J. Appl. Phys.*, vol. 91, no. 2, pp. 719–723, Jan. 2002. doi: 10.1063/1.1423389.

[53] I.-T. Cho, W.-S. Cheong, C.-S. Hwang, J.-M. Lee, H.-I. Kwon, and J.-H. Lee, "Comparative study of the low-frequency-noise behaviors in a-IGZO thin-film transistors with Al_2O_3 and $Al_{23}SiN_x$ gate dielectrics," *IEEE Electron Device Lett.*, vol. 30, no. 8, pp. 828–830, Aug. 2009. doi: 10.1109/LED.2009.2023543.

[54] T.-C. Fung, G. Baek, and J. Kanicki, "Low frequency noise in long channel amorphous In-Ga-Zn-O thin film transistors," *J. Appl. Phys.*, vol. 108, no. 7, Oct. 2010, Art. no. 074518. doi: 10.1063/1.3490193.

[55] F. M. Klaassen, "Characterization of low 1/f noise in MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-18, no. 10, pp. 887–891, Oct. 1971. doi: 10.1109/T-ED.1971.17301.

[56] A. van der Ziel, "Some general relationships for flicker noise in MOSFETs," *Solid-State Electron.*, vol. 21, no. 4, pp. 623–624, Apr. 1978. doi: 10.1016/0038-1101(78)90327-1.

[57] L. K. J. Vandamme and H. M. M. de Werd, "1/f; noise model for MOSTs biased in nonohmic region," *Solid-State Electron.*, vol. 23, no. 4, pp. 325–329, Apr. 1980. doi: 10.1016/0038-1101(80)90199-9.

[58] F. A. Levinzon and L. K. J. Vandamme, "Comparison of 1/f noise in JFETs and MOSFETs with several figures of merit," *Fluctuation Noise Lett.*, vol. 10, no. 4, pp. 447–465, Apr. 2011. doi: 10.1142/S0219477511000685.

[59] G. S. Bhatti and B. K. Jones, "1/f noise in ohmic silicon JFET channels," *J. Phys. D, Appl. Phys.*, vol. 17, no. 12, pp. 2407–2422, Dec. 1984. doi: 10.1088/0022-3727/17/12/009.

[60] F. A. Levinzon, "Measurement of low-frequency noise of modern low-noise junction field effect transistors," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 6, pp. 2427–2432, Dec. 2005. doi: 10.1109/TIM.2005.858534.

[61] G.-F. D. Betta, M. Boscardin, F. Fenotti, L. Pancheri, C. Piemonte, L. Ratti, and N. Zorzi, "Low noise junction field effect transistors in a silicon radiation detector technology," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 5, pp. 3004–3012, Oct. 2006. doi: 10.1109/TNS.2006.882606.

[62] F. A. Levinzon, "Ultra-low-noise high-input impedance amplifier for low-frequency measurement applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 7, pp. 1815–1822, Aug. 2008. doi: 10.1109/TCSI.2008.918213.

[63] F. N. Hooge, "1/f noise is no surface effect," *Phys. Lett. A*, vol. 29, no. 3, pp. 139–140, Apr. 1969. doi: 10.1016/0375-9601(69)90076-0.

[64] M. Shur, *Physics of Semiconductor Devices*. Upper Saddle River, NJ, USA: Prentice-Hall, 1990, pp. 405–409.

[65] S. M. Sze and K. N. Ng, *Physics of Semiconductor Devices*, 3rd ed. Hoboken, NJ, USA: Wiley, 2007, pp. 375–381.

[66] R. S. Müller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 3rd ed. Hoboken, NJ, USA: Wiley, 2003, pp. 212–219.

[67] B. G. Streetman and S. K. Banerjee, *Solid State Electronic Devices*, 6th ed. London, U.K.: Pearson Education, 2006, pp. 254–261.

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