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Influence of Digital Delay on the Zero-Sequence Voltage Injection Neutral-Point Potential Balance Algorithm for Three-Level NPC Inverters and Its Compensation Method

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ABSTRACT Three-level neutral-point-clamped (NPC) inverters need to ensure the balance of the neutral-point (NP) potential during operation. The zero-sequence voltage injection balance algorithms based on the carrier-based pulse width modulation (CBPWM) have been proposed in many papers and proved to be effective in controlling the NP potential. In industrial applications, the algorithms are mostly implemented by digital controllers, which have inherent computation digital delay. However, there is little attention to how the digital delay influences the balance algorithms. In this paper, the influence of the digital delay on the zero-sequence voltage injection balance algorithm has been studied in detail. It is found that the digital delay causes a fluctuation of the NP potential. The frequency of the fluctuation is 1/6 control frequency, and the amplitude of the fluctuation is related to the control frequency, the modulation index, the output current, and the dc-side capacitance. Furthermore, in order to eliminate the NP potential fluctuation caused by the digital delay, a digital delay compensation method is proposed in this paper. The correctness of the theoretical analysis and the effectiveness of the compensation method have been verified by the simulation and experiment results.

INDEX TERMS Balance algorithm, digital delay compensation, neutral-point potential, three-level inverter,zero-sequence voltage injection.

I. INTRODUCTION

The three-level neutral-point-clamped (NPC) topology is first proposed in [1]. Compared with the two-level topology, each switch of the three-level topology only bears half of the dc voltage, and the total harmonic distortion (THD) of the ac-side output current is also smaller, so the three-level topology is more suitable for high-voltage and high-power applications [2]. But the three-level topology also has its own drawbacks: more switches and additional neutral-point (NP) potential balance management.

The NP potential balance methods can be classified into hardware methods and software methods [3]. The hardware methods maintain the NP potential balanced by adding extra circuits to actively charge and discharge the two capacitors on the dc side [4], but the hardware cost increases. The software methods can be further divided into two types based on the space vector pulse width modulation (SVPWM) and the carrier-based pulse width modulation (CBPWM). In fact, these two types of software balance algorithms are equivalent [5], [6].

In SVPWM, there are four kinds of vectors: zero vectors, short vectors, medium vectors, and long vectors [8]. The medium vector is the main factor that causes the unbalance of the NP potential, and the redundant short vectors can be used to control the NP potential [7], [8]. The virtual space vector (VSV) is proposed in [9], [10] to keep the NP potential balanced under full power-factor range by avoiding the use of the medium vectors. However, VSV brings about the increase of switching loss and output current THD.

The balance algorithms based on CBPWM generally control the NP potential by injecting a zero-sequence voltage into the modulation signals. Reference [11] proposes an algorithm to select the zero-sequence voltage, but it easily causes

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the saturation of the modulation signals. A test-verify-revise algorithm is proposed in [12] to calculated the zero-sequence voltage, but it is not accurate enough in some cases. The zero-sequence voltage is calculated in each control cycle by an accurate algorithm in [13], which shows a good ability of balancing the NP potential. To avoid the saturation of the modulation signals, [14] adopts a proportion-integration (PI) controller to generate the zero-sequence voltage. A dynamic modulation offset balance algorithm is proposed in [15], but how to obtain the real-time power factor is difficult. The balance algorithms based on the double-signal pulse width modulation are proposed in [16]–[18], which are similar to VSV.

All the balance algorithms mentioned above can achieve the balance of the NP potential, but there is little research on how the digital delay influences the performance of the balance algorithms when a digital controller is used.

Digital signal processors (DSP) have been widely used in industrial applications [19], which provide the foundation for digital control. But compared with analog control, one cycle digital delay cannot be avoided in DSP, which may deteriorate the performance of the digital control. In [20], the digital delay is taken into account when designing the linear-quadratic regulators (LQR) for the three-level NPC inverter. However, the influence of the digital delay on the NP potential balance algorithm is neglected in [20]. A repetitive controller is used to suppress the low-frequency fluctuation of the NP potential in [21]. In order to reduce the digital delay influence on the NP potential balance control, [21] uses a dual sampling method to reduce the effect of the digital delay, but the compensation is not complete. Reference [22] reveals the influence of the digital delay on the balance algorithm by simulation, but does not explain the principles, or propose a compensation method.

This paper focuses on the influence of the digital delay on the zero-sequence voltage injection NP potential balance algorithm and proposes a digital delay compensation method. It is found that the digital delay causes a certain fluctuation of the NP potential. The frequency of the fluctuation is 1/6 control frequency, and the amplitude of the fluctuation is related to multiple variables. This paper also deduces an expression of the fluctuation based on these variables. Moreover, a digital delay compensation method is proposed to eliminate the fluctuation completely, and simulation and experiment results have verified the effectiveness of the proposed method.

The organization of this paper is as follows: a brief review of the zero-sequence voltage injection NP potential balance algorithm is given in section II. Section III analyses the digital delay influence on the balance algorithm in detail. A digital delay compensation method is proposed in section IV. Simulation results are shown in section V. Section VI includes the experiment results based on a three-level NPC inverter prototype. The conclusion is made in section VII.

II. A BRIEF REVIEW OF THE BALANCE ALGORITHM

The whole system of the three-level NPC inverter is shown in Fig. 1. The inverter works in a voltage source mode and the load is a series connection of the inductors and resistors. The voltages of the dc-side capacitors and the ac-side output currents are sampled by the sensors at the beginning of each control cycle, and the sampling signals are sent to the digital controller after filtered by the anti-alias pre-filters. The cut-off frequency of the pre-filters is about 1/3 to 1/2 control frequency. The control frequency and the switch frequency of the three-level inverter system in this paper are set to be the same. The digital controller is realized by a DSP, so all the variables are discrete in the digital control. The normalized three-phase sinusoidal reference signals $v_{A,B,C}(k\mathrm{T_s})$ are generated by an open-loop control for simplicity. Depending on the feedback variables and $v_{A,B,C}(k\mathrm{T_s})$, the NP potential balance algorithm generates the desired zero-sequence voltage $v_0(k\mathrm{T_s})$, which is added to $v_{A,B,C}(k\mathrm{T_s})$ to balance the NP potential. The balance algorithm used in Fig. 1 is the same as that in [22], and the modulation method is phase disposition (PD) CBPWM. It should be emphasized that the calculation process of the zero-sequence voltage needs some time, and usually the modulation reference signals $v_{Am,Bm,Cm}$ $((k-1)\mathrm{T_s})$ are outputted one control cycle later after the finishing of sampling. Therefore, Z^{-1} represents the digital delay in Fig. 1. Before the analysis of the digital delay influence, the balance algorithm proposed in [22] is reviewed briefly in this section, and the digital delay is ignored temporarily.

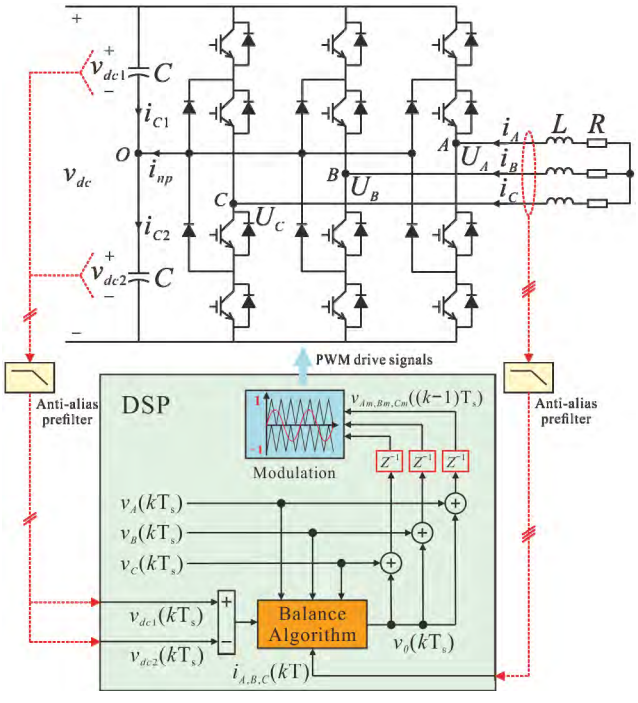

FIGURE 1. The system schematic of the three-level NPC inverter.

Based on the dc-side circuit in Fig. 1, (1) can be obtained,

$$\Delta v_{dc}(t) = v_{dc1}(t) - v_{dc2}(t) = -\frac{1}{C}\int i_{np}(t)dt \qquad (1)$$

where $v_{dc1}(t)$ and $v_{dc2}(t)$ are the voltages of the two dc-side capacitors; $\Delta v_{dc}(t)$ represents the difference between $v_{dc1}(t)$ and $v_{dc2}(t)$; C is the capacitance of the dc-side capacitors; $i_{np}(t)$ represents the neutral current.

In order to keep $\Delta v_{dc}(t)$ to be zero in one control cycle, the reference value of $i_{np}(t)$ should satisfy (2) in discrete domain,

$$i_{npref}(kT_s) = \frac{C}{T_s}\left(v_{dc1}(kT_s) - v_{dc2}(kT_s)\right) \tag{2}$$

where T_s is the control cycle, and $i_{npref}(kT_s)$ represents the reference value of the neutral current.

According to [22], the desired value of $i_{npref}(kT_s)$ can be achieved by injecting a zero-sequence voltage $v_0(kT_s)$ into the modulation reference signals, and $v_0(kT_s)$ can be calculated from (3),

$$i_{npref}(kT_s) = -\sum_{i=A,B,C}\left(|v_i(kT_s) + v_0(kT_s)| \cdot i_i(kT_s)\right) \tag{3}$$

where $i_{A,B,C}(kT_s)$ represent the three-phase ac-side output currents.

Supposing that F represents the balance algorithm in [22], $v_0(kT_s)$ can be expressed as (4).

$$v_0(kT_s) = F\left(\Delta v_{dc}(kT_s), i_{A,B,C}(kT_s), v_{A,B,C}(kT_s), C, T_s\right) \tag{4}$$

Therefore, $v_0(kT_s)$ calculated by (4) can be used to balance NP potential. However, it does not mean that the balance algorithm can compensate the fluctuation of the NP potential completely in all situations. The balance ability depends on the power factor and the modulation index according to [13], and the fully controllable region are shown as the green area in Fig. 2.

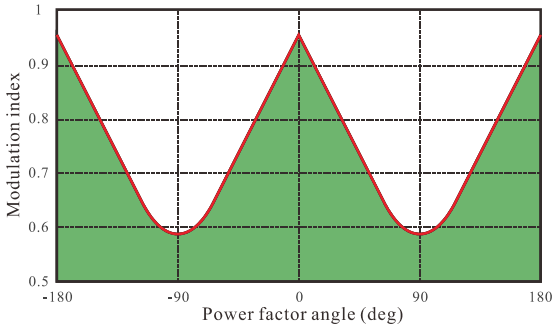

FIGURE 2. Fully controllable region of the balance algorithm.

This paper focuses on the influence of the digital delay on the balance algorithm, and the fluctuation of the NP potential caused by different power factors is not within the scope of this paper. Therefore, the power factor used in this paper is set to be about 1, which means the cases studied in this paper are within the fully controllable region in Fig. 2.

III. INFLUENCE OF THE DIGITAL DELAY

In the reality, the computation process of the DSP and the modulation pattern used in this paper are shown in Fig. 3, which can be used to clarify the digital delay effect in detail.

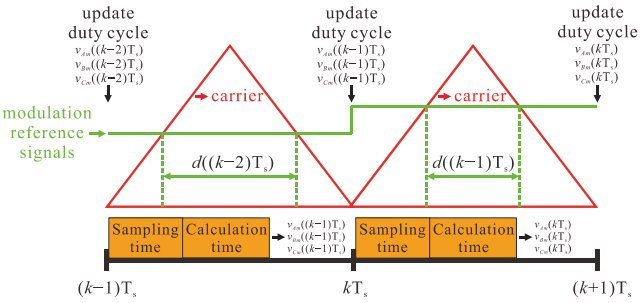

FIGURE 3. The computation process of the DSP and the modulation pattern.

First, the control frequency and the switch frequency are set to be the same in this paper. As shown in Fig. 3, in each control cycle, such as $(k-1)T_s$ to kT_s, the outside signals (currents and voltages) are sampled, then the control algorithm calculates the modulation reference signals ($v_{Am,Bm,Cm}((k-1)T_s)$). But $v_{Am,Bm,Cm}((k-1)T_s)$ cannot be used to update the duty cycle d immediately until the time is kT_s. If there is no sampling time and calculation time, the $v_{Am,Bm,Cm}((k-1)T_s)$ can be outputted at the time of $(k-1)T_s$, but the sampling time and calculation time cannot be avoided, so the digital delay is one control cycle.

Actually, in this paper, even though the sampling time or the calculation time can be reduced by some optimization, the modulation reference signals are still not outputted until the next control cycle. In this paper, the duty cycle is updated at the beginning of each control cycle instead of at the end of the calculation time, so optimizing the computational cost of the control or reducing the sampling time will not influence the digital delay effect, and the digital delay is still one control cycle.

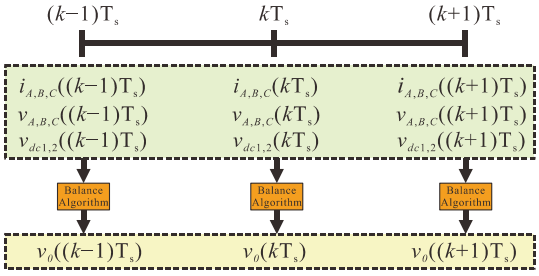

FIGURE 4. The sequence diagram without the digital delay.

Supposing that there is no digital delay in the controller as shown in Fig. 4, $v_{dc1,2}(kT_s)$ and $i_{A,B,C}(kT_s)$ are sampled at the time of kT_s, and $v_0(kT_s)$ is calculated by (4) and outputted to the modulation part immediately. In this case, $\Delta v_{dc}((k+1)T_s)$ can be deduced as (5),

$$\begin{aligned}\Delta v_{dc}((k+1)T_s) &= \Delta v_{dc}(kT_s) - i_{np}(kT_s)\cdot\frac{T_s}{C} \\ &= \Delta v_{dc}(kT_s) + \frac{T_s}{C}\cdot\sum_{i=A,B,C}\left(|v_i(kT_s) \right. \\ &\quad \left. + v_0(kT_s)|\cdot i_i(kT_s)\right) = 0\end{aligned} \tag{5}$$

where $i_{np}(k\mathrm{T_s}) = i_{npref}(k\mathrm{T_s})$ as shown in (3) by injecting a suitable $v_0(k\mathrm{T_s})$, so that $\Delta v_{dc}((k+1)\mathrm{T_s})$ equals 0. The NP potential can be totally balanced by the balance algorithm without considering the digital delay.

When the one control cycle digital delay is taken into account, the desired $v_0(k\mathrm{T_s})$ is outputted at the time of $(k+1)\mathrm{T_s}$ instead of $k\mathrm{T_s}$. The changes of the sequence diagram are shown in Fig. 5.

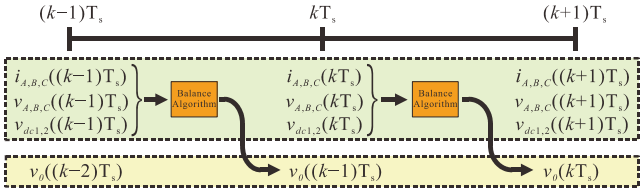

FIGURE 5. The sequence diagram with the digital delay.

Due to the existence of the digital delay, the zero-sequence voltage calculated in each control cycle cannot be outputted immediately, which results in the unbalance of the NP potential, and $\Delta v_{dc}((k+1)\mathrm{T_s})$ can be expressed in (6) when considering the digital delay.

$$\begin{aligned}\Delta v_{dc}((k+1)\mathrm{T}_s) &= \Delta v_{dc}(k\mathrm{T}_s) - i_{np}(k\mathrm{T}_s)\cdot\frac{\mathrm{T}_s}{C}\\ &= \Delta v_{dc}(k\mathrm{T}_s) + \frac{\mathrm{T}_s}{C}\cdot\sum_{i=A,B,C}(|v_i(k\mathrm{T}_s)\\ &\quad + v_0((k-1)\mathrm{T}_s)|\cdot i_i(k\mathrm{T}_s)) \qquad (6)\end{aligned}$$

Comparing (5) and (6), $\Delta v_{dc}((k+1)\mathrm{T_s})$ cannot be zero with the existence of the digital delay, even within the fully controllable region in Fig. 2, because $v_0(k\mathrm{T_s})$ is replaced by $v_0((k-1)\mathrm{T_s})$.

The unbalance of the NP potential resulted from the digital delay is a fluctuation with a certain frequency and amplitude according to the research in this paper, the rest part of this section is the derivation process of expressions of the frequency and amplitude.

A. FREQUENCY OF THE FLUCTUATION

Depending on (5), $\Delta v_{dc}((k-1)\mathrm{T_s})$ can be expressed as (7).

$$\begin{aligned}\Delta v_{dc1}((k-1)\mathrm{T}_s) = -\frac{\mathrm{T}_s}{C}\sum_{i=A,B,C}&(|v_i((k-1)\mathrm{T}_s)\\ &+ v_0((k-1)\mathrm{T}_s)|\cdot i_i((k-1)\mathrm{T}_s)) \qquad (7)\end{aligned}$$

Because $v_{A,B,C}$ and $i_{A,B,C}$ mainly consist of the fundamental frequency components, and the control frequency is generally higher enough than the fundamental frequency, the assumptions in (8) are reasonable. In order to clarify the rationality of the assumption in (8), the waveforms of $v_A(k\mathrm{T_s})$ and $v_A((k-1)\mathrm{T_s})$ are shown in Fig. 6, where the control frequency is 5 kHz and the fundamental frequency is 50 Hz. From Fig. 6, it can be seen that there is only a phase difference between $v_A(k\mathrm{T_s})$ and $v_A((k-1)\mathrm{T_s})$, and the phase difference is very small relative to a 50 Hz component.

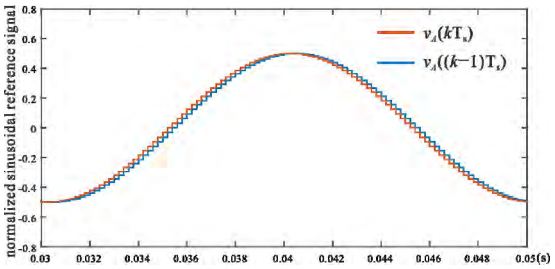

FIGURE 6. The waveforms of $v_A(k\mathrm{T_s})$ and $v_A((k-1)\mathrm{T_s})$.

This phase difference accounts for only one percent of a 50 Hz component period, so the assumption in (8) is rational.

$$\begin{aligned}v_i(k\mathrm{T}_s) &\approx v_i((k-1)\mathrm{T}_s)\\ i_i(k\mathrm{T}_s) &\approx i_i((k-1)\mathrm{T}_s) \qquad (8)\end{aligned}$$

According to (6), (7) and (8), the relationship between $\Delta v_{dc}((k-1)\,\mathrm{T_s})$, $\Delta v_{dc}(k\mathrm{T_s})$ and $\Delta v_{dc}((k+1)\mathrm{T_s})$ can be presented as (9).

$$\Delta v_{dc}((k+1)\mathrm{T}_s) = \Delta v_{dc}(k\mathrm{T}_s) - \Delta v_{dc}((k-1)\mathrm{T}_s) \qquad (9)$$

Assuming that the waveform of Δv_{dc} is sinusoidal, and the expressions of Δv_{dc} are shown in (10),

$$\begin{aligned}\Delta v_{dc}(k\mathrm{T}_s) &= A\sin(\omega_{\Delta dc}k\mathrm{T}_s+\varphi)\\ \Delta v_{dc}((k-1)\mathrm{T}_s) &= A\sin(\omega_{\Delta dc}(k-1)\mathrm{T}_s+\varphi)\\ \Delta v_{dc}((k+1)\mathrm{T}_s) &= A\sin(\omega_{\Delta dc}(k+1)\mathrm{T}_s+\varphi) \qquad (10)\end{aligned}$$

where A is the amplitude of Δv_{dc}; $\omega_{\Delta c}$ is the angle frequency; φ is the phase angle of Δv_{dc}. The simulation waveforms of $\Delta v_{dc}((k+1)\mathrm{T_s})$, $\Delta v_{dc}(k\mathrm{T_s})$ and $\Delta v_{dc}((k-1)\mathrm{T_s})$ in discrete domain are shown in Fig. 7, from which, the NP potential fluctuation Δv_{dc} can be indeed seen as a sinusoidal component approximately.

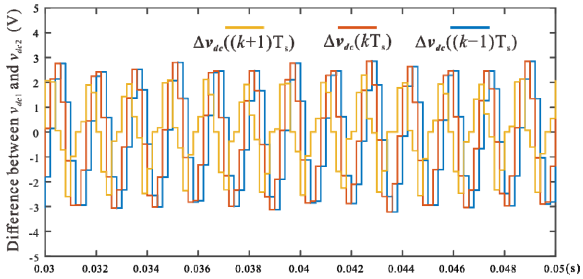

FIGURE 7. The simulation waveforms of Δv_{dc} in discrete domain.

Substituting (10) into (9), the simplification result can be obtained in (11).

$$\cos(\omega_{\Delta dc}\mathrm{T}_s) = 1/2 \qquad (11)$$

Therefore, the frequency of Δv_{dc} can be deduced as (12), where $f_{\Delta dc}$ represents the frequency of Δv_{dc}, and f_s represents the control frequency.

$$f_{\Delta dc} = f_s/6 \qquad (12)$$

It can be concluded that the one control cycle digital delay causes a fluctuation of the NP potential at the frequency of 1/6 f_s. So, when $f_s = 5$ kHz, Δv_{dc} includes a fluctuation of 833 Hz.

In fact, in addition to the one control cycle digital delay, the anti-alias filters also have a certain delay effect, which will also influence the frequency of the NP potential fluctuation. According to [23], in digital control system, the sampling signals are generally filtered by the anti-alias pre-filters before sent to the digital controller, and the cutoff frequency of the pre-filters is about 1/3 to 1/2 control frequency. In this paper, the cutoff frequency of the pre-filters is chosen to be 1/3 control frequency. The transfer function of the anti-alias pre-filter in s domain can be expressed as (13), where f_c represents the cutoff frequency.

$$G_{filter} = \frac{2\pi f_c}{s + 2\pi f_c} = \frac{2\pi \cdot (f_s/3)}{s + 2\pi \cdot (f_s/3)} = \frac{2\pi}{3T_s s + 2\pi} \tag{13}$$

The transfer function of the delay in s domain can be expressed as (14), where τ represents the time of the delay.

$$G_{delay} = e^{-\tau \cdot s} \tag{14}$$

Supposing that $T_s = 0.0001$ s, $\tau = 0.25T_s$, the bode graphs of G_{filter} and G_{delay} are shown in Fig. 8. From Fig. 8, it can be seen that the magnitude and phase characteristics of the bode graphs of G_{filter} and G_{delay} are close, so the anti-alias pre-filter can be seen as a small digital delay approximately.

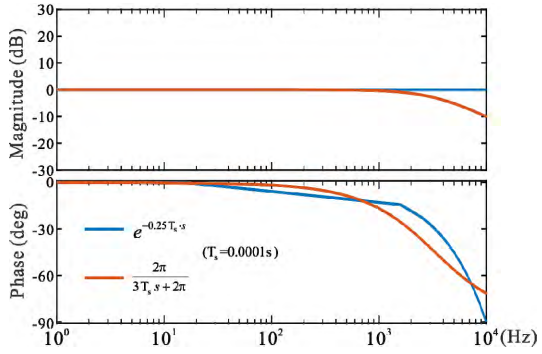

FIGURE 8. The bode graphs of G_{filter} and G_{delay}.

Therefore, the delay effect of the anti-alias pre-filter and the one cycle digital delay can be combined into one unified digital delay as shown in (15), where x represents the delay effect of the anti-alias pre-filter. For example, when the cutoff frequency of the pre-filters is chosen to be 1/3 control frequency, the value of x is 0.25.

$$G_{delay\_sum} = G_{delay} \cdot G_{filter} = e^{-T_s \cdot s} \cdot \frac{2\pi f_c}{s + 2\pi f_c} \approx e^{-(1+x)T_s \cdot s} \tag{15}$$

Based on the analysis above, when considering the delay effect of the anti-alias pre-filters and the one control cycle digital delay, Fig. 5 can be changed to Fig. 9, which means that if the anti-alias pre-filters are removed, the control frequency should be changed to $f_s/(1 + x)$ to keep the whole

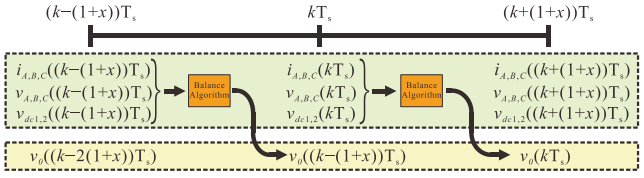

FIGURE 9. The sequence diagram with the digital delay and the anti-alias pre-filter delay.

system equivalent. The correctness of this assertion will be verified in the simulation results section.

So if we take the delay effect of the anti-alias pre-filter into account, the control cycle will be $(1 + x)T_s$ rather than T_s, and $f_{\Delta dc}$ can be changed to (16) by repeating the derivation process above.

$$f_{\Delta dc} = \frac{f_s}{6(1+x)} \tag{16}$$

From (16), when $f_s = 5$ kHz and $x = 0.25$, $f_{\Delta dc}$ is 666 Hz, which is consistent with the simulation and experiment results.

B. AMPLITUDE OF THE FLUCTUATION

According to (5), $\Delta v_{dc}(t)$ can be expressed as (17), where T_{sum} represents the equivalent control cycle when considering the delay effect of the anti-alias pre-filter, and $T_{sum} = (1 + x)T_s$.

$$\Delta v_{dc}(t) = -\frac{T_{sum}}{C} \cdot \sum_{i=A,B,C} (|v_i(t) + v_0(t)| \cdot i_i(t)) \tag{17}$$

In order to simplify the expression of $\Delta v_{dc}(kT_s)$, the variables in (17) are assumed as (18),

$$\begin{aligned} v_A(t) &= M\sin(\omega t) \\ v_B(t) &= M\sin(\omega t - 2\pi/3) \\ v_C(t) &= M\sin(\omega t - 4\pi/3) \\ i_A(t) &= I\sin(\omega t) \\ i_B(t) &= I\sin(\omega t - 2\pi/3) \\ i_C(t) &= I\sin(\omega t - 4\pi/3) \end{aligned} \tag{18}$$

where M represents the modulation index; I represents the amplitude of the output currents; ω represents the fundamental angle frequency. The power factor is considered to be 1. In addition, in order to prevent the three-level operation mode from degrading to two-level operation mode, the value of M is supposed to be greater than 0.5.

According to [13] and [22], if the digital delay does not exist, the injected zero-sequence voltage is approximately a third harmonic. However, a fluctuation exists in the NP potential because of the digital delay, so that it can be inferred that $v_0(t)$ mainly includes a third harmonic and a special harmonic of $f_{\Delta dc}$. The expression of $v_0(t)$ can be assumed as (19),

$$v_0(t) = M_1\sin(3\omega t) + M_2\sin(\omega_{\Delta dc} t) \tag{19}$$

where M_1 and M_2 are the amplitudes of the third harmonic and the special harmonic of $f_{\Delta dc}$, and $\omega_{\Delta dc} = 2\pi f_{\Delta dc}$.

Substituting (18) and (19) into (17), $\Delta v_{dc}(t)$ can be expressed as (20),

$$\begin{aligned}\Delta v_{dc}(t) = &-\frac{T_{sum}I}{C}\cdot\\ &\left\{\begin{array}{l}|M\sin(\omega t)+v_0(t)|\cdot\sin(\omega t)\\ +|M\sin(\omega t-2\pi/3)+v_0(t)|\cdot\sin(\omega t-2\pi/3)\\ +|M\sin(\omega t-4\pi/3)+v_0(t)|\cdot\sin(\omega t-4\pi/3)\end{array}\right\}\\ v_0(t) = &\,M_1\sin(3\omega t)+M_2\sin(N\omega t)\end{aligned} \tag{20}$$

where $\omega_{\Delta dc}$ is assumed to be $N\omega$. It can be seen that $\Delta v_{dc}(t)$ has a relationship with T_{sum}, I, C, M, M_1 and M_2. In fact, the values of M_1 and M_2 depend on M, and these two variables are deduced as follows.

The Fourier expansion of (20) is expressed in (21) and (22),

$$\Delta v_{dc}(t) = -\frac{T_{sum}I}{C}\cdot[g(t)+g(t-2\pi/3)+g(t-4\pi/3)] \tag{21}$$

where,

$$\begin{aligned}g(t) &= \sum_{n=1}^{\infty}\left(\frac{Y(n)}{2}[\sin((2n+1)\omega t)-\sin((2n-1)\omega t)]\right)\\ Y(n) &= -\frac{4}{\pi}\cdot\left[\frac{M}{(2n+1)(2n-1)}\right.\\ &\quad\left.+\frac{3M_1}{(2n+3)(2n-3)}+\frac{NM_2}{(2n+N)(2n-N)}\right]\\ &\quad n=1,2,3,\ldots\end{aligned} \tag{22}$$

The detailed calculation process of the Fourier expansion of (20) has been attached as an appendix at the end of this paper.

Therefore, according to (21) and (22), the components of each frequency in $\Delta v_{dc}(t)$ can be obtained. It can be deduced that the fundamental frequency component is zero in $\Delta v_{dc}(t)$, and the 3rd and N^{th} harmonics occupy a larger proportion than the other components. The amplitudes of the 3rd and N^{th} harmonics are represented by A^{3rd} and A^{Nth}, which are expressed as (23) and (24).

$$\begin{aligned}A^{3rd} &= \left|-\frac{T_{sum}I}{C}\cdot\frac{3}{2}[Y(1)-Y(2)]\right|\\ &\approx \frac{24T_{sum}I}{5\pi C}\cdot\left(\frac{M}{3}-\frac{9M_1}{7}\right)\end{aligned} \tag{23}$$

$$\begin{aligned}A^{Nth} &= \left|-\frac{T_{sum}I}{C}\cdot\frac{3}{2}\left[Y(\frac{N-1}{2})-Y(\frac{N+1}{2})\right]\right|\\ &\approx \frac{6T_{sum}I}{\pi C}\cdot M_2\end{aligned} \tag{24}$$

From (23), the 3rd harmonic in $\Delta v_{dc}(t)$ can be reduced to zero, if M_1 satisfies (25), and this is also why an injected 3rd harmonic zero-sequence voltage can eliminate the 3rd fluctuation of the NP potential in [22].

$$M_1 = \frac{7}{27}M \tag{25}$$

Based on (24), it can be seen that if M_2 does not equal 0, there will be a N^{th} harmonic in $\Delta v_{dc}(t)$. According to the simulation and experiment results in section V and VI, the balance algorithm can hardly suppress M_2 to be 0 when the digital delay exists. In order to calculate the value of A^{Nth}, M_2 can be estimated as below.

Generally, to prevent over modulation, the range of $v_0(kT_s)$ should be limited as (26).

$$\begin{aligned}|M\sin(\omega kT_s)+v_0(kT_s)| &\le 1\\ |M\sin(\omega kT_s-2\pi/3)+v_0(kT_s)| &\le 1\\ |M\sin(\omega kT_s-4\pi/3)+v_0(kT_s)| &\le 1\end{aligned} \tag{26}$$

Through appropriate transformation of (26), the range of $v_0(kT_s)$ is expressed in (27),

$$Lim_{upper} \le v_0(kT_s) \le Lim_{lower} \tag{27}$$

where,

$$\begin{aligned}Lim_{lower} &= -1-\min[v_A(kT_s), v_B(kT_s), v_C(kT_s)]\\ Lim_{upper} &= 1-\max[v_A(kT_s), v_B(kT_s), v_C(kT_s)].\end{aligned} \tag{28}$$

The ranges of $v_0(kT_s)$ with different modulation indexes are shown in Fig. 10.

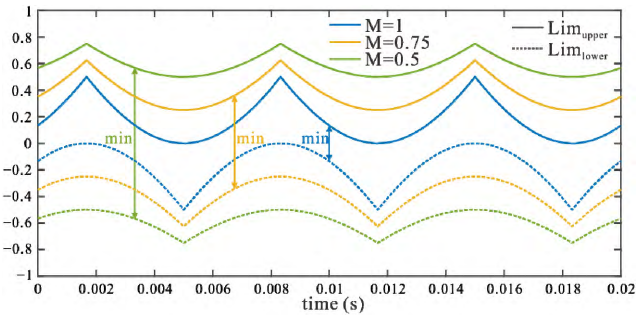

FIGURE 10. The range of $v_0(kT_s)$ with different M.

The N^{th} harmonic in $v_0(kT_s)$ should be also constrained within the value range of (27). Therefore, the value of M_2 should be smaller than the half of the distance between Lim_{upper} and Lim_{lower} as shown in (29).

$$M_2 \le \left(Lim_{upper}-Lim_{lower}\right)/2 \tag{29}$$

From a conservative point of view, the minimum value of (Lim_{upper} - Lim_{lower})/2 should be chosen as M_2, which has a relationship with M as shown in (30).

$$M_2 = \frac{2-\sqrt{3}M}{2} \tag{30}$$

Substituting (30) into (24), the amplitude of $\Delta v_{dc}(t)$ in (10) can be expressed as (31).

$$A = \frac{3T_{sum}I}{\pi C}\cdot\left(2-\sqrt{3}M\right) \tag{31}$$

In summary, the digital delay has a negative effect on the performance of the NP potential balance algorithm, which

leads to a fluctuation at 1/6 control frequency in the NP potential. The amplitude of the fluctuation has a relationship with the control frequency, the modulation index, the amplitude of the ac-side output currents, and the capacitance of the dc-side capacitors. The formula of the amplitude with these variables is shown in (31). The fluctuation in the NP potential increases not only the dc-side capacitor energy loss, but also the ac-side output current distortion. In order to eliminate the fluctuation, an advanced NP potential balance algorithm with a digital delay compensation method is proposed in section IV.

IV. DIGITAL DELAY COMPENSATION METHOD

From the above discussion, the digital delay deteriorates the performance of the zero-sequence voltage injection NP potential balance algorithm. In order to relieve the digital delay influence, the most straightforward method is to increase the computing rate of the DSP, but this puts higher demands on the hardware. In this section, a digital delay compensation method is proposed, which can eliminate the influence of digital delay by enhancing the original balance algorithm.

When ignoring the digital delay as shown in Fig. 4, the calculation process of $v_0(k\mathrm{T_s})$ depends on $\Delta v_{dc}(k\mathrm{T_s})$, and the balance algorithm used to calculate $v_0(k\mathrm{T_s})$ is shown in (4). The unbalance of the NP potential can be compensated completely from $k\mathrm{T_s}$ to $(k+1)\mathrm{T_s}$, so that $\Delta v_{dc}((k+1)\mathrm{T_s})$ is zero as shown in (5).

However, when the digital delay is considered in Fig. 5, if the balance algorithm is still the original one, $v_0(k\mathrm{T_s})$ is generated depending on $\Delta v_{dc}(k\mathrm{T_s})$, but $v_0(k\mathrm{T_s})$ has an impact on the NP potential until $(k+1)\mathrm{T_s}$, which results in the extra fluctuation of the NP potential. In this case, the right approach to obtain the value of $v_0(k\mathrm{T_s})$ is not depending on $\Delta v_{dc}(k\mathrm{T_s})$, but depending on $\Delta v_{dc}((k+1)\mathrm{T_s})$, so that the balance algorithm in (4) should be revised as (32).

$$v_0(k\mathrm{T_s}) = F\left(\Delta v_{dc}((k+1)\mathrm{T_s}), i_{A,B,C}(k\mathrm{T_s}), v_{A,B,C}(k\mathrm{T_s})\right) \tag{32}$$

Although $\Delta v_{dc}((k+1)\mathrm{T_s})$ cannot be directly obtained at the time of $k\mathrm{T_s}$, the value of $\Delta v_{dc}((k+1)\mathrm{T_s})$ can be predicted as expressed in (6).

Based on (6) and (32), the advanced balance algorithm with digital delay compensation can be depicted as Fig. 11. The advanced balance algorithm does not change the calculation process of $v_0(k\mathrm{T_s})$, but only uses $\Delta v_{dc}((k+1)\mathrm{T_s})$ in place of $\Delta v_{dc}(k\mathrm{T_s})$, so the original balance algorithm still remains in Fig. 11.

V. SIMULATION RESULTS

This section verifies the influence of the digital delay on the balance algorithm and the correctness of the proposed digital delay compensation method by means of Matlab/Simulink. The structure of the simulation model is the same as Fig. 1. In order to focus on the NP potential balance algorithm, this paper adopts an open loop control to generate the modulation reference voltage $v_{A,B,C}(k\mathrm{T_s})$. Moreover, the load in Fig. 1 is

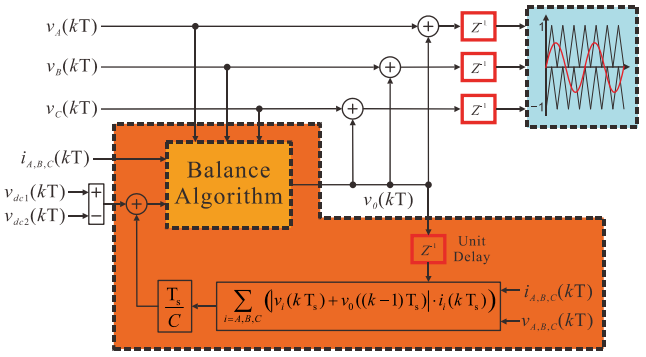

FIGURE 11. The advanced NP potential balance algorithm with digital delay compensation.

a series connection of the resistor and inductor, where R is 10 Ω and L is 600 μH. The power factor can be seen as 1 approximately. The cut-off frequency of the anti-alias pre-filters is set to be 1/3 of the control frequency.

As analyzed in section III, the influence of the digital delay on the balance algorithm has a relationship with four different variables: the control frequency, the modulation index, the amplitude of the output current, and the dc-side capacitance. The following simulations will start from these four variables, and verify the validity of the digital delay compensation algorithm in each case.

A. INFLUENCE OF THE CONTROL FREQUENCY

The influence of different control frequencies on the NP potential balance algorithm is verified in Fig. 12 and Fig. 13, where $f_s = 5$ kHz in Fig. 12 and $f_s = 10$ kHz in Fig. 13.

From 0 s to 0.2 s, the balance algorithm is disabled, and there is obvious unbalance in the NP potential. At the time of 0.2 s, the balance algorithm is enabled and Δv_{dc} starts to decrease, but there is still an apparent fluctuation in the NP potential caused by the digital delay. When the digital delay compensation method is added to the balance algorithm at 0.5 s, the difference between the two capacitor voltages are completely eliminated.

Comparing Fig. 12 and Fig. 13, from 0.2 s to 0.5 s, the amplitudes of Δv_{dc} are 3 V and 1.2 V respectively in Fig. 12 and 13, so it can be seen that when the control frequency is doubled, Δv_{dc} reduces to about half of the original value.

Fourier analysis is also applied to the zero-sequence voltage and the NP potential fluctuation (Δv_{dc}) when the balance algorithm works without the digital delay compensation method. It can be seen that in addition to the 3rd harmonic, there is a high frequency component in the zero-sequence voltage, and there is also a same high frequency component in the NP potential fluctuation.

According to the above analysis, the frequency of the high frequency component should be 1/6 of the control frequency. However, in the Fourier analysis, the frequency of the component is 650 Hz when $f_s = 5$ kHz, and 1350 Hz when $f_s = 10$ kHz, which is not in complete agreement with the

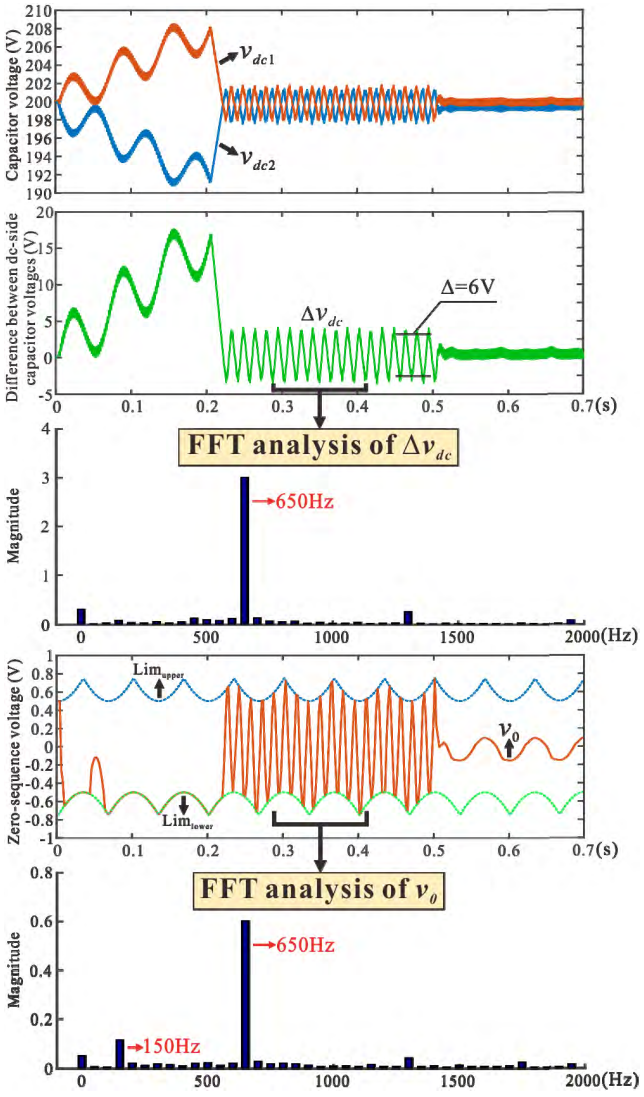

FIGURE 12. Simulation results with f_S = 5 kHz, M = 0.5, I = 10 A, C = 720 μF, v_{dc} = 400 V.

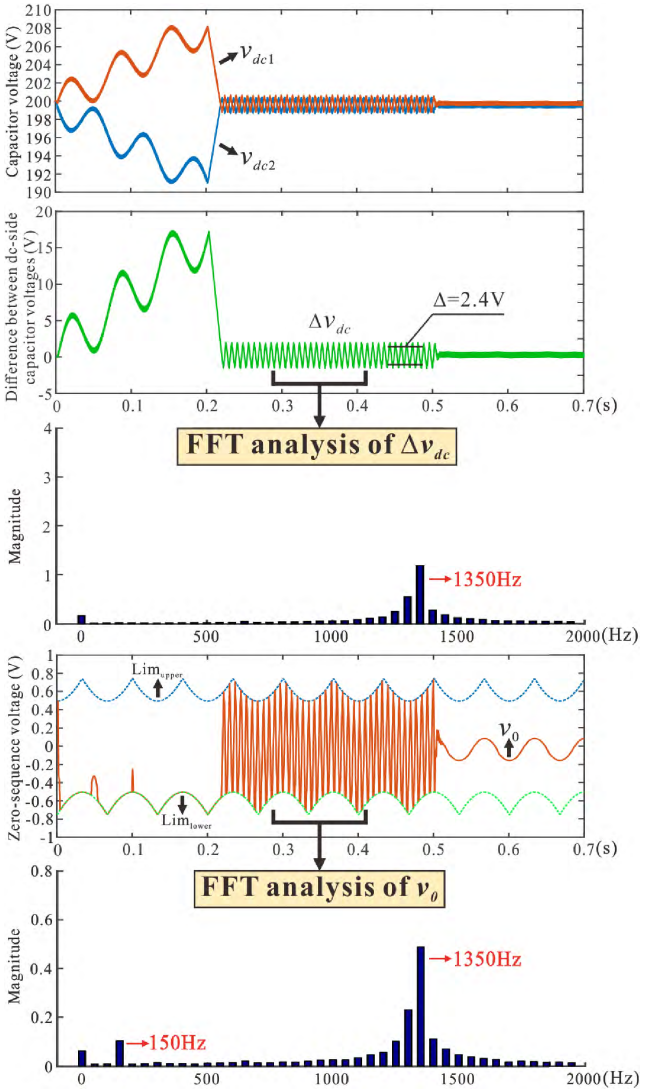

FIGURE 13. Simulation results with f_S = 10 kHz, M = 0.5, I = 10 A, C = 720 μF, v_{dc} = 400 V.

theoretical analysis in (12). This is due to the delay effect of the anti-alias pre-filters. These filters are usually one-order low-pass filters, which can also be seen as a small digital delay equivalently. Therefore, the simulation results are a little bit different from the theoretical analysis. In order to verify the influence of the anti-alias pre-filters, the simulation results without the anti-alias pre-filters are shown in Fig. 14 and Fig. 15.

In Fig. 12, the control frequency is 5 kHz with the anti-alias pre-filters, but, in Fig. 14, the control frequency is 4 kHz without the anti-alias pre-filters. It can be seen that the simulation results in Fig. 12 and Fig. 14 are almost the same, which verifies that the "the anti-alias pre-filter delay + one cycle digital delay" can be seen as "1.25 cycle digital delay" as analyzed in Section III, which means that if we delete the anti-alias pre-filters, the control frequency should be changed to $f_s/1.25$ to keep the whole system equivalent.

The anti-alias pre-filters are used in Fig. 12, but removed in Fig. 15. It can be seen that the if the anti-alias pre-filters are removed, the frequency of the NP potential fluctuation is the same as the theoretical analysis in (12). There is an another interesting phenomenon in Fig. 15: when the anti-alias pre-filters are removed, the amplitude of the NP potential fluctuation is smaller, which means the anti-alias pre-filters also has an effect on the amplitude of the NP potential fluctuation, which has been mentioned in the derivation process of the NP potential fluctuation amplitude.

B. INFLUENCE OF THE MODULATION INDEX

Fig. 16 (a) and (b) are compared to clarify the influence of the modulation index on the balance algorithm with consideration of the digital delay. In this case, the modulation index is 1 in Fig. 16 (a), and 0.75 in Fig. 16 (b). In order to keep the amplitudes of the output current in Fig. 16 (a) and (b) to be the same, the dc-side voltage is 200 V in (a) but 266 V in (b).

The simulation procedure is the same as that in the previous part, and the digital delay compensation method also

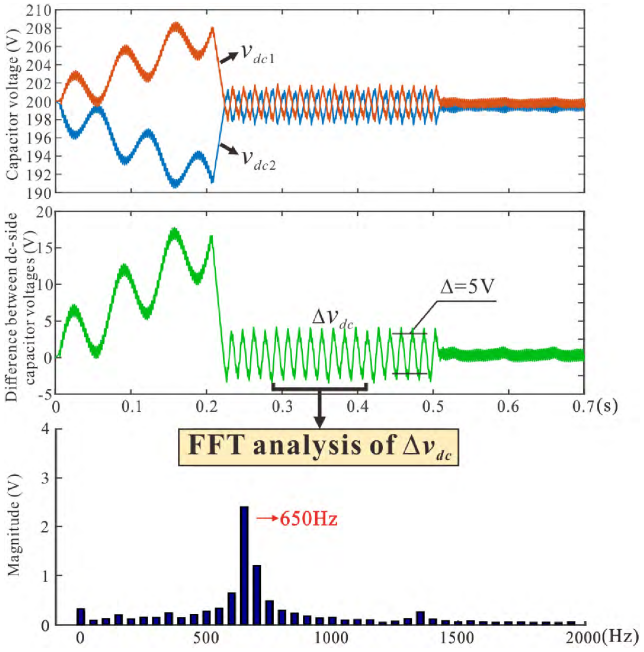

FIGURE 14. Simulation results with f_s = 4 kHz, M = 0.5, I = 10 A, C = 720 μF, v_{dc} = 400 V and no anti-alias pre-filters.

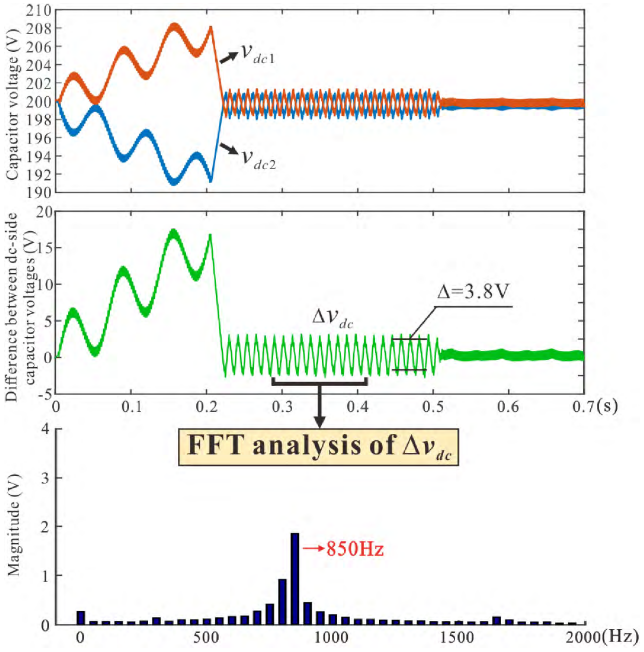

FIGURE 15. Simulation results with f_s = 5 kHz, M = 0.5, I = 10 A, C = 720 μF, v_{dc} = 400 V and no anti-alias pre-filters.

maintains a good performance in this situation. From Fig. 16, it can be seen that as soon as the digital delay compensation method operates, the zero-sequence voltage changes to an approximate 3rd harmonic, and the high frequency component disappears.

In addition, the amplitude of Δv_{dc} is only about 0.67 V when M = 1, whereas the amplitude increases to 2.11 V

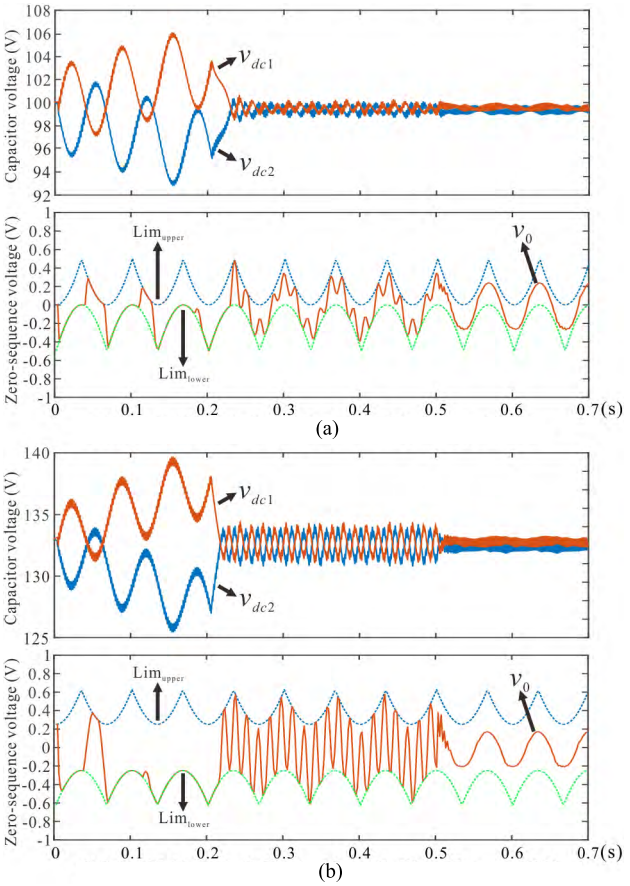

FIGURE 16. Simulation results with different modulation indexes.

when M = 0.75. This is because when the modulation is larger, the upper and lower limitation for the injected zero-sequence voltage is closer, so that the remaining space for the high frequency oscillation component is smaller, and the fluctuation in Δv_{dc} is smaller either.

TABLE 1. The error percentages.

f_s = 5 kHz, C = 720 μF, I = 10 A.					
M	0.6	0.7	0.8	0.9	1
v_{dc}	333V	285V	250V	222V	200V
A of (31)	3.18V	2.61V	2.04V	1.46V	0.88V
A of simulation	2.99V	2.45V	1.81V	1.18V	0.67V
Error percentage	6.3%	6.5%	12.7%	23.7%	33%

It should be noted that (31) is not a precise calculation formula, and the error percentages of the NP potential fluctuation amplitude between the calculation results of (31) and the simulation results under different modulation indexes are shown in Table 1 and Table 2 where A presents the amplitude of the NP potential fluctuation, and it can be seen the calculation results of (31) is more accurate when the control frequency is higher.

C. INFLUENCE OF THE OUTPUT CURRENT

In Fig. 17, different amplitudes of the output current are studied, where the amplitude is 8 A in (a) and 16 A in (b), and

TABLE 2. The error percentages.

f_s = 10 kHz, C = 720 μF, I = 10 A.					
M	0.6	0.7	0.8	0.9	1
v_{dc}	333V	285V	250V	222V	200V
A of (31)	1.59V	1.31V	1.02V	0.73V	0.44V
A of simulation	1.57V	1.34V	1.03V	0.68V	0.4V
Error percentage	1.3%	2.2%	0.9%	7.3%	10%

the other simulation conditions are kept the same. In order to achieve the same modulation index but different amplitudes of the output current, the dc-side voltage in Fig. 17 (a) is 200 V, but in Fig. 17 (b) is 400 V.

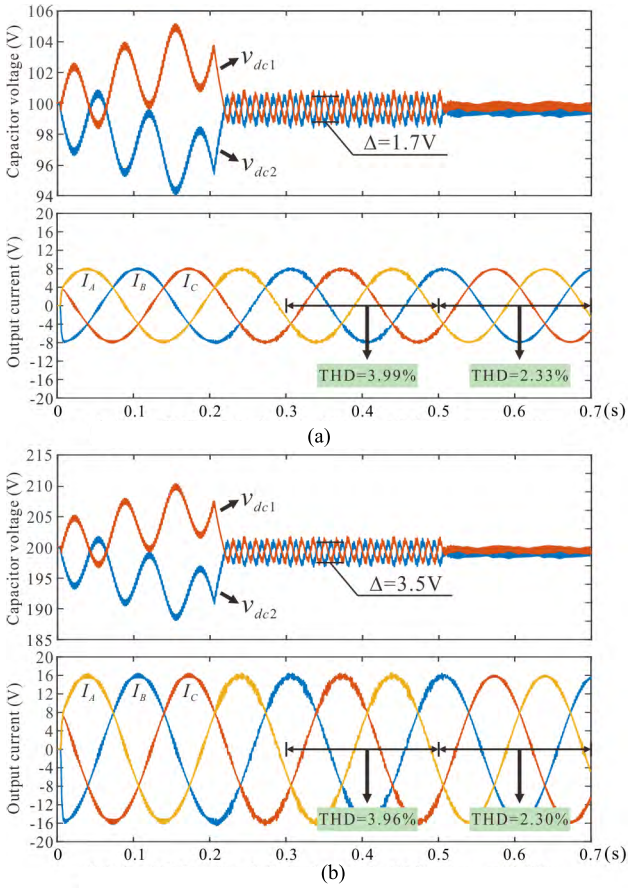

FIGURE 17. Simulation results with different output currents.

When the amplitude of the output current is doubled from 8 A to 16 A, Δv_{dc} is also doubled in Fig. 17. It can also be seen that when the digital delay influence is not eliminated, there is also more distortion in the output currents. Through the application of the digital delay compensation method, the THD of the output current reduces to 2.33% from 3.99% in Fig. 17 (a), and the THD reduces to 2.3% from 3.96% in Fig. 17 (b).

D. INFLUENCE OF THE DC-SIDE CAPACITANCE

Fig. 18 reveals the digital delay influence of the dc-side capacitance on the balance algorithm. The conditions used in the simulation are shown in Fig. 18. When the dc-side capacitance is 360 μF in Fig. 18 (a), the amplitude of Δv_{dc} is 7 V, whereas the capacitance in (b) reduces to 180 μF and the amplitude of Δv_{dc} increases to 14 V. Therefore, the digital delay compensation method is more needed in small dc capacitance applications.

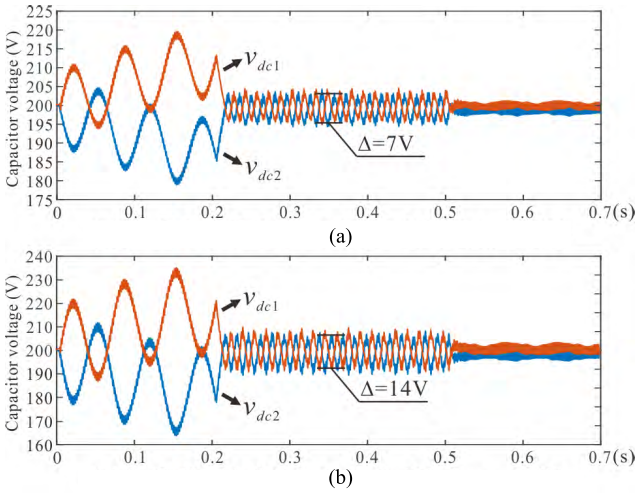

FIGURE 18. Simulation results with different dc-side capacitances.

E. INFLUENCE OF THE POWER FACTOR

The simulation results above are all within the fully controllable region as shown in Fig. 2. This part is used to verify that the digital delay compensation method is still effective beyond the fully controllable region, and the simulation results are shown in Fig. 19. The simulation conditions in Fig. 19 are: the control frequency is 5 kHz; the modulation index is 1; the dc-side capacitance is 720 μF; the dc-side voltage is 400 V; the inductance of the load is 30 mH; the resistance of the load is 10 Ω. Because the modulation index is 1 and the power factor angle of the load is 43.3°, this simulation case is beyond the fully controllable region according to Fig. 2. In Fig. 19, it can be seen that the maximum value of the difference between the two dc-side capacitor voltages decreases from 13 V to 11 V when the digital delay compensation method is applied, so the digital delay compensation method can still reduce the voltage difference beyond the fully controllable region, but the effect is not very obvious. This is because that the digital delay compensation method proposed in this paper can only eliminated the NP potential fluctuation caused by the digital delay. When the conditions are not in the fully controllable region, there will also be NP potential fluctuation, but this fluctuation is caused by the power factor and cannot be compensated by the method proposed in this paper. Therefore, in order to focus on the influence of the digital delay on the balance algorithm, the power factor used in this paper is set to be about 1, which

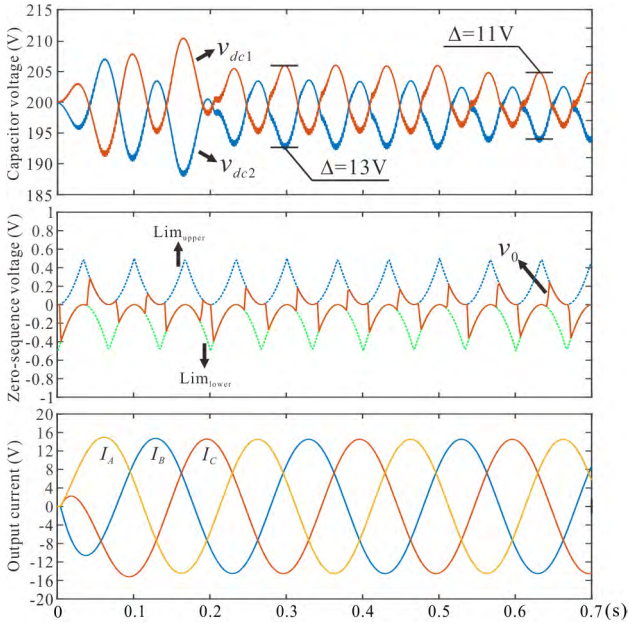

FIGURE 19. Simulation results beyond the fully controllable region.

TABLE 3. Parameters of the three-level NPC inverter.

Symbol	Descrition	Value
v_{dc}	dc-side voltage	200/266/400 V
C	dc-side capacitance	720 μF
f_s	control frequency	5/10 kHz
L	inductance of the load	600 μH
R	resistance of the load	10 Ω
f	fundamental frequency	50 Hz

means the cases studied in this paper are mainly within the fully controllable region.

VI. EXPERIMENT RESULTS

A three-level NPC inverter prototype as shown in Fig. 20 has been built to validate the influence of the digital delay on the balance algorithm and the digital delay compensation method. The parameters of the prototype are shown in Table 3. The digital controller is realized by a TMS320F28335 DSP. The PWM signals generated by the EPWM module of the DSP are processed by an ALTERA

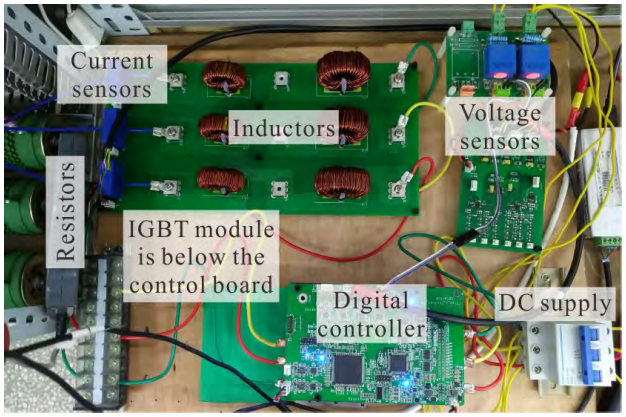

FIGURE 20. The photography of the setup and the prototype.

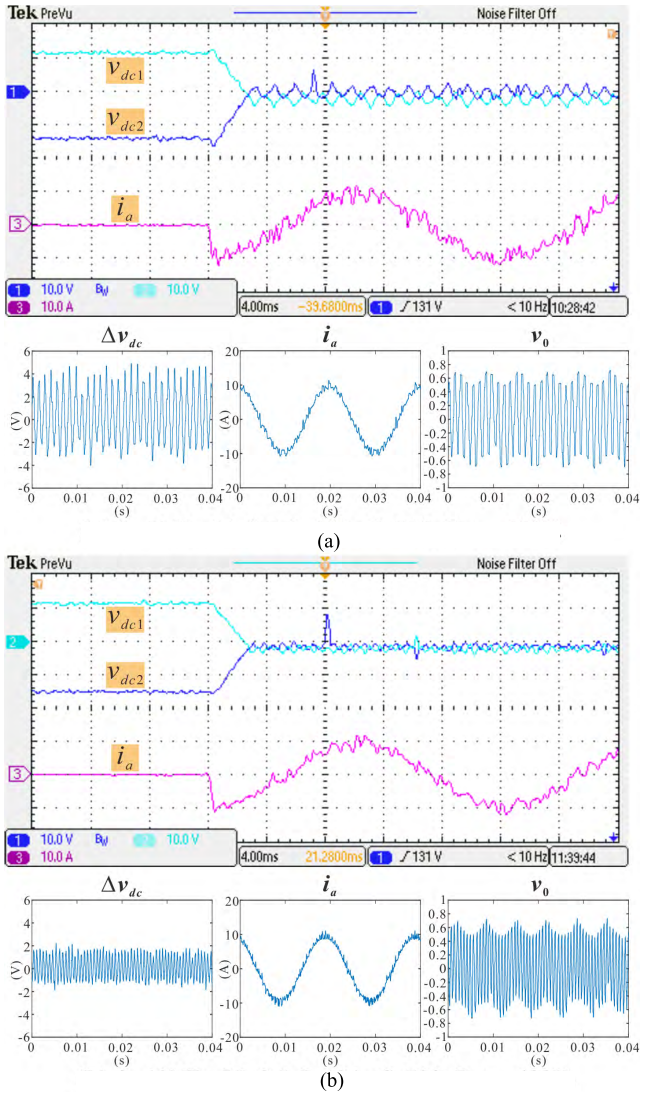

FIGURE 21. Experiment results without the digital delay compensation. (a) and (b) with different control frequencies.

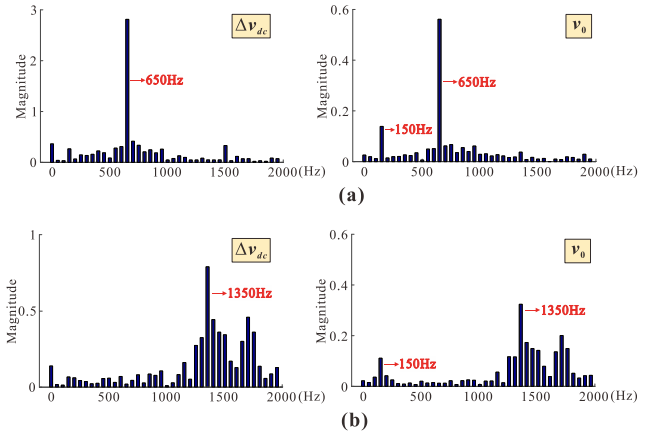

FIGURE 22. Fourier analysis of Δv_{dc} and v_0 in Fig. 21.

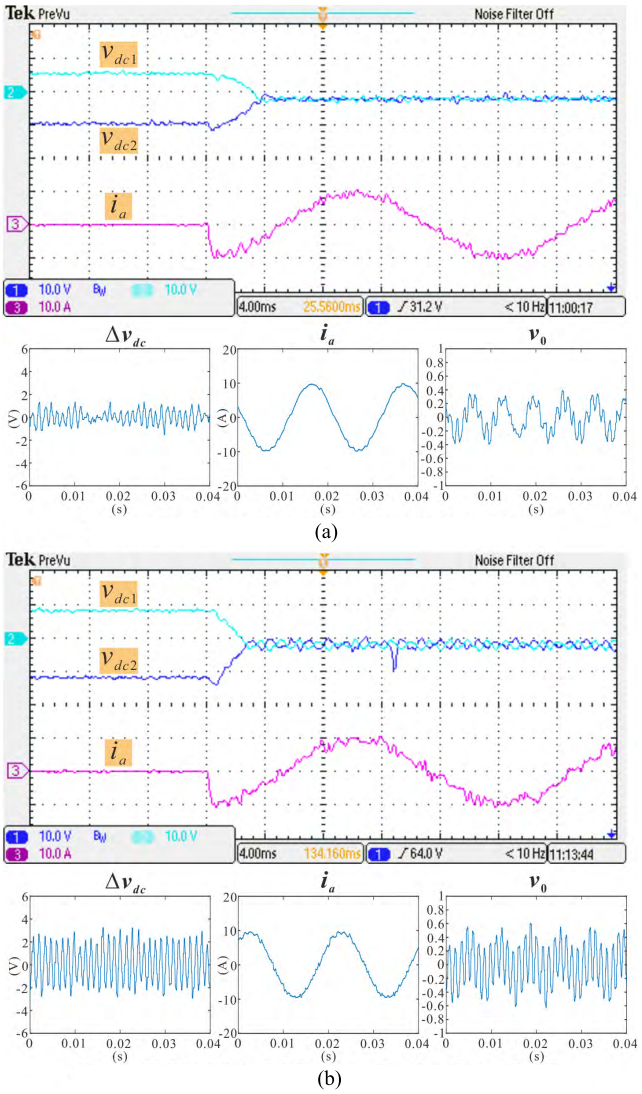

FIGURE 23. Experiment results without the digital delay compensation. (a) and (b) with different modulation indexes.

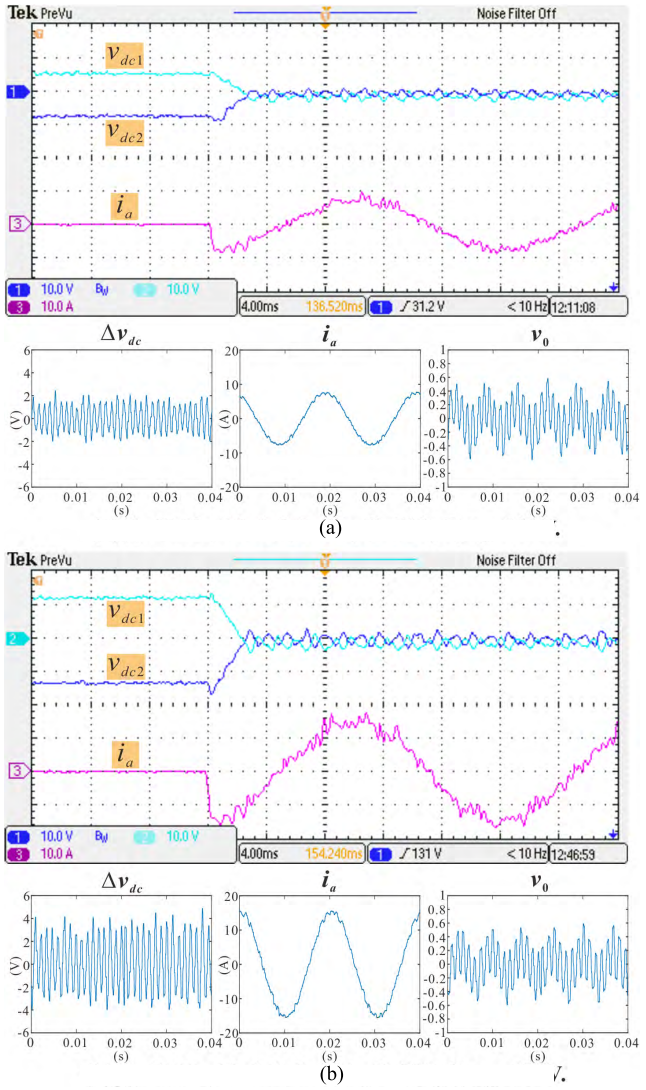

FIGURE 24. Experiment results without the digital delay compensation. (a) and (b) with different output current amplitudes.

MAX II Complex Programmable Logic Device (CPLD) then transmitted to the driver board of the FS3L50R07W2H3F Infineon IGBT module. The entire IGBT module is cooled by water. A TDK-LAMBDA GEN 500-30 programmable DC supply is used to act as a DC power source on the dc side of the prototype. The load of the three-level inverter is a series connection of the inductors and resistors, and the power factor is approximately equal to 1. Hall effect current and voltage sensors, whose types are LA 55-P and LV 25-P, are adopted to sample the current and voltage signals. The signals sampled by the sensors are transmitted to the DSP after filtered by the anti-alias filters. The whole control system is shown in Fig. 11.

During the experiment, the signals displayed by the oscilloscope are the voltages of the two dc-side capacitors and the ac-side output current of A phase. The directions of the voltages and currents are the same as that in Fig. 1. In addition, certain offsets have been set in the capacitor voltage channels of the oscilloscope for a clearer display. In order to display the waveform of the injected zero-sequence voltage, this paper uses the circular buffer function of the DSP: continuously collecting the value of the zero-sequence voltage at the control frequency, then uploading the data to the upper computer and saving the data as an Excel document, and finally importing the data into Matlab for waveform display and Fourier analysis.

Fig. 21, 23 and 24 tests the influence of the control frequency, the modulation index and the output current amplitude on the NP potential balance algorithm without the digital delay compensation. Since the power module of the prototype is relatively integrated, it is not convenient to disassemble the dc-side capacitors. So there is no test result with different dc-side capacitances. In Fig. 21, 23 and 24, the voltages of the two dc-side capacitors have obvious deviation before the balance algorithm operates. The dynamic process when the NP potential balance algorithm starts to work has been recorded in each case. It can be seen that the unbalance in the NP potential can be compensated by the balance algorithm

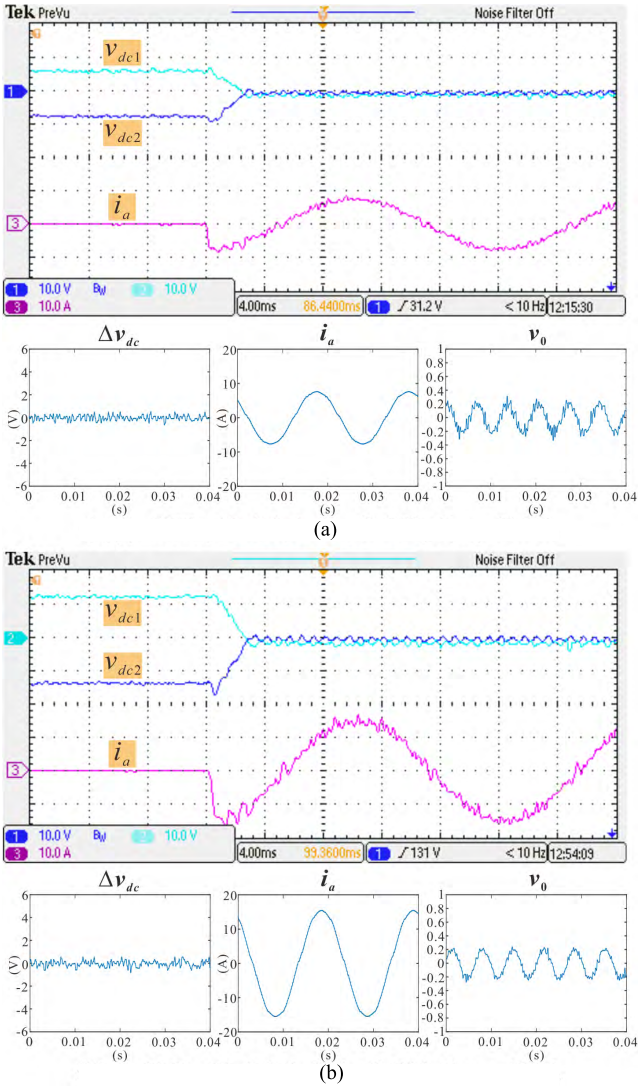

FIGURE 25. Experiment results with the digital delay compensation comparing with Fig. 24.

but not completely. Due to the existence of the digital delay, there are still fluctuation in the NP potential and the zero-sequence voltage is also mix by a high frequency component which leads to higher THD in the output currents.

The frequency of the fluctuation caused by the digital delay has a relationship with the control frequency as discussed in section III. The Fourier analysis of Δv_{dc} and v_0 in Fig. 21 (a) and (b) has been made as shown in Fig. 22. In Fig. 22, there is a 650 Hz component in Δv_{dc} when the control frequency is 5 kHz, and a 1350 Hz component when the control frequency is 10 kHz. The fluctuation frequency is about 1/6 of the control frequency and in agree with the simulation results. Furthermore, a corresponding high frequency component also exists in the zero-sequence voltage except the 150 Hz component.

The amplitude of the fluctuation is related to the control frequency, the modulation index, the amplitude of the output current and the dc-side capacitance. The estimation equation of the amplitude is shown in (31). In all the experiment results, the amplitudes of the fluctuation are almost the same as the calculation results of (31).

In order to verified the effectiveness of the proposed digital delay compensation method, the experiment results of the NP balance algorithm with the digital delay compensation are shown in Fig. 25 (a) and (b). Compared with Fig. 24 (a) and (b), Δv_{dc} almost reduces to zero, and v_0 also shows as an approximate pure 150 Hz component instead of being mixed with a high frequency component, so that the advanced balance algorithm with the digital delay compensation method is correct.

In general, in some cases, the fluctuation in the NP potential caused by the digital delay will be large. The advance balance algorithm proposed in this paper shows a good performance in eliminating the extra fluctuation.

VII. CONCLUSION

This paper has studied the digital delay influence on the zero-sequence voltage injection NP potential balance algorithm for three-level NPC inverters. It is found that the digital delay not only causes an extra NP potential fluctuation, but also increases the THD of the ac-side output current. In order to eliminate the adverse effects of the digital delay, this paper has proposed a digital delay compensation method. Finally, the enhanced balance algorithm has been verified by the simulation and experiment results.

VIII. APPENDIX

The detailed Fourier expansion process of (20) is as follows. Supposing,

$$f(t) = |\mathrm{M}\sin(\omega t) + \mathrm{M}_1\sin(3\omega t) + \mathrm{M}_2\sin(N\omega t)|$$
$$= f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(a_n\cos 2n\omega t + b_n\sin 2n\omega t)$$
$$n = 1, 2, 3, \ldots \quad \text{(A1)}$$

According to the principles of Fourier series,

$$a_n = \frac{2\omega}{\pi}\int_0^{\frac{\pi}{\omega}}\begin{pmatrix}\mathrm{M}\sin(\omega t)+\\ \mathrm{M}_1\sin(3\omega t)+\\ \mathrm{M}_2\sin(N\omega t)\end{pmatrix}\cos 2n\omega t dt$$
$$= -\frac{4}{\pi}\begin{bmatrix}\dfrac{\mathrm{M}}{(2n+1)(2n-1)}+\\ \dfrac{3\mathrm{M}_1}{(2n+3)(2n-3)}+\\ \dfrac{N\mathrm{M}_2}{(2n+N)(2n-N)}\end{bmatrix} = Y(n)$$
$$b_n = \frac{2\omega}{\pi}\int_0^{\frac{\pi}{\omega}}\begin{pmatrix}\mathrm{M}\sin(\omega t)+\\ \mathrm{M}_1\sin(3\omega t)+\\ \mathrm{M}_2\sin(N\omega t)\end{pmatrix}\cdot\sin 2n\omega t dt = 0 \quad \text{(A2)}$$

Therefore,

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}(Y(n)\cos 2n\omega t), \quad n = 1, 2, 3, \ldots \quad \text{(A3)}$$

So the Fourier series of (20) can be obtained as shown in (A4).

$$\begin{aligned}\Delta v_{dc}(t) &= -\frac{T_{sum}I}{C}\cdot\begin{Bmatrix} f(t)\cdot\sin(\omega t)+ \\ f(t-\frac{2\pi}{3\omega})\cdot\sin(\omega t-2\pi/3)+ \\ f(t-\frac{4\pi}{3\omega})\cdot\sin(\omega t-4\pi/3)\end{Bmatrix} \\ &= -\frac{T_{sum}I}{C}\cdot[g(t)+g(t-2\pi/3)+g(t-4\pi/3)] \\ g(t) &= \sum_{n=1}^{\infty}\left(\frac{Y(n)}{2}[\sin((2n+1)\omega t)-\sin((2n-1)\omega t)]\right)\end{aligned} \tag{A4}$$

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