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A Varactor-Less DCO With 7 *GHz* Tuning Range for 77 *GHz* Automotive Radars

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ABSTRACT The generation of precise linear frequency modulation is a critical requirement for millimeter-wave automotive radars. This paper presents the analysis and design of a CMOS 75.5 − 82.5 *GHz* monotonically linear digitally controlled oscillator (ML-DCO) fulfilling the requirements of the 77 *GHz* automotive radar. Non-linear large varactors are avoided. Linear coarse, intermediate, and fine-tuning ranges are achieved by arranging the available minimum Metal-Oxide-Metal (MoM) capacitor in unique configurations. Moreover, a new tuning mechanism derived from a Colpitts topology is discussed to meet the wide tuning requirements without losing linearity. The new arrangement results in a minimal amplitude variation while the ML-DCO is tuned. The coarse, intermediate, and fine-tuning steps from the post-layout simulation are 0.22, 10, and 346 *KHz*, respectively. The power consumption is 14 *mW* from a 1.2 *V* supply. The achieved phase-noise is −98.53 *dBc*/*Hz* at a 1 *MHz* offset when oscillating at 77 *GHz*. The ML-DCO demonstrates −185 Figure of Merit and −184 Figure of Merit for Tuning.

INDEX TERMS Digitally controlled oscillator (DCO), frequency resolution, millimeter-wave frequency, stable amplitude of oscillation, varactor-less digitally controlled oscillator (DCO), wide tuning range.

I. INTRODUCTION

A. BACKGROUND

Automotive radar sensors are mounted around vehicles to enable a 360° safety zone. While millimeter-wave (mm-wave), infrared, laser, and ultrasonic sensors have been proposed, the mm-wave automotive sensor offers superior robustness against extreme weather environments such as temperature, rain, snow and fog [1].

The automotive Short Range Radar (SRR) detects objects in the distance range of 0.15-30 *m*, enabling pre-crash sensing, blind-spot detection, and collision avoidance. In contrast, the automotive Long Range Radar (LRR) is primarily used for Automatic Cruise Control (ACC), which senses long distance range of 10-250 *m*.

The Frequency Modulated Continuous Wave (FMCW) method is usually utilized in automotive radar transceivers, which calls for a linear frequency sweep to measure the range and velocity of objects [2]. The accuracy of the measurement in FMCW radar depends on the linearity of the frequency sweep generated by the frequency synthesizer, which in turn requires linearizing the DCO frequency response. Non-linearity in the sweeping range widens and shifts the peaks along the frequency axis, which increases the estimation variance and introduces a systematic bias in distance estimation [2].

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B. MOTIVATION

CMOS is an appealing technology due to its low cost and potential for System-on-Chip (SoC) integration [3]. CMOS automotive transceivers for automotive radars have been reported in [1] and [4]. The typical distance resolutions for commercial SRR and the LRR are 10 *cm* and 50 *cm* respectively [2]. The mm-wave automotive radar operating bands are located near 24 *GHz* or 77 *GHz*. The wavelength of the 77 *GHz* W-band is smaller than that of the 24 *GHz* K-band automotive radar. The significant reduction in the wavelength leads to a more compact size allowing for further integration [4].

The All-Digital-Phase-Locked-Loop (ADPLL) is an attractive system architecture for realizing a frequency synthesizer in the W-band. The digital implementation for the loop-filter allows full integration to allow scalability and total loop parameter reconfigurability (e.g. loop bandwidth and phase margin) [5]. The DCO is the heart of ADPLL and its application in FMCW radar mandates low Phase-Noise (PN) and wide Tuning Range (TR) [6].

C. OUR CONTRIBUTION

In [7], we report a 77 GHz DCO with 5 GHz linear TR to alleviate the need for an ideal switch. This paper expands and optimizes the description in [7] to present more detailed design considerations and rigorous analysis for the proposed ML-DCO.

The contributions of this paper are as follows.

1) We design a varactor-less DCO with TR as wide as 7 GHz to allow for Process, Voltage, and Temperature (PVT) calibration while still covering the bands of the 77 GHz automotive SRR and LRR.
2) We demonstrate the operation of the varactor-less new frequency step generating mechanism, which can potentially open a new era for the design of a linear wide TR mm-wave DCO.
3) We analyze amplitude stability across the TR, which is enforced by the new tuning mechanism without the need for extra circuitry to automatically stabilize the amplitude. Moreover, amplitude stability is not in trade-off with the wide TR.
4) We evaluate the innovative linear coarse, intermediate and fine-tuning steps and the DCO performance with post-layout simulations.

The rest of this paper is organized as follows. Section II details the design challenges. Section III presents related work in overcoming the trade-off in the design requirements. The Colpitts oscillator and the negative resistance models are presented in Section IV. Section V discusses design constraints, drawing attention to the tuning constraints and analyzing amplitude stability. The mechanism of the new frequency step generator is presented in Section VI. Section VII describes the circuit design. The corners, Monte Carlo, post-layout simulations, and fabrication measurements of the first prototype are reported in section VIII.

II. DESIGN CHALLENGES

Low PN oscillators call for Colpitts or LC-tank based topologies. The start-up condition for the conventional LC-tank topology is more relaxed than the Colpitts. However, the LC-tank topology suffers from narrow TR, low output power, and higher PN [8]–[10]. Moreover, the TR of the LC-tank operating beyond 20 GHz is inadequate since the binary-weighted band-switching technique is no longer applicable [11].

Range resolution (ΔR) is a crucial requirement of the FMCW radar, which depends on the transmitter bandwidth and consequently on the TR of the local oscillator. The bandwidth (B) and ΔR are related by $\Delta R = c/2B$, where c is the speed of light. The 77 GHz FMCW automotive radar mandates a DCO with 5 GHz TR to realize ΔR of 3 cm.

The frequency of oscillation for a resonator based oscillators is expressed by:

$$f_o = \frac{1}{2\pi\sqrt{LC_L}} \tag{1}$$

where f_o is the oscillating frequency, L is the tank inductor, and C_L is the effective capacitor, which appears in parallel with the L.

By taking the derivative $\frac{\delta f_o}{\delta C_L}$, the frequency resolution is approximated by:

$$\Delta f_o = \Delta C_L \frac{f_o}{2C_L} \tag{2}$$

where the frequency resolution $\Delta f_o \approx \delta f_o$ and $\Delta C_L \approx \delta C_L$ is the minimum capacitance step.

Since Δf_o in Eq. (2) is proportional to ΔC_L, the fine frequency step deteriorates in higher frequencies if the minimum unit capacitor is not decreased by the same factor. Therefore, the fine frequency step becomes an issue in the design of W-band DCO [12].

Another significant issue related to the PN is the quality factor of the LC tank, which is expressed by:

$$\frac{1}{Q_T} = \frac{1}{Q_L} + \frac{1}{Q_{C_L}} \tag{3}$$

where Q_T, Q_L, and Q_{C_L} are the quality factors of the tank, the tank inductor, and the effective capacitor respectively.

The value of Q_L tends to increase with frequency, while Q_{C_L} decreases with frequency [13].

When the radar is operating in the W-band frequency, the effect of Q_{C_L} dominates Q_T. The PN performance is affected by the degradation of the Q_T and is a major challenge in designing W-band DCOs [8].

The linearity and the quality factor of the NMOS transistor in N-well Accumulation MOS (AMOS) varactors are better than the transistor or the diode varactors [13]. However, AMOS is sensitive to PVT variations. Here, the AMOS is avoided in the design of mm-wave DCOs due to the significant drop in its quality-factor at mm-wave frequencies which severely degrade the PN performance [14]. Moreover, DCOs tuned with switched AMOS suffer from poor frequency resolution. As an example, if L and C_L of a 77 GHz LC-tank DCO are 80 pH and 53 fF respectively, then a fine-tuning step of 1 MHz requires a minimum varactor size $\Delta C_L = 1.4\ aF$, which may not be justified in the CMOS process.

A unit capacitor cell consisting of an NMOS switch connecting two series MoMs or Metal-Insulation-Metal (MiM) capacitors is often used to provide the large tuning step for the DCOs [1], [15]. While this configuration can be used to facilitate wide tuning requirements, it is restricted to coarse tuning. The precision and matching of the minimum switched MoM capacitor for the fine tuning is affected by the series parasitic capacitance of the NMOS switch and the interconnections being higher than minimum MoM capacitance [6].

III. RELATED WORK

In order to overcome the design challenges in Section II, the effect of the switch and varactor loading were addressed in [11] by proposing a nonuniform standing-wave oscillator topology with switched transmission lines. The reported TR and centre frequency are 20% and 40 GHz respectively. However, the wide TR is non-linear and is segmented into several smaller linear tuning regions. Moreover, the distributed VCO structure is at the expense of area and power consumption.

Reference [6] propose a varactor-less CMOS 60 *GHz* DCO with 6 *GHz* TR. The magnetic field of the resonator is disturbed by digitally varying the position of the metal strips (acting as switched capacitors) distributed beneath the resonator. The reported PN is limited to -94 dBc/Hz. The disturbed field can deteriorate the quality-factor of the inductor and increase the design complexity. One of the conventional techniques used to reduce the substrate loss and to improve the inductor quality factor is to place a patterned ground shield below the inductor [8], [16]. Transformer coupling was also proposed by [6] for the fine-tuning. However, a small coupling factor is needed to scale down the switched capacitor turning it to be sensitive to process variations.

While MOS switches are not used in [12], a 60 Hz CMOS DCO with 14% TR is designed based on C-2C switched capacitor ladder technique. However, non-linearity is still present, and it was assumed that it would be calibrated later in the digital domain.

The variation of the amplitude of oscillation (V_{osc}) is another issue to be avoided in wide TR DCOs. Stabilizing V_{osc} at the steady-state oscillation suppresses the amplitude-to-phase conversion [17]. However, V_{osc} variation changes the phase of oscillation that appears in the impulse response of the DCO [18]. Moreover, the decrease in V_{osc} leads to an increase in the PN [19].

The amplitude of an mm-wave VCO is stabilized in [20] by employing vackar topology. However, amplitude stability is in trade-off with the TR limitation and the TR is limited to just 1.7%. The work in [21] reports a 4.56% amplitude variation for 24 *GHz* SRR that is not in trade-off with wide TR requirement of 29%. The Colpitts-Clapp topology is implemented and an automatic amplitude stabilization circuitry is added to adjust the biasing current based on the coarse tuning bits.

IV. COLPITTS NEGATIVE RESISTANCE MODEL

Fig. 1(a) shows a common-drain differential Colpitts oscillator, where the capacitor C_2 is the tuning capacitor of the Colpitts oscillator. The impedance (Z_{in}) looking into the gate of M_1 is derived using the half circuit model shown in Fig. 1(b) and can be expressed by:

$$Z_{in} = \frac{V_x}{I_x} \cong \frac{1}{j\omega C_1'} + \frac{1}{j\omega C_2'} - \frac{g_{m1}}{\omega^2 C_1' C_2'} \tag{4}$$

where C_1' is the combination of the feedback capacitor between the gate and the source of the switching device M_1 and the parallel parasitic capacitors of M_1 ($C_1' = C_1 + C_{gs1} + C_{gd1}$), C_2' represents the tuning capacitor of the Colpitts and the associated parallel parasitic capacitors ($C_2' = C_2 + C_{sb1}$), and g_{m1} is the small signal transconductance of M_1.

Equation (4) reveals that Z_{in} is equivalent to a series combination of C_1' with C_2' and a negative resistance R_{neg1} that is equal to:

$$R_{neg1} = -\frac{g_{m1}}{\omega^2 C_1' C_2'} \tag{5}$$

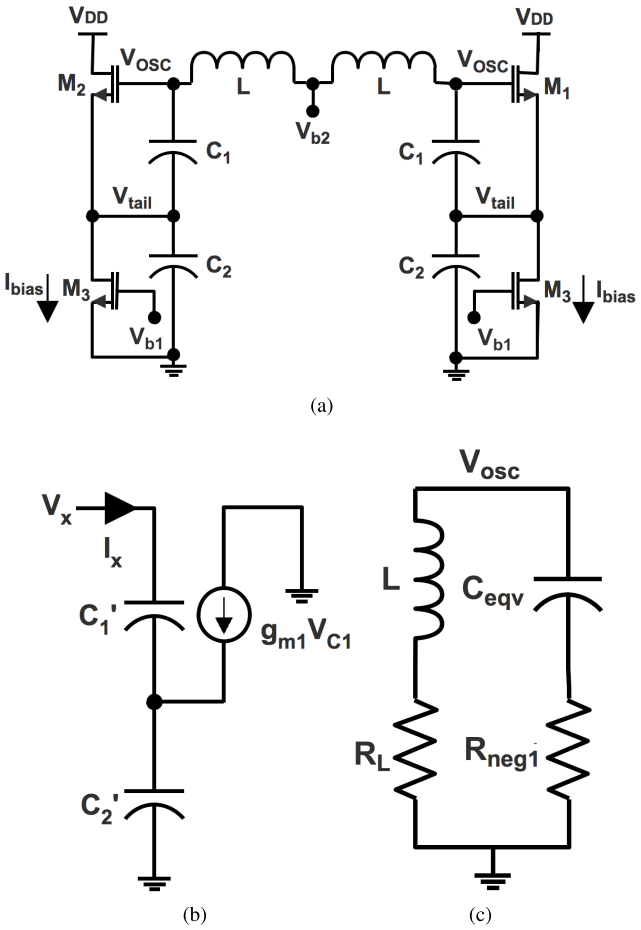


FIGURE 1. (a) Differential Colpitts schematic. (b) Small-signal impedance model looking into the gate of M_1. (c) Colpitts small signal negative resistance based model.

The small-signal negative resistance model is shown in Fig. 1(c). The lossy inductor L in series with the parasitic resistance R_L is connected to Z_{in}.

If $\mid R_{neg1} \mid > R_L$, instability is enforced and oscillation starts, where V_{osc} grows-up until it is stopped by the non-linearity of the circuit.

At the frequency of oscillation, the inductor L resonates with C_1' in series with C_2' and the central frequency $f_{o_{colpitts}}$ is given by:

$$f_{o,colpitts} = \frac{1}{2\pi\sqrt{L(\frac{C_1' C_2'}{C_1' + C_2'})}} \tag{6}$$

V. DESIGN CONSIDERATIONS

In this section, we illustrate the design considerations for tuning at the W-band operation frequency. We explain the MOS Transmission Gate (TG) switch Model and analyze the oscillation amplitude to establish independence from the tuning capacitors and remain stable across the wide TR.

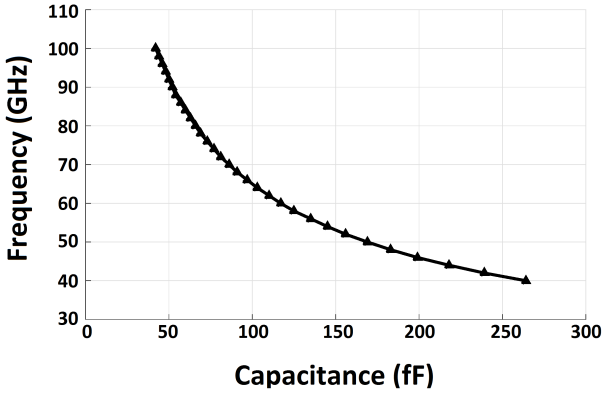
A. TUNING CONSTRAINTS

While the Colpitts oscillator in Fig. 1(a) is tuned by C_2, the ML-DCO [7] utilizes the capacitors C_1 and C_2 together

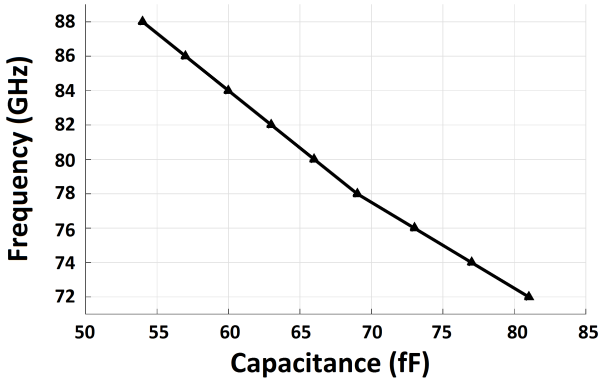
to perform the tuning functionality by setting $C_1 = C_2 = C$. At the resonance frequency, C_{eqv} (C_1' in series with C_2') is converted to an equivalent parallel capacitor (C_L) as follows:

$$C_L = C_{eqv} Q_{C_{eqv}} / (1 + Q^2_{C_{eqv}}) \tag{7}$$

where Q_{C_eqv} is the quality factor of C_{eqv}. Such that for high $Q_{C_{eqv}}$, $C_L \cong C_{eqv} = \frac{1}{2}C$.



(a)



(b)

FIGURE 2. (a) Frequency versus C_L for LC-tank and ML-DCO. (b) Piecewise linear regions.

The frequency of oscillation is similar to the LC-tank as given in Eq. (1), and shows a non-linear relation between f_o and C_L, assuming that L is kept constant. The plot in Fig. 2 (a) shows f_o vs. C_L where L is fixed at 60 pH. The non-linear relations can be considered as a piecewise linear function.

Fig. 2 (b) shows two linear segments in the range of $72 - 78$ GHz and $80 - 88$ GHz that can cover 16 GHz TR. The piecewise linear function for the two segments can be defined by:

$$f = \begin{cases} 124 - 0.7C_L & : 54 \le C_L \le 66 \\ 112 - 0.5C_L & : 69 \le C_L \le 81 \end{cases}$$

The units for f and C_L are GHz and fF respectively. The higher the frequency, the sharper is the slope which calls for smaller coarse step.

As an example, working in the linear segment $f = 112 - 0.5\ C_L$, a coarse step of 0.2 GHz requires 0.4 fF change in C_L which is translated to a change of 0.8 fF in C. The minimum MoM/MIM provided by the foundry is typically limited to a few fF. For instance, the minimum MoM size in the 65 nm TSMC process is 2.16 fF and this capacitive change in C corresponds to a 1.08 fF change in C_L, resulting in a 0.5 GHz coarse step for the same line segment.

Tuning capacitors are partitioned into an overlapped Coarse Bank (CB), an Intermediate Bank (IB), and a Fine Bank (FB) to maximize linearity in the step size of the tuning characteristics. A large coarse step relaxes the number of coarse tuning bits, but also leads to additional intermediate and fine-tuning bits.

The resolution (Δf_o) defines the fine step. Based on Eq. (2), for $\Delta f_o = 1$ MHz and with $f_o = 78$ GHz and $C_L = 69$ fF, $\Delta C_L = 1.8$ aF and hence ΔC as low as 3.6 aF should be realized. Thus the realization of the three tuning banks capacitors is the central constraint in the design of a W-band DCO.

B. TRANSMISSION GATE SWITCH DESIGN CONSIDERATIONS

The parasitic capacitors associated with the PMOS and NMOS devices (M_p and M_n) of the MOS TG switch are shown in Fig. 3(a).

During the OFF TG state, M_n and M_p are turned OFF. The TG off-resistance (R_{off}) is high and is equal to the parallel combination of the substrate resistance R_{sub} and the n-well resistance (R_{nw}). The parasitic capacitors at the terminals A, B are given by

$$C_{A_{off}} = C_{gs_p} + C_{gd_n} + C_{sb_p} + C_{db_n} \tag{8}$$
$$C_{B_{off}} = C_{gd_p} + C_{gs_n} + C_{sb_n} + C_{db_p} \tag{9}$$

Advanced CMOS technology offers placing the switch inside an isolated deep n-well to add a large resistance of few $K\Omega$ in series with the substrate resistance to improve isolation.

At the ON state, at least one of the MOS switches is turned ON. Since $M_n || M_p$, the TG on-resistance (R_{on}) can be expressed as

$$(R_{on_p} || R_{on_n}) \le R_{on} \le (R_{on_n} or R_{on_p}) \tag{10}$$

where R_{on_n} and R_{on_p} are the on-resistance for M_n and M_p respectively.

The Nanoscale CMOS technology provides improved symmetric switch topologies that make use of the improved p-MOSFETs. Equal NMOS and the PMOS sizes present the same parasitic capacitors and therefore, C_p can be defined to be the equivalent parasitic capacitor appearing at the terminal A and B.

$$C_p = C_{gs} + C_{gd} + C_{sb} + C_{db} \tag{11}$$

The TG ON/OFF model is shown in Fig. 3(b).

C. OSCILLATION AMPLITUDE: IMPACT AND STABILITY ANALYSIS

If the start-up condition is satisfied, such that $| R_{neg1} | > R_L$, then oscillation continues steadily until non-linearity forces

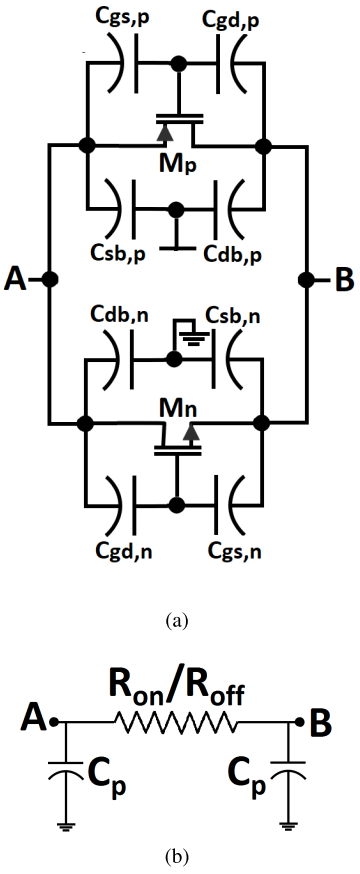


FIGURE 3. Transmission Gate equivalent circuits (a) Parasitic capacitors contribution in the TG. (b) Equivalent ON/OFF TG models.

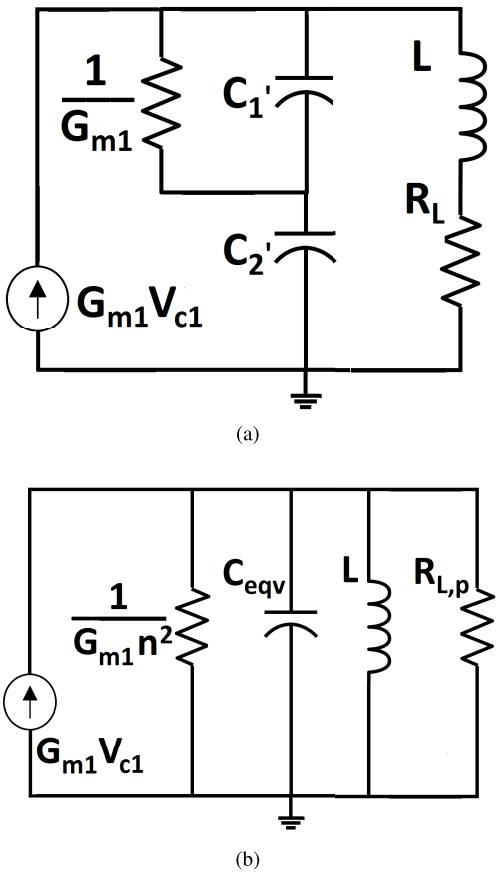


FIGURE 4. Steps to derive the ML-DCO large signal model. (a) Circuit to obtain the ML-DCO large signal model. (b) ML-DCO large signal model.

the signal to stop growing. The steady-state oscillation amplitude is an important characteristic and can have a significant impact on other neighboring system blocks.

The describing function model in [22] approximates the large signal transconductance (G_m) of the steady-state oscillation by:

$$G_{m1} \approx \frac{I_{1,peak}}{V_{C1}} \approx \frac{2I_{bias}}{V_{C1}} \approx \frac{2I_{bias}}{nV_{osc}} \tag{12}$$

where $I_{1,peak}$ is the peak of the pulse current in $M_{1,2}$, I_{bias} is the biasing current, V_{osc} is the amplitude of oscillation, V_{C1} is the amplitude of the gate-source voltage, and $n = C_2/(C_1 + C_2)$. The function model approximates $I_{1,peak} \approx 2I_{bias}$.

The Large signal representation, based on the NMOS T model and shown in Fig. 4 (a), is employed to calculate the oscillation amplitude. The tapped capacitors C_1' and C_2' with $1/G_{m1}$ are transformed to a capacitor C_{eqv} (C_1' in series with C_2') in parallel with a resistor $1/G_{m1}n^2$ [23].

At the resonanet frequency, the equivalent parallel resistance of the inductor L can be derived from the series losses equivalent resistor R_L by:

$$R_{L,P} = R_L(1 + Q_L^2) \cong R_L Q_L^2 \tag{13}$$

where $R_{L,P}$ is the losses equivalent parallel resistance of the L. With $Q_L \gg 1$, $Q_L = \frac{\omega_o L}{R_L}$, and $\omega_o = 2\pi f_o$, $R_{L,P}$ can be approximated by:

$$R_{L,P} \cong R_L Q_L^2 = Q_L \omega_o L \tag{14}$$

The inductor losses characterized by R_L eventually become a function of the oscillating frequency due to the induced losses from the substrate eddy current and the skin effect.

Fig. 4(b) shows the transformed model. The total parallel resistance is expressed as follows:

$$R_{total} = (1/G_{m1}n^2) \| R_{L,P} \tag{15}$$

At ω_o, the amplitude V_{osc} is given by:

$$V_{osc} = 2I_{bias}R_{total} = 2I_{bias}\frac{R_{L,p}}{1 + G_{m1}n^2 R_{L,P}} \tag{16}$$

Substitution of Eq. (12) in (16) and rearranging the terms result in:

$$V_{osc} = 2I_{bias}R_{L,P}(1 - n) = I_{bias}R_{L,P} \tag{17}$$

where $n = 1/2$ in the ML-DCO. Finally substitution of $R_{L,p}$ from Eq. (14) results in:

$$V_{osc} = I_{bias}Q_L\omega_o L \tag{18}$$

To investigate amplitude stability with the TR, ω_o is modified by $\Delta\omega_o$ with $\Delta\omega_o \ll \omega_o$. This change results in modification

of $V'_{osc} = I_{bias}Q_L\omega'_oL$, where V'_{osc} is associated with the incremental increase of $\omega'_o = \omega_o + \Delta\omega_o$ enforced by the incremental change in $C'_L = C_L + \Delta C_L$.

The normalized amplitude is:

$$\frac{V'_{osc}}{V_{osc}} = \frac{(\omega_o + \Delta\omega_o)^2}{\omega_o^2} = 1 + 2\frac{\Delta\omega_o}{\omega_o} + \frac{\Delta\omega_o^2}{\omega_o^2} \tag{19}$$

Similarly, the ratio of $\frac{(\omega_o+\Delta\omega_o)^2}{\omega_o^2} = \frac{C_L}{C_L+\Delta C_L}$ can be derived based on the relation $\omega_o^2 = \frac{1}{LC_L}$ and expressed by:

$$(1 + \frac{\Delta\omega_o}{\omega_o})^{-2} = 1 + \frac{\Delta C_L}{C_L} \tag{20}$$

Since $\Delta\omega_o/\omega_o$ is much smaller than one, the left side of Eq. (20) can be approximated by the first-order Taylor expansion that results in:

$$1 - 2\frac{\Delta\omega_o}{\omega_o} = 1 + \frac{\Delta C_L}{C_L} \tag{21}$$

Therefore

$$\frac{\Delta\omega_o}{\omega_o} = -\frac{\Delta CL}{2C_L} \tag{22}$$

The last term in Eq. (19) is $\ll 1$ and can be ignored. With the substitute of Eq. (22), the normalized amplitude of the ML-DCO can be approximated to:

$$\frac{V'_{osc}}{V_{osc}} = \frac{(\omega_{osc} + \Delta\omega_o)^2}{\omega_o^2} = 1 - \frac{\Delta C_L}{C_L} \approx 1 \tag{23}$$

for $\Delta C_L \ll C_L$.

Therefore, the amplitude of oscillation of the ML-DCO can be stable across the TR being independent on the tuning capacitors.

Stabilizing the amplitude is important for suppressing the amplitude-to-phase conversion [20]. Amplitude stability needs to be addressed in the design of the frequency synthesizer. The pre-scaler (or divider) is a neighboring system block whose performance is affected by the DCO amplitude stability. If the DCO is part of a synthesizer inside the receiver, then the conversion gain of the mixer would vary if the DCO amplitude changes widely.

VI. NEW FREQUENCY STEP GENERATING MECHANISM

Fig. 5(a) presents the proposed frequency step generating mechanism formed by two special capacitive structures (C_s) connected in series. Each C_s consists of two unit capacitors (C_u) and a *TG*, where C_u is the minimum available MoM capacitor supplied by the foundry. The *TG* connects the bottom plates of C_u, while the top plates are shorted together. In constructing the TG, deep-n-well low V_{th}, which is available in the process design kit, and minimum size devices are used for both of M_n and M_p to keep the minimum size parasitic capacitors.

In the interest of obtaining an intuitive analysis, R_{on} in the model of Fig. 3(b) is assumed too small to be replaced by a short circuit. For the same reason, it is assumed that R_{off} is large enough to disconnect the TG terminals

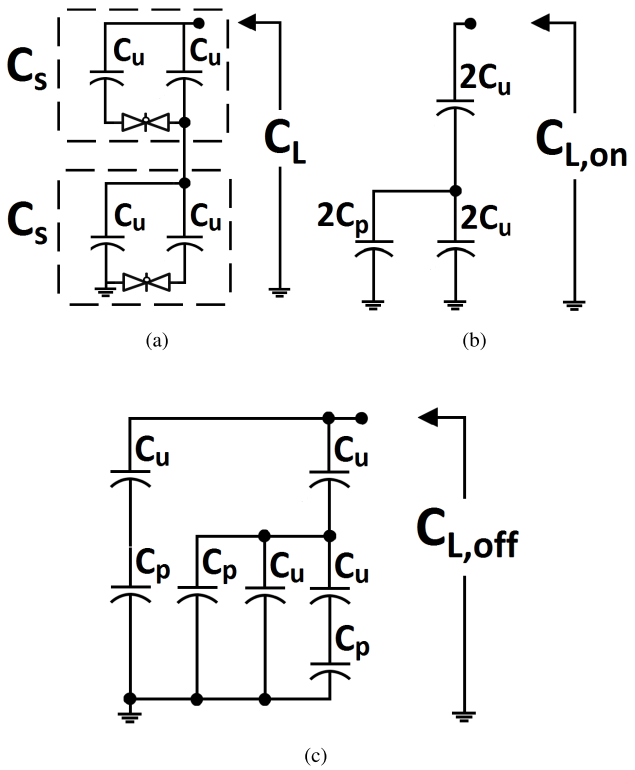


FIGURE 5. (a) Frequency step generating mechanism. (b) The frequency step generator at the ON state. (c) The frequency step generator at the OFF state.

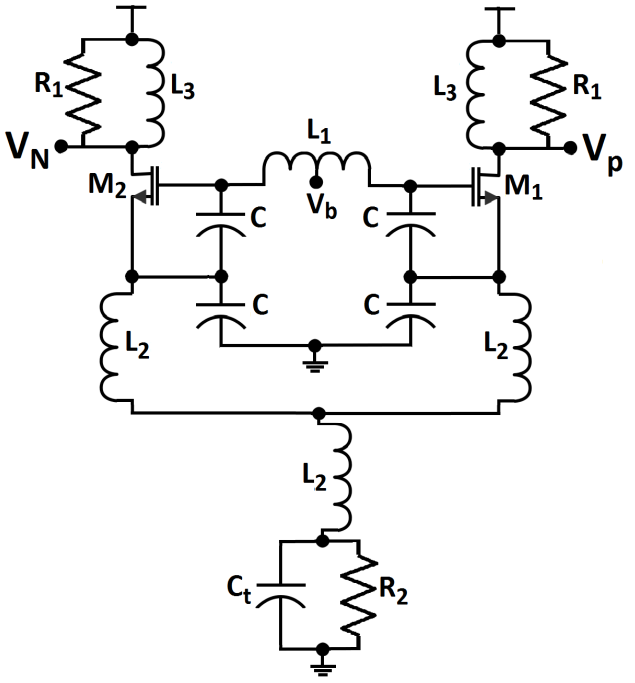


FIGURE 6. Schematic of the proposed 77 *GHz* ML-DCO.

A and B. The resulting frequency step generating units at the ON and OFF states are shown in Fig. 5(b) and(c) respectively.

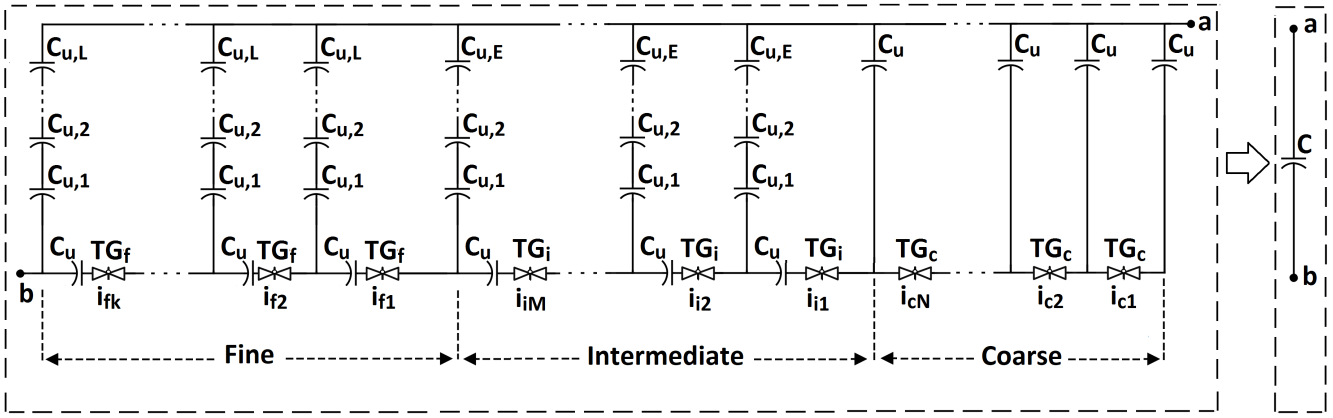


FIGURE 7. Tuning network banks.

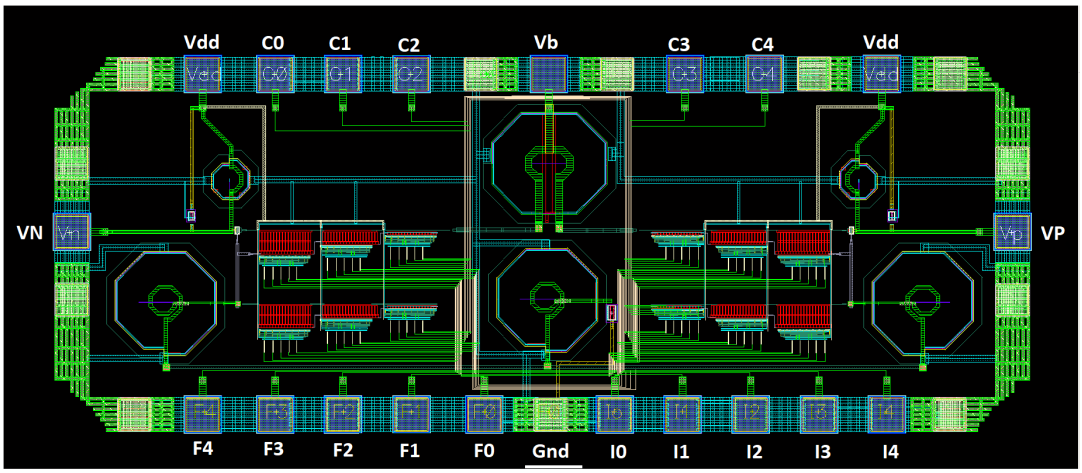


FIGURE 8. Chip layout of the proposed 77 *GHz* DCO.

In 65 *nm* CMOS technology, the value of the parasitic capacitors C_{gs}, C_{sb}, and C_{db} for $1\mu m/65nm$ NMOS and PMOS devices is 0.7 fT. C_{gd} is 0.4 fT and C_u is around 2 fF [8]. C_p per $1\mu m$ wide device in Eq. (11) comes to be 2.5 fF, which is translated to 0.5 fF by scaling the width down to 200 *nm*. The equivalent ON and OFF capacitor of the frequency step generator in Fig. 5 (b), (c) are 2.22 fF and 1.58 fF respectively. The resulting $\Delta C = 0.64\ fF$ is translated to $\Delta f = 0.4\ GHz$ in Eq. (2) for $f_o = 82\ GHz$ and $C_L = 63\ fF$. The frequency step is generated utilizing the minimum size MoM and low V_{th} devices that can be supplied by the foundry.

VII. CIRCUIT DESIGN OF THE PROPOSED 77 GHz DCO

The W-band ML-DCO is designed based on the proposed topology in Fig. 1. Fig. 6 shows the schematic of the W-band ML-DCO. The switching NMOS RF devices (M_1, M_2) of 60 *nm* length and 20 *um* width provide sufficient gain to sustain the oscillation. The transistors M_1 and M_2 are biased at the minimum noise figure current density (JOPT) of 0.15 $mA/\mu m$ to obtain low PN.

A single turn central tap tank inductor (L_1) with 120 pH is selected and implemented in Metal 9. It achieves Q_L of 49 at 82 GHz. The current source tail is replaced with a resistor (R_2), a capacitor (C_t), and an inductor (L_2) to filter out the noise introduced by the bias circuitry [8]. The output is taken from the drain such that an output buffer is not needed and the output power is increased with the drain inductor (L_3) without reducing the headroom for the transistor [24].

The ML-DCO offers three-stage tuning; the coarse, intermediate, and fine-tuning networks, which bridge the gap between the coarse and the fine frequency step size. Thermometer encoding is employed to ensure monotonicity, which controls the new tuning mechanism.

The three tuning networks providing the coarse, intermediate, and fine-tuning steps are configured as shown in Fig. 7. Intermediate and fine-tuning are accomplished by adding more C_u in series to reduce the total effective capacitance and hence the step. Placing C_u in series with the TG enhances

the intermediate and the fine steps to maintain the consistent effect. If all the leftmost TG in the network is OFF while the rest are ON, then the frequency is stepped up by flipping next TG to the OFF state.

The thermometer indices are $(i_{c1} - i_{cN})$, $(i_{i1} - i_{iM})$, and $(i_{f1} - i_{fK})$ for the coarse, intermediate, and fine network respectively. The unit MoM capacitor (C_u) is 2.16 fF. The number of the series C_u to realize the intermediate and fine steps are E and L respectively. In this design, $N = M = K = 31$ for 5 binary bits controlling each network, while $E = 3$ and $L = 7$.

All the *TGs* incorporate symmetrical low threshold NMOS and PMOS devices. If the gate capacitors are equal, opposite charge packets injected by the NMOS and PMOS transistors of the TG cancel each other that results in minimal charge injection effect [25].

The width/length of the PMOS and NMOS transistors of all the TGs are identical in each tuning bank. The sizes of the transistors for the coarse (TG_c), the intermediate (TG_i), and the fine (TG_f) TGs are (200 nm/120 nm), (200 nm/60 nm), and (200 nm/60 nm) respectively. The length of TG_c is twice that of TG_i and TG_f to increase the coarse step.

The layout of the proposed ML-DCO is accomplished in a 65 nm bulk CMOS process. The chip layout is shown in Fig. 8. The total chip area is 1 mm^2, which is pad limited. The ML-DCO core fits in a rectangular of 1.3 $mm \times 0.5$ mm. The power dissipation is 14 mW from a 1.2 V supply.

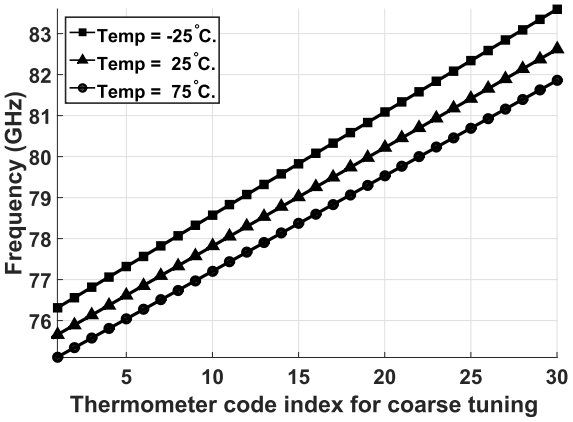


FIGURE 9. Coarse tuning for the ML-DCO.

VIII. SIMULATION AND FABRICATION MEASUREMENT RESULTS

Post-layout simulation is conducted to plot the coarse, intermediate, and fine tuning shown in Fig. 9, Fig.10, and Fig. 11 respectively. The coarse tuning is plotted in Fig. 9 in three different temperatures. At 25°C, the TR extends from 75.5 GHz to 82.5 GHz, and the ML-DCO realizes linear coarse tuning step at 220 MHz with less than 12% variation. The average linear coarse steps are 240 MHz and 211 MHz at $-25°C$ and 75°C respectively.

The linear intermediate tuning at each coarse thermometer code index $(C01 - C29)$ is plotted in Fig. 10 to provide 10 MHz intermediate step. More than 9% overlap between the adjacent intermediate tuning curves guarantees continuous tuning across the entire range.

Fig. 11 plots the fine-tuning step against the thermometer index while the ML-DCO is oscillating at three different frequencies, being 76 GHz, 77 GHz, and 81 GHz. The average fine steps are 385 KHz, 346 KHz, and 408 KHz when oscillating at 76 GHz, 77 GHz, and 81 GHz respectively. Thus, a TR as wide as 7 GHz and a frequency resolution of 346 KHz are achieved simultaneously using the new mechanism.

Monte Carlo statistical analysis is performed in TSMC 65 nm to check the effect of the inter-die and the intra-die variations on the frequency and the amplitude of oscillation. A proper Monte Carlo configuration is set up by varying the process and mismatch of the NMOS and PMOS transistors in order to evaluate the effect of the inter-die and the intra-die variations on the oscillating frequency and the amplitude of oscillation. Simulations are performed under the minimum, middle and maximum index coarse tuning code of the oscillating frequency, with 1100 runs per simulation. The simulation results corresponding to these cases are presented in Fig. 12(a), (b), and (c) respectively. The mean (mu) oscillating frequencies for the minimum, middle and maximum indices are 75.508, 79.005, 82.506 GHz and the standard deviations (sd) are 14, 13, 13.2 MHz respectively. The process and mismatch statistical coefficient variation for all cases is less than 0.02%. The robustness is due to the uniqueness of the topology, which depends on varying C_1 and C_2 (Fig. 1) simultaneously throughout the tuning process that makes the frequency depends on ratio of capacitors and consequently less sensitive to process variations.

Monte Carlo simulation is also performed to check the process and mismatch fluctuation effect on the amplitude while the design is oscillating at 77 GHz. The results of the 1100 runs are depicted in Fig. 12(d). The values of mu and sd are 941 mV and 22 mV respectively. The amplitude varies by just 2.34% with process and mismatch for 1100 runs. All Monte Carlo simulations and subsequent analyses show Gaussian distributions, highlighting the robustness of the design. The results show that the proposed design is very promising.

Process corner analysis is performed to simulate the frequency, the current consumption, and the V_{osc}. The analysis is repeated for seven different coarse indexes ($C01$, $C05$, $C11$, $C16$, $C21$, $C26$, $C30$). The corners are the typical process at 25°C (Typ.), fast-best corner at $-25°C$ (F.B.), and slow-worst corner at 75°C (S.W.). The results are shown in Fig. 13. The frequency tuning across the entire range at the three process corners is presented in Fig. 13(a) and tabulated in Table 1. The TR is the same for all frequency corners and linearity is maintained. The highest current consumption of 16 mA appears in the F.B at $C26$ coarse index shown in Fig. 13(b). The maximum amplitude variation with process corners across the TR in Fig. 13(c) occurs at the S.W corner, and V_{osc} varies by 25% between 0.6 V and 0.75 V. At the Typ. corner, V_{osc} varies by 9% across the TR between 0.84 V

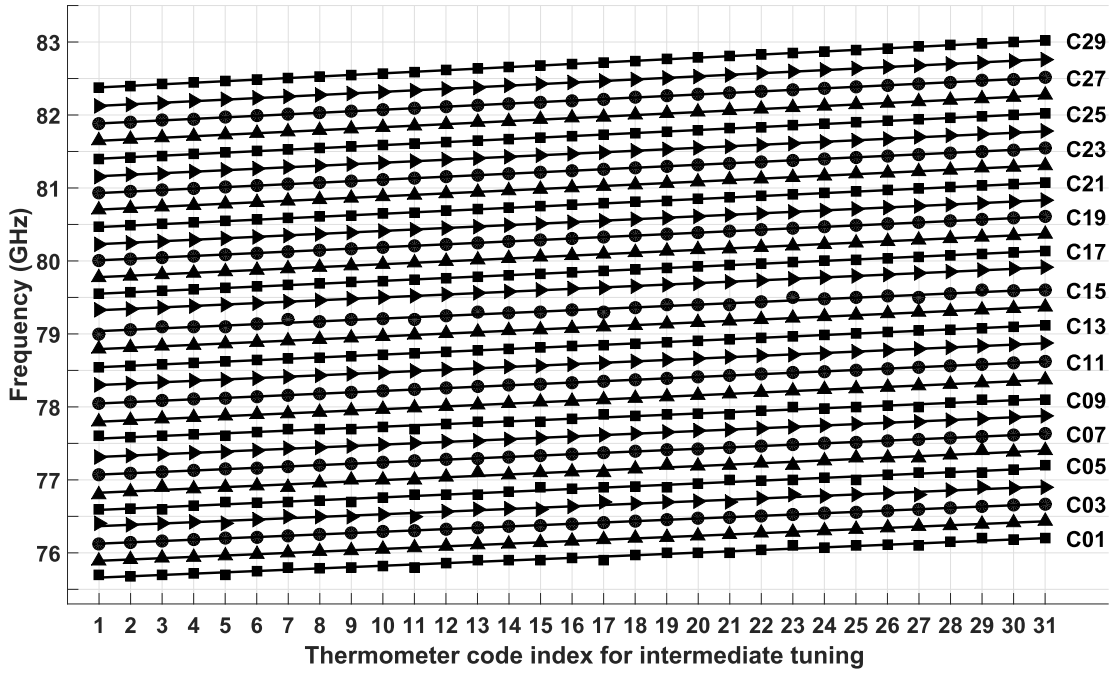


FIGURE 10. ML-DCO intermediate tuning curves for each coarse thermometer index tuning.

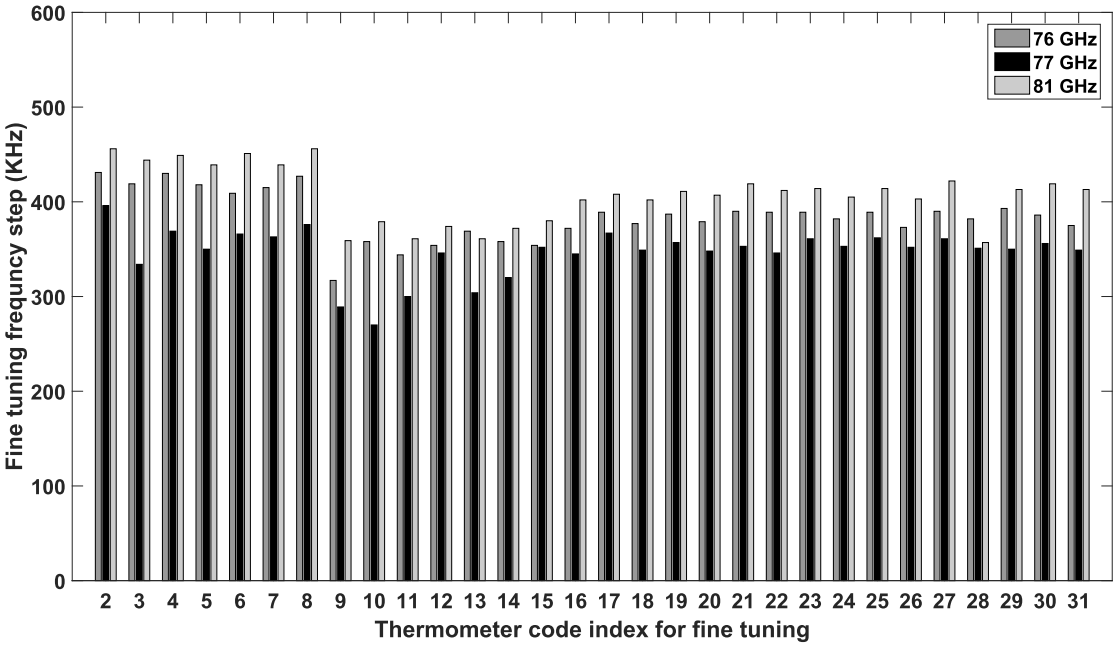


FIGURE 11. ML-DCO fine-tuning frequency steps in three different oscillating frequencies.

and 0.94 V. The results of the process corner effect on PN are shown in Table 2. The analysis is conducted at 75.5 GHz, 79 GHz, and 82.5 GHz. The results show that the PN at 1 MHz offset frequency is better than -95 dBc/Hz among all cases.

Post-layout simulation for the PN at $-25°C$, $25°C$, and $75°C$ are presented in Fig. 14 corresponding to an oscillation frequency of 77 GHz. The PN at 1 MHz offset at $-25°C$, $25°C$, and $75°C$ is -98.73 dBc/Hz, -98.53 dBc/Hz, and -97.12 dBc/Hz respectively.

The first prototype resembles a half circuit of the differential ML-DCO in Fig. 6. It is implemented in TSMC 65 nm 1P9M CMOS process. The die photo is shown in Fig. 15. The prototype draws 6 mA current from 1.2 V supply. The core occupies an area of $700 \times 500 \mu m^2$.

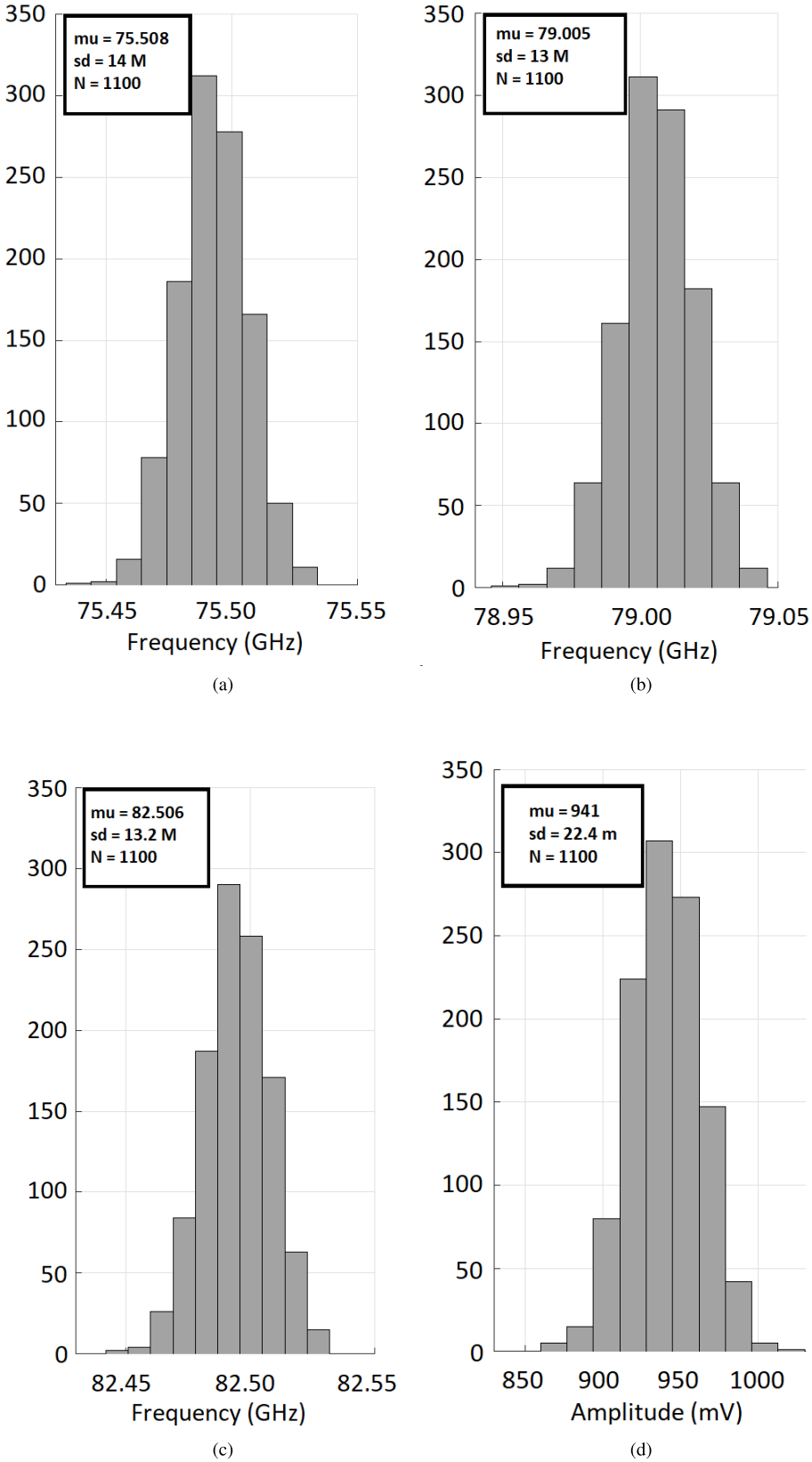
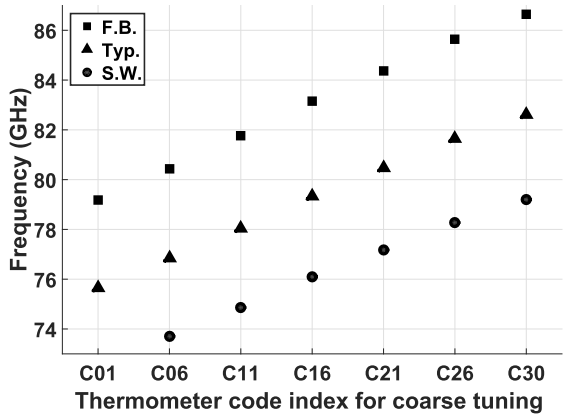
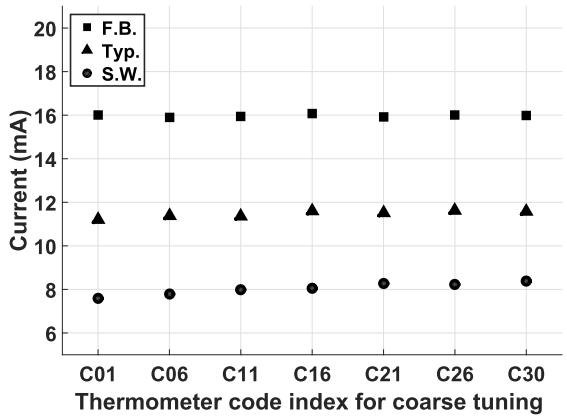


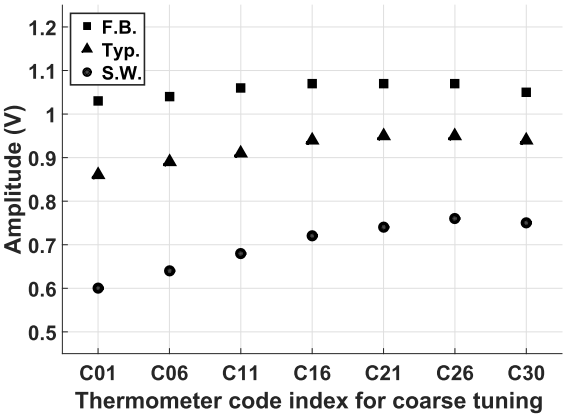
FIGURE 12. Monte Carlo simulation results. (a) minimum tuning frequency variation. (b) middle tuning frequency variation. (c) maximum tuning frequency variation. (d) Amplitude variation.



(a)



(b)



(c)

FIGURE 13. Corners simulation results at (Typ. 25°C), (F.B. −25°C), and (S.W. 75°C), repeated in (a)-(c) for seven coarse tuning codes (C01, C05, C11, C16, C21, C26, C30). (a) The frequency. (b) The current consumption. (c) The amplitude of oscillation.

Fabrication measurement is conducted to test the performance of the first prototype. Oscillating at 77 *GHz*, Fig. 16 shows the measured PN spectrum. The PN at 1 *MHz* offset is −96.32 *dBc*/*Hz*. Fig. 17 shows 4-bit coarse tuning and the measured PN ranging from −94 *dBc*/*Hz* to −96.55 *dBc*/*Hz*

TABLE 1. Frequency over process corners and temperature variations.

Corner Temp.	C01 (GHz)	C06 (GHz)	C11 (GHz)	C16 (GHz)	C21 (GHz)	C26 (GHz)	C30 (GHz)
S.W. $75°C$	72.59	73.71	74.87	76.09	77.17	78.28	79.2
Typ. $25°C$	75.66	76.84	78.05	79.33	80.47	81.65	82.61
F.B. $-25°C$	79.19	80.44	81.76	83.16	84.37	85.64	86.65

TABLE 2. Phase noise over process corners.

Corner Temp.	PN (dBc/Hz) of 76 GHz @ 1MHz offset	PN (dBc/Hz) of 77 GHz @ 1MHz offset	PN (dBc/Hz) of 82 GHz @ 1MHz offset
S.W. $75°C$	-97	-96	-95
Typ. $25°C$	-98.5	-98	-96.5
F.B. $-25°C$	-100	-99	-97

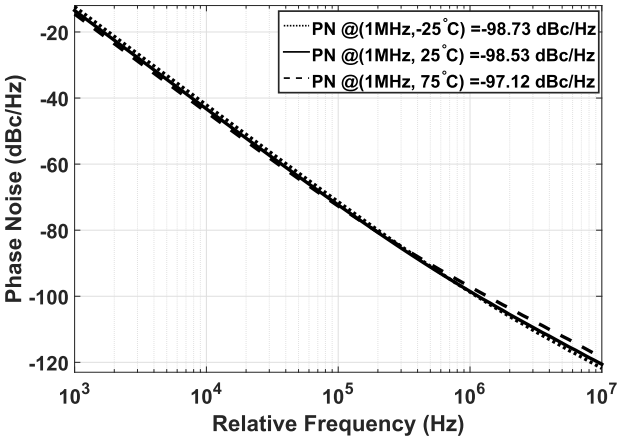


FIGURE 14. Phase-noise of the ML-DCO.

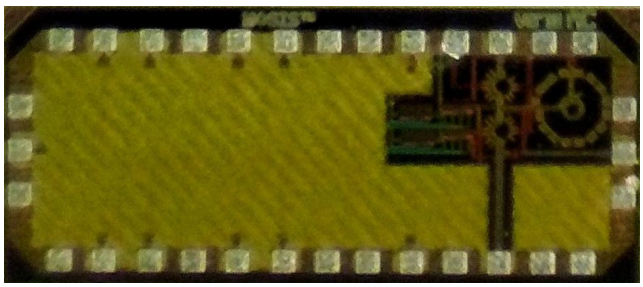


FIGURE 15. Chip photograph for the prototype.

at a 1*MHz* offset throughout a linear tuning range from 76 *GHz* to 81 *GHz*.

To quantify and compare the overall performance with other designs from the current literature, the Figure of Merit (*FoM*) and Figure of Merit for Tuning range (FoM_T) are defined similarly to [12] as follows:

$$FoM = PN - 20log\frac{f_{center}}{\Delta f} + 10log\frac{PDC}{1\ mW} \quad (24)$$

$$FoM_T = PN - 20log\frac{f_{center}}{\Delta f}.\frac{TR\%}{10\%} + 10log\frac{PDC}{1\ mW} \quad (25)$$

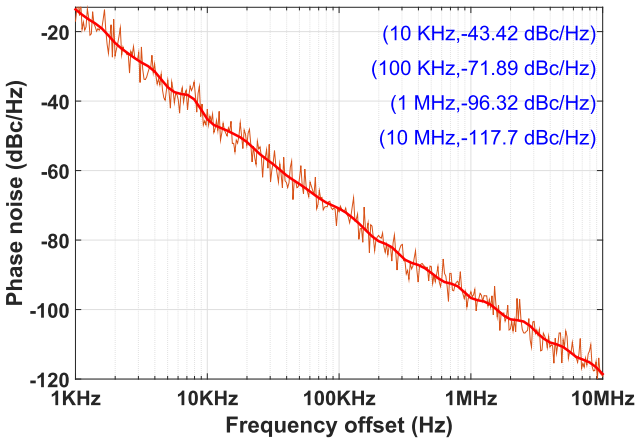


FIGURE 16. Measured phase-noise spectrum at 77 *GHz* for the ML-DCO prototype.

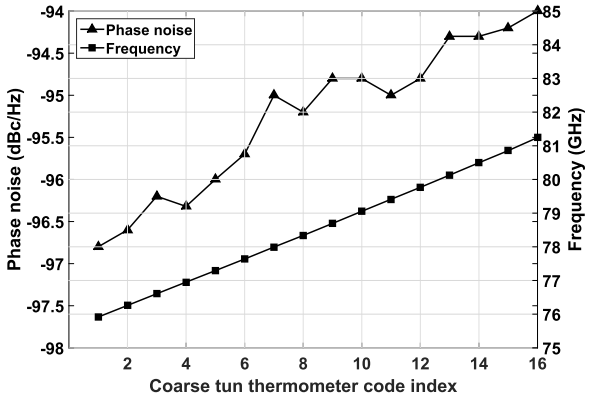


FIGURE 17. Measured results for oscillation frequencies and phase-noises at 1 *MHz* offset with respect to the frequency of the ML-DCO prototype across the tuning range.

TABLE 3. Performance summary and comparison.

[Ref]Type	F_o (GHz)	TR (%)	PN ($\frac{dBc}{Hz}$)	PDC (mW)	FoM ($\frac{dBc}{Hz}$)	FoMT ($\frac{dBc}{Hz}$)	CMOS (nm)
[12]DCO	60	14	-90.7	18	-169	-176.6	130
[27]VCO	26	25	-104	9.96	-182	-190	130
[6]DCO	60	10	-93	12	-178	-178	90
[26]DCO	25	16	-117	23	-171	-175	40
[1]VCO	38.5	11	-87	11.7	-168	-169	65
Prototype	77	6.5	-96.3	7.2	-185	-181	65
ML-DCO	77	9	-98.5	14	-185	-184	65

where *PDC* is the power dissipation, *PN* is the phase-noise and Δf is the offset from the center frequency (f_{center}) of 77 *GHz* and 1.2 *V* supply is used.

Table 3 shows the comparison results with state-of-the-art mm-wave VCOs and DCOs. Except for 10 *MHz* in [26], the Δf for all the references is 1 *MHz*. The prototype has -185 *FoM* and -181 FoM_T. The proposed ML-DCO has the highest *FoM* and FoM_T of -185 and -184 respectively.

Operating in W-band frequency, the new tuning technique alleviates the varactors while effectively stretches the TR in uniform linear steps across a 7 *GHz* TR.

IX. CONCLUSIONS

This paper presents simultaneous wide tuning-range and small tuning steps for the 77 *GHz* DCO. MoM capacitors are employed for the coarse, intermediate as well as the fine-tuning banks. Therefore, low quality-factor MOS varactors are avoided. High linearity overlapped tuning banks are obtained to be perfect for FMCW ADPLL applications. New coarse, intermediate, and fine-tuning techniques and configurations have been demonstrated in 77 *GHz* ML-DCO in 65 *nm* CMOS. Oscillating at 77 *GHz*, the ML-DCO achieves a total TR of 7 *GHz* while the average fine frequency resolution is 346 *KHz*, corresponding to a capacitance change of $\Delta C_L = 1.6\ aF$. The phase-noise is better than -98.53 at 1 *MHz* offset. The tuning bits of the three banks can be readjusted to obtain a better fine resolution while still maintaining the overlap of the three tuning banks and the TR. Moreover, since the three tuning banks are linear, a simple binary-to-thermometer decoder is sufficient for tuning word generation in an ADPLL. The distributed switchable MoM capacitors make a wide-band and high-resolution DCO feasible at W-band operation.

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