IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received January 4, 2019, accepted February 17, 2019, date of current version June 4, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2902505

Soft Error Reliability Improvement of Digital Circuits by Exploiting a Fast Gate Sizing Scheme

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ABSTRACT Due to the reduction in device feature size and supply voltage, achieving soft error reliability in sub-micrometer digital circuits is becoming extremely challenging. We consider the problem of choosing the gate sizes in a combinational logic circuit in order to minimize the soft error rate (SER) of the circuit. This problem can be solved using the heuristic as well as the greedy-based approaches for small-size problems; however, when the circuit size increases, the computational time grows exponentially, and hence, the previous methods become impractical. This paper proposes a novel technique for soft error tolerant design of large-scale combinational circuits using a cone-oriented gate sizing. Circuit partitioning is used to split the circuit into a set of small sub-circuits. The gates of sub-circuits are resized, such that the entire circuit SER is reduced based on a new soft error descriptor metric. The proposed cone-oriented gate sizing framework is used for selective gate sizing, leading up to 31% SER reduction with less than 17% area overhead when applied to large-scale benchmarks. The results also show that the proposed method is 21% more efficient and up to 292 times faster when compared with that obtained using a similar work based on the sensitive-based gate sizing scheme.

INDEX TERMS Reliability, large-scale circuits, soft error, soft error rate, partitioning, gate sizing, combinational logic.

I. INTRODUCTION

Circuit reliability is becoming a critical issue in the deep sub-micrometer CMOS technology nodes [2]. Crosstalk, voltage drop and radiation-induced transient faults are currently some of the main factors in reliability degradation of digital circuits. Due to the current technology scaling trends (encompassing shrinking feature sizes, lower supply voltages, smaller node capacitances, etc.), digital designs are becoming more susceptible to transient faults which originate from radiation-induced particle hits, resulting from radioactive decay or cosmic rays [3]–[5]. A low-energy particle, which had no effect on a circuit before, can now flip the state of a storage node. Such a bit-flip of a storage node is called a Single Event Upset (SEU). If an energetic particle hits a gate in combinational logic, it can cause a glitch in the gate output. This unwanted voltage pulse is called Single Event Transient (SET). An SEU or a soft error occurs if the SET is propagated through the combinational circuit, arrived at a Primary Output (PO) and latched into a memory element. The occurrence rate of soft errors is evaluated using a metric called Soft Error Rate (SER) [6].

Contrary to soft errors in memories, occurring by particles strike (with high enough energy), SETs in combinational logic have to be propagated to the outputs before being captured. While SETs are propagated through the combinational circuit, the following three mechanisms are used to provide logic circuits with effective protection against soft errors [6], [7]:

1) Logical masking occurs when the input value of a given gate blocks the propagation of the transient fault under a specific input pattern.

2) One transient fault attenuated by electrical masking may disappear due to the electrical property of gates.

The associate editor coordinating the review of this manuscript and approving it for publication was Yi Ren.

3) Timing masking represents the situation that the transient faults arrive the memory element outside its latching window.

These three mechanisms prevent some SETs from being latched and alleviate the effects of soft errors in digital circuits. However, recent studies have shown that the contribution of combinational logic soft errors per latch increases with scaling and may exceed the latch cross section at the 40-nm node [7], [8]; therefore, for high-speed circuits that operate under single-Event Effect (SEE) reliability constraints, there is a need to develop soft error mitigation strategies for combinational logic circuits.

Typically, there are two approaches proposed for soft error hardening of logical circuits. The first approach is based on minimizing the SET occurrence/generation probability at the most sensitive nodes [9], [10] and in the second one, the impacts of three masking mechanisms are increased in order to decrease the probability of changing SETs into soft errors [11]–[13].

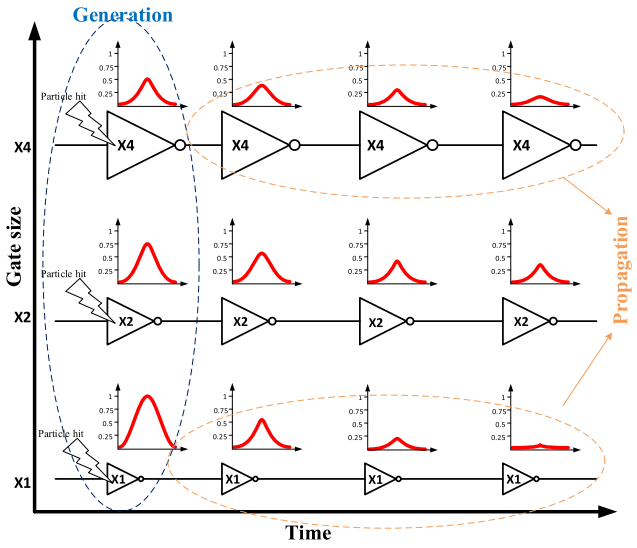

FIGURE 1. The impact of gate sizing on SET generation and propagation.

The simplest yet effective method of soft error hardening techniques is gate sizing. Gate sizing is a technique for optimizing circuits parameters such as performance, power and also reliability challenges like soft errors [1], [5], [14]. In this technique, the sizing of a gate (i.e. W/L in gate transistors) is perturbed to increase its resilience against the particle strikes. In the gate sizing technique, the gates are upsized in order to increase the output capacitances of which charging/discharging results in an SET at the hit gate [5], [15] or downsized to increase the electrical attenuation occurred on the SET while it is propagating through the gates in the circuit [1]. Figure 1 shows the effects of gate sizing on transient fault generation and propagation. The effective capacitance of the device is increased by upsizing a gate, making it less likely that the injected transient current results in a voltage glitch. Otherwise, an upsized gate has significantly higher drive strength which allows for better propagation of the input transients at a gate. Contrary to upsizing, both the gate delay and the initial transient current are increased as the gate is sized down. Since the gates with larger delays show more attenuation on propagating glitches [1], downsizing a gate leads to more glitch attenuations.

Over the past decade, many heuristic approaches based on gate sizing have been introduced subjected to soft error resilient circuit design [15]–[17]. It is notable that, all the previous gate sizing approaches re-compute the entire circuit SER for each resizing action. Re-computing SER is such time consuming that these methods could not be applied to large-scale circuits. In addition, the sizes of the circuits are so large that resizing all the gates is not practical by common gate sizing-based optimization approaches. These algorithms choose a small set of gates as the candidate set which consists of the gates which can potentially be resized for maximum SER improvement. In other words, they ignore a large part of circuit during SER improvement to make the runtime acceptable. So, the runtime of these traditional radiation hardening-oriented gate sizing is unacceptable for Very Large-Scale Integration (VLSI) design, where time-to market pressures and shortening product cycles are the primary objectives of today's digital system design. This shift raises an increasing need of scalable gate sizing techniques. However, we introduce a partitioning-based gate sizing approach in [18] that considerably speeds up the gate sizing optimization procedure. In this method, the circuit is divided into the topologically levelized small sub-circuits. The sub-circuits which are located in the same level are resized individually and independently, but the sub-circuits in different levels are not independent. In other words, a sub-circuit cannot be resized unless all sub-circuits in the previous levels are resized. Furthermore, this method is expensive in terms of computational complexity as the Probabilistic Vulnerability Window (PVW) metric which is utilized to evaluate the sub-circuits reliability is a relatively complex concept.

This paper presents a novel soft error hardening methodology for very large-scale combinational circuits. In this methodology, the circuit is partitioned into a set of small sub-circuits based on the cone structures which are originated from the POs. We introduce the Soft Error Descriptor (SED) concept which is a descriptor related to all SETs that originated from each sub-circuit. The gate resizing technique is applied to reduce the SED of individual sub-circuits, independently. We show that reducing each sub-circuit SED will decrease the entire SER of the circuit. During sub-circuit optimization, the gates are ranked based on a priority parameter in order to provide a selective hardening given a constraint on area overhead. Note that, in the proposed design flow, after resizing a gate, instead of re-computing the entire circuit SER, it just needs to re-compute the sub-circuit SER in which the resized gate is located. Since the sub-circuits are much smaller than the original circuit, the SER re-computation time

is reduced and consequently, the optimization runtime will be significantly decreased, making this methodology suitable for SER reduction of very large-scale circuits. In addition, due to partitioning the circuit into smaller sub-circuits and resizing sub-circuits independently, the proposed method enables us to resize all the gates in the circuit, resulting in more SER improvement. The experimental results on ISCAS'85 benchmarks show that, partitioning the circuit into small sub-circuits and resizing all sub-circuits reduces 31% of original SER with 17% area overhead, on average. Moreover, the results show that the proposed technique is 165X faster and 21% more efficient in comparison with a sensitivity-based gate sizing SER optimization approach [1].

The rest of the paper is organized as follows. Section II summarizes the previous techniques related to soft error tolerant circuit design. Section III describes the proposed cone-oriented gate sizing technique. Section IV presents the optimization parameters and the simulation results are provided in section V. Finally, the paper concludes in section VI.

II. PREVIOUS WORK

To overcome the effect of soft errors in combinational circuits, various fault tolerance techniques have been introduced in the literature [19]–[21]. In synthesis-based techniques, a combinational circuit is either restructured or resynthesize to maximize the logical masking properties of a circuit. In [22], the logical masking of errors is increased by taking advantage of conditions already present in the circuit, such as observability don't-care terms. In [23], two algorithms are proposed to improve input error resilience. They focus on input errors due to the propagated failures from the previous blocks. Both algorithms determine 0/1 assignments for the most critical don't-care terms. El-Maleh and Daud [24] proposes a simulation-based approach to maximize the probability of logical masking. Rewiring method, which has been extensively used for transforming a logic circuit in order to meet different design constraints, is also applied for increasing the circuit robustness to soft errors [13], [25]. The rewiring-based algorithm does not provide a systematic guideline but follows a greedy heuristic considering only logical masking to trade SER with various design penalties. Decreasing logic depth in super-pipeline stages reduces the probability of logical masking since the path from where a SET originates to a latch is more easily sensitized. Moreover, by reducing the logic depth, the number of gates in the circuit paths is generally decreased and therefor, the effect of electrical masking by circuit gates may be decreased. Hence, synthesis-based soft error hardening techniques will not be effective anymore.

The physical characteristics-based techniques attempt to reduce SER based on the physical characteristics of the gates and flip-flops to maximize the electrical and latching-window masking mechanisms. In [26], a soft error hardening strategy based on optimal assignments of gate sizes, threshold voltages, supply voltages and output capacitive loads is proposed to decrease the circuit SER while keeping overheads smaller. Another scheme [27] focuses on selecting flip-flops from a given set for increasing the probability of latching-window masking by lengthening the latching-window intervals. A hybrid approach combines flip-flop selection with gate resizing scheme to achieve more SER improvement [1]. In a recent technique presented in [28], the highly vulnerable gate cells are replaced with alternative cells to reduce the overall vulnerability of a circuit. The pulse width and drain area are used in this study as the reliability metrics to rank cells. In [29], standard cells are used to selectively harden vulnerable nodes in combinational logic based on replacing two-input gates with four-input gates. A new gate sizing technique to reduce SER of combinational circuits in the presence of process variation is introduced in [30]. This technique uses statistical information to make effective decisions during optimization subjected to different delay constraints and soft error. In [37], a sensitivity-based gate sizing methodology is presented to reduce the soft error rate (SER) of combinational circuits in the presence of process variations. A backward traversing algorithm with capability for SER analysis is developed for computing the distribution of circuit gates of SER random variables. In [38], the impacts of supply voltage, combinational-logic delay, flip-flop SEU performance, and particle linear energy transfer values are analyzed for SE cross sections of sequential circuits. A transmission-gate approach to filter out soft errors is proposed in [39] based on adjusting the gate and body bias voltages. A vulnerability analysis approach introduced in [31] is applied in order to consider the impacts of process variation in finding the most vulnerable circuit gates to soft error. The mentioned related works are suffering from a serious shortcoming. Due to time consuming of optimization process in these methods, their runtime is unacceptable for large-scale circuits.

III. THE PROPOSED CONE-ORIENTED GATE SIZING TECHNIQUE

In this section, the proposed soft error rate reduction framework is introduced. The proposed flow firstly partitions the circuit into a set of small sub-circuits and then, the soft error rate of each small sub-circuit is reduced during a gate re-sizing process. Finally, the size of the gates in the main circuit are replaced. The proposed framework contains three main steps: 1) netlist partitioning and 2) sub-circuit optimization 3) main circuit modification (Figure 2):

- In the first step, the original circuit is split into a set of small sub-circuits using cone structures which are originated from POs of the circuit. The parts of the circuit which are located only in one cone are considered as the circuit clusters. In addition, the parts of the circuit which have been shared between several cones are also considered as clusters (Figure2.a).
- The second step of the optimization flow tries to minimize the SER of the circuit using a gate

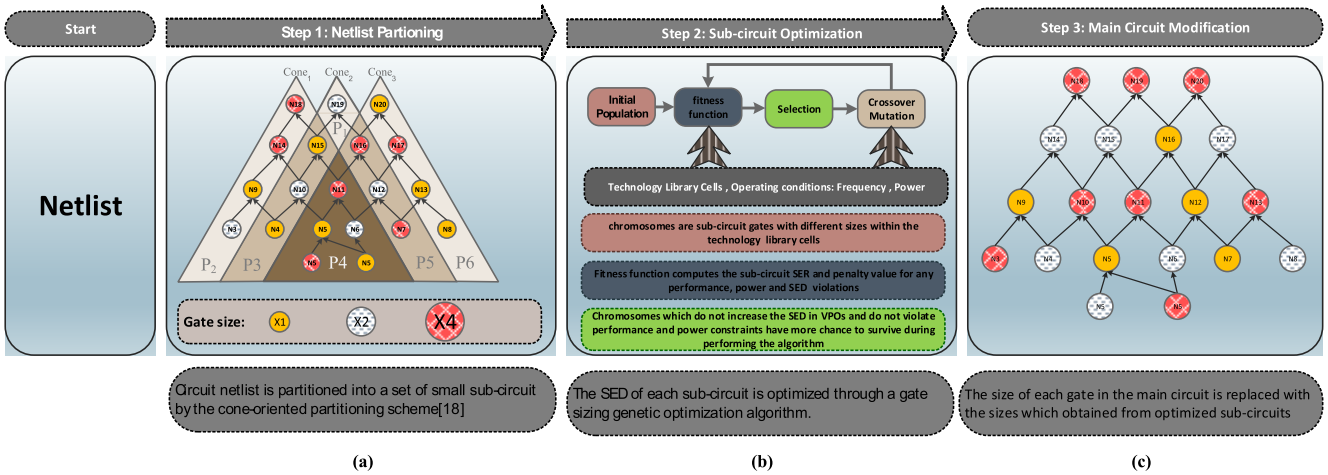

FIGURE 2. The proposed SER reduction framework.

re-sizing approach. The Soft Error Descriptor (SED) of a sub-circuit is introduced as an optimization metric for the sub-circuits gates resizing process. Reducing the SED of a sub-circuit causes the input error rate of the subsequent sub-circuits to be reduced, in addition to the output error rate of the sub-circuit. Hence, by reducing the input and output error rate of all sub-circuits, the entire SER of the circuit will be decreased. A genetic optimization strategy is used to provide maximum SER improvement under area and performance overhead constraint. For this purpose, an objective function is presented based on the SER improvement, area and performance overhead. (Figure 2.b)

- Finally, after optimization of all sub-circuits, each gate in the main circuit whose size has been changed during the sub-circuits SER optimization, will be replaced with the same new size gate. (Figure 2.c)

A. CONE-ORIENTED CLUSTERING

Cone structure is introduced as a set of gates which are located between a specific PO and Primary Inputs (PIs). A circuit netlist is partitioned into a set of small and independent sub-circuits by the cone-oriented partitioning approach introduced in [18]. In this approach the circuit is traversed backwardly from POs to PIs. During each backward traversing a tag is assign to each circuit gate corresponding to its topological level and connectivity. Finally, a sub-circuit is defined as the set of gates in the circuit with the same tag list. An example of a circuit netlist which is partitioned into six small sub-circuits (P1 – P6) shown in Figure 2.a. It's notable that the extracted sub-circuits are considered as the separate and independent small circuits. More details can be found in [18].

B. SER MITIGATION USING SUB-CIRCUITS GATE RE-SIZING

In this section, we present a circuit SER reduction technique based on the resizing the extracted sub-circuits, independently. At first, the circuit SER and sub-circuit SED parameters are defined. Next, we show how resizing the sub-circuit gates and reducing the SED of sub-circuits decreases the entire circuit SER. Finally, the resizing process of sub-circuits is described.

1) CIRCUIT SER

The soft error rate of circuit C (SER_C) can be calculated by summing up the soft error rate of individual gates (SER_j) in the circuit:

$$SER_C = \sum_{j \in N_{node}} SER_j \tag{1}$$

where $N_{node}$is the number of gates in the circuit which may be hit by the high energetic particle.

SER_j is formulated as the product of the SET generation probability ($P_{gen}(j)$) and the SET propagation probability ($P_{prop}(j)$):

$$SER_j = P_{gen}(j) * P_{prop}(j) \tag{2}$$

where $P_{gen}(j)$ is the logical probability of generating a transient fault in gate j and P_{prop} (j)shows the probability that the generated transient fault in gate j results in a soft error in any flip-flops at the circuit outputs.

$P_{prop}(j)$ is dependent on the triple masking mechanisms (i.e. logical, electrical, and timing masking) and is calculated as follows:

$$P_{prop}\ (j) = \sum_{k \in N_{ff}} P_{ele}(j,k) * P_{logic}(j,k) \tag{3}$$

where N_{ff} is the number of flip-flops in the circuit output, $P_{logic}(j,k)$ shows the sum of logical probability of transient faults propagation through the path between gate j and output k, and$P_{ele}(j,k)$ is the electrical probability representing the electrical masking of the gates located in the propagation path of transient fault and the timing masking of the memory elements.

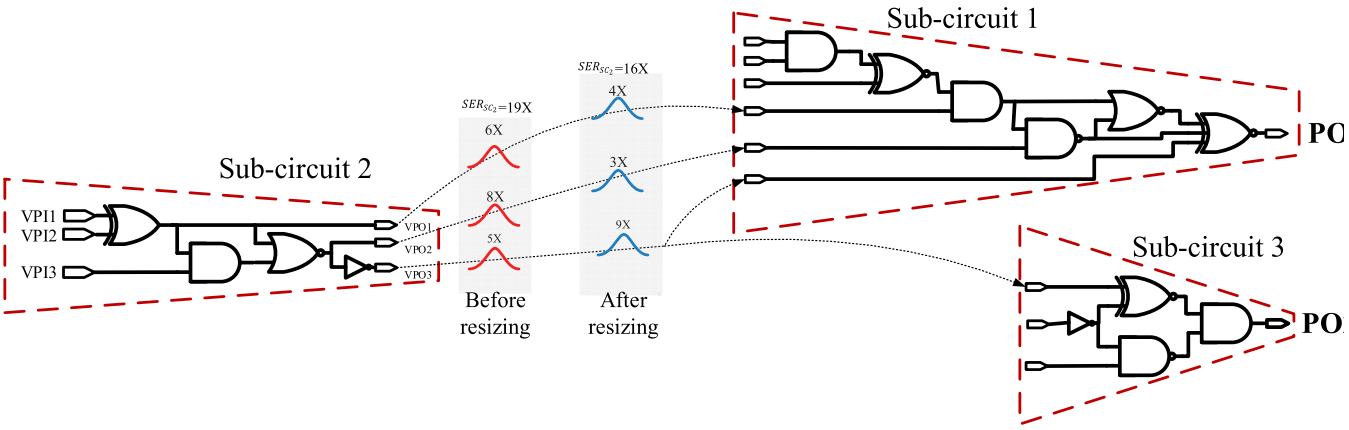

FIGURE 3. Effects of resizing sub-circuit gates on the SER and SEDs values of the sub-circuit.

2) SUB-CIRCUIT SED

As it is shown in sub-circuit2 in figure3, the outputs of a sub circuit are named Virtual Primary Outputs (VPOs) and the inputs is named Virtual Primary Inputs(VPIs). Then, the Soft Error Descriptor of sub-circuit SC_i (SED^{SC_i}) is defined as an n-tuple as follows:

$$SED^{SC_i} = \left(SED_1^{SC_i}, SED_2^{SC_i}, SED_3^{SC_i}, \ldots, SED_n^{SC_i}\right) \quad (4)$$

where kth element is a descriptor due to all SETs that originated from SC_i gates and are visible in the kth VPOs SC_i. Hence, we have:

$$SED_p^{SC_i} = \sum_{\forall N_{node}(SC_i)} P_{gen}(j) * P_{prop}(j,p) \quad (5)$$

where $N_{node}(SC_i)$ is the number of gates in sub-circuit SC_i and $P_{prop}(j,p)$ represents the probability that the generated transient fault in gate j results in a soft error in a flip-flop which is assumed connected to the outputs of P.

In order to model the transient faults which are originated from the other sub-circuits and arrive to the sub-circuit inputs, in equation 6, we consider the inputs of sub-circuits as the same as the other circuit nodes which transient faults are generated in their output. For $N_{node}(SC_i)$ in equation 6 we have:

$$N_{node}(SC_i) = SC_i gates \cup VPIs_{SC_i} \quad (6)$$

where VPI_{SC_i} represents VPIs of SC_i.

According to equations 5 and 6, the SER of a sub-circuit SC_i, (SER_{SC_i}) can be calculated as the sum of $SED_p^{SC_i}$ in the VPOs of that sub-circuit. (Here, it has been assumed that VPOs of sub-circuits are connected directly to the flip-flops):

$$SER_{SC_i} = \sum_{P \in VPO_{SC_i}} SED_p^{SC_i} \quad (7)$$

Considering equation 2 and 7, it is required to compute $P_{gen}(j)$ and $P_{prop}(j,p)$ to find $SED_p^{SC_i}$. Without loss of generality, the analytical approach proposed in [32] is used in order to calculate $P_{gen}(j)$ and $P_{prop}(j,p)$ (other techniques can be adapted to the proposed flow). In this method the value of $P_{prop}(j,p)$ is calculated considering the impacts of electrical, logical and timing masking. The proposed model in [33] is used to model the electrical attenuation of the transient glitches.

3) SUB-CIRCUIT GATE-SIZING

Since SER_{SC_i} of a sub-circuit (SC_i) is affected by both the transient faults which arrive to VPIs of SC_i and the transient faults caused by direct particle hitting to the gates included SC_i, the aim of gate resizing should be reducing both the propagation probability of transient faults through the sub-circuit and the probability of generating transient faults at the gates in SC_i.

It is notable that re-sizing the sub-circuit gates for SER_{SC_i} reduction, will not necessarily reduce the entire circuit SER. Any subsequent sizing operation on gate g of SC_i changes the $SED_p^{SC_i}$ value for each $p \in VPI_{SC_i}$ which has a path from gate g. Even though according to equation 10, reducing SER_{SC_i} results in reducing the sum of $SED_p^{SC_i}$, it may increase the value of some $SED_p^{SC_i}$. Hence, the entire circuit SER can be increased, as there probably exists a path from such VPO (the VPOs whose $SED_p^{SC_i}$is increased) to the original circuit POs.

Consider figure 3 which shows a combinational circuit, partitioned into three sub-circuit by introduced partitioning scheme. For instance, in figure 3, before resizing the gates in sub-circuit2, the value of SER_{SC_2} is 19×, while after resizing sub-circuit2, SER_{SC_2} is reduced to 16×. It is notable that resizing such sub-circuit increases the value of $SED_3^{SC_2}$ from 5× to 9× and thus, the entire circuit SER can be increased, as there is a path from such VPO3 to the PO2 in addition to PO1. PO2 and PO1 are the primary outputs of the main circuit.

The partitioning-based gate sizing approach proposed in [18], employed the latching probability concept to ensure that increasing the SED value in a VPO will not lead to

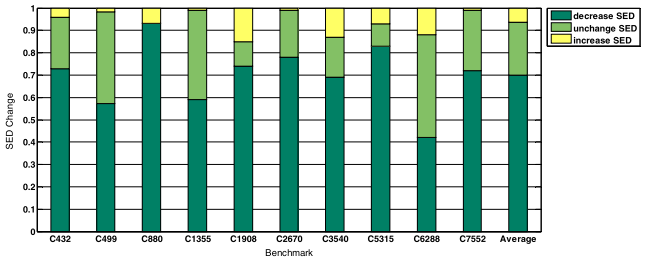

FIGURE 4. The effect of SER_{SC_i} reduction gate sizing of SED value.

increasing the main circuit SER. Latching probability denotes the probability of the triple constraints (logical, electrical and timing masking) being satisfied by a SET (with any width and amplitude) in a VPO, through the propagation path to at least one of the circuit POs and latching as a soft error at the circuit flip-flops. Latching probability is a computational complex concept that should be computed frequently during the gate sizing optimization process. Moreover, the complexity of this approach will get worse when the size of the circuit increases.

Here, in order to address this issue, the gate sizing in the sub-circuits is limited to the ones which results in reducing the SER_{SC_i}, without increasing the $SED_p^{SC_i}$ in any of VPOs. In other words, a gate sizing in the sub-circuit SC_i, is acceptable if and the value of resized sub-circuit SED^{SC_i} ($SED^{'SC_i}$) is less than or equal to the sub-circuit SED^{SC_i} before resizing.

A set of experimental on ISCAS'85 benchmarks shows (Figure 4) that when the sub-circuit gate sizing is performed to reduce only SER_{SC_i} and without any constraint on SED^{SC_i}, the value of SED^{SC_i} will not be increased in 92% of VPOs, in average. In order word only 8% of gate sizing in the sub-circuits increase SED^{SC_i} in VPOs while reducing SER_{SC_i}. Therefore, the ignorance of 8% of gate sizing is not a tight constraint which is imposed by the proposed framework.

IV. OPTIMIZATION PARAMETERS

The proposed algorithm considers the SER_{SC_i}, area and delay as the three major parameters which are affected by the gate resizing process. The cell area is defined as the sum of the width of all transistors in the cell, and the circuit area is determined as the sum of the area of all the cells in the circuit. The defined circuit area correlates fairly with the total static power consumption because the widths of transistors are directly related to the total effective capacitance. Here, we only focus on area and delay overheads when resizing any given gates.

As shown in Figure 2.b, after choosing a sub-circuit, the algorithm proceeds by performing a genetic optimization algorithm on each sub-circuit, where each gene in a chromosome represent the size considered for a gate. For each gate, S different sizes which are available in the technology library cells, are considered during the optimization process. The algorithm begins with the initial population which is set by valid random sizes for each gate in the sub-circuit. Then the objective function evaluates the fitness of each chromosome. In the proposed method, the objective function aims to minimize the SER_{SC_i} of sub-circuit without any increasing in SED^{SC_i} values. Also, the optimization is performed under performance as well as area constraints. The fitness function f_{SC_i} is introduced as follow:

$$f_{SC_i} = \frac{P_{SED}}{SER_{SC_i}} + P_{A/D} \tag{8}$$

here P_{SED} is the penalty for any SED^{SC_i} increment and defined in equation 9.

Where γ is considered a big negative number so that the chromosomes which increase the SED^{SC_i} have negative fitness value and no chance to survive in the next generations. In order to prevent any performance and area violation we introduced $P_{A/D}$ in equation 10, where the chromosomes which violate performance or area constraints will have a negative fitness value.

In order to evaluate the circuit delay, we use slack timing analysis. The slack of a gate is the amount of delay by which a gate delay may be increased without affecting the critical delay of the circuit [34]. In the proposed technique, before resizing the sub-circuits gates, the slack time of each gate in the circuit is computed to determine the circuit gates that can be down-sized. During the gate sizing, we limit the downsizings to the ones that do not make gates slack negative.

V. EXPERIMENTAL RESULTS

In order to investigate the proposed design flow, we conduct the experiments in two parts. Firstly, we study the impacts of the proposed method on the circuit SER reduction. In the second part, we investigate the accuracy and runtime of the proposed approach by comparing the proposed technique with a sensitivity-based gate sizing method [1].

$$P_{SED} = \begin{cases} 1 & if\ for\ each\ p \in VPO_{SC_i}\ SED^{SC_i}_{Pbefore\ sizing} \leq SED^{SC_i}_{Pafter\ sizing} \\ \gamma & else \end{cases} \tag{9}$$

$$P_{A/D} = \begin{cases} \dfrac{Performance_{after\ sizing} - performance_{before\ sizing}}{performance_{before\ sizing}} + \dfrac{Area_{after\ sizing} - Area_{before\ sizing}}{Area_{before\ sizing}} \\ \quad if\ performance\ and\ Area\ constrains\ are\ not\ violated \\ \gamma \quad else \end{cases} \tag{10}$$

The proposed framework is implemented in C++ and run on a windows machine with a core i5 Intel processor (2.53 GHz) and 6GB RAM. The proposed approach was applied to ISCAS'85 and the large scale EPFL [35] benchmark circuits synthesized based on the library gates from 45 nm NANGATE technology [36].

A. EFFICIENCY OF THE PROPOSED TECHNIQUE

The impacts of sub-circuit gate sizing on the SER and area of sub-circuits are studied for C6288 benchmark in details. As presented in Figure 5, resizing the sub-circuit gates reduces SER_{SC_i} in all sub-circuits while the sub-circuits area is increased. As shown in this figure, the area overhead is not the same for all sub-circuits and considerable for some cases. During the algorithm running, resizing the sub-circuit gates may impose significant area overhead when providing SER_{SC_i} improvement. For example, in figure 5, resizing sub-circuit 21 imposes 15% of sub-circuit area overhead while reducing SER_{SC_i} by 33%. In the proposed method, we control the area overhead which is imposed by each gate sizing movement using the priority parameter (equation 10); the algorithm prioritizes gate downsizing over upsizing.

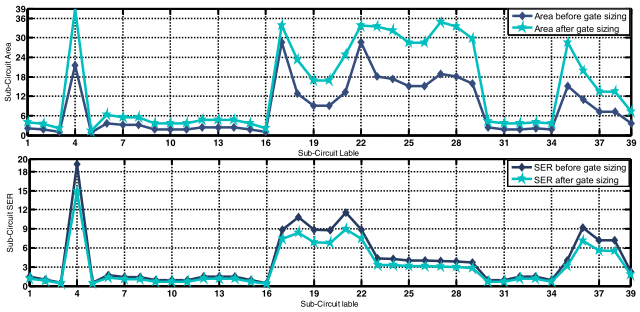

FIGURE 5. Impacts of gate sizing on sub-circuit SER and area in C6288 circuit.

Figure 6 compares the circuit SER values for C880 and C6288 benchmarks in three different cases: 1) before sub-circuits resizing (green line), 2) the circuit SER after resizing individual sub-circuits (violet line), and 3) the circuit SER during consecutive sub-circuits resizing (black line). As can be seen in the figure, using the proposed resizing technique and reducing each sub-circuit SED results in considerable reduction in the entire circuit SER. The SER reduction values of different sub-circuits are not equal and are dependent on the sub-circuits area and its location in the circuit graph. The circuit SER is reduced continuously as the sub-circuits are resized consecutively. As the result shows, resizing all sub-circuits significantly reduces the entire circuit SER.

B. COMPARISON WITH SIMILAR METHODS

In order to explore the accuracy and scalability of the proposed algorithm, we compare the results of cone-oriented gate sizing with a sensitivity-based gate sizing approach [1]. The sensitivity-based gate sizing approach aims to minimize

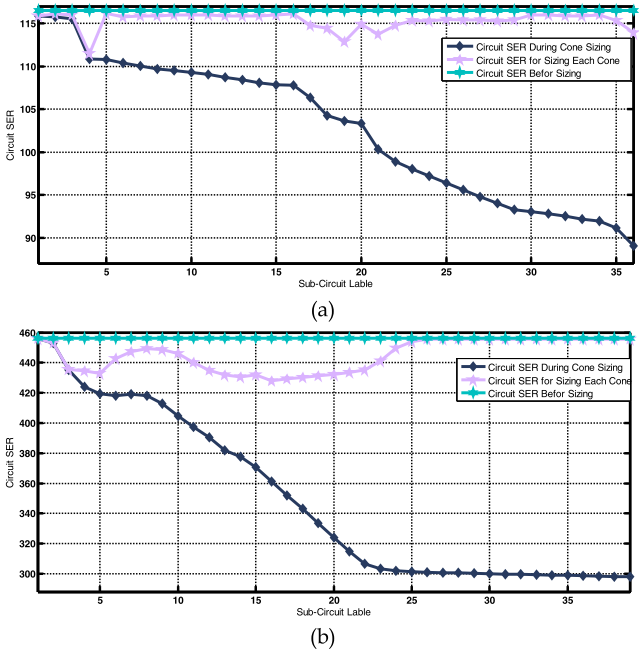

FIGURE 6. Impact of sub-circuit gate sizing on circuit SER (a) C880 circuit, (b) C6288 circuit.

the circuit SER using a sensitivity parameter. This approach firstly prunes the entire circuit into a smaller set of gates by computing bounds on the achievable SER reduction by modifying a gate. This set of gates is considered as possible candidates for resizing, i.e. the gates that provide the maximum SER improvement while incurring the least amount of area overhead. Then, the candidate gates are resized during a greedy optimization process.

In the first step of the proposed technique, the slack time of each gate has been computed, with the delay constraint set to the length of the longest structural path in the circuit.

Both methods are run in the same condition with 20% area constraint. Table 1 shows the results of these two gate sizing algorithms on ISCAS'85 benchmark circuits. The first part of Table 1 represents the information of the benchmarks; column 1 shows the circuit name while the number of gates, number of POs and PIs are of each circuit are represented in column 2, respectively. The second part of Table 1 indicates the results obtained by the cone-oriented gate sizing approach while the third part shows the sensitivity-based gate sizing results. The remaining columns show the SER improvement, area overhead, delay overhead and the number of resized gates, respectively.

The sensitivity based-gate sizing method ignores a large fraction of the circuit gates during the circuit perturbing which may have a significant role on the circuit SER. Only 10-20% of gates are typically considered for resizing procedure [1] while the proposed partitioning method is able to consider all circuit gates during resizing process. Hence, more gates have been resized in the proposed framework in comparison with sensitivity-based algorithm and thus,

TABLE 1. Comparison of the proposed method with the sensitivity-based SER reduction method [1].

Benchmark information		Proposed Method				Sensitivity-based method [1]			
Circuit name	#of gates(PI,PO)	SER Imp	Area change	Delay change	#of resized gates	SER Imp	Area change	Delay change	#of resized gates
C432	160(36, 7)	22.5%	9%	-1%	110	5.6%	4.2%	0%	8
C499	650(41, 32)	23.1%	12%	-2.6%	118	4.9%	4%	0.1%	47
C880	512(60, 26)	24%	18%	-4%	379	8.3%	7.7%	1.1%	39
C1355	653(41, 32)	39.8%	23%	-3.7%	312	11.8%	9.3%	2.1%	52
C1908	699(33, 25)	28.3%	17%	-2.8%	317	9%	8.8%	1.5%	48
C2670	756(233, 140)	46.4%	32%	-5.7%	432	10.6%	7.5%	2.1%	59
C3540	1467(50, 22)	12.2%	14%	-4%	1129	3.1%	3%	3.1%	62
C5315	2115(178, 123)	24.6%	9%	-3%	1771	7.3%	6.8%	4.1%	89
C6288	4507(32, 32)	37.1%	18%	-7%	2262	11.8%	8.4%	3.1%	211
C7552	2534(207, 108)	35.0%	26%	-4%	1184	10.6%	9.1%	2.4%	154
Bar	5648(135,128)	32.2%	15.4%	-7.6%	3826	12.4%	7.2%	9.8%	381
Round Robin	23233(256,129)	43.6%	16.1%	-11.5%	13856	-	-	-	-
Square	35564(64,128)	39.7%	12.7%	-9.3%	20197	-	-	-	-
Log2	54494(32,32)	29.8%	17.4%	-18.6%	39537	-	-	-	-
Average		31%	17%	-6%		8.6%	6.91%	2.67%	

further SER improvement has been achieved. As shown in Table 1, the sensitivity based-algorithm provides only 8% SER reduction by imposing more than 6% circuit area overhead. On the other hand, the proposed method imposes less than 17% area overhead to provide 31% SER improvement. Note that, in the proposed method, more gates are resized and hence, the SER reduction and area overhead will be larger.

Although a gate delay is increased by downsizing, the proposed technique rejects the downsizings which results in negative gate slacks and thus, the critical delay of the circuit dose not affected. Hence, the proposed technique not only does not impose any delay overhead, but also improves circuit performance by the 6% on average as well due to the upsizing actions.

Although, in order to reduce the runtime, the sensitivity-based algorithm considers only 10-20% of gates for sizing, yet it carries out several minutes to converge for medium-scale circuits and as it is shown in table 1 sensitivity-based algorithm does not converge for large-scale ones. Hence, it cannot be practically used during the design of digital systems. Partitioning the circuit into a set of smaller circuits and optimizing smaller circuits independently instated of the original circuit has made the proposed method far faster. It takes less than few minutes to run the proposed method for the medium and large-scale circuits. Very short runtime makes the proposed technique a practical solution for soft error tolerant design. In order to investigate the proposed method more deeply, we change the sensitivity based-gate sizing algorithm such that each gate is considered as a potential candidate for being resized. This approach firstly ranks all gates according to their sensitivity to the soft error and then, selects the gate with the highest sensitivity and aims to minimize circuit SER by resizing it. In the following, we call this method as the *greedy-based method*. The greedy-based method is similar to sensitivity-based method and the only difference is where greedy-based method considers all gates as the resizing candidates.

Table 2 shows the results obtained from the greedy-based algorithm and the proposed cone-oriented-based gate sizing method. As the results show, the greedy-based algorithm provides more SER improvement in comparison with the proposed method. Since all gates are considered in the re-sizing process in the greedy-based method, the most sensitive gate to the soft error in the entire circuit is distinguished and resized. Hence, more SER reduction is achieved. Contrary to the proposed method which locally optimizes the sub-circuits SER, the greedy-based resizing algorithm is an optimization technique which makes a global resizing decision at each step. Therefore, the greedy-based algorithm provides more SER improvement with less area overhead in comparison with the proposed method. However, the greedy-based algorithm takes several hours even for small combinational circuits and it does not converge after several weeks for medium- and large-scale circuits. So, it cannot be used for the SER optimization in a design flow of industrial digital design of combinational circuits.

The proposed approach is also compared to one state-of-the-art SER reduction method (hereinafter called as SERR)

TABLE 2. Comparison of the proposed method with the greedy-based SER reduction method.

Benchmark information		Proposed Method					Greedy-based method			
Circuit name	#of gates (PI,PO)	SER Improve prove-ment	Area change	Delay change	#of resized gate	Run time (sec)	SER Improve prove-ment	Area change	Delay change	#of resized gate
C432	160(36, 7)	22.5%	9%	-1%	110	2	35%	12.8%	3.1%	117
C499	650(41, 32)	23.1%	12%	-2.6%	118	4	31.7%	14%	6.2%	328
C880	512(60, 26)	24%	18%	-4%	379	12	41%	13.3%	2.8%	461
C1355	653(41, 32)	39.8%	23%	-3.7%	312	31	42.7%	11.6%	-4.7%	388
C1908	699(33, 25)	28.3%	17%	-2.8%	317	37	39%	11.5%	5.3%	466
Average		27.5%	16%	-3%		17.2	38%	13%	3%	

TABLE 3. Comparison of the proposed method with one of the state-of-the-art SER reduction method presented in [37].

Benchmark information		Proposed Method				SERR [37]			
Circuit name	#of gates(PI,PO)	SER Imp	Area change	Delay change	#of resized gates	SER Imp	Area change	Delay change	#of resized gates
C432	160(36, 7)	22.5%	9%	-1%	110	13.5%	8.2%	0.3%	9
C499	650(41, 32)	23.1%	12%	-2.6%	118	11.7%	7.6%	0.9%	63
C880	512(60, 26)	24%	18%	-4%	379	13.8%	17.7%	5.1%	43
C1355	653(41, 32)	39.8%	23%	-3.7%	312	17.2%	12.3%	4.3%	50
C1908	699(33, 25)	28.3%	17%	-2.8%	317	14.2%	11.8%	1.9%	45
C2670	756(233, 140)	46.4%	32%	-5.7%	432	13.4%	10.5%	3.3%	61
C3540	1467(50, 22)	12.2%	14%	-4%	1129	7.1%	5.3%	2.7%	58
C5315	2115(178, 123)	24.6%	9%	-3%	1771	14.1%	5.2%	4.0%	81
C6288	4507(32, 32)	37.1%	18%	-7%	2262	15.8%	11.4%	4.7%	303
C7552	2534(207, 108)	35.0%	26%	-4%	1184	20.6%	12.2%	3.6%	201
Average		31%	17%	-6%		14.4%	10.22%	3.08%	

presented in [37]. Table 3 shows the results obtained from the proposed sizing approach and SERR. The results show that SERR provides about 14% SER reduction by imposing more than 10% circuit area over-head but the proposed cone-oriented gate sizing method imposes less than 17% area overhead to provide 31% SER improvement. The main reason is that, more gates are resized in the proposed method and hence, the SER reduction will be larger which increases the area overhead, too.

C. RUN TIME COMPARISON

The run-time for the greedy-based optimization method, the sensitivity-based approach and the proposed method is compared and shown in Figure 8. Note that the Y-axis in this figure is logarithmic. As shown in the figure, the proposed approach is about 165 orders of magnitude faster than the sensitivity-based approach, on average. The proposed method is far faster than both sensitivity and greedy-based optimization algorithms. For example, to optimize the SER of the largest ISCAS'85 circuit using the sensitivity-based gate sizing, it takes at least two days while the runtime of the proposed method for the same circuit is less than twenty minutes.

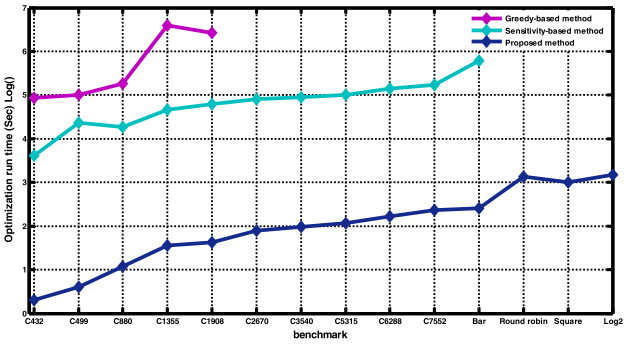

FIGURE 7. Runtime of the proposed method, the sensitivity-based approach and the greedy-based method.

As shown in Figure 7, sensitivity-based gate sizing does not converge for large scale circuit. Also, the greedy-based

method is completely intractable even for medium-sized circuits. For instance, it takes more than three weeks in order to optimize the SER of C1908 circuit with 699 gates by applying the greedy-based optimization technique, while the proposed method reduce 28% of the C1908 circuit SER in less than 63 seconds.

VI. CONCLUSIONS

In this paper, we introduce a framework for SER reduction of large-scaled combinational circuit using a novel gate sizing technique. In this framework, the circuit SER is reduced by partitioning the circuit into a set of small sub-circuits through the cone structures and resizing the small sub-circuit gates independently. By splitting the circuit into small sub-circuits, we only need to estimate the small sub-circuits SER instead of entire circuit SER during gate sizing process; a property which leads to significant reduction in the SER optimization runtime. We verify the efficiency of the proposed method by comparing it with a similar gate sizing approach. The simulation results on ISCAS '85 and EPFL benchmarks show that the proposed method reduces 31% of original SER with 17% area overhead, on average. Very short runtime beside high efficiency makes the proposed method a practical solution for soft error mitigation for large-scale combinational circuits.

REFERENCES

[1] R. R. Rao, D. Blaauw, and D. Sylvester, "Soft error reduction in combinational logic using gate resizing and flipflop selection," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2006, pp. 502–509.
[2] S. Borkar, "Thousand core chips: A technology perspective," in *Proc. 44th Annu. Design Autom. Conf.*, Jun. 2007, pp. 746–749.
[3] R. C. Baumann, "Soft errors in advanced computer systems," *IEEE Des. Test. Comput.*, vol. 22, no. 3, pp. 258–266, May/Jun. 2005.
[4] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 305–316, Sep. 2005.
[5] F. Dabiri, A. Nahapetian, T. Massey, M. Potkonjak, and M. Sarrafzadeh, "General methodology for soft-error-aware power optimization using gate sizing," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 27, no. 10, pp. 1788–1797, Oct. 2008.
[6] K.-C. Wu and D. Marculescu, "Soft error rate reduction using redundancy addition and removal," in *Proc. Asia South Pacific Design Autom. Conf. (ASPDAC)*, Mar. 2008, pp. 559–564.
[7] P. Shivakumar, M. Kistler, S. W. Keckler, D. Burger, and L. Alvisi, "Modeling the effect of technology trends on the soft error rate of combinational logic," in *Proc. Int. Conf. Dependable Syst. Netw.*, Jun. 2002, pp. 389–398.
[8] N. N. Mahatme *et al.*, "Comparison of combinational and sequential error rates for a deep submicron process," *IEEE Trans. Nucl. Sci.*, vol. 58, no. 6, pp. 2719–2725, Dec. 2011.
[9] J. Baggio *et al.*, "Neutron-induced SEU in bulk and SOI SRAMS in terrestrial environment," in *Proc. IEEE Int. Rel. Phys. Symp.*, Apr. 2004, pp. 677–678.
[10] E. H. Cannon, D. D. Reinhardt, M. S. Gordon, and P. S. Makowenskyj, "SRAM SER in 90, 130 and 180 nm bulk and SOI technologies," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2004, pp. 300–304.
[11] K. Mohanram and N. A. Touba, "Cost-effective approach for reducing soft error failure rate in logic circuits," in *Proc. Int. Test Conf.*, Sep./Oct. 2003, pp. 893–901.
[12] M. Nicolaidis, "Time redundancy based soft-error tolerance to rescue nanometer technologies," in *Proc. 17th IEEE VLSI Test Symp.*, Apr. 1999, pp. 86–94.
[13] S. Almukhaizim, Y. Makris, Y.-S. Yang, and A. Veneris, "Seamless integration of SER in rewiring-based design space exploration," in *Proc. IEEE Int. Test Conf. (ITC)*, Oct. 2006, pp. 1–9.
[14] D. Sinha, N. V. Shenoy, and H. Zhou, "Statistical timing yield optimization by gate sizing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 10, pp. 1140–1146, Oct. 2006.
[15] W. Sootkaneung and K. K. Saluja, "Soft error reduction through gate input dependent weighted sizing in combinational circuits," in *Proc. 12th Int. Symp. Qual. Electron. Design (ISQED)*, Mar. 2011, pp. 1–8.
[16] Q. Zhou and K. Mohanram, "Gate sizing to radiation harden combinational logic," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 25, no. 1, pp. 155–166, Jan. 2006.
[17] R. R. Rao, V. Joshi, D. Blaauw, and D. Sylvester, "Circuit optimization techniques to mitigate the effects of soft errors in combinational logic," *ACM Trans. Des. Autom. Electron. Syst.*, vol. 15, no. 1, pp. 1–27, 2009.
[18] M. A. Sabet, B. Ghavami, and M. Raji, "A scalable solution to soft error tolerant circuit design using partitioning-based gate sizing," *IEEE Trans. Rel.*, vol. 66, no. 1, pp. 245–256, Mar. 2017.
[19] E. L. Hill, M. H. Lipasti, and K. K. Saluja, "An accurate flip-flop selection technique for reducing logic SER," in *Proc. IEEE Int. Conf. Dependable Syst. Netw. FTCS DCC (DSN)*, Jun. 2008, pp. 128–136.
[20] H. S. Deogun, D. Sylvester, and D. Blaauw, "Gate-level mitigation techniques for neutron-induced soft error rate," in *Proc. 6th Int. Symp. Qual. Electron. Design (ISQED)*, Mar. 2005, pp. 175–180.
[21] N. Miskov-Zivanov and D. Marculescu, "MARS-C: Modeling and reduction of soft errors in combinational circuits," in *Proc. 43rd ACM/IEEE Design Autom. Conf.*, Jul. 2006, pp. 767–772.
[22] S. Krishnaswamy, S. M. Plaza, I. L. Markov, and J. P. Hayes, "Enhancing design robustness with reliability-aware resynthesis and logic simulation," in *Proc. IEEE/ACM Int. Conf. Comput.-Aided Design (ICCAD)*, Nov. 2007, pp. 149–154.
[23] A. Zukoski, M. R. Choudhury, and K. Mohanram, "Reliability-driven don't care assignment for logic synthesis," in *Proc. Design, Autom. Test Eur.*, Mar. 2011, pp. 1–6.
[24] A. H. El-Maleh and K. A. K. Daud, "Simulation-based method for synthesizing soft error tolerant combinational circuits," *IEEE Trans. Rel.*, vol. 64, no. 3, pp. 935–948, Sep. 2015.
[25] S. Almukhaizim and Y. Makris, "Soft error mitigation through selective addition of functionally redundant wires," *IEEE Trans. Rel.*, vol. 57, no. 1, pp. 23–31, Mar. 2008.
[26] Y. S. Dhillon, A. U. Diril, A. Chatterjee, and A. D. Singh, "Analysis and optimization of nanometer CMOS circuits for soft-error tolerance," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 5, pp. 514–524, May 2006.
[27] V. Joshi, R. R. Rao, D. Blaauw, and D. Sylvester, "Logic SER reduction through flip flop redesign," in *Proc. 7th Int. Symp. Qual. Electron. Design (ISQED)*, Mar. 2006, pp. 611–616.
[28] D. B. Limbrick *et al.*, "Impact of logic synthesis on soft error vulnerability using a 90-nm bulk CMOS digital cell library," in *Proc. Southeastcon*, Mar. 2011, pp. 430–434.
[29] D. B. Limbrick, N. N. Mahatme, W. H. Robinson, and B. L. Bhuva, "Reliability-aware synthesis of combinational logic with minimal performance penalty," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 4, pp. 2776–2781, Aug. 2013.
[30] M. Raji, B. Ghavami, and H. Pedram, "Gate resizing for soft error rate reduction in nano-scale digital circuits considering process variations," in *Proc. Euromicro Conf. Digit. Syst. Design*, Aug. 2015, pp. 445–452.
[31] M. Raji, H. Pedram, and B. Ghavami, "Soft error rate estimation of combinational circuits based on vulnerability analysis," *IET Comput. Digit. Techn.*, vol. 9, no. 6, pp. 311–320, Nov. 2015.
[32] M. Fazeli, S. G. Miremadi, H. Asadi, and S. N. Ahmadian, "A fast and accurate multi-cycle soft error rate estimation approach to resilient embedded systems design," in *Proc. IEEE/IFIP Int. Conf. Dependable Syst. Netw. (DSN)*, Jun./Jul. 2010, pp. 131–140.
[33] R. Rajaraman, J. S. Kim, N. Vijaykrishnan, Y. Xie, and M. J. Irwin, "SEAT-LA: A soft error analysis tool for combinational logic," in *Proc. 19th Int. Conf. VLSI Design, Held Jointly 5th Int. Conf. Embedded Syst. Design*, Jan. 2006, pp. 499–502.
[34] J. Vygen, "Slack in static timing analysis," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 25, no. 9, pp. 1876–1885, Sep. 2006.
[35] L. Amarù, P.-E. Gaillardon, and G. De Micheli, "The EPFL combinational benchmark suite," in *Proc. 24th Int. Workshop Logic Synthesis (IWLS)*, 2015, pp. 1–6.

[36] *NANGATE Library*. Accessed: Oct. 2018. [Online]. Available: http://www.nangate.com
[37] M. Raji and B. Ghavami, "Soft error rate reduction of combinational circuits using gate sizing in the presence of process variations," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 1, pp. 247–260, Jan. 2017.
[38] R. M. Chen *et al.*, "Impact of temporal masking of flip-flop upsets on soft error rates of sequential circuits," *IEEE Trans. Nucl. Sci.*, vol. 64, no. 8, pp. 2098–2106, Aug. 2017.
[39] S. Sayil, A. H. Shah, M. A. Zaman, and M. A. Islam, "Soft error mitigation using transmission gate with varying gate and body bias," *IEEE Des. Test*, vol. 34, no. 1, pp. 47–56, Feb. 2017.

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