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A Fully Integrated C-Band GaN MMIC Doherty Power Amplifier With High Efficiency and Compact Size for 5G Application

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ABSTRACT This paper presents a fully integrated C-band Doherty power amplifier (DPA) based on a 0.25-μm GaN-HEMT process for the 5G massive MIMO application. The performance degradation caused by nonlinear output capacitance is analyzed, and a novel compensation technique is proposed. A low-Q output network is employed to broaden the bandwidth, and its insertion loss in the back-off region is demonstrated to be mainly decided by the Q-factor of the drain bias inductor of the main PA. Hence, by adopting on-chip transmission lines with high Q-factors for drain biasing, a full integration, and a low loss can be achieved simultaneously. Reversed uneven power splitting and back-off input matching are proposed for gain enhancement. The fabricated DPA demonstrates a small-signal gain of 8.6–11.6 dB, an output power of 40.4–41.2 dBm, a 6-dB back-off drain efficiency (DE) of 47% - 50%, and a saturation DE of 55%–63% across a wide bandwidth from 4.5 to 5.2 GHz, with an ultra-compact size of 2.2 mm $\times$ 2.1 mm. Using a 40-MHz LTE signal with a 7.7-dB peak-to-average power ratio at the carrier frequency of 4.9 GHz, the measured average output power and efficiency are 33 dBm and 43%, respectively. The raw adjacent channel power ratio is -29 dBc and is improved to -46 dBc by applying digital predistortion.

INDEX TERMS Doherty power amplifier (DPA), fully integrated, 5G, gallium–nitride (GaN), high-efficiency, monolithic microwave integrated circuit (MMIC).

I. INTRODUCTION

The demand for data rates is increasing rapidly with the development of many emerging technologies. However, the spectrum below 3 GHz has been very crowded. Therefore, many new frequency bands are allocated in 5G communication, including mm-wave band and the spectrum below 6 GHz, especially C-band [1]. Compared with mm-wave band, C-band shows much lower path loss, and will be deployed in 5G system first with a strong commercial demand. Massive multiple-input multiple-output (MIMO) technique will be used in 5G system for spectrum efficiency improvement, and the number of power amplifiers (PAs) is typically up to 64 or 128. As a result, the power requirement of a unit PA is reduced greatly to tens of watts. In addition, the unit PA should be miniaturized to ensure a reasonable system size. GaN-based monolithic microwave integrated circuit (MMIC) is an excellent choice for such application. Since most power is consumed by PAs for a typical base transceiver system, the design of high-efficiency PAs is critical to the reduction of system power dissipation. Doherty power amplifier (DPA) is the most popular architecture for average efficiency enhancement due to its high back-off efficiency [2]–[7]. Many GaN MMIC DPAs, including those for microwave backhaul applications [8]–[17] and those for small-cell or femto-cell applications [18]–[28], have been reported. However, there are relatively few C-band GaN MMIC DPAs for 5G application [29]–[31]. Hybrid integration is adopted for the design

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TABLE 1. Power deterioration caused by nonlinear C_{out}.

C_{out} (pF)	L_p (nH)	Saturated Output Power (dBm)
0.70 @ Back-off	1.5	38.7
0.87 @ Saturation	1.2	39.3

of 3.5-GHz GaN MMIC DPAs in [29], and a state-of-the-art performance is achieved. Fully integrated sub−6 GHz DPAs with high back-off efficiency are presented in [30] and [31]. Nevertheless, the saturated power is below 10 watts, and high back-off efficiency is maintained in a narrow bandwidth. This paper demonstrates an ultra-compact fully integrated GaN DPAs with a saturated power up to 41.2 dBm. Moreover, the 6-dB back-off efficiency better than 47% is achieved in a relatively wide band from 4.5 GHz to 5.2 GHz.

To reduce the occupied size, the quarter-wavelength transformer (QWT) of the proposed DPA is implemented using a lumped π-type network, whose bandwidth is much narrower than that of the distributed QWT [32]. A low-Q output network proposed in [32] is adopted for bandwidth expansion. The back-off impedance transforming ratio (ITR) is reduced to 2 by setting the common load and characteristic impedance of the QWT to R_{opt} and $\sqrt{2}\,R_{opt}$, respectively. Furthermore, the gate width of the transistor is optimized for a R_{opt} of 50 Ω to eliminate the post matching network. The output capacitance of the transistor, which is commonly assumed to be constant in the conventional low-Q design [18], [20]–[24], is absorbed into the output network. In fact, the output capacitance of GaN-HEMT devices is not linear, and it changes with the output power instead, as demonstrated in [33] and [34]. The assumption of a constant C_{out} may deteriorate the load modulation of the DPA significantly. In this paper, the performance degradation caused by the nonlinear output capacitance is analyzed in depth, and a novel compensation technique is proposed. The insertion loss of the low-Q output network in the back-off region is evaluated, and it is found that the loss is mainly decided by the Q-factor of the drain bias inductor of the main PA. To achieve a full integration with a low loss, all drain bias inductors are realized by on-chip transmission lines (TLs), which exhibit much higher Q-factor than on-chip inductors and ensure a high back-off efficiency. Other inductors in the output network are realized by on-chip spiral inductors for a compact size.

A large transistor size is adopted to obtain an output power higher than 10 watts, and the power gain is reduced consequently. In our design, back-off input matching (BIM) and reversed uneven power splitting (RUPS) are proposed for gain enhancement. Different from the conventional design, the input matching of the main PA is optimized in the back-off power level with a load impedance of $2R_{opt}$. The back-off gain of the DPA is improved while maintaining the same the saturated gain. Uneven input power splitting is commonly used to improve the load modulation [35]. However, this method will reduce the gain of the DPA [18]. To solve this problem, different stabilizing circuits are applied for the main PA and the auxiliary PA, and a RUPS scheme is used to deliver more power to the main PA. As a result, the overall gain of the DPA is enhanced greatly.

II. PROPOSED OUTPUT NETWORK

A. LOW-Q NETWORK WITH NONLINEAR C_{OUT} COMPENSATION

Fig. 1 shows the conventional output network of symmetrical DPAs [27]. A high-pass π-type network is used as the QWT with a characteristic impedance of R_{opt}. The output capacitance, C_{out}, of the transistor is neutralized by a shunt inductor L_p. A compact output network with only three inductors can be achieved after merging shunt inductors. However, the requirement of open circuit in the low power (LP) region and optimal power matching in the high power (HP) region cannot be satisfied at the same time with merely one shunt inductor, since the output capacitance of the auxiliary transistor in the LP region is different from that in the HP region.

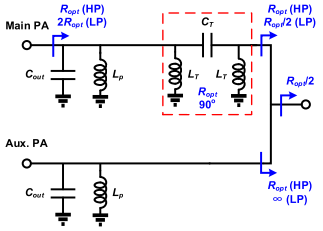

FIGURE 1. Conventional output network.

The large-signal model of GaN-HEMT devices is very complicated, and the output capacitance is modulated by both drain-source and gate-source voltages. Assuming only a dependence on drain-source voltage, the typical characteristic of nonlinear C_{out} according to the drain-source voltage is plotted in Fig. 2(a) [33], [34]. It is observed that the capacitance increases dramatically as the drain-source voltage becomes smaller, which means the average C_{out} will increase with the output power.

A transistor with a gate width of 10 × 200 μm is used to demonstrate the nonlinear output capacitance. The output capacitance under different output powers can be extracted

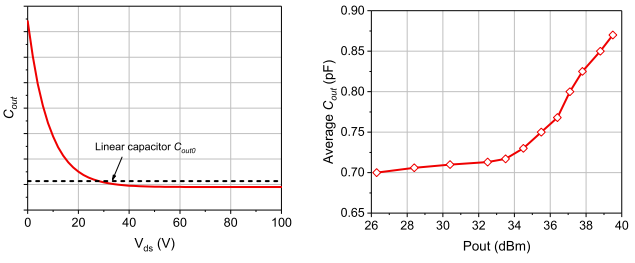

FIGURE 2. (a) Nonlinear C_{out} versus V_{ds}. (b) Average C_{out} versus output power.

from load-pull simulation results. As shown in Fig. 2(b), average C_{out} increases rapidly when the output power is close to saturation. Assuming an operating frequency of 4.9 GHz, the output capacitances in the back-off and saturation region, the corresponding resonant inductances, and the saturated power for each inductance is summarized in Table 1. The shunt inductance for open circuit in the back-off region and optimal power matching in the saturation region are 1.5 nH and 1.2 nH, respectively. In the conventional output network, the saturation output power of the auxiliary PA will be reduced by 0.6 dB if the open circuit in the back-off region is guaranteed, as shown in Table 1, and consequently the load modulation of the DPA is deteriorated.

To overcome the output power degradation caused by the nonlinear C_{out}, a small series inductor is inserted behind the auxiliary PA, as shown in Fig. 3. Shunt inductor L_p of the auxiliary PA is used to resonate with the output capacitance in the back-off region. Owing to the high supply voltage of GaN devices, R_{opt} is a relatively large value. Thus, we assume the impedance of L_s is much smaller than R_{opt}, as defined in (1), where ω is angular frequency.

$$\omega L_s < 1/5R_{opt} \tag{1}$$

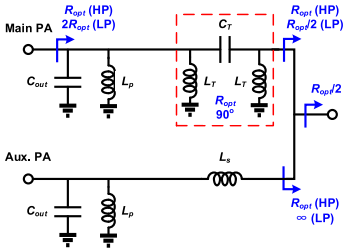

FIGURE 3. Improved output network with a small inductor L_s inserted.

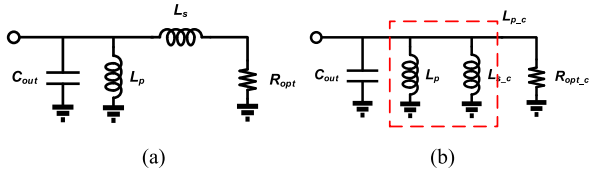

FIGURE 4. (a) Small series inductor L_s is converted to (b) a large shunt inductor L_{s_c}.

In the back-off region, open circuit is maintained in view of the small impedance of L_s. In the saturation region, the output matching network of the auxiliary PA is shown in Fig. 4(a). In Fig. 4(b), the series inductor is converted to the shunt inductor using the following equations:

$$R_{opt\_c} = R_{opt}(1 + Q^2) \tag{2}$$

$$L_{s\_c} = L_s(1 + 1/Q^2) \tag{3}$$

$$Q = \omega L_s/R_{opt} \tag{4}$$

Q is a very small value according to (1), thus, (2) and (3) can be simplified to (5) and (6), respectively.

$$R_{opt\_c} \approx R_{opt} \tag{5}$$

$$L_{s\_c} > 26L_s \tag{6}$$

L_{s_c} is a large inductor, and the merging of L_{s_c} and L_p will result in an inductor smaller than L_p, denoted by L_{p_c} in Fig. 4(b). Consequently, although the output capacitance increases rapidly in the saturation region, the shunt inductor is able to resonate with C_{out} around the operating frequency, and the performance deterioration can be overcome. The example in Table 1 shows a power reduction of 0.6 dB when using a 1.5-nH shunt inductor. After a 0.3-nH series inductor is inserted, the saturation power is restored to 39.2 dBm, which is only 0.1 dB lower than the maximum power from the simulation results. Since the inductance of L_s is very small, the introduced insertion loss is negligible and power improvement can be maintained.

Besides the performance deterioration caused by nonlinear output capacitance, the conventional network in Fig. 1 also exhibits limited bandwidth because of the high ITR in the back-off region. To expand the bandwidth of the DPA, a low-Q QWT is adopted [32]. Fig. 5 presents the schematic of the low-Q output network. The common load and characteristic impedance of the transformer are set to R_{opt} and $\sqrt{2}R_{opt}$, respectively. Therefore, the ITR in the back-off region is reduced to 2, and a larger bandwidth can be achieved. A lower ITR means a lower insertion loss, and the back-off efficiency will also be improved. The ITR in the saturation region has the same value, hence, the saturation performance is not a limiting factor of the overall bandwidth. The post matching network is an additional bandwidth limiting factor. It also occupies a large size and introduces additional insertion loss. Hence, the gate width of the transistor is optimized to realize a R_{opt} of 50 Ω, which results in a transistor size of 10×200 μm.

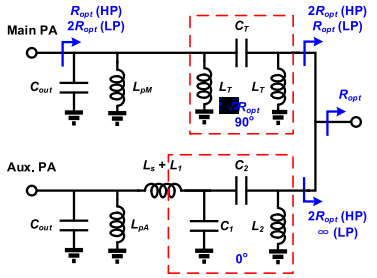

FIGURE 5. Low-Q output network.

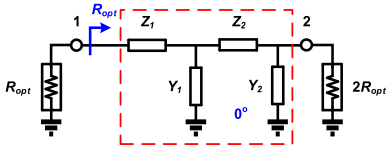

FIGURE 6. Structure of zero-phaseshift network.

A band-pass network with a zero phaseshift is used to realize the impedance transformation in the saturation region and maintain the open circuit of the output impedance in the back-off region at the same time. The network is composed of L_1, C_1, L_2, and C_2, and its structure is presented in Fig. 6,

where $Z_1 = j\omega L_1$, $Z_2 = 1/j\omega C_2$; $Y_1 = j\omega C_1$, and $Y_2 = 1/j\omega L_2$. To determine element values, the S-parameter matrix of the network is derived. Firstly, the cascaded matrix can be calculated by multiplying that of each element, denoted by

$$A = A_{Z_1} A_{Y_1} A_{Z_2} A_{Y_2} \tag{7}$$

where A_{Z1}, A_{Y1}, A_{Z2}, and A_{Y2} are the cascaded matrixes of each element. Then the cascaded matrix is converted to S-parameter matrix. Considering the function of the network, the following equations should be satisfied:

$$S11 = 0 \tag{8}$$

$$\angle S21 = 0 \tag{9}$$

After some simplification, we can get

$$Z_2 + Y_1 Z_1 Z_2 + Z_1 = 0 \tag{10}$$

$$Y_1 + Y_1 Y_2 Z_2 + Y_2 = 0 \tag{11}$$

$$1 + Y_1 Z_2 = 2(1 + Y_1 Z_1) \tag{12}$$

The solution is not unique, as the number of equations is less than that of variables. Different solutions result in different bandwidths, occupied areas and insertion losses. The principle of determining final solution is that the values of L_1 and L_2 should be as small as possible while a reasonable bandwidth is guaranteed.

B. FULL INTEGRATION WITH LOW LOSS

Fig. 7 shows the impedance transforming in the back-off region, where L_M is the merged inductance of L_{pM} and L_T, R_M and R_T represent the loss of L_M and L_T, respectively, and the loss of capacitor is not considered. To achieve a high back-off efficiency, the insertion loss of the QWT should be minimized, which relies on the Q-factors of L_M and L_T. The resistor network in Fig. 7 divides the current, and dissipates RF power. Assuming R_M and R_T are much larger than R_{opt}, the insertion loss can be expressed as

$$Loss = R_M/(R_M + 2R_{opt}) * R_T/(R_T + R_{opt}) \tag{13}$$

Denoting the Q-factor of L_M and L_T by Q_M and Q_T, respectively, R_M and R_T can be calculated using

$$R_T = \omega L_T Q_T \tag{14}$$

$$R_M = \omega L_M Q_M \tag{15}$$

where L_T and L_M are decided by

$$L_T = \sqrt{2} R_{opt}/\omega \tag{16}$$

$$L_M = L_T // L_p < L_T \tag{17}$$

Using (14)-(17), (13) can be simplified to

$$Loss = Q_T/(Q_T + 1/\sqrt{2}) * Q_M/(Q_M + 2/\beta) \tag{18}$$

where $\beta = \omega L_M/R_{opt} < \sqrt{2}$. Since $2/\beta$ is much larger than $1/\sqrt{2}$, it can be concluded that the insertion loss is more sensitive to Q_M.

In [20]–[25], [27], and [28], L_M is realized using off-chip inductors or bonding wires with high Q-factors. However, the requirement of off-chip components reduces the consistency and reliability of PA modules. Therefore, on-chip components are adopted for both L_M and L_T to achieve a full integration. Due to the limited dc-current capacity of on-chip inductors, L_M is realized by an on-chip TL. Compared with on-chip inductors, on-chip TLs exhibit much higher Q-factor, which guarantees a low loss of the QWT according to (18). For a 10 × 200 μm transistor, L_M and L_T are 0.79 nH and 2.3 nH, respectively, and R_{opt} is 50 Ω. Fig. 8 illustrates the insertion loss as a function of Q_M and Q_T at 4.9 GHz. It is observed that the loss shows very small variation with Q $_T$, and mainly depends on Q_M. Fig. 9 presents the Q-factor of the on-chip TL and spiral inductor with the same inductance of 0.79 nH. At 4.9 GHz, the Q-factor of the spiral inductor is only 17 while that of the on-chip TL is up to 46. Assuming a Q-factor of 20 for L_T, the network with on-chip TL exhibits an insertion loss of only 0.55 dB according to Fig. 8.

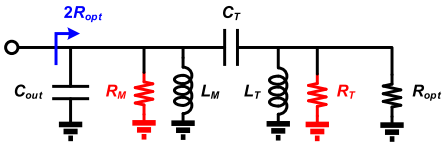

FIGURE 7. Impedance transforming of the QWT in the back-off region.

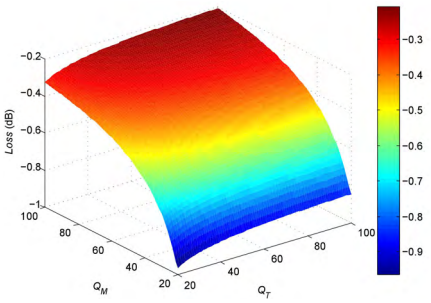

FIGURE 8. Insertion loss of the QWT as a function of Q_T and Q_M in the back-off region.

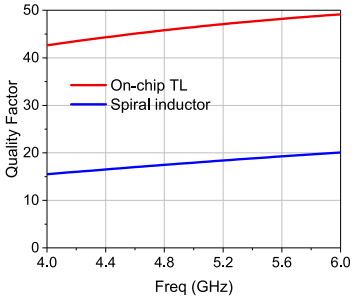

FIGURE 9. Q-factor of the on-chip TL and spiral inductor.

The final version of the proposed output network is shown Fig. 10. The drain bias inductor of the auxiliary PA is also realized by an on-chip TL. A small loaded capacitor C_L is employed to avoid a lengthy TL at the cost of a little

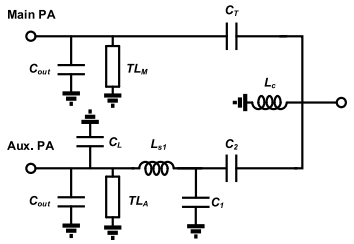

FIGURE 10. Final version of the proposed output network.

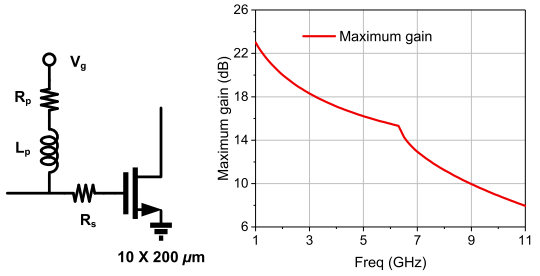

FIGURE 11. (a) Stabilizing circuit and (b) maximum gain of a 10 × 200 μm transistor.

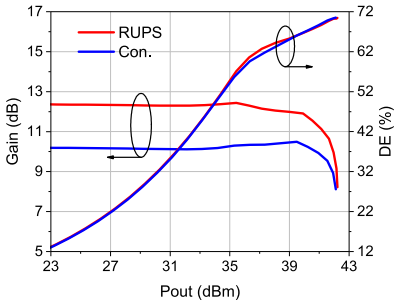

FIGURE 12. Performance of the DPA with RUPS and the conventional DPA.

bandwidth deterioration. L_T and L_2 in Fig. 5 are merged into L_c. Series inductors L_s and L_1 are merged into L_{s1}.

III. GAIN ENHANCEMENT

Fig. 11(a) shows the stabilizing circuit, where a small series resistor R_s is used to improve in-band stability and a relatively large parallel resistor R_p is applied to remove possible low-frequency oscillations. With R_s set to 3 Ω, the maximum gain of the 10 × 200 μm transistor is shown in Fig. 11(b). The device is conditionally stable in the operating frequency band, but the unconditional stability can be achieved when the losses of all passive networks are considered according to the final layout simulation results. The maximum gain of the transistor is about 16 dB at 4.9 GHz, thus, the maximum gain of the DPA is 13 dB assuming an even input splitter. Input network is realized by lumped components to achieve a compact size, and the gain of the DPA will be further reduced due to the high loss of on-chip inductors. In our design, RUPS and BIM are proposed to enhance the gain.

A. REVERSED UNEVEN POWER SPLITTING

Conventionally, main PA and auxiliary PA employ the same stabilizing circuit, and the gain of the auxiliary PA is much lower than that of the main PA because of the class-C biasing. To prevent an inappropriate load modulation, an uneven power splitter is commonly adopted to deliver more power to the auxiliary branch, and auxiliary PA is biased at a deeper class- C to prevent the early turn-on [35]. However, this method will reduce the gain in the back-off region due to a shortage of the input power towards the main PA and, also, the gain in the HP region due to a deep class-C operation [18].

In fact, the small-signal stability of the DPA is dominated by the main PA since auxiliary PA provides no gain in the back-off region [36]. Hence, the stabilizing circuit of the auxiliary PA can be relaxed, and asymmetrical stabilizing networks are applied for the DPA. In our design, R_s is set to 3 Ω for the main PA while it is reduced to 1 Ω for the auxiliary PA, which increases the gain of the auxiliary PA. Contrary to the conventional DPA, we adopt a reversed uneven power splitter to provide more power to the main PA, and then the auxiliary PA can be biased at a shallower class-C. As a result, the overall gain of the DPA is improved greatly. Fig. 12 shows the performance of the conventional DPA and the DPA with RUPS. For the conventional DPA, the series resistors of the main PA and the auxiliary PA are both 3 Ω, and 1 dB more power is delivered to the auxiliary PA with −4.6 V gate biasing. For the proposed DPA, the series resistors of the main PA and auxiliary PA are 3 Ω and 1 Ω, respectively, 4 dB more power is delivered to the main PA, and the auxiliary PA is biased at −3.7 V. It is observed that the proposed RUPS technique enhances the gain by about 2 dB in the back-off region and 1.5 dB in the saturation region, with a similar efficiency performance.

B. BACK-OFF INPUT MATCHING

Fig. 13(a) presents a simplified equivalent circuit for the GaN-HEMT device [37]. The capacitor C_{gd} can be split, according to the Miller's theorem, into two grounded

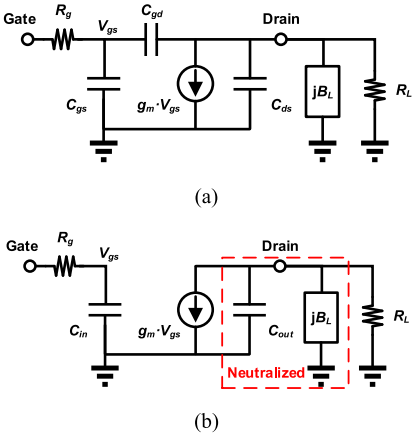

FIGURE 13. Equivalent circuit for the GaN-HEMT device (a) before and (b) after applying Miller's theorem to C_{gd}.

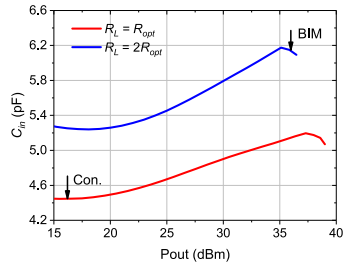

FIGURE 14. Input capacitance of the main PA for the load impedances of R_{opt} and $2R_{opt}$.

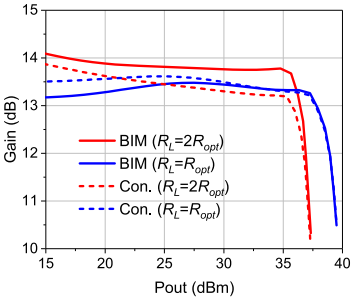

FIGURE 15. Gain of the main PA with BIM and the conventional main PA for the load impedances of R_{opt} and $2R_{opt}$.

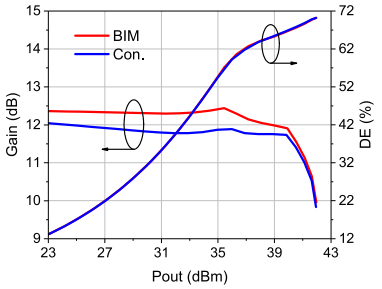

FIGURE 16. Performance of the DPA with BIM and the conventional DPA.

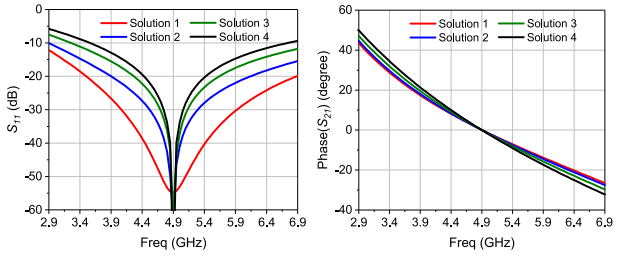

FIGURE 17. Frequency response of the zero-phaseshift network.

elements in parallel to C_{gs} and C_{ds}, respectively, resulting in the equivalent capacitors C_{in} and C_{out}, as shown in Fig. 13(b). Assuming C_{out} is neutralized by susceptance jB_L, the input capacitance can be approximated as

$$C_{in} = C_{gs} + C_{gd}(1 + g_m R_L) \tag{19}$$

where R_L is the load impedance. Since g_m, C_{gs}, and C_{gd} are all nonlinear, C_{in} is a function of power level. Moreover, it should be noted that C_{in} also depends on load impedance R_L. Fig. 14 depicts the extracted input capacitance of the main PA versus output power for the load impedance of R_{opt} and $2R_{opt}$. Conventionally, the input matching of the main PA is designed in the small-signal region with the load impedance of R_{opt}. A mismatch will be produced in the back-off power level and the gain will be degraded consequently. To solve this problem, BIM is adopted in our design, which means that the input matching is designed in the back-off power level with the load impedance of $2R_{opt}$. The gain of the main PA with BIM is compared with the conventional main PA in Fig. 15. In the back-off power level (Pout $=$ 36 dBm, $R_L = 2R_{opt}$), BIM improves the gain by about 0.6 dB. In the saturation power level (Pout $=$ 39 dBm, $R_L = R_{opt}$), BIM shows no impact on the gain. Fig. 16 presents the performance comparison between the DPA with BIM and the conventional DPA. The back-off gain of the DPA is enhanced by about 0.5 dB while almost the same efficiency is achieved.

IV. CIRCUIT DESIGN

A. OUTPUT NETWORK

As mentioned before, the transistors with a gate width of 10×200 μm are adopted to realize a R_{opt} of 50 Ω. Load-pull simulations are launched, and the maximum output power is about 39.5 dBm with 28-V supply. The output capacitances in the back-off region and the saturation region are extracted to be 0.7 pF and 0.87 pF, respectively. With an operating frequency of 4.9 GHz, the element values in Fig. 5 are calculated first. Some component values have been provided in the previous sections, and they are not repeated here. Using (10)-(12), the output matching network of the auxiliary PA can be synthesized, and a group of solutions are shown in Table 2. Frequency response of the network in Fig. 6 for each solution is depicted in Fig. 17. It is found that different solutions result in different matching bandwidths. Solution 1 shows the largest bandwidth with the largest inductances, while Solution 4 exhibits the smallest bandwidth with the smallest inductances. In practical design, the inductance is expected to be smaller for chip miniaturization. With both bandwidth and inductance taken into consideration, Solution 2 is chosen for circuit implementation.

To decide the linewidth of TL_M and TL_A, dc supply current should be assessed first. Since the maximum output power of the employed transistor is 39.5 dBm, the maximum dc current is calculated to be 530 mA assuming a drain efficiency of 60%. The dc-current density of TLs is 29.6 mA/μm, and thus the allowable minimum linewidth is calculated to be 18 μm. A larger linewidth of 50 μm is used for both TL_M and TL_A to realize a low loss at the cost of a little larger occupied area. Table 3 summarizes the component values of the proposed output network in Fig. 10. Electromagnetic (EM) simulation is launched to evaluate the performance of the proposed output network, the insertion loss of which under different output powers is presented in Fig. 18. In the back-off region, the insertion loss is only about 0.85 dB, ensuring a high back-off efficiency.

TABLE 2. Synthesization OF Zero-phaseshift network.

Solution	Component Values (nH, pF)
Solution 1	L_1=1.03, L_2=4.97, C_1=0.30, C_2=0.72
Solution 2	L_1=0.77, L_2=3.73, C_1=0.40, C_2=0.97
Solution 3	L_1=0.62, L_2=2.98, C_1=0.50, C_2=1.21
Solution 4	L_1=0.52, L_2=2.49, C_1=0.60, C_2=1.45

TABLE 3. Component values of the Proposed output network.

Component	Values
TL (μm)	TL_M=1390, TL_A=1530
Inductor (nH)	L_c=1.42, L_{s1}=1.07
Capacitor (pF)	C_7=0.46, C_1=0.40, C_2=0.97, C_L=0.5

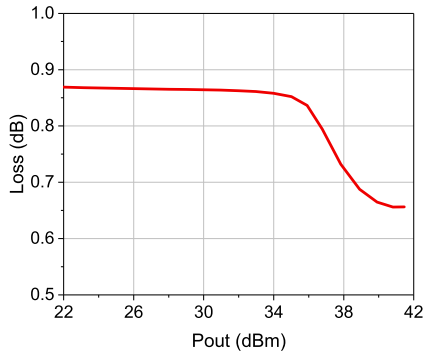

FIGURE 18. Insertion loss of the proposed output network versus output power.

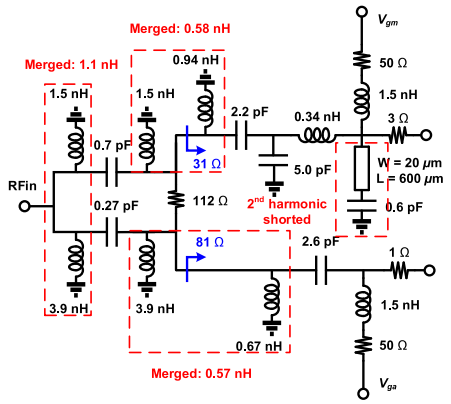

FIGURE 19. Input network of the proposed DPA.

B. INPUT NETWORK

The schematic of the input network is shown in Fig. 19, where all components values are given. Due to the nonlinear input capacitor, the second harmonic of the input voltage is out-of-phase to the fundamental component, and the conduction angle is increased as a result, which will degrade the efficiency obviously [21]. Therefore, a second harmonic short-circuit network is inserted at the gate of the main PA, which improves both the back-off and saturated efficiencies. At fundamental frequency, the harmonic network is equivalent to a shunt capacitor, and acts as a part of the input matching network. The QWT and different biasings result in a phase difference of 100° between the two branches. The phase compensation is integrated with the input matching of the main PA by adopting a band-pass network for the main PA and a high-pass network for the auxiliary PA. High-pass and band-pass networks exhibit a phase shift of 80° and −20°, respectively, and then the phase difference of 100° is compensated. A Wilkinson divider realized by lumped inductors and capacitors is used for power splitting. The port impedance is 31 Ω for the main PA and 81 Ω for the auxiliary PA. The divider is designed at 4.9 GHz, and provides a fractional bandwidth of 20%, which is enough for our design. The shunt inductors at the same node can be merged for a reduced size.

C. IMPLEMENTATION

The overall schematic of the proposed DPA is shown in Fig. 20. A 0.25-μm GaN-HEMT process from WIN Semiconductors is adopted for implementation. The power density is about 4 W/mm with 28-V drain supply, and the cutoff frequency is 24.5 GHz. All passive circuits are simulated using the Momentum in Keysight's Advanced Design System (ADS). The dimensions of passive devices have been fine tuned in view of many non-ideal factors, such as coupling effect, connecting line and bending effect. Fig. 21 shows the EM simulation results of the proposed DPA from 4.7 to 5.4 GHz. The saturation power is over 40.8 dBm and the 6-dB back-off DE is better than 49% across the bandwidth.

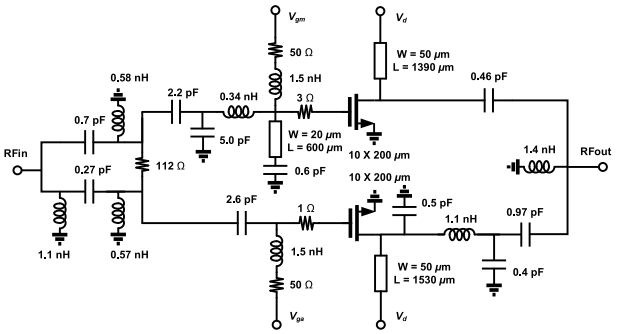

FIGURE 20. Complete schematic of the proposed DPA.

V. MEASUREMENT RESULTS

The photo of the fabricated DPA is shown Fig. 22, and the chip size is only 2.2 mm × 2.1 mm. The chip is measured with on-wafer probes under the following bias condition: V_d = 28 V (I_{DQ} = 27 mA), V_{gm} = −2.4 V,V_{ga} = −3.8 V. Fig. 23 presents the measured S-parameters, where the simulated S-parameters is also depicted for comparison. A rather good agreement is observed in spite of a frequency shift of about 200 MHz towards the lower frequency band. The small-signal gain is higher than 8.5 dB from 4.1 to 5.3 GHz, and the input return loss is better than −10 dB from 3.7 to 5.4 GHz.

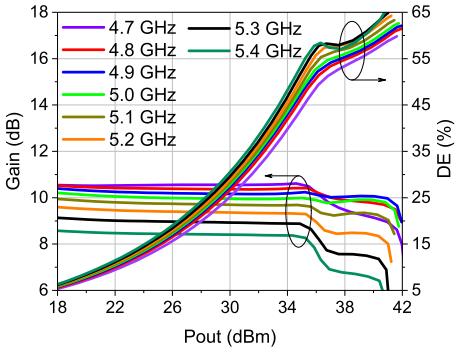

FIGURE 21. Simulated performance of the DPA from 4.7 to 5.4 GHz.

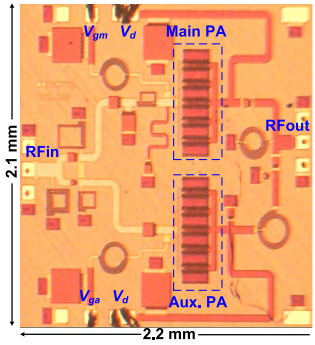

FIGURE 22. Photo of the fabricated DPA.

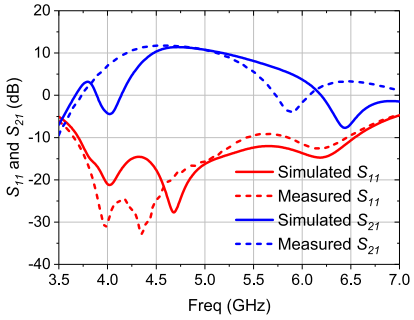

FIGURE 23. Measured S-parameters of the fabricated DPA.

Large-signal performance also exhibits a frequency shift, and the actual operating frequency band is 4.5 – 5.2 GHz. Fig. 24 shows the measured DE and gain characteristics for the continuous-wave signal across the bandwidth with 0.1 GHz step. At the center frequency of 4.9 GHz, the fabricated DPA demonstrates a power gain of 11 dB, a saturated output power of 41 dBm, a 6-dB back-off DE up to 50%, and a peak DE of 58%. As shown in Fig. 25, a saturated power of 40.4 – 41.2 dBm, a 6-dB back-off DE (PAE) of 47% - 50% (40% - 45%), and a saturated DE (PAE) of 55% - 63% (45% - 51%) are obtained from 4.5 GHz to 5.2 GHz. Compared with the simulated performance in Fig. 21, measured results show a saturation power degradation of about 0.5 dB, and a DE decrease of about 3% at both saturation and 6-dB back-off, which could be caused by process variation, model inaccuracy, or the error of test system. In addition, the measured gain exhibits a larger compression, and the reason may be that

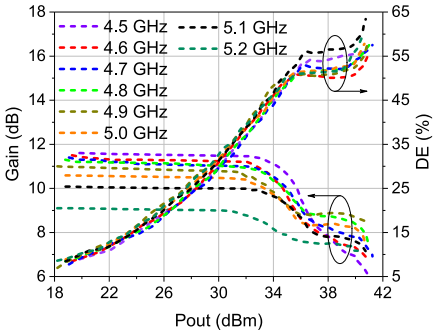

FIGURE 24. Gain and DE of the fabricated DPA from 4.5 to 5.2 GHz.

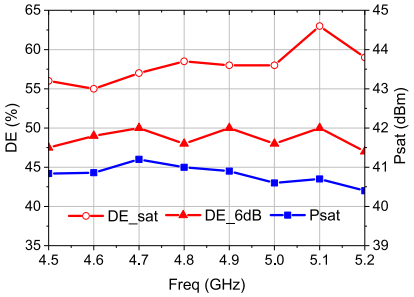

FIGURE 25. Measured saturation power, saturation DE and 6-dB back-off DE from 4.5 to 5.2 GHz.

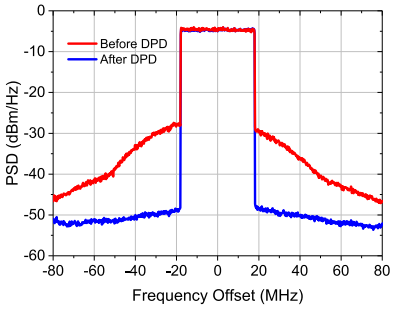

FIGURE 26. ACPR before and after DPD.

the power device with class-C biasing is not well modeled. To measure the DPA's performance under the modulated signal excitation, a 40-MHz LTE signal with a peak-to-average power ratio (PAPR) of 7.7 dB is employed at the carrier frequency of 4.9 GHz. The measured efficiency is 43% at the average output power of 33 dBm. DPD based on generalized memory polynomial (GMP) model is performed to linearize the DPA. Fig. 26 presents the measured power spectrum density (PSD) before and after DPD at the average output power of 33 dBm. The ACPR of the proposed DPA is −29 dBc and is improved to −46 dBc after DPD linearization.

The performances are summarized and compared with other fully integrated C-band GaN MMIC DPAs in Table 4, where the power density is defined as the ratio of the saturated power to chip size. The proposed DPA demonstrates the largest saturated power with a high efficiency. Moreover, the power density is also the largest because of the ultra-compact size. Therefore, the proposed design is a very good candidate for 5G MIMO application.

TABLE 4. Comparision with other fully integrated C-band GaN MMIC DPAs.

Ref.	Architecture	Freq (GHz)	Gain (dB)	Psat (dBm)	PAE (%) @ Back-off	PAE (%) @ Psat	Linearization	Chip Size (mm^2)	Power Density (W/mm^2)
[8]	Asym.	7.0	10	37	47 @ 7 dB[a]	50[a]	N/A	21.6	0.23
[9]	Asym.	6.35 – 7.35	10.5	38	40 – 42 @ 7 dB[a]	46 – 50[a]	N/A	25	0.25
[10]	Asym.	6.8 – 8.5	13.5	35	24 – 37 @ 9 dB[b]	38 – 50	DPD	3.2	1.1
[11]	Asym.	5.8 – 8.8	10	36	31 – 39 @ 9 dB	28 – 42	DPD	8.4	0.48
[16]	Sym.	6.6 – 7.3	16	38	40 – 43 @ 6 dB[b]	55 – 58[b]	Analog	9	0.7
[30]	Asym.	4.0 – 4.5	17	36	35 – 44 @ 6 dB[b]	48 – 55[b]	N/A	3.5	1.1
[31]	Asym.	5.1 – 5.9	14.4	38.7	31.6 – 49.5 @ 6 dB	43.2 – 47.3	DPD[c]	3.9	1.9
This work	**Sym.**	**4.5 – 5.2**	**11.6**	**41.2**	**40 – 45 @ 6 dB**	**45 – 51**	**DPD**	**4.6**	**2.9**

a DE

b Read from graph

c Simulation based on X-parameters

VI. CONCLUSION

A fully integrated GaN MMIC DPA with high-efficiency and compact size has been designed for 5G MIMO application. The performance degradation caused by the nonlinear output capacitance is analyzed in depth, and is overcome by inserting a small series inductor. A low-Q output network is employed to broaden the bandwidth. Its insertion loss in the back-off region is demonstrated to be mainly decided by the Q-factor of the drain bias inductor of the main PA. To achieve a full integration and low loss simultaneously, all drain bias inductors are realized by on-chip TLs with high Q-factors. Using the proposed RUPS and BIM, the gain of the DPA is enhanced greatly. The fabricated DPA demonstrates a measured saturation power of 40.4 – 41.2 dBm, and a 6-dB back-off DE of 47% - 50% from 4.5 to 5.2 GHz, with a chip size of 2.2 mm $\times$ 2.1 mm. Under an excitation of 40-MHz LTE signal with 7.7-dB PAPR, the ACPR at the average output power of 33 dBm is improved to -46 dBc after applying DPD.

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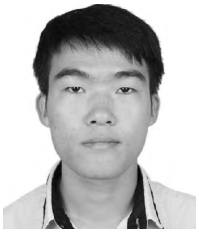

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