IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received April 22, 2019, accepted May 16, 2019, date of publication May 27, 2019, date of current version June 27, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2919124

Compact Quasi-Planar Four-Way Power Divider With Wide Isolation Bandwidth

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This work was supported in part by the National Natural Science Foundation of China under Grant 61771094, and in part by the Sichuan Science and Technology Program under Grant 2019JDRC0008.

ABSTRACT A novel compact quasi-planar four-way power divider with a wide isolation bandwidth is proposed in this paper. The signal is fed through the coplanar waveguide and then divided to the four microstrip-line output ports through a metal via. To realize the high output isolation, the multi-layer circuit structure is used. The isolation network is composed of four isolation resistors and a metal via (common node). Equivalent circuits are given to analyze and design the novel power divider. The detailed analyses are given according to the equivalent circuits. A four-way high-isolation power divider with the center frequency of 2.1 GHz is designed and fabricated. The measured 20-dB relative isolation bandwidth between the output ports is about 58%, while 30-dB relative isolation bandwidth between the output ports is about 10%. The measured results agree well with the simulated ones. The total size of the fabricated four-way power divider is $0.17\lambda_g \times 0.22\lambda_g$ (λ_g is the wavelength of the center frequency). It shows that the proposed power divider has not only the advantages of high output isolation and compact size but also the advantages of excellent output and input impedance matching and very low insertion loss. The presented power divider can be used in antenna feed, power-combining amplifier, and so on.

INDEX TERMS Power divider, wide isolation band, high isolation.

I. INTRODUCTION

With the rapid development of RF and microwave communication systems, the demand for all kinds of high-performance active [1]–[3] or passive circuits [4]–[33] has increased greatly. Among these different circuits, the power divider/combiner, which is used to divide signal into several ways or combine signals, show its indispensable role in communication systems. The introduction of the Wilkinson power divider in the 1960s [7] has resulted in great interest in developing various power distribution/combination circuits, like the power divider with the structure of planar/quasi-planar [20]–[39], high integration, it is used in microwave systems more widely compared with other dividers. Moreover, in these structures, the impedance matching at the output port and isolation between output ports will be better after isolation network added.

Several planar power dividers that can achieve high isolation and good impedance between all the output ports have been studied in [21]–[28]. However, because of structural limitation, these power dividers can only achieve 2 or 3 ways of signal distribution, which will make the fact that in practical systems, these power dividers are not suitable. In order to get great isolation between output ports, several power dividers in [29]–[31] choose to introduce the planar multi-stage binary, however, high insertion loss and large size become problems that come with it. To make the output impedance matching and isolation performance be better, different structures were used in [16] and [33], [34]. However, due to the use of the complicated structure of air-bridge, their applications in N-way (N 4) power dividers are limited. And the isolations perform good in [16] and [33], which are all less than 20dB. Therefore, high isolation, low loss, compact size, and good impedance matching at all ports are urgent characteristics for an N-way (N 4) planar/quasi-plane divider.

In this paper, a novel quasi-planar four-way power with high output isolation is proposed. It consists of two-layer

The associate editor coordinating the review of this manuscript and approving it for publication was Macquarie Jahangir Hossain.

substrate structure with a CPW input port and the microstrip output ports. To get high output isolation and good output impedance matching, the isolation network is used in this circuit. Moreover, the detail equivalent circuit model and the even- and odd-mode analysis method are used to design the presented power divider. Finally, the presented high-isolation power divider is designed and fabricated. The presented four-way power divider using two-layer substrate structure can be used in multi-layer substrate structure four-antenna array, the four-way power-combining amplifier, and so on.

II. ANALYSIS AND DESIGN

The structure of the presented power divider has been shown in Fig.1. It consists of two-layer substrates and three layer metal which are located on the top, bottom and middle of the substrate layers. The input port and output ports are CPW and microstrip lines respectively. CPW is located in the middle metal layer and microstrip lines are located in the top and bottom metal layer. The ground of the top microstrip lines and the ground of the bottom microstrip lines are both the middle metal layer. At the input port, the input signal is fed through the CPW and then divided into four ways in phase and amplitude by the metal via1. The isolation network is composed of four resistors and the metal via2 which used as the common node of the four resistors in here. The resistor is located on the substrate. It's one end is connected to the microstrip line, while the other end is connected to the metal via2 (common node). The assembly layout of the resistors is shown in Fig. 2. The metal via2 connects the resistors on the top layer and the resistors on the bottom layer, while the ground is etched around this metal via. This operation is to avoid the signal and ground connection. To let the impedance matching be better, the bended microstrip line is used, thus, l1's length is about λm/4 (λm is the guide wavelength of the microstrip line at the central frequency).

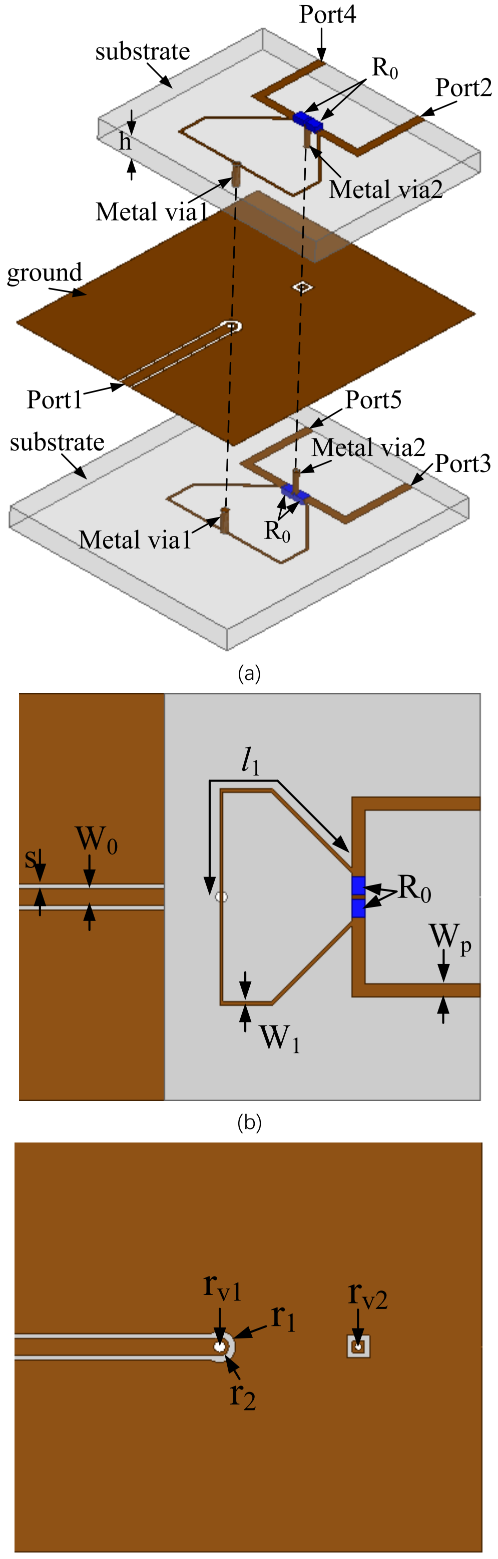
Fig. 3 gives the detail equivalent circuit of the proposed quasi-planar power divider. Z_{CPW}, Z_1 and Z_p are the impedance of the input CPW transmission line, bended microstrip line and the output transmission line respectively. The capacitor C_{V1}, C_{V2}, inductor L_{V1}, L_{V2}, and resistor R_{V1}, R_{V2} are the parasitic parameters [36] of metal via1 and metal via2 respectively. C_{V1}, C_{V2}, L_{V1}, L_{V2}, and R_{V1}, R_{V2} could be given by

$$L_{v1} = \alpha_1 \frac{\mu_0}{2\pi} \left| \ln\left(\frac{2h}{r_{v1}}\right) - 1 \right| h \tag{1}$$

$$L_{v1} = \alpha_2 \frac{\mu_0}{2\pi} \left| \ln\left(\frac{2h}{r_{v2}}\right) - 1 \right| h \tag{2}$$

where μ_0 is the permeability of vacuum, h is the height of substrate, r_{v1}, r_{v2} is the radius of the metal via, and α_1, α_2 are the fitting parameters, which are

$$\alpha_1 = 0.94 + 0.52\, e^{-10\left|\frac{h}{2\, r_{v1}} - 1\right|},\quad \alpha_2 = 0.94 + 0.52\, e^{-10\left|\frac{h}{2\, r_{v2}} - 1\right|}$$



(a)

(b)

(c)

FIGURE 1. Structure of the proposed four-way power divider. (a) 3-D structure. (b) Top view. (c) Middle view.

and

$$C_{V1} = 2\pi r_{v1} \varepsilon \tag{3}$$

$$C_{V2} = 2\pi r_{v2} \varepsilon \tag{4}$$

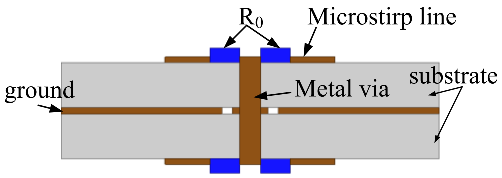


FIGURE 2. View of the isolation resistor.

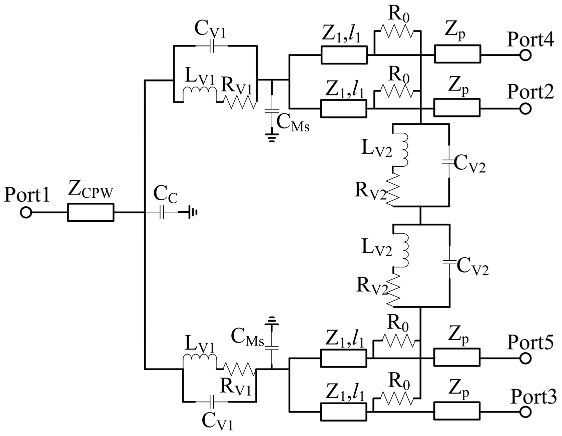


FIGURE 3. Equivalent circuit of the designed four-way power divider.

and

$$R_{V_1}=\left(\frac{\alpha_3 h}{\sigma\left[r_{v1}^2-(r_{v1}-\delta)^2\right]}-\frac{h}{\sigma\pi r_{v1}^2}\right)\sqrt{\frac{f}{f_{1GHz}}}+\frac{h}{\sigma\pi r_{v1}^2} \tag{5}$$

$$R_{V2}=\left(\frac{\alpha_4 h}{\sigma\left[r_{v2}^2-(r_{v2}-\delta)^2\right]}-\frac{h}{\sigma\pi r_{v2}^2}\right)\sqrt{\frac{f}{f_{1GHz}}}+\frac{h}{\sigma\pi r_{v2}^2} \tag{6}$$

where σ is the conductivity and f is the operating frequency, δ is the skin depth and α_3, α_4 are the fitting parameters, which are

$$\delta=\frac{1}{\sqrt{\pi f \mu_0 \sigma}}$$
$$\alpha_3=2.358\,(2\,r_{v1})^{0.283}\ln\left(\frac{h}{2\,r_{v1}}\right)+0.06\,(2\,r_{v1})^{-0.269}$$
$$\alpha_4=2.358\,(2\,r_{v2})^{0.283}\ln\left(\frac{h}{2\,r_{v2}}\right)+0.06\,(2\,r_{v2})^{-0.269}$$

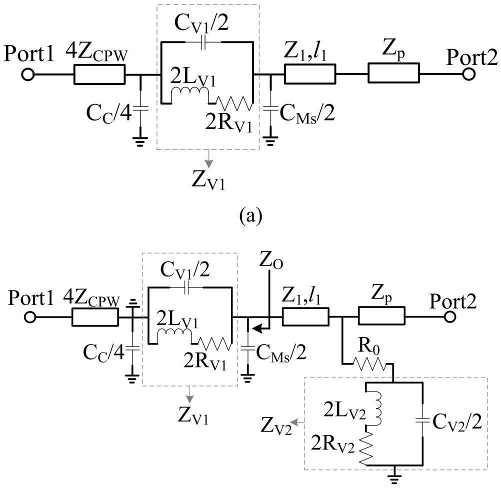
C_C and C_{Ms} is the equivalent capacitor [41], [42] of the open CPW and the stepped microstrip line, which can be given by

$$C_C=\frac{2\varepsilon}{\pi}\left\{(s+W_0)\left[\frac{\ln\left(\eta+\sqrt{1+\eta^2}\right)}{\eta}+\ln\left(\frac{1+\sqrt{1+\eta^2}}{\eta}\right)-\frac{1}{3}\left(\frac{1}{1+\sqrt{1+\eta^2}}+\frac{1}{\eta+\sqrt{1+\eta^2}}\right)\right]-\left(s+\frac{2}{3}W_0\right)\right\} \tag{7}$$

where $\eta=(r_1-r_2)/(s+W_0)$.

$$C_{M_s}\approx\left((10.11g\varepsilon_r+2.33)\frac{r_{v1}}{W_1}-12.6\lg\varepsilon_r-3.17\right)\sqrt{r_{v1}W_1} \tag{8}$$

where ε_r is the relative dielectric constant and the unit of C_{Ms} is pF.



(a)

(b)

FIGURE 4. Even- and Odd-mode equivalent circuits of the designed power divider. (a) Even-mode. (b) Odd-mode.

Fig. 4 shows the even- and odd-mode equivalent circuits of the proposed four-way power divider. Z_{V1} and Z_{V2} (shown in Fig. 4(a)) could be given by

$$\begin{aligned}Z_{v1}&=\frac{j\omega L_{v1}+R_{v1}}{1-\omega^2 C_{v1}L_{v_1}+j\omega C_{v1}R_{v1}}=R_{Z_{v1}}+jI_{z_{v1}}\\ R_{Z_{v_1}}&=\frac{R_{v_1}}{\left(1-\omega^2 C_{v_1}L_{v_1}\right)^2+\omega^2 C_{v_1}^2 R_{v_1}^2}\\ I_{Z_{v1}}&=\frac{\omega L_{v1}\left(1-\omega^2 C_{v1}L_{v_1}\right)-\omega C_{v1}R_{v1}^2}{\left(1-\omega^2 C_{v_1}L_{v_1}\right)^2+\omega^2 C_{v1}^2 R_{v1}^2}\end{aligned} \tag{9}$$

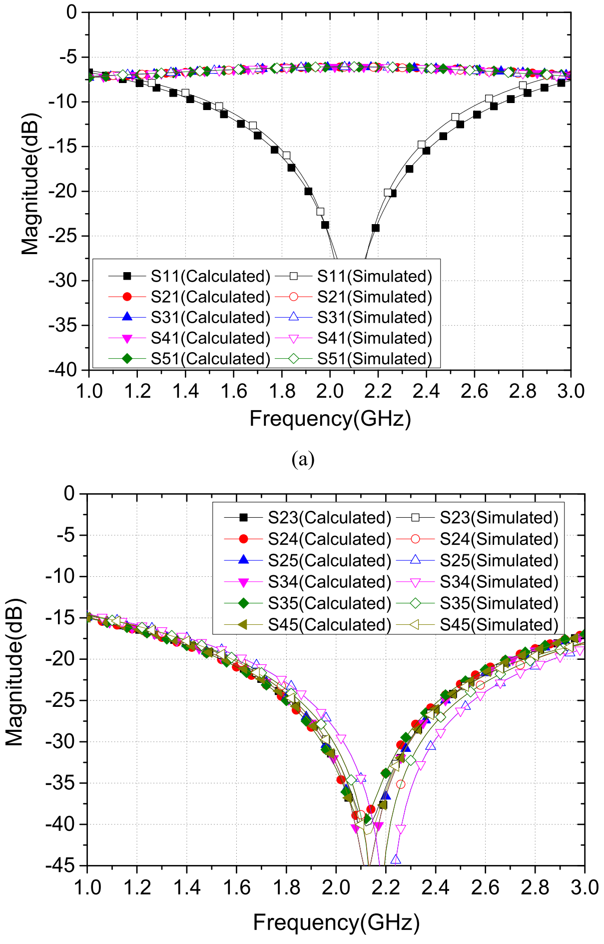
$$\begin{aligned}Z_{v2}&=\frac{j\omega L_{v2}+R_{v2}}{1-\omega^2 C_{v2}L_{v2}+j\omega C_{v2}R_{v2}}=R_{Z_{v2}}+jI_{Z_{v2}}\\ R_{Z_{v_2}}&=\frac{R_{v2}}{\left(1-\omega^2 C_{v2}L_{v2}\right)^2+\omega^2 C_{v2}^2 R_{v2}^2}\\ I_{Z_{v2}}&=\frac{\omega L_{v2}\left(1-\omega^2 C_{v2}L_{v2}\right)-\omega C_{v2}R_{v2}^2}{\left(1-\omega^2 C_{v2}L_{v2}\right)^2+\omega^2 C_{v2}^2 R_{v2}^2}\end{aligned} \tag{10}$$

where $\omega=2\pi f$. According to the even-mode circuit shown in Fig. 4(a), there will be

$$Z_{CPW}\approx\frac{Z_E}{j\omega Z_E C_C+4} \tag{11}$$

where

$$Z_E=\frac{4\,Z_1^2 Z_p-j2\omega Z_1^4 C_{MS}}{4\,Z_p^2+\omega^2 Z_1^4 C_{Ms}^2}+R_{Z_{v1}}+\mathrm{j}I_{Z_{v1}}=R_{Z_E}+jI_{Z_E}$$



(a)

(b)

FIGURE 5. Calculated and simulated frequency responses of the proposed power divider (Taconic RF-35, h = 0.508 mm, $\varepsilon_r = 3.5$, $l_1 = 22.1$ mm, s = 0.13 mm, $W_0 = 1.46$ mm, $W_1 = 0.23$ mm, $R_0 = 51\,\Omega$, $C_{V1} = 97.4$ fF, $C_{V2} = 58.4$ fF, $C_{Ms} = 4.7$ fF, $C_C = 73$ fF, $L_{V1} = 27.9$ pH, $L_{V2} = 23.5$ pH, $R_{V1} = 0.43$ mΩ, $R_{V2} = 1.77$ mΩ and $W_p = 1.14$ mm). (a) S-parameter. (b) Isolation between the output ports.

$$R_{Z_E} = \frac{4\,Z_1^2 Z_p}{4\,Z_p^2 + \omega^2 Z_1^4 C_{Ms}^2} + R_{z_{v1}}$$

$$I_{Z_E} = \mathrm{I}_{Z_{v1}} - \frac{2\omega Z_1^4 C_{Ms}}{4Z_p^2 + \omega^2 Z_1^4 C_{Ms}^2} \tag{12}$$

Through the odd-mode circuit shown in Fig. 4(b), the isolation resistor R_0 could be derived by

$$Z_p \approx \frac{Z_1^2\,(R_0 + Z_{v2})}{Z_1^2 + Z_O R_0 + Z_o Z_{v2}} \tag{13}$$

where

$$Z_O = \frac{4R_{z_{v1}} + j\left(4I_{z_{v1}} - 2\omega R_{z_{v1}}^2 C_{Ms} - 2\omega I_{z_{v1}}^2 C_{Ms}\right)}{\left(2 - \omega I_{z_{v1}} C_{Ms}\right)^2 + \omega^2 R_{z_{v1}}^2 C_{Ms}^2} = R_{Z_o} + jI_{ZO}$$

$$R_{Z_O} = \frac{4R_{V1}}{\left(2 - \omega I_{Z_{v1}} C_{Ms}\right)^2 + \omega^2 R_{z_{v1}}^2 C_{Ms}^2}$$

$$I_{z_o} = \frac{4I_{z_{v1}} - 2\omega R_{z_{v1}}^2 C_{Ms} - 2\omega I_{z_{v1}}^2 C_{Ms}}{\left(2 - \omega I_{z_{v1}} C_{Ms}\right)^2 + \omega^2 R_{z_{v1}}^2 C_{Ms}^2} \tag{14}$$

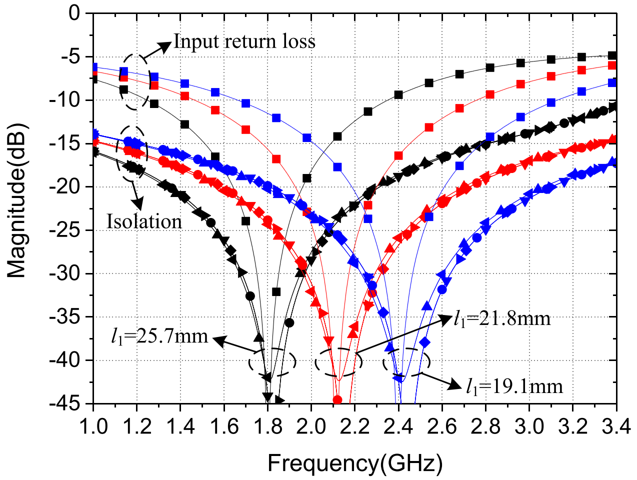


FIGURE 6. Calculated results of the proposed power divider according to the given equivalent circuit at different values of l_1.

According to equation (11)-(13), there will be

$$Z_{CPW} \approx \frac{R_{Z_E}\left(4 - \omega I_{Z_E} C_C\right) + \omega R_{Z_E} I_{Z_E} C_C}{\left(4 - \omega I_{Z_E} C_C\right)^2 + \left(\omega R_{Z_E} C_C\right)^2} \tag{15}$$

$$R_0 \approx \frac{Z_1^2 Z_p + Z_p R_{z_o} R_{Z_{v2}} - Z_p I_{Z_o} I_{Z_{v2}} - Z_1^2 R_{Z_{v2}}}{Z_1^2 - Z_p R_{Z_O}} \tag{16}$$

Thus, the initial size and the value of the isolation resistors of the proposed power divider could be easily got according to above analyses. Through (1)-(8), the calculated values of the capacitors, inductors and resistor are found to be (as illustrated in Fig. 3) $\mathrm{C_{V1}} = 97.4$ fF, $\mathrm{C_{V2}} = 58.4$ fF, $\mathrm{C_C} = 73$ fF, $\mathrm{C_{Ms}} = 4.7$ fF, $\mathrm{L_{V1}} = 27.9$ pH, $\mathrm{L_{V2}} = 23.5$ pH, $\mathrm{R_{V1}} = 0.43$ mΩ and $\mathrm{R_{V2}} = 1.77$ mΩ. From the above analysis, the presented power divider can be designed as follows:

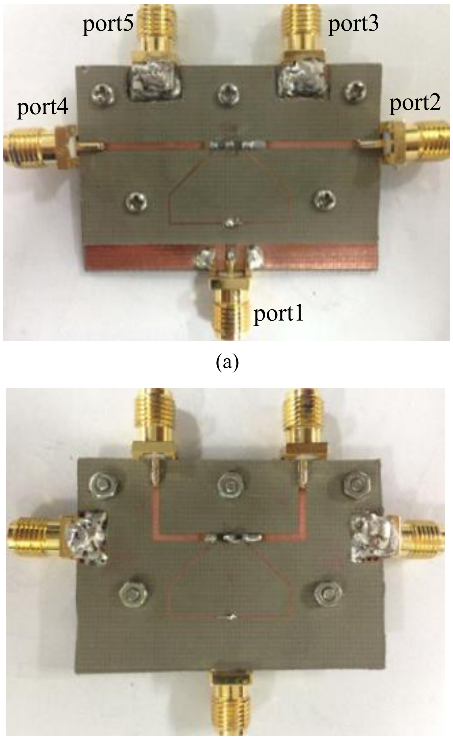
1) When substrate is chosen, the wavelength of microstrip line λ_m can be got by desired frequency f_0. Thus, the value of l_1, W_0, W_p and s could be got.

2) Analyzing parasitic parameters brought by metal vias and giving parasitic parameter expression like (1)-(8).

3) According to (1)-(12), the equivalent parameters brought by the metal vias can be accurately expressed. Thus, the size of the metal via could be determined to make the parasitic parameters small.

4) Analyzing circuits of odd mode and even mode. According to (13) and (15)-(16), the value of the isolation resistor R_0 and the impedance Z_1 can be determined.

The calculated and simulated S parameters (including the input return loss, insertion loss, and isolation between outports) are shown in Fig.5. The calculated results are from the above equivalent circuit, while the simulated ones are get by using HFSS. The calculation and simulation results are in good agreement with each other. The operating frequency bandwidth can be increased by adding wideband input matching circuit or increasing λm/4 impedance transition between the input and output ports. Fig. 6 gives the calculated



(a)

(b)

FIGURE 7. **Photograph of the power divider. (a) Top view. (b) Bottom view.**

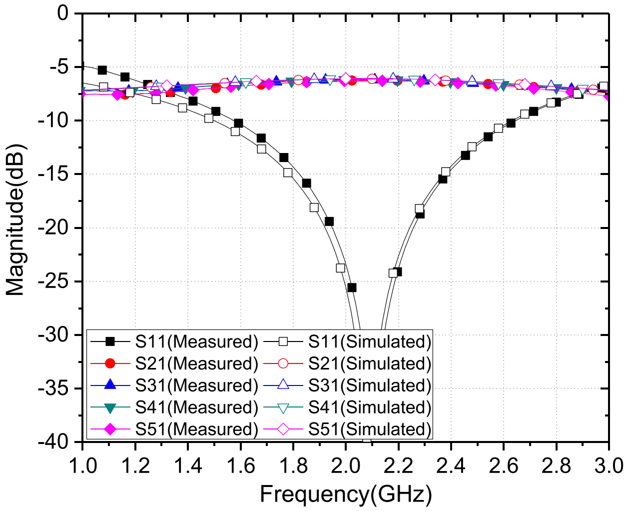


FIGURE 8. **Simulated and measured S parameters of the fabricated power divider.**

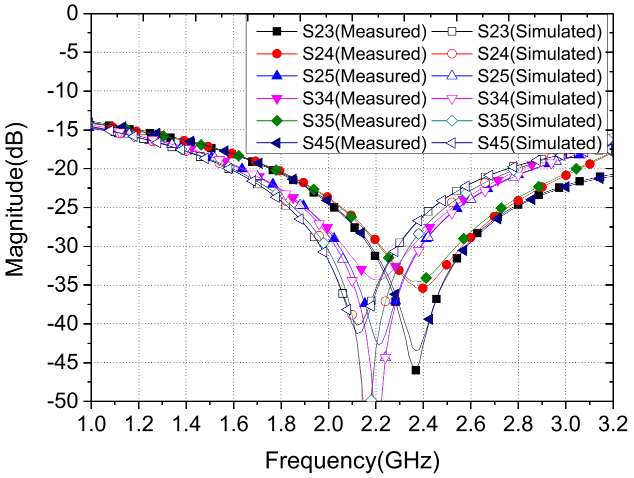


FIGURE 9. **Simulated and measured isolation of the power divider.**

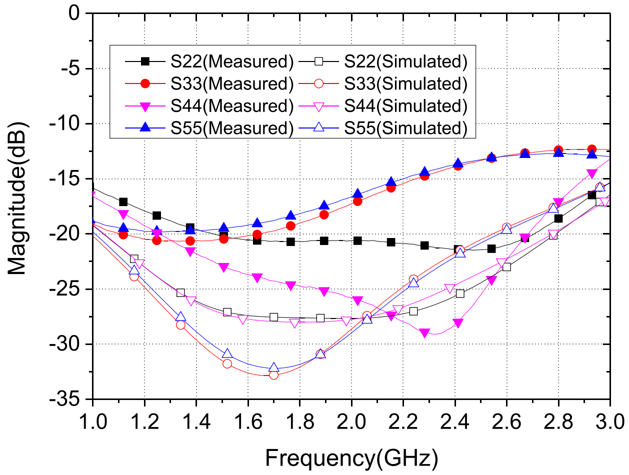


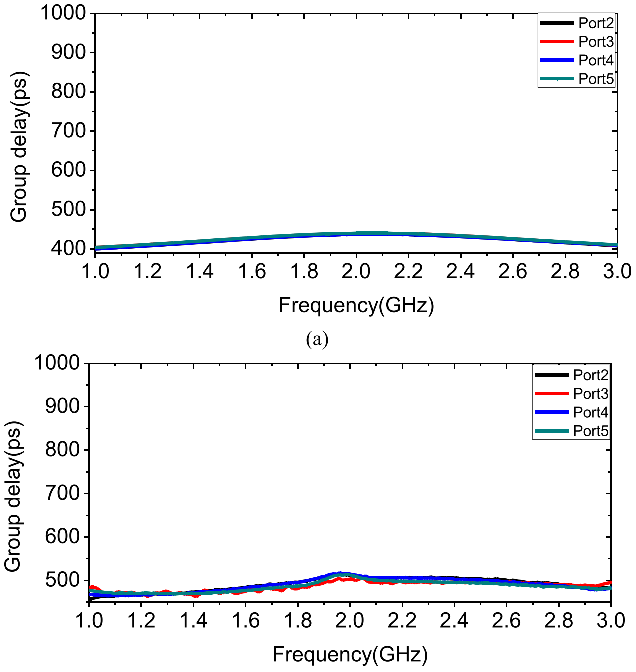
FIGURE 10. **Comparison of simulated and measured output return loss.**

results of the proposed power divider according to the given equivalent circuit at different values of l_1.

III. SIMULATION AND MEASURED RESULTS

Through the previous analysis, a four-way high isolation power divider/combiner is designed and fabricated with a two-layer substrate Taconic RF-35. The related parameters of this substrate are as follows: dielectric constant ε_r of 3.5, a thickness of 0.508 mm, and a loss tangent of 0.0018. The structure is optimized in Ansys-HFSS. The optimized dimensions shown in Fig.1 are: $l_1 = 23.5$ mm, $s = 0.13$ mm, $W_0 = 1.46$ mm, $W_1 = 0.3$ mm, $R_0 = 50\ \Omega$, and $W_p = 1.14$ mm. Fig. 7 gives the fabricated high isolation four-way power divider. All the ports are connected by the type-SMA connectors.

The simulated and measured results of the S-parameters are given in Fig. 8 to Fig. 12. It can be seen that the measured results agree well with the simulation ones within the operating frequency range. The measured input return loss is greater than 15dB within the frequency range of 1.8 to 2.4GHz, while that is greater than 20 dB within the frequency range 1.9 to 2.2GHz, as shown in Fig. 8. The measured insertion losses are about 6.13 ± 0.1 dB from 1.8 to 2.35 GHz, which also includes the transition loss of the SMA connector to microstrip line. The comparison of the measured and simulated results of the isolation between the four output ports are shown in Fig. 9. The measured isolations are all greater



(a)

(b)

FIGURE 11. **Measured and simulated group delay. (a) Simulated results. (b) Measured results.**

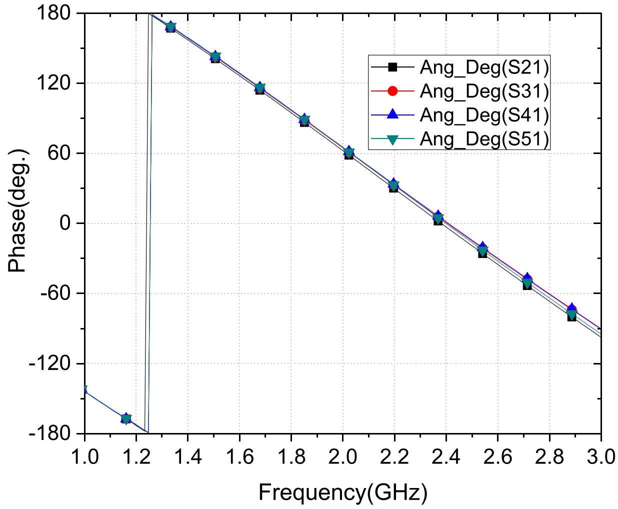


FIGURE 12. **Measured phase of the output ports.**

than 15 dB over the frequency from 1.1 to 3.2 GHz, while the isolations are all greater than 32 dB at 2.3 GHz. The measured 20-dB relative isolation bandwidth between the output ports is about 58%. Fig. 10 gives the measured and simulated output return loss. The simulated output return losses are greater 20dB from 1 to 2.4 GHz, which illustrates a good output impedance matching, while the measured output return loss are greater than 14dB. The decreased output return loss may be due to the processing and assembly deviation. The simulated and measured group delays are also shown in Fig. 11. Their results agree closely with each other. Fig. 12 gives the measured phase at each output ports It can be seen that the proposed power divider has a good phase balance.

TABLE 1. **Comparison with other four-port power divider.**

	Center Frequency (GHz)	20dB Isolation RBW	Size ($\lambda_g\times\lambda_g$)	Insertion loss(dB)
Ref.[16]	9.3	None	0.62×2.58	7±0.5
Ref.[17]	35.5	None	Not given	6.2±0.3
Ref.[24]	1.5	13.3%	Not given	6.29±0.2
Ref.[30]	1.0	35.3%	0.46×0.46	6.15±0.5
Ref.[32]	2.1	17.5%	0.36×0.38	6.2±0.1
Ref.[33]	6.9	None	0.52×0.54	6.8±0.4
Ref.[34]	2.0	24.4%	0.17×0.31	6.35±0.2
Ref[36]	1.5	None	0.54×0.45	6.19±0.5
Ref[37]	1.05	65%	Not given	7±0.5
Ref[38]	9.75	None	Not given	6.5±0.15
This work	2.1	58%	0.17×0.22	6.13±0.1

RBW: relative bandwidth. None: isolations less than 20dB

Table 1 shows the comparison with previous research work about the planar four-port power dividers. It can be seen that the power divider presented in this paper has the advantage of the compact size, low insertion loss, and wide and high output isolation.

IV. CONCLUSION

In this paper, a compact quasi-planar four-way high isolation power divider has been presented. The structure of two-layer CPW-microstrip transition has been used to imply the isolation circuit. To analyze the proposed power divider, the equivalent circuit has been used. The measured results of the novel four-way power divider consistent with the simulated ones closely. From the measured results, many advantages of this proposed power dividers can be summarized as follows: low insertion loss, excellent impedance matching, good balance of amplitude and phase at the output ports, and high isolation among the output ports.

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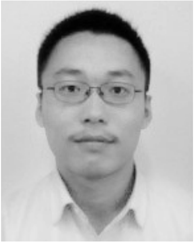

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