IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received April 26, 2019, accepted May 17, 2019, date of publication May 22, 2019, date of current version June 26, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2918187

A Large-Signal Model for Two-Dimensional Hole Gas Diamond MOSFET Based on the QPZD

YU FU[1], RUIMIN XU[1], (Member, IEEE), JIANJUN ZHOU[2], XINXIN YU[2], ZHANG WEN[3], YUECHAN KONG[2], TANGSHENG CHEN[2], YONG ZHANG[1], (Senior Member, IEEE), BO YAN[1], JIJUN HE[4], AND YUEHANG XU[1], (Senior Member, IEEE)

[1]Department of Microwave Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China
[2]Nanjing Electronic Devices Institute, Nanjing 210016, China
[3]Microsystem and Terahertz Research Center, China Academy of Engineering Physics, Chengdu 610200, China
[4]Chongqing Chang'an Industry Group Co., Ltd., Chongqing 401120, China

Corresponding author: Yuehang Xu (yuehangxu@uestc.edu.cn)

ABSTRACT A compact large-signal model for hydrogen-terminated (C–H) diamond metal-oxide field effect transistors (MOSFETs) is presented based on an improved quasi-physical zone division (QPZD) model. Unlike the conventional QPZD model for the AlGaN/GaN high-electron-mobility transistors (HEMTs), the linear-mode current-voltage (I-V) model of the diamond FET is analytically deduced with an improved velocity-electric field relation and temperature-dependent effective hole mobility $\mu_{\rm eff}(T)$. The I–V model can directly demonstrate the relation between the negative $V_{\rm ds}$ and the negative $I_{\rm ds}$ of the p-type diamond FETs, which cannot be achieved by the conventional QPZD model. Finally, the proposed model has been verified by the on-wafer measurements of an in-house 2×500 μm diamond FET. The good consistency shows that the presented compact large-signal model can accurately predict the DC I-V, multibias scattering-parameters (S-parameters), and large-signal performances. The results of this paper will be useful for the microwave diamond-based transistor and circuit designs.

INDEX TERMS Diamond MOSFET, zone division, thermal resistance, current-voltage model, large-signal model.

I. INTRODUCTION

Diamond is a type of ultrawide bandgap semiconductor material with high thermal conductivity, high breakdown field, and high room temperature intrinsic drift mobility, which is 4500 $cm^2/(V{\cdot}s)$ for electrons and 3800 $cm^2/(V{\cdot}s)$ for holes [1]. It is difficult for conventional dopants to achieve effective doping in diamond because of their high activation energy, especially effective n-type doping [2]. Lateral MOSFETs based on the oxygen-terminated boron-doped diamond display excellent switching characteristics, although they exhibit a relatively low current density [3]. In the last two decades, C-H diamond FETs have shown good properties in power electronics [4] and radio-frequency (RF) applications [5]. For this type of diamond device, $f_{\rm T} = 70$ GHz and $f_{\rm MAX} = 80$ GHz were achieved [6]. The highest output power reported was 3.8 W/mm at 1 GHz with a gain of 11.6 dB and a power-added efficiency (PAE) of 23.1 % [7]. In addition, some theories and experiments have shown that electrons transfer from the C-H diamond: hydrogen side to the surface adsorbates after the hydrogenation treatment on the surface of diamond [8], [9]. Therefore, a two-dimensional hole gas layer (2DHG) is formed near the diamond surface [10]. As a result, a similar modeling method to AlGaN/GaN HEMTs can be expanded to the diamond FETs. Due to the fast development of diamond FETs, it is time to develop a compact large-signal model for the perspective microwave circuits.

V. Camarchia *et al.* reported a large-signal model for C-H diamond MESFETs, which is completely based on the empirical Angelov model [11]. Although high accuracy can be achieved, the empirical model contains dozens of fitting parameters and hardly demonstrates the unique operation mechanism of this transistor. Recently, physics-based transistor models such as the surface potential (SP)-based [12], [13], charge-based [14], and zone division (ZD)-based models [15], [16] have been highly attractive. They have shown the advantages of much fewer empirical parameters and links to the transistor's mechanisms.

The associate editor coordinating the review of this manuscript and approving it for publication was Andrei Muller.

However, to the best knowledge of the authors, a compact model that corresponds to the actual operation mechanisms of C-H diamond MOSFETs has not been reported.

Compared with other physics-based models, the emerging QPZD large-signal model for AlGaN/GaN HEMTs shows much fewer fitting parameters [17]. This advantage enables fast parameter extraction and better convergence at the cost of fewer links to the physical mechanisms. In the ZD [15] and QPZD [17] models, the deduction of the current-voltage model originates from the smooth velocity-electric field relation, which is given by

$$v = \frac{\mu E}{\sqrt[p]{1 + (E/E_c)^p}} \tag{1}$$

where p is an empirical parameter, μ is the constant low-field mobility, and E_c is the critical electric field that marks the onset of the high-field region. For the C-H diamond FETs with the surface channel, the carrier mobility suffers from various scattering mechanisms [18], so the mobility exhibits a strong gate voltage dependence [19]. As a result, for the compact modeling of diamond FETs in this work, the gate-bias dependence of the effective hole mobility and the critical electric field are considered. In addition, the conventional QPZD model extracts the model parameters empirically instead of by the quasi-physical insights, which limits its application in developing the new devices.

In this paper, the C-H diamond MOSFET was fabricated in house, as shown in Section II. Based on the improved QPZD method, the current model is derived in Section III. The model parameter extraction is shown in Section IV. In Section V, for verification, the simulated and measured results are compared, including the DC I-V, multibias S-parameters, and large-signal power sweep characteristics. Finally, Section VI is the conclusion.

II. DEVICE FABRICATION

The C-H diamond MOSFET was fabricated on 5 × 5 × 0.5 mm^3 CVD single-crystal (100) commercial diamond substrates. The detailed fabrication process is identical to that of [6], and a 2DHG channel layer with high concentration was formed very close to the diamond surface. The homoepitaxial diamond layer featured a thickness of 0.5 μm and was unintentionally boron-doped to a level of approximately 5 × 10^{16} cm^{-3}. The Al_2O_3 gate oxide was 20 nm thick. The gate length L_g and total gate width W_g of the fabricated device were 0.5 μm and 1 mm (2 × 500 μm), respectively. The gate-source access distance L_s and gate-drain access distance L_d were both 0.2 μm. The optical microscope image of the fabricated device is shown in Fig. 1. Due to the large activation energies of p-type boron dopants (0.37 eV), the results of the Hall effect measurement indicate that the activation fraction of boron as the acceptor in diamond is extremely low at room temperature [20]. As a result, the C-H diamond MOSFET with a highly conductive 2DHG layer has a higher maximum current than the boron-doped diamond MOSFET by 1-2 orders of magnitude [21]. The

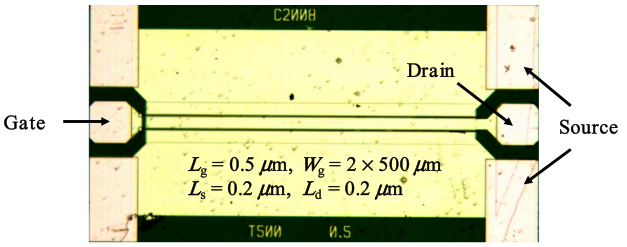


FIGURE 1. Optical microscope image of the fabricated C-H diamond MOSFET.

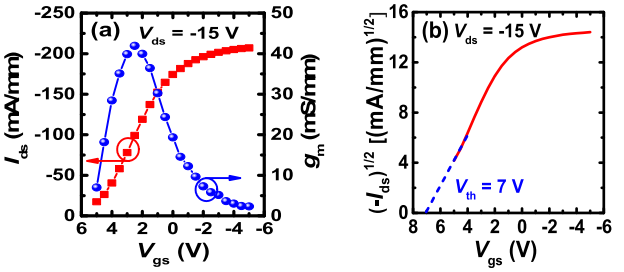


FIGURE 2. (a) Experimental transfer characteristics of the C-H diamond MOSFET at $V_{ds} = -15$ V, and (b) extraction of the threshold voltage by the second-derivative method at the saturation drain voltage $V_{ds} = -15$ V; the threshold voltage V_{th} is 7 V.

presence of boron does not significantly affect the output current, so this paper assumes that only the 2DHG channel exists in the C-H diamond MOSFET.

Fig. 2(a) shows the experimental transfer characteristics of the device. The drain current I_{ds} gradually saturates at a high negative gate voltage, and the maximum current density is only − 206 mA/mm. The typical bell-shaped transconductance (g_m) as a function of the gate voltage (V_{gs}) is observed, which may be correlated to the saturation of channel hole density or the effective hole mobility degradation [22]. The specific evaluation of such physical mechanisms and their effective influence on the device performance requires further research. The threshold voltage is extracted using the second-derivative method at saturated operation ($V_{ds} = -15$ V) [23], [24]. Fig. 2(b) shows that the threshold voltage (V_{th}) extracted from the $|-I_{ds}|^{1/2}$ vs. V_{gs} relation is 7 V, which is relatively high [25]. The extracted V_{th} is the foundation to determine the critical saturation current I_{dsat} at each V_{gs}, which is demonstrated in Section IV.

III. CURRENT MODEL

The current model is essential to the compact large-signal modeling. It is deduced in the linear- and saturated-operation modes. The complete model flowchart is demonstrated in Fig. 3.

A. LINEAR-MODE MODEL DESCRIPTION

Based on our previous TCAD simulation work [10], the physics-based simulation for the modeled device is performed using the TCAD tool-SILVACO. Fig. 4 shows the hole concentration and lateral electric field along the channel with

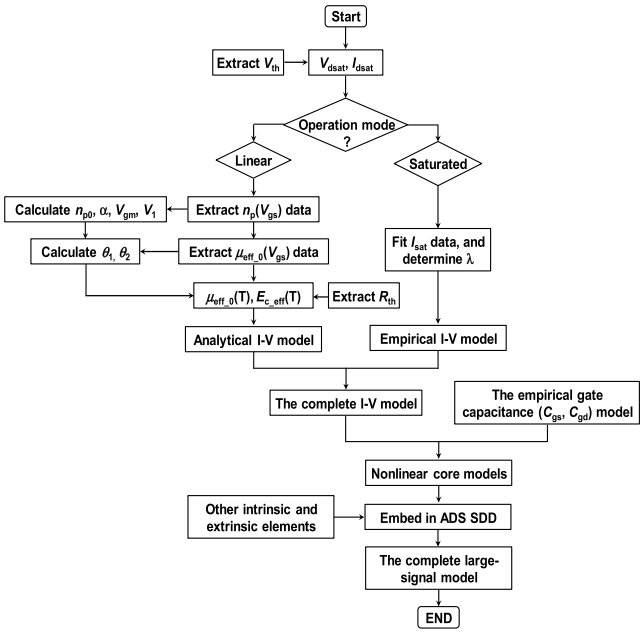


FIGURE 3. Flowchart of the large-signal model for C-H diamond MOSFETs.

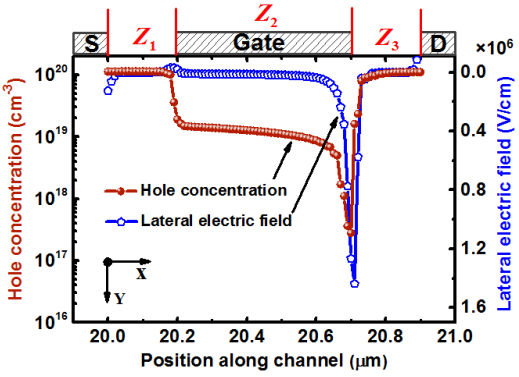


FIGURE 4. Hole concentration and lateral electric field along the channel with 0.4 nm beneath the diamond surface at $V_{gs} = 0$ V and $V_{ds} = -4$ V; the simulation was conducted in TCAD SILVACO.

0.4 nm beneath the diamond surface, which is conducted in the linear-mode bias condition ($V_{gs} = 0$ V, $V_{ds} = -4$ V), and the three-zone frame is clearly observed. In the access regions, the holes in the conduction path do not have control of the gate voltage, and the quantum wells at the diamond surface are full of holes. As a result, the hole concentration and lateral electric field E in the access regions are almost constant, and the voltage linearly drops. In contrast, E varies with the lateral position under the gate region.

The corresponding schematic diagram of the three-zone division method for the linear-mode I-V model is shown in Fig. 5. Specifically, the zones from the source to the drain are denoted as the source access zone (Z_1), intrinsic FET zone beneath the gate (Z_2), and drain access zone (Z_3). The linear-mode I-V model contains the core current model and boundary conditions. The core current model originates from the carrier transport performance in the intrinsic

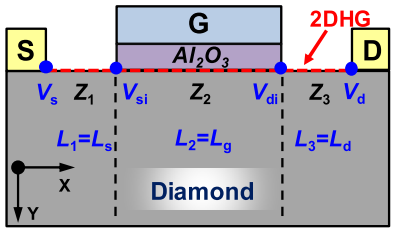


FIGURE 5. Schematic diagram of the three-zone division model for the diamond MOSFETs operating in the linear mode. Z_2 is the intrinsic FET zone. Z_1 and Z_3 are the source and drain access zones, respectively. The core current model is deduced in Z_2, and the boundary conditions are deduced in Z_1 and Z_3.

FET zone (Z_2), and the boundary conditions (V_{si}, V_{di}) are deduced from the velocity-electric field relationship in the access zones (Z_1, Z_3).

According to the Time of Flight (TOF) mobility measurement [26], Eqn. (1) with p = 1 can best reproduce the velocity-electric field data of diamond. Hence, a more precise velocity-field model, which was proposed for Si-based MOS devices, is adopted in this work [27]

$$\begin{aligned} v &= \frac{\mu_{\text{eff}} E}{1 + E/E_{c\_\text{eff}}} \quad E \le E_{c\_\text{eff}} \\ &= v_{\text{sat}} \quad E > E_{c\_\text{eff}} \end{aligned} \tag{2}$$

where μ_{eff} is the effective hole mobility that models the degradation of the mobility due to the vertical electric field [28], and E_{c_eff} is the critical electric field at which the carrier velocity is saturated and is equal to $2v_{\text{sat}}/\mu_{\text{eff}}$. For the C-H diamond FETs with the 2DHG conduction channel, the drain current I_{ds} can be written as

$$I_{\text{ds}} = W\,(-q)\,n_{\text{p}}\,(x)\,v\,(x) \tag{3}$$

where W is the total gate width,q is the elementary charge, $n_{\text{p}}(x)$ is the density of holes in the 2DHG channel, and $v(x)$ is the velocity of the carriers in the channel. In the linear-mode, the gradual channel approximation (GCA) is valid in Z_2 [15]; n_{p} can be given by

$$n_{\text{p}} = \frac{C_{\text{ox}}}{q}\left[V_{\text{gt}} - V\,(x)\right] \tag{4}$$

where C_{ox} is the gate oxide capacitance per unit area ($C_{\text{ox}} = \varepsilon_{\text{ox}}\varepsilon_0/d_{\text{ox}}$), ε_{ox} is the relative permittivity of Al_2O_3 with the value of 7.4 [29], $V(x)$ is the potential in the 2DHG channel, and $V_{\text{gt}} = V_{\text{gs}} - V_{\text{th}}$. In the intrinsic FET zone Z_2, substituting the field-potential relation $E(\text{x}) = -\,dV(\text{x})/dx$ into Eqn. (2) and simultaneously solving Eqns. (2)-(4), we obtain

$$L_{\text{g}} I_{\text{ds}} = \left(\beta V_{\text{gt}} + I_{\text{ds}}/E_{c\_\text{eff}}\right)(V_{\text{di}} - V_{\text{si}}) - \beta\left(V_{\text{di}}^2 - V_{\text{si}}^2\right)/2 \tag{5}$$

where L_{g} is the gate length, $\beta = WC_{\text{ox}}\mu_{\text{eff}}$, V_{si} is the potential at the source-side gate edge, and V_{di} is the potential at the drain-side gate edge. In the source and drain access zones, the quantum wells of the C-H diamond/adsorbates heterojunction are filled with holes, and the lateral electric field can be deduced from Eqn. (2). According to the velocity-electric

field relation in Eqn. (2) and assuming that I_{ds} is equal to I_{dsat} when $v = v_{sat}$, the lateral electric field E in Z_1 and Z_3 can be written as

$$E = \frac{I_{ds}E_{c\_eff}}{2I_{dsat} - I_{ds}} \tag{6}$$

which implies

$$V_{si} = \frac{I_{ds}E_{c\_eff}L_s}{I_{ds} - 2I_{dsat}} \tag{7}$$

$$V_{di} = V_{ds} - \frac{I_{ds}E_{c\_eff}L_d}{I_{ds} - 2I_{dsat}} \tag{8}$$

where L_s is the length of Z_1, and L_d is the length of Z_3. Substituting the boundary conditions Eqns. (7)-(8) into Eqn. (5) and considering that $V_{di} + V_{si}$ is equal to V_{ds} since L_s is equal to L_d for the modeled device, we can write Eqn. (5) as

$$\begin{aligned} 0 = {} & L_g I_{ds}\left(I_{ds} - 2I_{dsat}\right) + \left[\beta\left(V_{ds}/2 - V_{gt}\right) - I_{ds}/E_{c\_eff}\right] \\ & \times \left[V_{ds}\left(I_{ds} - 2I_{dsat}\right) - E_{c\_eff}I_{ds}\left(L_s + L_d\right)\right] \end{aligned} \tag{9}$$

To simplify the complexity of the model without sacrificing much accuracy, the term $(I_{ds}/E_{c\_eff})\times[V_{ds}(I_{ds}\text{-}2I_{dsat})\text{-}E_{c\_eff}I_{ds}(L_s + L_d)]$ in Eqn. (9) can be ignored since its value is much smaller than the other terms. Based on this simplification, we obtain

$$\begin{aligned} 0 = {} & L_g I_{ds}^2 + \left\{\beta\left(V_{ds}/2 - V_{gt}\right)\left[V_{ds} - E_{c\_eff}\left(L_s + L_d\right)\right]\right. \\ & \left. -2L_g I_{dsat}\right\} I_{ds} - 2\beta I_{dsat}V_{ds}\left(V_{ds}/2 - V_{gt}\right) \end{aligned} \tag{10}$$

(V_{dsat}, I_{dsat}) is the dividing point of the linear region and the saturated region on I-V characteristics, and I_{ds} is proportional to V_{ds} in the linear region ($|V_{ds}| < |V_{dsat}|$). Thus, we obtain

$$\frac{I_{ds}}{V_{ds}} \approx \frac{I_{dsat}}{V_{dsat}} \tag{11}$$

Substituting Eqn. (11) into Eqn. (10), we obtain a linear equation of I_{ds}. Eventually, the linear-mode I-V model can be written as

$$I_{ds} = \frac{\beta\left(V_{gt} - V_{ds}/2\right)\left[V_{ds} - 2V_{dsat} - E_{c\_eff}(L_s + L_d)\right] + 2L_g I_{dsat}}{L_g} \tag{12}$$

The characterization and modeling of V_{dsat}, I_{dsat}, μ_{eff}, and E_{c_eff} are demonstrated in Section IV.

B. SATURATED-MODE MODEL DESCRIPTION

In the saturated-mode, a charge deficit zone will appear at the drain-side gate edge [30]. The gradual channel approximation is valid only in part of the entire intrinsic FET zone (Z_2) [31]; therefore, the current model developed from the linear-mode is difficult to expand to the saturation cases from physical insights. The following empirical saturated-mode I-V equation is introduced in this work [12], which can largely simplify the I-V model

$$I_{sat} = I_{dsat}\left[1 - \lambda\left(V_{ds} - V_{dsat}\right)\right] \tag{13}$$

TABLE 1. List of I-V model parameters.

Parameter	Description	Value
V_{th} (V)	Threshold voltage	7
W (m)	Total gate widths	1×10^{-3}
L_g (m)	Gate length	5×10^{-7}
L_s (m)	Length of the source access region	2×10^{-7}
L_d (m)	Length of the drain access region	2×10^{-7}
d_{ox} (m)	Thickness of the gate-oxide Al_2O_3 layer	2×10^{-8}
v_{sat} (m/s)	Saturation velocity of diamond	6×10^{4}
ε_{ox}	Relative permittivity of Al_2O_3	7.4
n_{p0} (cm^{-2})	Maximum 2DHG density	2.05×10^{12}
α	Fitting parameter in the $n_p(V_{gs})$ relation	0.32
V_{gm} (V)	Inflection voltage point in the $n_p(V_{gs})$ relation	2.84
V_1 (V)	Slope coefficient of the $n_p(V_{gs})$ relation	-4.27
μ_0 ($cm^2/V\cdot s$)	Low-field mobility of boron-doped diamond	1800
θ_1 (1/V)	Mobility degradation coefficient first order	0.42
θ_2 ($1/V^2$)	Mobility degradation coefficient second order	0.66
R_{th} (°C/W)	The extracted thermal resistance	1.07
λ (V^{-1})	The fitting parameter in the saturation *I-V* model	0.03

where λ is a fitting parameter, and I_{dsat} is the critical saturation current when $V_{ds} = V_{dsat}$. This simple expression can ensure that I_{sat} is equal to I_{dsat} when V_{ds} is equal to V_{dsat}. The parameters and their values in the I-V model are summarized in Table 1.

IV. MODEL PARAMETER EXTRACTION

A. I-V MODEL PARAMETER EXTRACTION

For the C-H diamond MOSFETs with a 2DHG channel, the critical saturation drain current is

$$I_{dsat} = -Wqn_p v_{sat} \tag{14}$$

If an analytic or numerical expression, which describes the $n_p(V_{gs})$ relation, is proposed for diamond FETs, the analytic expression of $I_{dsat}(V_{gs})$ can be easily provided. However, the comprehensive understanding about the formation mechanism of the 2DHG channel in C-H diamond MOSFETs requires further research [22], [32]. Few theoretical calculation works have been reported about the density of state distribution at the surface of the H-terminated diamond [33]. To the best of our knowledge, the numerical calculation or analytic expression of the $n_p(V_{gs})$ relation, which originates from the physical mechanism, has not been reported.

In this work, the experimental I_{dsat} is extracted at V_{dsat} biasing at different V_{gs}, and V_{dsat} can be estimated by

$$V_{dsat} \approx V_{gs} - V_{th} \tag{15}$$

where V_{th} is the threshold voltage. This simple expression originates from the Si-based MOS devices [34] and assumes that the carrier velocity first saturates at the drain-side gate edge. According to the small-signal parameter extraction results in Part B, the extracted parasitic resistance R_g (13.9 Ω) is larger than R_d (3.43 Ω) and R_s (1 Ω), so the assumption Eqn. (15) is reasonable by omitting the effect of the drain

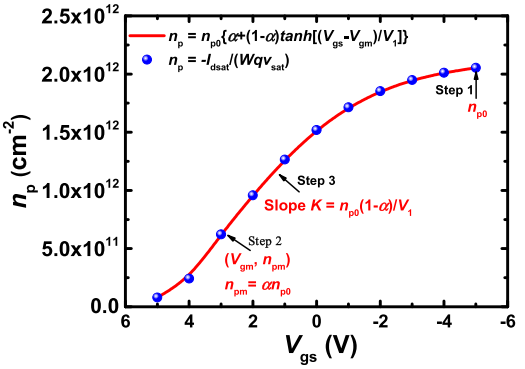


FIGURE 6. Hole sheet density n_p versus gate voltage V_{gs} for the C-H diamond MOSFET and its parameter extraction steps. Symbols: Extracted from the experimental saturation current I_{dsat} data. Curve: The unified analytic expression of the charge sheet density versus gate voltage considered in [35], where $n_{p0} = 2.05 \times 10^{12}$ cm^{-2}, $\alpha = 0.32$, $V_{gm} = 2.84$ V, and $V_1 = -4.27$ V.

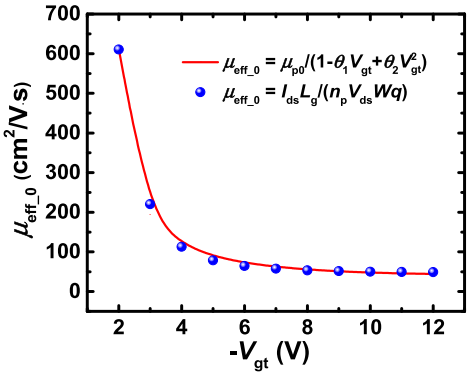


FIGURE 7. Extracted (symbols) and modeled (lines) effective hole mobility μ_{eff_0} for C-H diamond MOSFETs, where $\mu_0 = 1800$ cm^2/V·s, $\theta_1 = 0.42$, and $\theta_2 = 0.66$.

access resistance. Then, n_p is extracted based on Eqn. (14) as shown in Fig. 6. The channel hole density saturates at high negative gate voltage; the mechanism behind this phenomenon remains unclear and will not be discussed here. The following analytic expression is introduced to reproduce the $n_p(V_{gs})$ data, which has been used for MODFET devices [35]

$$n_p = n_{p0}\left\{\alpha + (1-\alpha)\, tanh\left[\left(V_{gs} - V_{gm}\right)/V_1\right]\right\} \quad (16)$$

where n_{p0} is the maximum 2DHG density; V_{gm} is the voltage of the inflection point (V_{gm}, n_{pm}), near which the curve can be approximated by its tangent; α is the fitting parameter; V_1 is the parameter correlated to the slope ($K = n_{p0}(1-\alpha)/V_1$) of the tangent at the inflection point. The parameter extraction details can be seen in [35]. Based on the analytic $n_p(V_{gs})$ relation, the critical saturation current I_{dsat} versus V_{gs} of the modeled device can be naturally obtained.

Based on the aforementioned extracted 2DHG density, the effective hole mobility can be derived from the DC transistor performance. At the small drain voltage ($V_{ds} = -0.5$ V was selected), the conductance between source and drain can be evaluated as [36]

$$G_{ds} = \frac{I_{ds}}{V_{ds}} = qn_p \frac{W}{L_g}\mu_{eff\_0} \quad (17)$$

where I_{ds} is the measured drain current, μ_{eff_0} is the effective hole mobility at room temperature T_0, n_p is the 2DHG density, W is the total gate width, and L_g is the gate length. Fig. 7 shows the extracted results of μ_{eff_0} as a function of -V_{gt}; the decrease in μ_{eff_0} can be attributed to the enhanced diamond-oxide interface Coulomb scattering or interface roughness scattering, since the centroid of the 2DHG shifts closer to the diamond surface when the 2DHG density increases [10], [19].

The 2DHG carrier mobility μ_{eff_0} is modeled by [37]

$$\mu_{eff\_0} = \mu_0 / \left(1 - \theta_1 V_{gt} + \theta_2 V_{gt}^2\right) \quad (18)$$

where μ_0 is the low-field carrier mobility with the value of 1800 cm^2/V·s for boron-doped diamond [38]; θ_1 and θ_2 are the fitting parameters that model the degradation of the carrier mobility due to the vertical field; $V_{gt} = V_{gs} - V_{th}$. For the boron-doped C-H diamond, the Hall effect measurement shows that the hole mobility versus temperature can be approximated by $\mu \propto T^{1.2}$ [39]. This positive relationship suggests that the temperature dependence of Hall mobility is due to the scattering of ionized impurities. Therefore, the temperature-dependent effective hole mobility is given by [40]

$$\mu_{eff}(T) = \mu_{eff\_0} \cdot (T/T_0)^{1.2} \quad (19)$$

Furthermore, the channel temperature increase in a device can be expressed as

$$T - T_0 = P_{diss} R_{th} \quad (20)$$

where T is the channel temperature, T_0 is the ambient temperature with the typical value of 25 °C, $P_{diss} = I_{ds} \times V_{ds}$ is the static dissipation power, and R_{th} is the thermal resistance of the device. This work uses the professional 3D-FEM simulation tool COMSOL to extract the thermal resistance instead of the 2D-like model in TCAD SILVACO. The gate fingers are equivalent to two linear heat sources. All geometry sizes set in the 3D thermal model are in accordance with the 2 × 500 μm diamond sample sizes. In addition, the carrier is set to the entire diamond substrate (5 × 5 × 0.5 mm^3) instead of the area of a single transistor. Because only the DUT is biased during the I-V measurement, the entire diamond substrate will transfer heat. The schematic cross-section picture of the simulation model is shown in Fig. 8(a). The surroundings are set to thermal insulation conditions, which are similar to our previous work [41]. The thermal conductivity of diamond is expressed as [42]

$$\kappa(T_L) = K_{300} \times (T/300)^{-1.02} \quad (21)$$

where K_{300} is the thermal conductivity at 300 K; T is the temperature; K_{300} is set to 22 W/cm·K [2]. Fig. 8(b) shows the established simulation model and thermal distribution of the entire diamond sample at $P_{diss} = 1$ W. The increase in temperature in diamond FETs is extremely low,

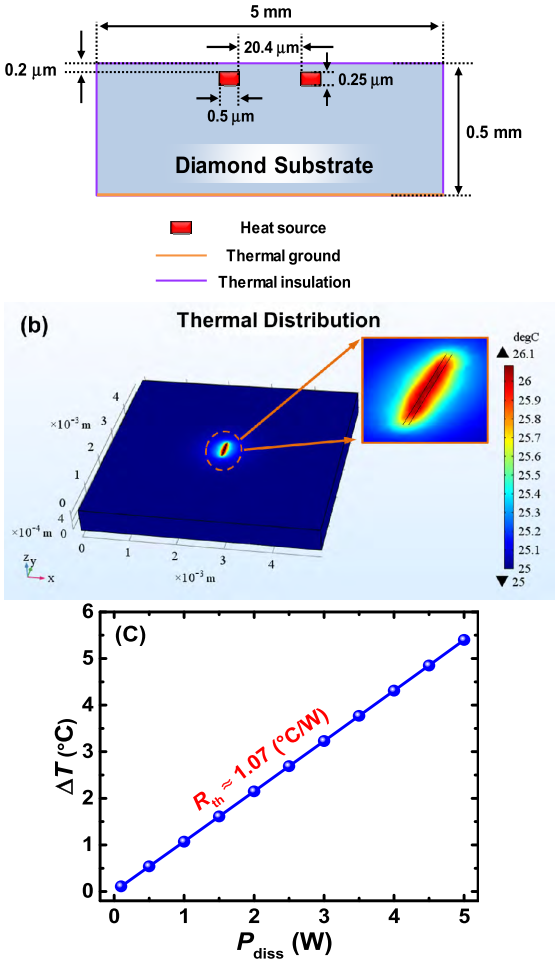


FIGURE 8. (a) Schematic cross-section picture of the simulation model, (b) simulation model built in the thermal simulator-COMSOL and thermal distribution of the entire diamond sample at P_{diss} = 1 W, (c) temperature increase ΔT of the device at different dissipation powers; the extracted thermal resistance R_{th} is approximately 1.07 °C/W.

which is actually reasonable due to the high thermal performance of diamond materials. The temperature increase ΔT of the device at different dissipation powers is shown in Fig. 8(c). The extracted thermal resistance $R_{\rm th}$ is approximately 1.07 °C/W, which is consistent with the thermograph measurement results in [43]. Finally, $E_{\rm c\_eff}$ can be correlated to $V_{\rm gs}$ and temperature T: $E_{\rm c\_eff} = 2v_{\rm sat}/\mu_{\rm eff}(T)$, where $v_{\rm sat}$ is considered with a constant value of 6×10^6 cm/s [32].

B. C-V MODEL PARAMETER EXTRACTION

The equivalent circuit parameters extraction is based on multibias S-parameter measurements up to 20 GHz [44], [45]. Parasitic pad capacitances and inductances were de-embedded using conventional open and short patterns fabricated on the same substrate [6]. The values of the extrinsic parasitic parameters are shown in Table 2, where $C_{\rm pga}$, $C_{\rm pda}$, and $C_{\rm gda}$ are the pad connection parasitic capacitances, and $l_{\rm g}$, $l_{\rm d}$, $l_{\rm s}$ and $R_{\rm g}$, $R_{\rm d}$, $R_{\rm s}$ are the parasitic inductances and resistances, respectively. The extracted extrinsic parasitic inductances and resistances values are higher than those

TABLE 2. List of extracted parasitic parameters.

Parameter	Value
$C_{\rm pga}$ (fF)	0.34
$C_{\rm pda}$ (fF)	0.34
$C_{\rm gda}$ (fF)	0.05
$l_{\rm g}$ (pH)	63.2
$l_{\rm d}$ (pH)	61
$l_{\rm s}$ (pH)	6
$R_{\rm g}$ (Ω)	13.9
$R_{\rm d}$ (Ω)	3.43
$R_{\rm s}$ (Ω)	1

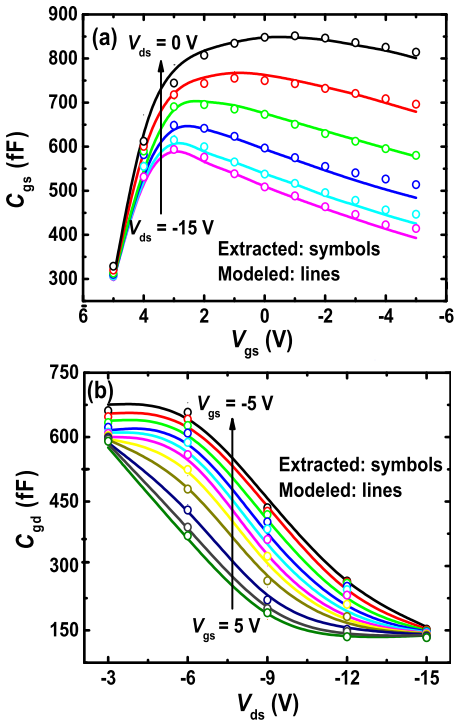


FIGURE 9. Comparison of the extracted (symbols) and modeled (lines) gate capacitance. (a) $C_{\rm gs}$ versus $V_{\rm gs}$ from $V_{\rm ds}$ = 0 V to − 15 V with − 3 V steps, and (b) $C_{\rm gd}$ versus $V_{\rm ds}$ from $V_{\rm gs}$ = −5 V to 5 V with 1 V steps.

of [5] due to the larger gate width device that we employed. Fig. 9 shows the extracted and modeled bias-dependent intrinsic parameters $C_{\rm gs}$ and $C_{\rm gd}$, and the C-V characteristics were modeled using the empirical Angelov model [46]. The obvious decrease in extracted $C_{\rm gs}$ at high negative gate voltage indicates the saturation of the 2DHG concentration.

V. MODEL VERIFICATION

The developed compact large-signal model is embedded in the Agilent Advanced Design System software [46] by using the symbolically-defined devices (SDD) method. The large-signal equivalent circuit topology for the C-H diamond MOSFET is shown in Fig. 11, which ignores the effect of gate leakage and dielectric breakdown.

A. DC I-V CHARACTERISTICS

Fig. 11 shows the simulated I-V curves and measured data of the fabricated 2 × 500 μm C-H diamond MOSFET.

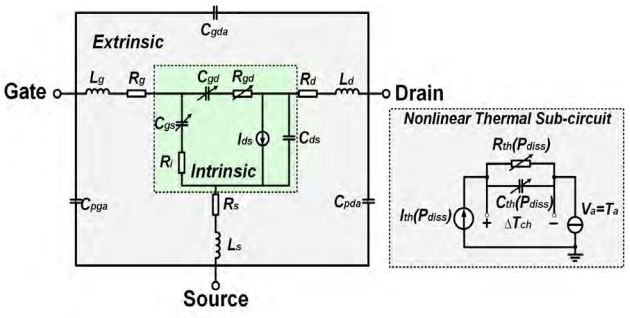


FIGURE 10. Large-signal equivalent circuit topology.

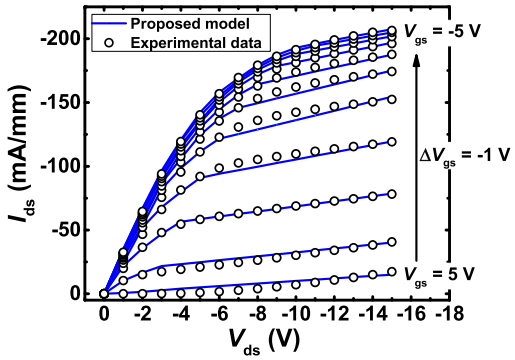


FIGURE 11. Simulated (lines) and measured (circles) I-V characteristics of the fabricated 2 × 500 μm C-H diamond MOSFET. V_{gs} ranges from 5 V to −5 V with the steps of −1 V.

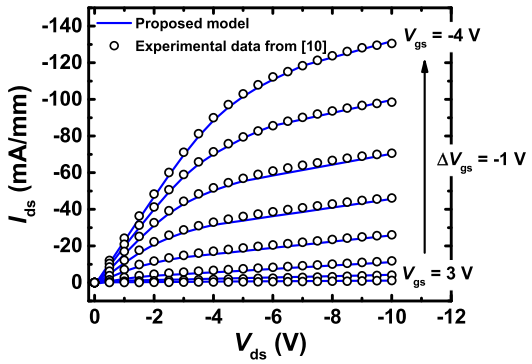


FIGURE 12. Simulated (lines) and measured (circles) I-V characteristics of the fabricated 2 × 50 μm C-H diamond MOSFET in [10]. V_{gs} ranges from 3 V to −4 V with the step of −1 V.

To further demonstrate the validity of the developed I-V model, Fig. 12 shows the comparison between the I-V modeling results and the experimental data of the 2 × 50 μm single-crystal diamond MOSFET in [10]. The proposed current model based on the improved QPZD method can predict the DC I-V performance of C-H diamond MOSFETs with different sizes.

B. SMALL-SIGNAL CHARACTERISTICS

Before verifying the large-signal characteristics, the small-signal S-parameters should first be verified to ensure the consistency between small- and large-signal models.

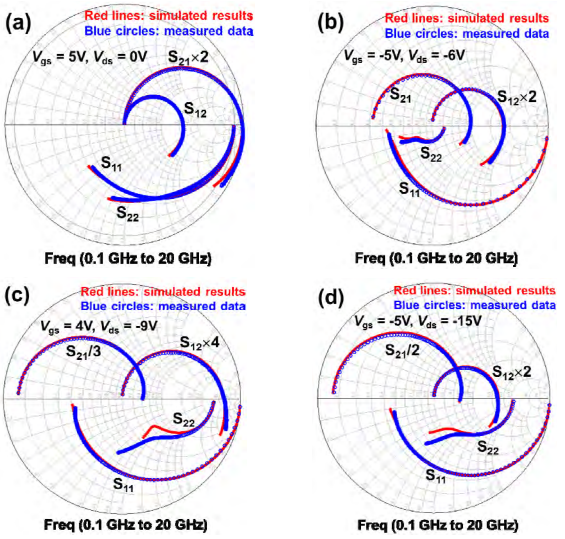


FIGURE 13. Measured (symbols) and modeled (solid lines) multi-bias S- parameters from 0.1 to 20 GHz for the 2 × 500 μm C-H diamond MOSFET. (a) V_{gs} = 5 V, V_{ds} = 0 V, (b) V_{gs} = −5 V, V_{ds} = − 6 V, (c) V_{gs} = 4 V, V_{ds} = −9 V, (d) V_{gs} = −5 V, V_{ds} = −15 V.

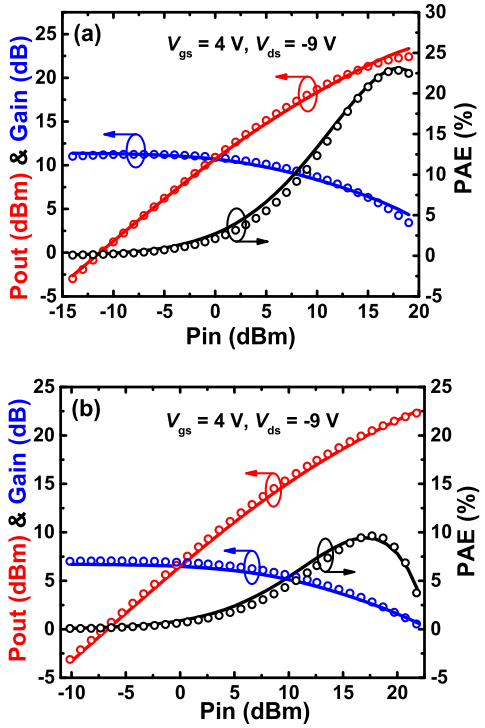


FIGURE 14. Single-tone power sweep simulations (lines) and measurements (symbols) for large-signal characteristics (P_{out}, Gain, and PAE) at (a) 1 GHz and (b) 2 GHz and the bias of V_{gs} = 4 V and V_{ds} = −9 V.

Fig. 13 shows the measured and modeled S-parameters for the 2 × 500 μm C-H diamond MOSFET in the frequency range of 0.1 ∼ 20 GHz in multibias conditions. (V_{gs} = 5 V, V_{ds} = 0 V) is the bias of the cold FET mode; (V_{gs} = −5 V, V_{ds} = −6 V) and (V_{gs} = −5 V, V_{ds} = −15 V) are the bias points of the linear mode and saturated mode of the I-V curves, respectively. (V_{gs} = 4 V, V_{ds} = −9 V) is the bias where the

transistor operates in class AB. The good consistency between simulation and measurement results demonstrates that the proposed model can accurately predict the S-parameters over a wide frequency range in multibias conditions. However, there are slight deviations in the high-frequency S_{22} because the bias-dependent C_{ds} is not considered in the model [13].

C. LARGE-SIGNAL CHARACTERISTICS

The simulation and measurement results of the output power, gain, and power-added efficiency under class AB operation condition (V_{gs} = 4 V, V_{ds} = −9 V) at 1 GHz and 2 GHz are compared in Fig. 14. The power sweep measurement was performed based on the optimum resistance for the maximum PAE. The optimum source and load resistance are Z_S = (75.91 + j ×107.25)Ω and Z_L = (103.88 + j ×34.26)Ω at 1 GHz and Z_S = (35.68 + j ×74.19)Ω and Z_L = (102.91+ j ×33.43)Ω at 2 GHz. Unlike the 1 GHz and 2 GHz power sweep verification for different devices in [11], in this paper, the consistency between measurement and simulation results of the same device indicates that the proposed compact model can accurately predict the large-signal behaviors of the C-H diamond MOSFET on different frequency conditions. In addition, it is well known that there is a dielectric barrier that separates the 2DHG channel and Al gate metal contact, which can prevent the tunneling current [47]. When the permittivity and thickness of the barrier layer are confirmed, the proposed large-signal model for C-H diamond MOSFETs in this work is suitable to expand to the MESFET cases.

VI. CONCLUSION

A compact I-V model and its application to the large-signal modeling of the emerging C-H diamond MOSFET are presented in this work. Based on the improved quasi-physical zone division method and the extracted thermal resistance, the analytic current-voltage expressions for the device in the linear and saturated modes are deduced, respectively. The current-voltage expressions can directly demonstrate the relation between negative V_{ds} and I_{ds} of the p-type diamond MOSFET and involve in the critical electrical field E_{c_eff}, which corresponds to the channel temperature and gate bias. Compared with the empirical model proposed for the C-H diamond MESFET, this model originates from the zone division operation mechanism of the C-H diamond MOSFET and includes more physical parameters. Hence, the proposed model in this paper has guiding significance for the design and optimization of diamond FETs. The C-V, DC I-V, small-signal S-parameters, and large-signal power sweep verification results show that the proposed model can accurately predict the device characteristics and is suitable to be embedded in commercial software.

REFERENCES

[1] J. Isberg, J. Hammersberg, E. Johansson, T. Wikström, D. J. Twitchen, A. J. Whitehead, S. E. Coe, and G. A. Scarsbrook, "High carrier mobility in single-crystal plasma-deposited diamond," *Science*, vol. 297, no. 5587, pp. 1670–1672, Sep. 2002. doi: 10.1126/science.1074374.

[2] K. Hirama, H. Takayanagi, S. Yamauchi, Y. Jingu, H. Umezawa, and H. Kawarada, "High-performance p-channel diamond MOSFETs with alumina gate insulator," in *IEDM Tech. Dig.*, Washington, DC, USA, Dec. 2007, pp. 873–876. doi: 10.1109/IEDM.2007.4419088.

[3] T. T. Pham, J. Pernot, C. Masante, D. Eon, E. Gheeraert, G. Chicot, F. Udrea, and N. Rouger, "200V, 4MV/cm lateral diamond MOSFET," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2017, pp. 25.4.1–25.4.4. doi: 10.1109/IEDM.2017.8268458.

[4] Y. Kitabayashi, T. Kudo, H. Tsuboi, T. Yamada, D. Xu, M. Shibata, D. Matsumura, Y. Hayashi, M. Syamsul, M. Inaba, A. Hiraiwa, and H. Kawarada, "Normally-off C–H diamond MOSFETs with partial C–O channel achieving 2-kV breakdown voltage," *IEEE Electron Device Lett.*, vol. 38, no. 3, pp. 363–366, Mar. 2017. doi: 10.1109/LED.2017.2661340.

[5] S. Russell, S. Sharabi, A. Tallaire, and D. A. J. Moran, "RF operation of hydrogen-terminated diamond field effect transistors: A comparative study," *IEEE Trans. Electron Devices*, vol. 62, no. 3, pp. 751–756, Mar. 2015. doi: 10.1109/TED.2015.2392798.

[6] X. Yu, J. Zhou, C. Qi, Z. Cao, Y. Kong, and T. Chen, "A high frequency hydrogen-terminated diamond MISFET with f_T/f_{max} of 70/80 GHz," *IEEE Electron Device Lett.*, vol. 39, no. 9, pp. 1373–1376, Sep. 2018. doi: 10.1109/LED.2018.2862158.

[7] S. Imanishi, K. Horikawa, N. Oi, S. Okubo, T. Kageura, A. Hiraiwa, and H. Kawarada, "3.8 W/mm RF power density for ALD Al_2O_3-based two-dimensional hole gas diamond MOSFET operating at saturation velocity," *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 279–282, Feb. 2019. doi: 10.1109/LED.2018.2886596.

[8] C. E. Nebel, B. Rezek, D. Shin, and H. Watanabe, "Surface electronic properties of H-terminated diamond in contact with adsorbates and electrolytes," *Phys. Status Solidi A*, vol. 203, no. 13, pp. 3273–3298, Oct. 2006. doi: 10.1002/pssa.200671401.

[9] F. Maier, M. Riedel, B. Mantel, J. Ristein, and L. Ley, "Origin of surface conductivity in diamond," *Phys. Rev. Lett.*, vol. 85, no. 16, pp. 3472–3475, Oct. 2000. doi: 10.1103/PhysRevLett.85.3472.

[10] Y. Fu, R. Xu, Y. Xu, J. Zhou, Q. Wu, Y. Kong, Y. Zhang, T. Chen, and B. Yan, "Characterization and modeling of hydrogen-terminated MOSFETs with single-crystal and polycrystalline diamond," *IEEE Electron Device Lett.*, vol. 39, no. 11, pp. 1704–1707, Nov. 2018. doi: 10.1109/LED.2018.2870668.

[11] V. Camarchia, F. Cappelluti, G. Ghione, M. Pirola, G. Conte, B. Pasciuto, E. Limiti, and E. Giovine, "Accurate large-signal equivalent circuit of surface channel diamond FETs based on the Chalmers model," *Diamond Rel. Mater.*, vol. 26, pp. 15–19, Jun. 2012. doi: 10.1016/j.diamond.2012.03.010.

[12] F. M. Yigletu, S. Khandelwal, T. A. Fjeldly, and B. Iñiguez, "Compact charge-based physical models for current and capacitances in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 60, no. 11, pp. 3746–3752, Nov. 2013. doi: 10.1109/TED.2013.2283525.

[13] Q. Wu, Y. Xu, Y. Chen, Y. Wang, W. Fu, B. Yan, and R. Xu, "A scalable multiharmonic surface-potential model of AlGaN/GaN HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 3, pp. 1192–1200, Mar. 2018. doi: 10.1109/TMTT.2017.2775639.

[14] U. Radhakrishna, P. Choi, J. Grajal, L.-S. Peh, T. Palacios, and D. Antoniadis, "Study of RF-circuit linearity performance of GaN HEMT technology using the MVSG compact device model," in *IEDM Tech. Dig.*, Dec. 2016, pp. 3.7.1–3.7.4. doi: 10.1109/IEDM.2016.7838341.

[15] H. Yin, G. L. Bilbro, and R. J. Trew, "A new physics-based compact model for AlGaN/GaN HFETs," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Honolulu, HI, USA, Jun. 2007, pp. 787–790. doi: 10.1109/MWSYM.2007.380058.

[16] D. Hou, G. L. Bilbro, and R. J. Trew, "A compact physical AlGaN/GaN HFET model," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 639–645, Feb. 2013. doi: 10.1109/TED.2012.2227323.

[17] Z. Wen, Y. Xu, Y. Chen, H. Tao, C. Ren, H. Lu, Z. Wang, W. Zheng, B. Zhang, T. Chen, T. Gao, and R. Xu, "A quasi-physical compact large-signal model for AlGaN/GaN HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5113–5122, Dec. 2017. doi: 10.1109/TMTT.2017.2765326.

[18] Y. Li, J.-F. Zhang, G.-P. Liu, Z.-Y. Ren, J.-C. Zhang, and Y. Hao, "Mobility of two-dimensional hole gas in H-terminated diamond," *Phys. Status Solidi RRL*, vol. 12, no. 3, pp. 1700401-1–1700401-5, Mar. 2018. doi: 10.1002/pssr.201700401.

[19] J. Zhang, Z.-Y. Ren, J.-C. Zhang, C.-F. Zhang, D.-Z. Chen, S.-R. Xu, Y. Li, and Y. Hao, "Characterization and mobility analysis of MoO_3-gated diamond MOSFET," *Jpn. J. Appl. Phys.*, vol. 56, no. 10, Sep. 2017, Art. no. 100301. doi: 10.7567/JJAP.56.100301.

[20] N. Fujimori, H. Nakahata, and T. Imai, "Properties of boron-doped epitaxial diamond films," *Jpn. J. Appl. Phys.*, vol. 29, no. 5, pp. 824–827, May 1990. doi: 10.1143/JJAP.29.824.

[21] H. Kawarada, T. Yamada, D. Xu, Y. Kitabayashi, M. Shibata, D. Matsumura, M. Kobayashi, T. Saito, T. Kudo, M. Inaba, and A. Hiraiwa, "Diamond MOSFETs using 2D hole gas with 1700V breakdown voltage," in *Proc. 28th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Prague, Czech Republic, Jun. 2016, pp. 483–486. doi: 10.1109/ISPSD.2016.7520883.

[22] V. Camarchia, F. Cappelluti, G. Ghione, E. Limiti, D. A. J. Moran, and M. Pirola, "An overview on recent developments in RF and microwave power H-terminated diamond MESFET technology," in *Proc. Int. Workshop Integr. Nonlinear Microw. Millimetre-Wave Circuits (INMMiC)*, Apr. 2014, pp. 1–6. doi: 10.1109/INMMIC.2014.6815102.

[23] J. J. Liou, A. Ortiz-Condez, and F. G. Sanchez, "Extraction of the threshold voltage of MOSFETs: An overview," in *Proc. IEEE Hong Kong Electron Devices Meeting*, Hong Kong, Aug. 1997, pp. 31–38. doi: 10.1109/HKEDM.1997.642325.

[24] Z. Ren, J. Zhang, J. Zhang, C. Zhang, S. Xu, Y. Li, and Y. Hao, "Diamond field effect transistors With MoO_3 gate dielectric," *IEEE Electron Device Lett.*, vol. 38, no. 6, pp. 786–789, Jun. 2017. doi: 10.1109/LED.2017.2695495.

[25] C. Verona, W. Ciccognani, S. Colangeli, E. Limiti, M. Marinelli, G. Verona-Rinati, D. Cannatà, M. Benetti, and F. Di Pietrantonio, "V_2O_5 MISFETs on H-terminated diamond," *IEEE Trans. Electron Devices*, vol. 63, no. 12, pp. 4647–4653, Dec. 2016. doi: 10.1109/TED.2016.2617362.

[26] S. Gkoumas, A. Lohstroh, and P. J. Sellin, "Low temperature time of flight mobility measurements on synthetic single crystal diamond," *Diamond Rel. Mater.*, vol. 18, no. 11, pp. 1338–1342, Nov. 2009. doi: 10.1016/j.diamond.2009.07.006.

[27] C. G. Sodini, P.-K. Ko, and J. L. Moll, "The effect of high fields on MOS device and circuit performance," *IEEE Trans. Electron Devices*, vol. 31, no. 10, pp. 1386–1393, Oct. 1984. doi: 10.1109/T-ED.1984.21721.

[28] K. Y. Fu, "Mobility degradation due to the gate field in the inversion layer of MOSFET's," *IEEE Electron Device Lett.*, vol. 3, no. 10, pp. 292–293, Oct. 1982. doi: 10.1109/EDL.1982.25573.

[29] M. Kasu, K. Hirama, K. Harada, and T. Oishi, "Study on capacitance–voltage characteristics of diamond field-effect transistors with NO_2 hole doping and Al_2O_3 gate insulator layer," *Jpn. J. Appl. Phys.*, vol. 55, no. 4, 2016, Art. no. 041301. doi: 10.7567/JJAP.55.041301.

[30] H. Yin, D. Hou, G. L. Bilbro, and R. J. Trew, "Harmonic balance simulation of a new physics based model of the AlGaN/GaN HFET," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2008, pp. 1425–1428. doi: 10.1109/MWSYM.2008.4633046.

[31] M. H. Weiler and Y. Ayasli, "DC and microwave models for $Al_xGa_{1-x}As$/GaAs high electron mobility transistors," *IEEE Trans. Electron Devices*, vol. 31, no. 12, pp. 1854–1861, Dec. 1984. doi: 10.1109/T-ED.1984.21801.

[32] H. Kawarada, "High-current metal oxide semiconductor field-effect transistors on H-terminated diamond surfaces and their high-frequency operation," *Jpn. J. Appl. Phys.*, vol. 51, no. 9R, 2012, Art. no. 090111. doi: 10.1143/JJAP.51.090111.

[33] C. E. Nebel, B. Rezek, and A. Zrenner, "Electronic properties of the 2D-hole accumulation layer on hydrogen terminated diamond," *Diamond Rel. Mater.*, vol. 13, nos. 11–12, pp. 2031–2036, 2006. doi: 10.1016/j.diamond.2004.06.028.

[34] T. Ytterdal, Y. Cheng, and T. A. Fjeldly, *Device Modeling for Analog and RF CMOS Circuit Design*. New York, NY, USA: Wiley, 2003.

[35] H. Rohdin and P. Roblin, "A MODFET DC model with improved pinchoff and saturation characteristics," *IEEE Trans. Electron Devices*, vol. ED-33, no. 5, pp. 664–672, May 1986. doi: 10.1109/T-ED.1986.22549.

[36] X. Z. Dang, P. M. Asbeck, E. T. Yu, G. J. Sullivan, M. Y. Chen, B. T. McDermott, K. S. Boutros, and J. M. Redwing, "Measurement of drift mobility in AlGaN/GaN heterostructure field-effect transistor," *Appl. Phys. Lett.*, vol. 74, no. 25, pp. 3890–3892, Jun. 1999. doi: 10.1063/1.124214.

[37] N. S. Swamy and A. K. Dutta, "Analytical models for the 2DEG density, AlGaN layer carrier density, and drain current for AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 936–944, Mar. 2018. doi: 10.1109/TED.2018.2794460.

[38] A. Traoré, S. Koizumi, and J. Pernot, "Effect of n- and p-type doping concentrations and compensation on the electrical properties of semiconducting diamond," *Phys. Status Solidi A*, vol. 213, no. 8, pp. 2036–2043, Aug. 2016. doi: 10.1002/pssa.201600407.

[39] K. Hayashi, S. Yamanaka, H. Okushi, and K. Kajimura, "Study of the effect of hydrogen on transport properties in chemical vapor deposited diamond films by Hall measurements," *Appl. Phys. Lett.*, vol. 68, no. 3, pp. 376–378, Jan. 1996. doi: 10.1063/1.116690.

[40] W. Deng, J. Huang, X. Ma, and J. J. Liou, "An explicit surface potential calculation and compact current model for AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 36, no. 2, pp. 108–110, Feb. 2015. doi: 10.1109/LED.2015.2388706.

[41] Q. Wu, Y. Xu, J. Zhou, Y. Kong, T. Chen, Y. Wang, F. Lin, Y. Fu, Y. Jia, X. Zhao, B. Yan, and R. Xu, "Performance comparison of GaN HEMTs on diamond and SiC substrates based on surface potential model," *ECS J. Solid State Sci. Technol.*, vol. 6, no. 12, pp. Q171–Q178, Dec. 2017. doi: 10.1149/2.0441712jss.

[42] A. V. Sukhadolau, E. V. Ivakin, V. G. Ralchenko, A. V. Khomich, A. V. Vlasov, and A. F. Popovich, "Thermal conductivity of CVD diamond at elevated temperatures," *Diam. Rel. Mater.*, vol. 14, pp. 589–593, Mar./Jul. 2005. doi: 10.1016/j.diamond.2004.12.002.

[43] M. Kasu, K. Ueda, H. Ye, Y. Yamauchi, S. Sasaki, and T. Makimoto, "High RF output power for H-terminated diamond FETs," *Diamond Rel. Mater.*, vol. 15, nos. 4–8, pp. 783–786, Feb. 2006. doi: 10.1016/j.diamond.2005.12.025.

[44] Z. Wen, Y. Xu, C. Wang, X. Zhao, Z. Chen, and R. Xu, "A parameter extraction method for GaN HEMT empirical large-signal model including self-heating and trapping effects," *Int. J. Numer. Model., Electron. Netw., Devices Fields*, vol. 30, no. 1, Jan./Feb. 2017, Art. no. e2137. doi: 10.1002/jnm.2137.

[45] Y. Chen, Y. Xu, J. Zhou, Y. Kong, T. Chen, Y. Zhang, B. Yan, and R. Xu, "Temperature-dependent small signal performance of GaN-on-diamond HEMTs," *Int. J. Numer. Model., Electron. Netw., Devices Fields*, vol. 32, no. 3, May 2019, Art. no. e2620. doi: 10.1002/jnm.2620.

[46] C. Wang, Y. Xu, X. Yu, C. Ren, Z. Wang, H. Lu, T. Chen, B. Zhang, R. Xu, "An electrothermal model for empirical large- signal modeling of AlGaN/GaN HEMTs including self-heating and ambient temperature effects," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 2878–2887, Dec. 2014. doi: 10.1109/TMTT.2014.2364821.

[47] M. Kubovic, M. Kasu, Y. Yamauchi, K. Ueda, and H. Kageshima, "Structural and electrical properties of H-terminated diamond field-effect transistor," *Diamond Rel. Mater.*, vol. 18, pp. 796–799, May/Aug. 2009. doi: 10.1016/j.diamond.2009.01.020.

YU FU received the B.S. degree in electronic information engineering from the Beijing Information Science and Technology University, Beijing, China, in 2015. He is currently pursuing the Ph.D. degree with the University of Electronic Science and Technology of China (UESTC), Chengdu, China, majoring in electromagnetic field and microwave technology.

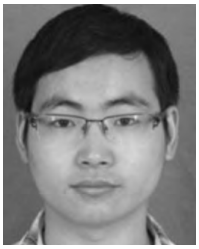
His current research interests include device fabrication, modeling, and the characterization of diamond microwave electronics.

RUIMIN XU (M'07) was born in Sichuan, China, in 1958. He received the B.S. and Ph.D. degrees in electromagnetic field and microwave techniques from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 1982 and 2007, respectively.

He is currently a Full Professor with UESTC. His current research interests include microwave and millimeter-wave technologies and applications, and radar systems.

JIANJUN ZHOU received the B.E. and Ph.D. degrees in solid electronics and microelectronics from Nanjing University, Nanjing, China, in 2002 and 2007, respectively.

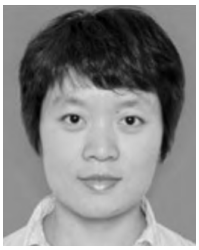
He has been a Professor with the Science and Technology on Monolithic Integrated Circuits and Modules Laboratory, since 2016. In 2007, he joined the Nanjing Electronic Devices Institute, China, where he was involved in the studies of nitride semiconductors. He is currently interested in the microwave and power devices of wide bandgap semiconductors.



XINXIN YU received the B.S. degree in physics (microelectronics) from Nanjing University, Nanjing, China, in 2011, and the M.S. degree in microelectronics and solid state electronics from the Nanjing Electronic Devices Institute, Nanjing, in 2014. Since 2014, he has been with the Science and Technology on Monolithic Integrated Circuits and Modules Laboratory, Nanjing Electronic Devices Institute, Nanjing, where he is currently an Engineer. His current research interests include GaN-based microwave power devices and diamond field-effect transistors.

ZHANG WEN received the B.S. degree in mathematics and applied mathematics and the Ph.D. degree in electromagnetic field and microwave techniques from the University of Electronic Science and Technology of China, Chengdu, China, in 2012 and 2018, respectively.

He has been an Assistant Professor with the Microsystem and Terahertz Research Center, China Academy of Engineering Physics, since 2018. His research interests include the characterization and the modeling of microwave devices and microsystems.



YUECHAN KONG received the B.S. and Ph.D. degrees in microelectronic and solid-state physics from Nanjing University, Nanjing, China, in 2002 and 2007, respectively.

In 2007, she was with the Science and Technology on Monolithic Integrated Circuits and Modules Laboratory, Nanjing Electronic Devices Institute, Nanjing, where she is currently the Vice Director of the MICM Laboratory. Her research interests include transport mechanism in III–V nitride heterostructures and GaN-on-diamond devices.

TANGSHENG CHEN was born in Hubei, China, in 1964. He received the B.S. and M.S. degrees in semiconductor physics and devices from Xi'an Jiaotong University, Xi'an, China, in 1986 and 1989, respectively.

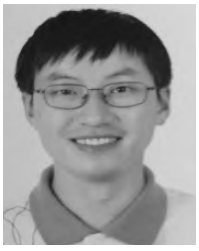
He joined the Nanjing Electronic Devices Institute, Nanjing, China, in 1989. His current research interests include fabrication, characterization, and the development of compound semiconductor high-frequency high-power electronic devices.

YONG ZHANG (M'05–SM'13) received the B.S., M.S., and Ph.D. degrees from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 1999, 2001, and 2004, respectively. He was invited as a Visiting Scholar with the Illinois Institute of Technology, USA, from 2009 to 2010. He was involved in the field of RF circuits for 18 years since he has joined the University of Electronic Science and Technology of China as the master's degree student. He is currently a Professor with the University of Electronic Science and Technology of China because of his outstanding research achievements. He has published over 100 journal and conference papers. He has applied 13 patents and five of them got the authorization.

His current research interests include the design and the applications of passive and active components at RF frequencies, and solid state terahertz technology.

BO YAN received the B.S. and M.S. degrees in electromagnetic field and microwave techniques and the Ph.D. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 1991, 1998, and 1998, respectively.

His current research interests include microwave and millimeter-wave hybrid integrated circuits, and MCM technology.



JIJUN HE received the B.E. degree in electronic information engineering from the Harbin University of Science and Technology, Harbin, China, in 2003. Since 2003, he has been with Chongqing Chang'an Industry Group Co., Ltd., Chongqing, where he has been involved in the research of automotive electronics.

YUEHANG XU (M'11–SM'16) received the B.S. and M.S. degrees in electromagnetic field and microwave techniques from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2004 and 2007, respectively, and the joint Ph.D. degree from UESTC and Columbia University, New York, NY, USA, in 2010.

He joined the Department of Electronic Engineering, UESTC, in 2010. He has been a Professor, since 2017. He was a Visiting Associate Professor with Case Western Reserve University, Cleveland, OH, USA, in 2016. He has authored or coauthored over 150 scientific papers in international journals. His current research interests include the modeling and the characterization of radio frequency micro/nano-scale electronic devices and MMIC design.