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QCA Based Error Detection Circuit for Nano Communication Network

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ABSTRACT This paper outlines low power nano-scale circuit design for even parity generator, as well as, even parity checker circuit using quantum-dot cellular automata (QCA). The proposed even parity generator and even parity checker are achieved by using a new layout of XOR gate. This new XOR gate as a state-of-the-art is much denser and faster than the existing ones. The proposed parity generator has outshined the existing design by reducing the cell count as 10%, area as 5.66%, and latency by 12.5%. The proposed parity checker has also outshined the existing design with an improvement in cell count as 17.94% and in the area as 38.46% having a reduction in latency of 22.22%. The comparison proves that the circuits are denser and faster than the existing one. Nano communication architecture with the proposed circuits also demonstrates the efficiency of this design. Furthermore, the bit-error coverage by the proposed method is described. Besides, the defects in the circuits are explored to facilitate guide to proper implementation. The tests vectors are proposed to identify the defects in the designs and the defect coverage by those test vectors. The estimation of dissipated energy by the layouts establishes a very low energy dissipation nature of the designs. Different parameters like a logic gate, density, and latency are utilized to evaluate the proposed designs that confirm the faster processing speed at nano-scale.

INDEX TERMS Communication, majority gate, parity checker, parity generator, power dissipation, QCA.

I. INTRODUCTION

Currently existing CMOS technology is approaching its physical limit such as quantum effects and power dissipation [1], [2]. Scaling down the logic circuit using CMOS technology to nanometer scale caused higher design complexity [1]–[5]. To continue the progress in scaling down the circuit and increasing the performance of a microprocessor, an alternative to CMOS is essential. As an alternative to CMOS, QCA was introduced [1]. QCA emerged as a promising technology to encode information beyond current switches [6]–[10]. QCA is nanotechnology-based transistor that has ultra low power consumption. It has high device density and faster switching speed [11]–[14]. The encoding in QCA is achieved by charge configuration of a QCA cell [15]–[19]. The columbic interaction occurs between cells is sufficient to perform the computation [20]–[21]. Therefore, interconnecting wire is not required between cells. Power dissipation is very low, as current is not flowing out of the cell. In digital communication, the detection of an error in received message is a key issue. Parity bit [22] is useful in detecting such errors. During transmission of binary message through network, an extra bit is padded with the information to detect the error within the message. This additional bit is called the parity bit. Parity bit is padded to produce total number of 1's (including parity bit) in a message either even or odd [22]. Besides, at nano-scale, the complexity of error detection and correction scheme [23] is the most challenging aspect at hardware level in terms of circuit area and energy dissipation. Thus, in this study, low power nano-scale circuit designs for even parity generator as well as even parity checker circuit using QCA are described. This paper has the principal contributions are as follows.

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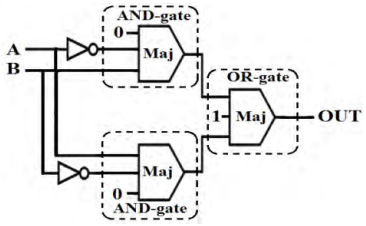
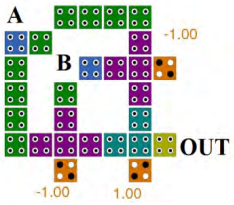
- Design of a new XOR gate using QCA.
- Design of even parity generator and even parity checker circuit by using proposed XOR gate.
- The proposed designs are compared with existing circuit based on area, latency and logic gates, which confirm they have higher device area and faster than existing one in the state of the art.
- Nanocommunication architecture with the proposed circuits is also demonstrated.
- The bit-error coverage by the proposed method described.
- Single missing cell and extra deposited cell based defects in the proposed designs are explored to facilitate guidance to proper implementation. Besides, the tests vectors are proposed to identify the defects in the designs and the defect coverage by those test vector are also described.
- Dissipated energy by all the layouts has been carried out.

The paper is outlined as follows. Related works are described in Section II. The low power nano-scale design for proposed error detecting circuit is described in Section III. Nanocommunication architecture is demonstrated in Section IV. Section V describes the error controlling codes, error coverage by the proposed method, design complexity, comparison with existing circuit, defects analysis and estimation of power dissipation. The conclusion is finally portrayed in Section VI.



(a)



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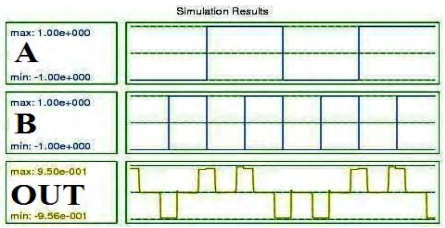

(c)

FIGURE 1. Proposed XOR gate (a) QCA schematic, (b) QCA layout, and (c) Simulation result.

II. RELATED WORK

Huge numbers of researches explores the communication technique through QCA [14], [24]–[30]. In [14], a simple stream cipher is designed using QCA. The QCA stream cipher is then used to show how secure nanocommunication can be achieved. Nanocommunication with reversible crossbar switch is explored in [24]. Besides, the fault analysis of the communication circuit is also performed in [24]. In [25], a path selector that can work as router to route information using QCA is proposed. The data transfer caused by this router to destinations is achieved through a single channel. Thus, channel utilization is maximized. In [26], the measure of computational fidelity with representational faithfulness for nanocomputing QCA channels is described. The efficacy measure is performed on noisy QCA arrays having random defects. In [27], a new nano-router architecture implementation in QCA is explored. Different building blocks like demultiplexer, parallel-to-serial converter, and crossbar are used during design process. The functionality of this nano-router is demonstrated elaborately. The work presented in [28] deals with 4-bit nano-sensor data processor realization in QCA. The multifunctional capabilities of this data processor are excelled. Different functions like sending raw data (preprocessed) to the next high-level processor, approximate sigmoid function generation etc. by the proposed processor are described. In [29], the design of router is achieved in QCA through reversible logic. The architecture of this router has reduced cell count and minimum complexity. Robust serial communication architecture is realized through QCA in [30]. The design is performed through bottom-up approach. The communication system is made up with QCA circuits of Parallel-to-Serial (PISO) converter, Hamming code, Parity Checker, and Serial-to-Parallel (SIPO) converter.

III. PROPOSED ERROR DETECTING CIRCUIT

A. EXCLUSIVE-OR (XOR) GATE DESIGN USING QCA

XOR gate [31]–[35] performs logic operation on two inputs and produce logic '1' if one of inputs has logic '1'; else it produces logic '0'. The logic expression of XOR gate is A⊕B i.e., $A\overline{B} + \overline{A}B$ [36]–[40]. The proposed QCA based circuit of XOR gate is given in Fig. 1(a). The QCA layout of XOR gate is in Fig 1(b) that consists of 3 MVs, 2 inverters, 27 cells, 0.02 μm^2 area and latency of 0.75.

The simulation result of Fig. 1(b) is shown in Fig. 1(c). It is seen from Fig. 1(c) that when A = 0, B = 0, the output will be OUT = 0. When A = 0, B = 1, the output will be OUT = 1. Thus, all the values of output bit OUT are in accordance with inputs A and B. This result satisfies the theoretical values of XOR gate, which indicates the accuracy of the design.

B. EVEN PARITY GENERATOR

A combinational logic circuit that makes even number of 1's to the sending message by generating the parity bit is called

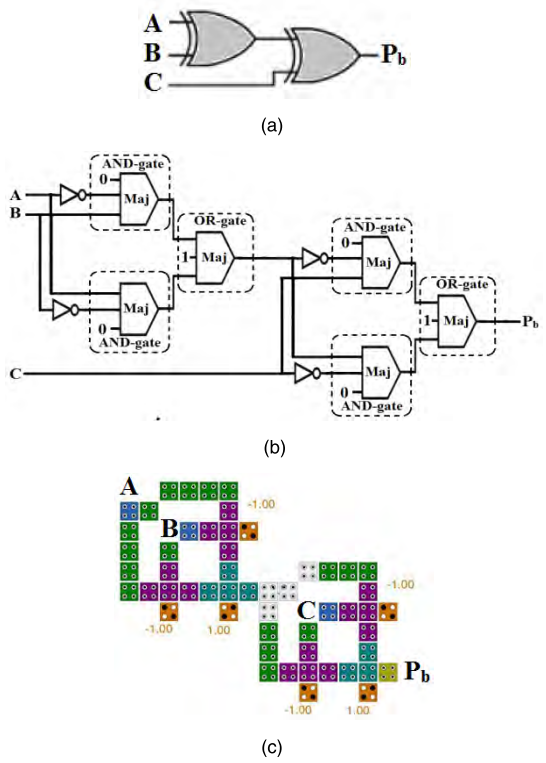

FIGURE 2. Proposed 3-bit even parity generator (a) Circuit diagram, (b) QCA schematic and (c) QCA layout.

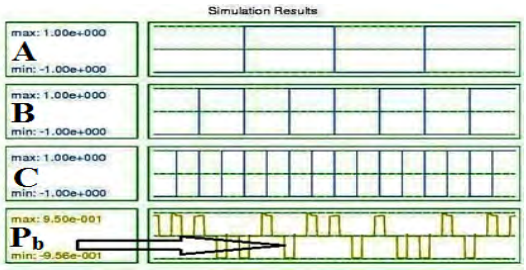

FIGURE 3. Simulation result of proposed 3-bit even parity generator.

parity generator [20], [35], [37]. Parity generator works at the sender node. Consider a 3-bit message with A, B, and C message bits. Again say P_b is the parity bit. P_b is 1 if and only if all of the 3-bits of the message have odd number of 1's; otherwise P_b is 0. It is understand that P_b is equal to the XOR value between inputs A, B, and C as drawn in (1). The gate label circuit for even parity generator is given in Fig. 2(a). Figure 2(b) shows the corresponding QCA schematic of Fig. 2(a).

$$P_b = A \oplus B \oplus C \tag{1}$$

The QCA layout of 3-bit even parity corresponding to Fig. 2(b) is shown in Fig. 2(c). The QCA layout consists of 6 MVs, 4 inverters, 54 cells, 0.05 μm^2 area and latency of 1.75.

The simulation-timing diagram for even parity generator is in Fig. 3. The arrow in Fig. 3 signifies the start position

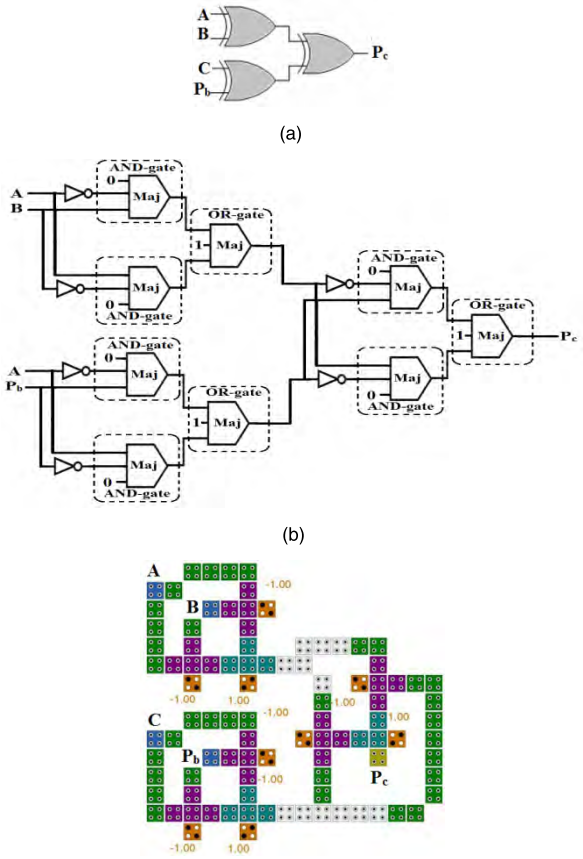

FIGURE 4. Proposed 4-bit even parity checker (a) Circuit diagram, (b) QCA schematic and (c) QCA layout.

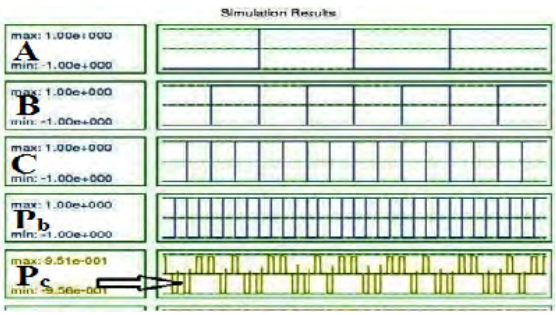

FIGURE 5. Simulation result of proposed 4-bit even parity checker.

of the required output. It is seen from Fig.3 that when A = 0, B = 0 and C = 0, the output will be $P_b = 0$. When A = 0, B = 0, and C= 1, the output will be $P_b = 1$. Thus, all the values of output bit P_b are in accordance with inputs A, B, and C. This result satisfies the theoretical values of parity generator circuit that signifies the accuracy of the design.

C. EVEN PARITY CHECKER

Define A combinational logic circuit that scans the parity bit at the receiver side to detect the error is a parity checker [20], [35], [37]. An even parity checker examines

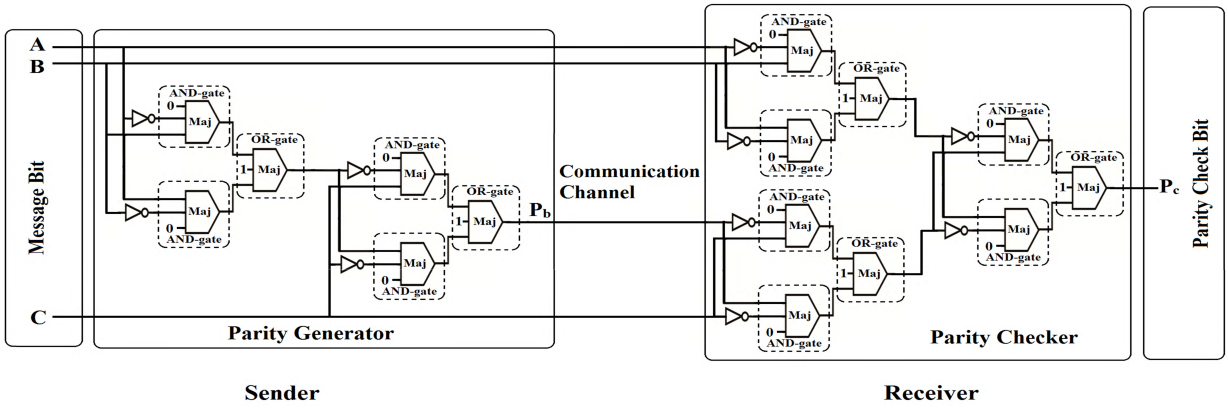

FIGURE 6. QCA circuit of proposed nanocommunication architecture.

the received message for even number of 1's. For example, consider a 4-bit received message with A, B, C, P_b message bits and P_c is the error check bit. P_c is 1 if and only if there is odd number of 1's in the received message; otherwise P_c is 0. Thus an error is in the received message if and only if P_c is 1. Therefore the value of P_c is the XOR-ed value of the inputs A, B, C and P_c. The logic expression for error check bit P_c can be written as XOR operation of the inputs as shown in (2). The logic circuit of even parity checker is shown in Fig. 4(a). Figure 4(b) shows the corresponding QCA schematic of Fig. 4(a).

$$P_c = A \oplus B \oplus C \oplus P_b \tag{2}$$

The QCA layout of 4-bit even parity checker corresponding to Fig. 4(b) is drawn in Fig. 4(c). This QCA layout consists of 9 MVs, 6 inverters, 96 cells, 0.08 μm^2 area and latency of 1.75. The simulation result of Fig. 4(c) is explored in Fig. 5. The arrow in Fig. 5 indicates the start position of the required output. It is seen from Fig. 5 that when A = 0, B = 0, C = 0, and $P_b = 0$, the output will be $P_c = 0$. When A = 0, B = 0, C = 0, and $P_b = 1$, the output will be $P_c = 1$. When A = 0, B = 0, C = 1, and $P_b = 0$, the output will be $P_c = 1$. Thus, all the values of output bit P_c are in accordance with inputs A, B, C, and P_b. This result satisfies the theoretical values of parity checker circuit, which proves the accuracy o the design.

IV. NANOCOMMUNICATION WITH PROPOSED CIRCUIT

The nanocommunication architecture with proposed even-parity generator and even-parity checker is shown in Fig. 6. The architecture consists of three parts: Sender part, communication channel and receiver part. The sender part has input block and parity generator block. The receiver part has parity checker block and output block. Here, A, B, and C is the input to the parity generator block. P_b is the output of the parity checker block. The communication procedure is as follows:

TABLE 1. Truth table for nanocommunication.

Input				Output
A	*B*	*C*	*Generated parity bit (P_b)*	*Parity checker bit (P_c)*
0	0	0	0	0
0	0	1	1	0
1	1	0	1	1 (Error)
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

- At the sender side, the parity generator block receives the three-bit text message, i.e., A, B, and C as the input produce the parity bit (P_b).
- Then, these three-bits, i.e., A, B, C and the generated parity bit, i.e., P_b are transmitted through the communication channel to their corresponding receiver.
- Finally, at the receiver section, the received four bits, i.e., A, B, C, and P_b are processed with the parity checker block. The parity checker block verifies the padded bit P_b within the received text message to detect the error.

The truth table for the proposed communication architecture system is shown in Table 1. The parity check bit (P_c) in Table 1 has all 0s which indicates that the text message is received in a good manner and no error, i.e., corrupted bit is present in the received text. But if $P_c = 1$, then there is a corrupted bit in the received text. For example, let the value of input A in third row of Table 1 is changed from 0→1 and the value of inputs B and C remains unchanged. In that case, P_c will be 1, i.e., there is a corrupted bit in the received message. This situation is shown with the help of highlighted row in Table 2. The parity bit generation and parity check bit generation with error detection procedure are explained

Algorithm 1 Algorithm for Parity Bit Generation

Input: n-bit text message (M)
Output: Parity bit (P_b)

Initialize: M = $m_1m_2m_3$ ..... m_n(m_i is the bit of message M where i=1, 2, 3, ..., n)
Initialize: a[p] = array elements, i.e., bits of M
Initialize: x = 0, i = 0, P_b = 0
1: /* Storing input message bits */
2: **For** i = 1 to n **Do**
3: a[i] ← m_i
4: **Next** i
5: **End For**
6: /∗ Storing XOR-ed value of first two bits ∗/
7: x ← a[1] ⊕a[2]
8: /* Generating parity bit */
9: **For** i = 3 to n **Do**
10: x ← x ⊕a[i]
11: **Next** i
12: **End For**
13: /* Storing parity bit */
14: P_b ← x

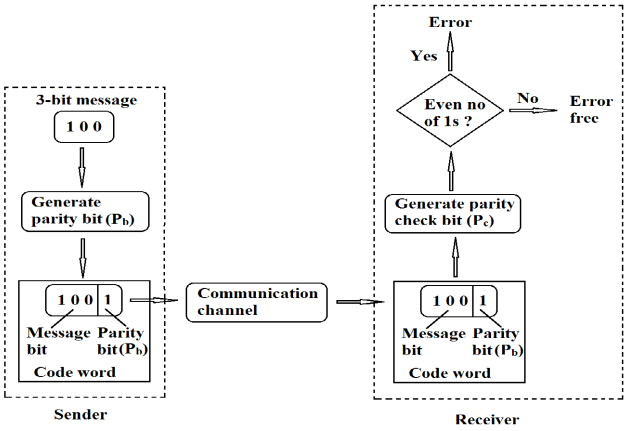

FIGURE 7. Error detection scheme during nanocommunication.

in algorithm 1 and algorithm 2. The overall error detection procedure is described with Fig. 7.

V. RESULT AND DISCUSSIONS

A. ERROR CONTROLLING CODES

This section describes the mathematical model for error controlling codes. Parity check bit is the simplest method to detect single or multiple bit errors in the received information [22]. The simple parity check code word is useful for purpose.

Definition 1: Let $C_i = (C_1, C_2, \ldots, C_n)$ is the even parity code with n-bits. Then, parity-check equation can be written as

$$F = (C_1 \oplus C_2 \oplus \ldots \oplus C_n) = (C_1 + C_2 + \ldots + C_n) \bmod 2 = 0 \tag{3}$$

Algorithm 2 Algorithm for Parity Check Bit Generation and Checking

Input: n-bit text message (M) with padded parity bit (P_b)
Output: Parity check bit (P_c)

Initialize: M = $m_1m_2m_3$ ..... m_n(m_i is the bit of message M where i=1, 2, 3,. ....., n)
Initialize: a[p] = array elements, i.e., bits of M
Initialize: x = 0, i = 0, P_c = 0
1: /* Storing input message bits */
2: **For** i = 1 to n **Do**
3: a[i] ← m_i
4: **Next** i
5: **End For**
6: /* Storing XOR-ed value of first two bits */
7: x ← a[1] ⊕a[2]
8: /* Generating parity check bit */
9: **For** i = 3 to n Do
10: x ← x ⊕a[i]
11: **Next** i
12: **End For**
13: P_c ← x ⊕P_b
14: /* Error checking */
15: **If** P_c = 0 **Then**
16: Error detected
17: **Else**
18: No error
19: **End If**

TABLE 2. Error detection in nanocommunication.

Input				Output
A	*B*	*C*	*Generated parity bit (P_b)*	*Parity checker bit (P_c)*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

Thus, the check bit can be computed as

$$C_n = (C_1 \oplus C_2 \oplus \ldots \oplus C_{n-1}) \tag{4}$$

It is noted that any bit $C_i (i = 1, 2, \ldots)$ can be considered as the check bit because it is possible to compute any C_i from rest $(n-1)$ bits, i.e., $C_i = \sum_{j \neq i} C_j$.

Definition 2: Let L be a regular language and X is a binary string belongs to L, i.e., $X \in L$. Thus, L can be defined as

$$L = \{X \in \{0, 1\}^* : X \text{ has even parity}\} \tag{5}$$

X will be even parity if and only if the number of 1s in X is even. The corresponding FSM is shown in Fig. 8.

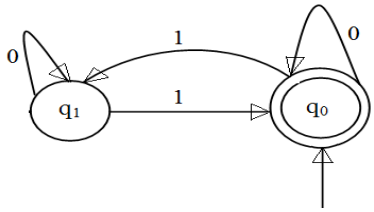

FIGURE 8. FSM for even parity code.

Definition 3: The $(n+1, n)$ parity check code is defined by the $1 \times (n+1)$ matrix with $(n+1)$ number of 1s, i.e., one row must have $(n+1)$ number of 1s.

Definition 4: Let the n-bit input message is $m = (m_0, m_1, \ldots, m_{n-1})$ where $m_i \in GF(2)$ and $0 \leq i \leq n-1$, then the parity bit P can be written as

$$P = m \cdot H_e^T = (m_0 + m_1 + \ldots + m_{n-1}) \tag{6}$$

Here, $H_e = (11 \ldots..1)$ is the row vector having k number of 1s [22]. The '+' operator denotes the addition operation with modulo-2 addition. The transmitted code word for parity check code will be

$$w = (mP) = (m_0 m_1 \ldots m_{n-1} P) \tag{7}$$

The received message (r) with $(n+1)$ bits will be

$$r = \left(m'P'\right) = \left(m'_0 m'_1 \ldots m'_{n-1} P'\right) \tag{8}$$

Thus, the parity check can be performed as

$$\begin{aligned} C = r \cdot H^T &= \left(m'_0 m'_1 \ldots\ldots m'_{n-1} P'\right) \cdot (11 \ldots.1)^T \\ &= \left(m'_0 + m'_1 + \ldots\ldots\ldots + m'_{n-1} + P'\right) \end{aligned} \tag{9}$$

Here, H is the row vector having $(n+1)$ number of 1s, i.e., $H = (111 \ldots.111)$. Now, if an error occurred in the received message, the error $(e) = (e_0, e_1, \ldots\ldots\ldots, e_{n-1}, e_P)$ is padded with the transmitted message. In this case, $e_i \in GF(2)\ i = (0, 1, \ldots\ldots, n-1, P)$ with $i = (0, 1, \ldots\ldots, n-1, P)$. Thus,

$$r = (w + e) = (m_0 + e, m_1 + e_1, \ldots, m_{n-1} + e_{n-1}, P + e_P) \tag{10}$$

where, $r_i = m'_i = m_i + e_i$ and $r_P = P' = P + e_P \quad \forall 0 \leq i \leq n-1$.

B. ERROR COVERAGE

If the error bits are independent and identically distributed (i.i.d) random variables with probability ρ, the number of error bits can be represented with probability mass function (p.m.f) as

$$P_{1\_error} = \binom{n}{1} \rho (1-\rho)^{n-1} \approx n\rho \tag{11}$$

$$P_{2\_error} = \binom{n}{2} \rho^2 (1-\rho)^{n-2} \approx \frac{1}{2} n^2 \rho^2 \tag{12}$$

$$P_{K\_error} = \binom{n}{k} \rho^k (1-\rho)^{n-k} \approx \frac{1}{k!} n^k \rho^k \tag{13}$$

TABLE 3. Proposed XOR gate and existing layouts.

QCA based XOR circuit	Cell count	Area (μm^2)	Latency
Proposed design	27	0.02	0.75
Previous design [31]	29	0.03	0.75
Previous design (design I) [32]	37	0.03	0.75
Previous design (design II) [32]	30	0.03	0.75
Previous design [33]	35	0.029	1.0
Previous design [34]	32	0.02	1.0
Previous design (design I) [35]	44	0.07	1.0
Previous design (design II) [35]	55	0.09	2.0
Previous design (design III) [35]	62	0.09	1.5
Previous design [36]	54	0.08	1.5
Previous design (design I) [37]	51	0.058	1.25
Previous design (design II) [37]	30	0.028	1.0
Previous design [38]	35	0.04	0.75
Previous design [39]	67	0.06	1.25
Previous design [40]	92	0.10	1.0
Previous design [41]	47	0.05	1.0
Previous design [42]	93	0.07	1.25
Previous design [43]	28	0.02	0.75
Previous design [44]	55	0.044	1.0
Previous design [45]	85	0.078	1.25
Previous design [46]	39	0.03	0.75
Previous design (design I) [47]	45	0.05	1.0
Previous design (design II) [47]	37	0.03	1.0

It can be noted that this approximation will be valid when n is large and ρ is small, i.e., $\rho << 1/\text{n}$. Now, for $\rho << 1/2$, the probability for undetected errors will be $(1/n - 2^{-n})$. So, the probability of undetected errors with parity check bits P is $\approx 2^{-P}$. It can be concluded that the proposed method has $1/(n+1)$ overhead, because parity check code padded an extra bit, i.e., 1 per n-bit information. Besides, the error pattern is a form of $(n+1)$ tuples having 1s in error place and 0s elsewhere. Out of binary $(n+1)$-tuples, 1/2 are odd and 1/2 are even. Thus, 50% of the error pattern is possible to detect. To detect more number of errors, more number of check bits must be padded with right codes.

C. PROPOSED XOR GATE AND EXISTING LAYOUTS

The proposed QCA circuit of XOR gate is compared with existing circuits [31]–[41] through Table 3. The proposed design has out shined the XOR gate reported in [31] by improving cell count as 6.89%, and area as 33.33%. A reduction of 27.03% and 11.11% in cell count over design I and design II of [32] are achieved, respectively whereas a reduction of 33.33% in area is achieved over both of the designs in [32]. 22.85% and 31.03% less number of QCA cell and area are required in the proposed circuit than the circuit reported in [33]. Similarly, the proposed design is compared with all the existing designs of XOR gate [34]–[41] and the results are explored in Table 3. The comparison confirms that the proposed XOR gate has higher device density and is faster than the existing ones.

D. PROPOSED PARITY GENERATOR AND PARITY CHECKER CIRCUIT AND EXISTING LAYOUTS

In this section, existing parity generator circuits [34]–[37], [39] as well as existing parity checker circuits [35], [37] are

TABLE 4. Proposed error detecting circuit and existing layouts.

QCA based circuit	Cell count	Area (μm^2)	Latency
Even parity generator			
Proposed	54	0.05	1.75
Previous design [34]	98	0.11	2.0
Previous design [35]	99	0.17	2.0
Previous design [36]	168	0.28	2.75
Previous design [37]	60	0.053	2.0
Previous design [39]	188	0.2	2.25
Previous design [47]	82	0.08	2.0
Previous design [39]	109	0.17	0.75
Previous design [43]	87	0.10	1.75
Even parity checker			
Proposed	96	0.08	1.75
Previous design [35]	145	0.28	3.0
Previous design [37]	117	0.13	2.25
Previous design [44]	179	0.23	2.0
Previous design [47]	111	0.14	2.0
Previous design [48]	220	0.38	1.25

compared with the proposed parity generator and the parity checker circuit, respectively. The results are explored through Table 4. The comparison proves that the proposed parity generator and the parity checker circuit are much denser and faster than the existing ones.

E. ANALYSIS OF DEFECTS FOR PROPOSED QCA DESIGNS

This section explores the defects of proposed QCA circuit. The analysis is achieved by observing the effect caused by single missing/additional QCA cell on the proposed circuit [49]. The testing is carried out as follows.

- First, the QCA layout of XOR gate, parity generator circuit and parity checker circuit is labeled according to cell position as shown in Fig. 9(a), Fig. 9(b) and Fig. 9(c), respectively.
- Second, the cells are marked by their grid positions. For example, in Fig. 9(a), the name 'J2' is marked for the cell just right side to the input cell A. The name 'J2' indicates the J^{th} row and 2^{th} column.
- Next, all the proposed QCA circuits are simulated using QCADesigner simulator tool [50] for every missing/additional QCA cell.
- The simulation results are examined.

The simulation parameters that are used during simulation are as follows.

$$\begin{aligned}
&\text{Cell type} = \text{Electrostatic QCA cell}\\
&\text{Distance between two cell} = 2\text{nm}\\
&\text{Diameter of quantum-dot} = 5\text{nm}\\
&\text{Relaxation time} = 1.0\text{e} - 15\text{s}\\
&\text{Time-step value} = 1.0\text{e} - 16\text{s}\\
&\text{Total simulation time} = 7.0\text{e} - 11\text{s}
\end{aligned}$$

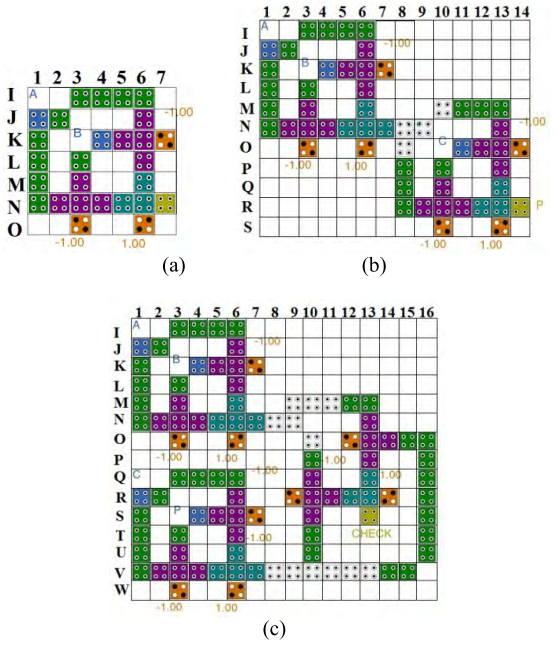

FIGURE 9. Design layer and the grid position of different cells of proposed (a) XOR gate, (b) Parity generator circuit, and (c) Parity checker circuit.

$$\begin{aligned}
&\text{Clock amplitude factor} 2.0\\
&\text{Clock-high} = 9.8\text{e} - 22\text{J}\\
&\text{Clock-low} = 3.8\text{e} - 23\text{J}\\
&\text{Relative permittivity} 12.9\\
&\text{Radius of effect} = 80\text{nm}\\
&\text{Layer separation} = 11.5\text{nm}
\end{aligned}$$

1) DEFECTS IN PROPOSED XOR GATE

Based on assessment of simulation result of proposed XOR circuit, the probable missing/additional QCA cell based defects in the designs are explored through Table 5 to Table 6, respectively. Table 5 shows the missing cell based defects in proposed XOR gate. Table 5 illustrates that if the cell I5 or K1 or L1 is missing, there is no effect on the output and the circuit is fault free. But if either the cell I3 or I4 is missing, generates the output 1. Test vector (11) can be used to identify this fault. The test vector (11) has an expected output 0. Therefore, the fault at output can easily be noticed by comparing the faulty output 1 with expected output 0. Similarly, for all probable missing QCA cell based defects, they are noticed and placed in Table 5. Table 6 shows the additional cell based defects in proposed XOR gate. It can be seen from Table 6 that the additional cell I7 or J5 has no effect on the output and the output is therefore fault free. For an additional cell I2 or J3 or J7, the faulty output 0 is produced. To identify this fault, the test vector (01) can be applied. The correct output corresponding to test vector (01) is 1. By comparing the correct output 1 and faulty output 0, the fault can easily be noticed. Similarly for all probable additional QCA cell based defects, they are identified and explored in Table 6.

TABLE 5. Single missing cell effect on Xor gate.

Location of missing cell (Fig. 9(a))	Test vector (AB)	Expected output (O)	Faulty output (O)
I3, I4, J2	11	0	1
I5		Fault free	
I6, J6, K5	01	1	0
K1, L1		Fault free	
K6, L6, M6	00	0	1
L3, M1, M3, N1	10	1	0
N2, N6	10	1	0
N3- N5	00	0	1

TABLE 6. Single addition cell effect on Xor gate.

Location of missing cell (Fig. 9(a))	Test vector (AB)	Expected output (O)	Faulty output (O)
I2, J3, J7	01	1	0
I7, J5		Fault free	
J4, L2, L4	11	0	1
K2, K3	10	1	0
L5, M2, M4, M5, M7		Fault free	
L7, O1, O2, O4	01	1	0
O5, O7		Fault free	

2) DEFECTS IN ERROR DETECTION CIRCUIT

By evaluating the simulation result, all probable missing and additional QCA cell based defects in the proposed parity generator are noticed and explored through Table 7 to Table 8, respectively. Table 7 deals with the exploration of missing cell based defects in the parity generator circuit. Table 7 shows that if the cell I5 or K1 or L1 or M11 is missing, there is no change in the output value and the circuit remains fault free. But if either the cell I3 or I4 is missing, generates the output value 0. Test vector (010) can be used to identify this faulty output. The test vector (010) has the acceptable output 1. Therefore, the faulty output value 0 can easily be noted by comparing the faulty output 0 with expected output 1. Similarly, for all probable missing QCA cell based defects of the parity generator are noticed and described in Table 7.

The corresponding additional cell based defects are illustrated in Table 8. It can be observed from Table 8 that the additional cell I7 or J5 or L5 etc. has no effect on the output value and the output, which is therefore fault free. But the additional cell I2 or J3 or J4 caused the faulty output 0. To detect this fault, the test vector (010) can be applied. The required output for test vector (010) is 1. Thus, the fault can easily be noticed. All probable additional QCA cell based defects for the proposed parity generator are examined and explored in Table 8. Similarly, defects caused by missing and additional QCA cell in the proposed parity checker circuit are analyzed and explored through Table 9 and Table 10.

3) DEFECT COVERAGE BY THE PROPOSED TEST VECTORS

The defect coverage with the proposed test vectors or XOR gate, parity generator and parity checker circuit is shown through Table 11-12. Table 11 shows the defect coverage

TABLE 7. Single missing cell effect on parity generator circuit.

Location of missing cell (Fig. 9(b))	Test vector (AB)	Expected output (O)	Faulty output (O)
I3, I4, J2, K6, L6	010	1	0
I5		Fault free	
I6, J6	111	1	0
K1, L1		Fault free	
K5	110	0	1
L3, M1, M3,	000	0	1
M6, M12, M13, N1, N2	010	1	0
M10	000	0	1
M11, N7, N9, O8, P8		Fault free	
N3-N6	010	1	0
N8	111	1	0
N13, O12, R13	010	1	0
O13, P13, Q13	000	0	1
P9, Q8, Q9, R8, R9	111	1	0
R10, R11, R12	000	0	1

TABLE 8. Single extra cell effect on proposed parity generator circuit.

Location of missing cell (Fig. 9(b))	Test vector (AB)	Expected output (O)	Faulty output (O)
I2, L2, L4	010	1	0
I7, J5		Fault free	
J3, J4	010	1	0
J7, L7	111	1	0
K2, K3	000	0	1
L5, M2, M4, M5		Fault free	
M7, M8		Fault free	
M9, O2, O4, O10	000	0	1
M14, O1, O5, O7, O9		Fault free	
P7, P12		Fault free	
P9, P11	000	0	1
P14	010	1	0
Q7, Q9, Q11, Q12, Q14		Fault free	
R7, S7, S12, S14		Fault free	
S8, S9, S11	001	1	0

by the proposed test vector for XOR gate. It is seen from Table 11 that the test vectors <11, 01, 00, 10> have 100% defect coverage with single missing cells and test vectors <01, 11, 10> have 100% defect coverage with extra added cells. Thus, four test vectors, i.e., <11, 01, 00, 10> are required to detect all the faults caused by the defect cells in XOR gate.

Table 12 shows the defect coverage by the proposed test vector for parity generator circuit. It is clear from Table that the test vectors <010, 111, 110, 000> have 100% defect coverage with single missing cells and test vectors <010, 111, 000, 001> have 100% defect coverage with extra added cells. Thus, five test vectors, i.e., <010, 111, 000, 001, 110> are required to detect all the faults caused by the defect cells in parity generator circuit. Similarly, the defect coverage by the proposed test vectors in case of parity checker circuit is explored in Table 13.

4) POWER DISSIPATION OF THE PROPOSED QCA LAYOUTS

In a QCA circuit, each QCA cell dissipates equivalent energy [51]. Total power dissipated by any QCA circuit is

TABLE 9. Single missing cell effect on proposed parity checker circuit.

Location of missing cell (Fig. 9(c))	Test vector (AB)	Expected output (O)	Faulty output (O)
I3, I4, J2	1100	0	1
I5, K1, L1, M10, M11		Fault free	
I6, J6, K5	0100	1	0
K6, L6, N3- N5	0000	0	1
N7-N9, O13	0000	0	1
L3, M1, M3, M6, M9,	1000	1	0
N1-N2	1000	1	0
M12-M13, N6, N10	0100	1	0
N13, O14	0100	1	0
O15, O16, P16, Q16	0100	1	0
R16, S16	0100	1	0
O10, R6	0101	0	1
P10	1100	0	1
P13, Q13, R11, R12, S6	0000	0	1
Q3, Q4, R2	0011	0	1
Q5, S1, T1		Fault free	
Q6, Q10, R10, R13	0001	1	0
S5, S10, T10, V6	0001	1	0
T3, U1, U3, V1, V2	0010	1	0
T6, U6, U10	0000	0	1
V3-V5, V10	0000	0	1
T16, U16, V13-V15	0101	0	1
V7-V9, V11-V12		Fault free	

TABLE 10. Single extra cell effect on proposed parity checker circuit.

Location of missing cell (Fig. 9(c))	Test vector (AB)	Expected output (O)	Faulty output (O)
I2, J3, J7, L7	0101	0	1
I7, J5, L5, M2	Fault free		
J4, L2	1100	0	1
K2, K3, L4, O2, O4	1000	1	0
M4, M5, M7	Fault free		
M8, M14, O1	Fault free		
O5, O7, O8, P2	Fault free		
P7, P9, P11, P14	Fault free		
O9, O11, P3, P5	0001	1	0
Q2, R3, R7	0001	1	0
P4, P6, R4, T2	0011	0	1
P12, P15, Q15, S15	0100	1	0
Q1, Q7-Q9	Fault free		
Q11-Q12, Q14, R5	Fault free		
R8, S8, S9, S11, S12	Fault free		
R15	0101	0	1
S2, S3, T4	0010	1	0
S14	Fault free (weak signal)		
T5, T8, T9, T11	Fault free		
T12, T13, T14	Fault free		
T7	0001	1	0
T15, U2,U4	Fault free		
U5, U7,U8, U9	Fault free		
U11-U15, W5	Fault free		
W7-W16	Fault free		
V16	0100	1	0
W1, W2, W4	0010	1	0

mainly depends on the number of inverters and majority gates used to design the circuit [51]. Hamming distance based methodology proposed in [51] is utilized to estimate the dissipated energy by the proposed QCA circuits which is described in this section. During estimation, fan-out and QCA wire are also considered. The dissipated energy by the proposed circuits is outlined through Fig. 10. γ is used to denote tunnelling energy. E_k stands for kink energy. It is seen

TABLE 11. Defect coverage with the proposed test vectors for Xor gate.

Proposed test vector	Defect coverage (%)
Defect with missing cell	
11	14.29
01	28.57
00	28.57
10	28.57
Defect with extra cell	
01	50
11	25
10	25

TABLE 12. Defect coverage for parity generator circuit.

Proposed test vector	Defect coverage (%)
Defect with missing cell	
010	33.33
111	25
110	8.34
000	333.33
Defect with extra cell	
010	37.5
111	12.5
001	12.5
000	37.5

TABLE 13. Defect coverage for parity checker circuit.

Proposed test vector	Defect coverage (%)
Defect with missing cell	
1100	10
0100	25
0000	25
1000	10
0101	10
0011	5
0001	10
0010	5
Defect with extra cell	
0101	16.67
1100	8.33
1000	8.33
0001	25
0011	8.33
0010	16.67
0100	16.67

from Fig. 10 that the proposed designs have low dissipated energy. The dissipated energy by the parity generator and parity checker circuit is higher than XOR gate. This is because the parity generator and parity checker circuit have more

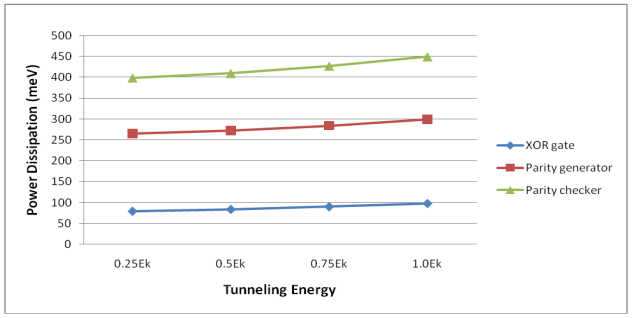

FIGURE 10. Power dissipated by proposed QCA layouts.

number of majority gates and inverters than the proposed XOR gate.

VI. CONCLUSION

The design of novel low power even parity generator and even parity checker is explored in this paper using QCA. The design is achieved by using a new XOR gate. This new layout of XOR gate is much faster and denser than existing ones in the literature. The proposed parity generator and parity checker has less number of cell count, area and latency than the existing designs. The bit-error coverage by the proposed method shows the efficiency of the error control codes. Single missing cell and extra deposited cell based defects in the proposed designs are explored to facilitate guide to proper implementation. The test vectors are use full to achieve 100% defect coverage. The estimation of dissipated energy shows that the layouts have very low energy dissipation. The testing of simulation result with truth table established the circuit's accuracy. The proposed design can be used as an essential building block in designing of QCA based transmitter and receiver for nanocommunication.

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