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Improved Space Vector Modulation of Quasi Z-Source Inverter to Suppress DC-Link Voltage Sag

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ABSTRACT The three traditional strategies ZSVM1, ZSVM2, and ZSVM6 have been commonly used to control the quasi Z-source inverter (qZSI). However, there is a serious problem that the dc-link voltage of the qZSI drops under light load, leading to the distortion of the output voltage and current of the inverter. The peak dc-link voltage also becomes much higher than its reference value, endangering the safety of the inverter and load. This paper proposes an improved SVM, namely M-ZSVM1, to suppress the dc-link voltage sag under a light load. Through analyzing the reason, the harm, and the influence factors of the dc-link voltage sag, the diode current interruption is seen as the cause of the dc-link voltage sag. Therefore, an asymmetric shoot-through state distribution method is presented to achieve the minimum current ripple, which can increase the diode current. The qZSI can work properly without the dc-link voltage sag under wide load range, improving the safety and reliability of the qZSI. Moreover, other improved ZSI topologies can also be controlled by the proposed strategy to suppress the dc-link voltage sag.

INDEX TERMS Quasi Z-source inverter, dc-link voltage sag, space vector modulation.

I. INTRODUCTION

In 2002, a new type of power converter topology Z-source inverter (ZSI) was proposed by Peng [1]. The ZSI can buck or boost input voltage by inserting the shoot-through state into the pulse width modulation (PWM), and the dead time is not required in the ZSI [2]. Unfortunately, the diode current is interrupted during the shoot-through state of the ZSI, causing a discontinuous dc source current which is not desired in solar cell, fuel cell, and other forms of source [3]. To solve this problem, the quasi Z-source inverter (qZSI) was proposed in 2008 [4]. Compared with the ZSI, the qZSI can sufficiently eliminate the problem of the discontinuous dc source current and reduce the voltage stress of capacitor [5]. As the shoot-through state is allowed in the ZSI and qZSI, the security and reliability of inverter are also highly improved [6], [7]. So far, the ZSI and qZSI topologies have been widely extended to improve their flexibility and efficiency, such as Z-source matrix inverter, trans-Z-source inverter, etc. [8]–[14].

The control strategies like ZSVM1, ZSVM2 and ZSVM6 have been developed since the space vector modulation (SVM) was introduced to control the qZSI [15]. However, these control strategies cause the problem of dc-link voltage sag under light load. Shen first found the problem and concluded that the ZSI has extra operation mode causing dc-link voltage sag when load power factor is low [16]. Recently, some papers have further reported the problem of dc-link voltage sag [17]–[19]. It is pointed out that when the diode current is discontinuous, a new state of the qZSI called discontinuous conduction mode (DCM) or abnormal operation state will appear. The influences and causes of the abnormal state are further analyzed.

The above research indicates that the methods for suppressing the dc-link voltage sag need to be studied. In [20], Zimmermann pointed out that light load can not be achieved by using the common SVM. He then proposed a modified SVM and added an anti-parallel switch in ZSI to overcome this limitation. However, if the switch is not reliably turned off

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during the shoot-through state, the capacitors of the ZSI will be short-circuited, reducing the security of the ZSI. Based on ZSVM6 and ZSVM2, [21] and [22] proposed two control strategies for the ZSI to minimize inductor current ripple. The shoot-through time is calculated and rearranged according to active and null states to achieve the minimum current ripple. However, the relationship between the inductor current ripple and the dc-link voltage sag is not further analyzed, so the performances of the proposed two methods are not clarified in suppressing the dc-link voltage sag. Abarzadeh proposed a new modified ZSVM switching method by fixing the shoot-through location [23], and then the dc-link voltage sag is effectively reduced. However, the relationship between the dc-link voltage sag and the load is still not clear. The choice of Z-source network parameters is discussed in [24] and [25] for avoiding dc-link voltage sag. However, the size of ZSI may be increased if the problem of dc-link voltage sag is solved only from the perspective of hardware.

Although a big effort has been made so far to solve the problem of dc-link voltage sag, there are still two related problems unsolved. One is that the relationship between the dc-link voltage sag and the load is not clear, that is to say, how much the light load can be used is unknown. The other is that the relationship between the inductor current ripple and the dc-link voltage sag is not clarified. Although some strategies to reduce the inductor current ripple have been effectively reported, it is still unknown that how much they can help to suppress the dc-link voltage sag. Therefore, the analysis of the dc-link voltage sag should be quantitative rather than qualitative.

In this paper, a systematical and comprehensive analysis for the dc-link voltage sag of qZSI is given, including the reason, the harm, and the influence factors of the dc-link voltage sag. The analysis results indicate that the reason of the dc-link voltage sag is the diode current interruption, and the influence factors are the average inductor current, the dc-side current, and the inductor current ripple. Therefore, from the perspective of reducing the inductor current ripple, an improved SVM is proposed to enhance the ability of suppressing the dc-link voltage sag. The inductor current ripple is reduced through asymmetric arrangement of the two shoot-through states in the switching cycle, so that the diode current interruption is avoided, and the dc-link voltage sag is suppressed. The stable dc-link voltage ensures the safety and reliability of qZSI. The main contributions of this paper are as follows:

1) By analyzing the factors that cause the dc-link voltage sag, a method is presented to calculate the load power range of qZSI.

2) An improved SVM for qZSI is proposed to enhance the ability of suppressing dc-link voltage sag under the light load. The qZSI controlled by the proposed strategy can work properly under wide load range, improving the safety and reliability of the qZSI.

3) The proposed strategy can suppress dc-link voltage sag in ZSI and other improved ZSI such as switched inductor ZSI, Trans-ZSI, and T-ZSI because they belong the same family topology of the impedance source inverter which has the similar problem of the dc-link voltage sag. Therefore, the proposed strategy is general applicable.

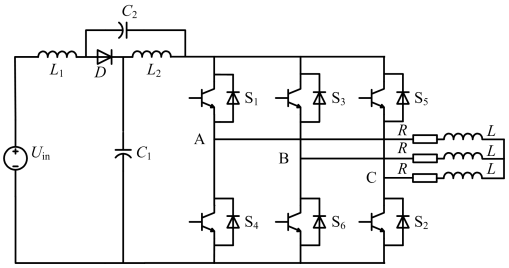

FIGURE 1. Topology of qZSI.

II. ANALYSIS OF DC-LINK VOLTAGE SAG IN ABNORMAL STATE OF QZSI

In this section, the reason for the abnormal state of qZSI is firstly explained. Then, the change of the dc-link voltage in the abnormal state is analyzed. Finally, the harm and the main influence factors of the abnormal state are analyzed in detail.

A. CAUSE ANALYSIS OF ABNORMAL STATE IN QZSI

The inductor of the quasi Z-source network discharges in the active state, leading to the decline of diode current. If the diode current decrease to zero, the equivalent circuit of qZSI will change. This results in the qZSI operating in the abnormal state.

As shown in Fig. 1, the qZSI consists of a quasi Z-source network, a two-level three-phase inverter, and an *RL* load. When the qZSI operates in the active and null states, the dc-source, the inductor L_1, and the capacitor C_1 constitute a loop, as shown in Fig. 2(a) and (b). The inductor voltage can be expressed by the voltages of the capacitor C_1 and the dc-source, which is given by

$$L_1 \frac{\mathrm{d}i_\mathrm{L}}{\mathrm{d}t} = U_{\mathrm{C1}} - U_{\mathrm{in}} \tag{1}$$

In the shoot-through state, the upper and lower bridge arms in the same phase are turned on, and the diode is in reverse biasing, as shown in Fig. 2 (c). The inductor L_2 and the capacitor C_1 constitute a loop, so the inductor voltage can be derived as

$$L_1 \frac{\mathrm{d}i_\mathrm{L}}{\mathrm{d}t} = U_{\mathrm{C1}} \tag{2}$$

where d_{sh} is the shoot-through duty ratio. If the same inductance is selected for the inductors L_1 and L_2, the currents of the two inductors will be the same, which brings benefit in qZSI design [4]. Therefore, the inductor L_2 is replaced by L_1 in (2).

The dc-link voltage U_{dc} in the active and null states is given by

$$U_{\mathrm{dc}} = \frac{1}{1 - 2d_{\mathrm{sh}}} U_{\mathrm{in}} \tag{3}$$

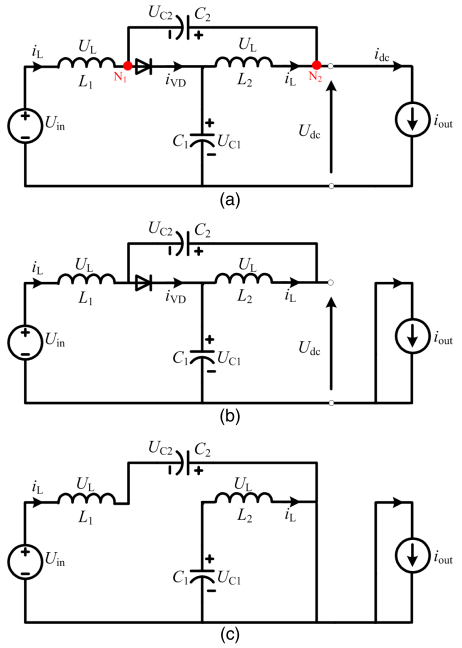

FIGURE 2. Equivalent circuits of qZSI in the (a) active state, (b) null state, and (c) shoot-through state.

The active state time T_1, T_2 and the null state time T_0 in the first sector can be expressed as

$$\begin{cases} T_1 = mT\sin(\pi/3-\theta) \\ T_2 = mT\sin\theta \\ T_0 = T - T_1 - T_2 = T - mT\cos(\theta-\pi/6) \end{cases} \tag{4}$$

where T is the switching cycle; θ is the phase angle of reference vector; m is the modulation index. When θ is $\pi/6$, the null state time T_0 gets the minimum value $T(1\text{-}m)$. As the shoot-through state time T_{sh} occupies the null state time, T_{sh} can not be greater than the minimum value of the null state time. The shoot-through state time satisfies

$$T_{sh} \le T_0 = T(1-m) \tag{5}$$

According to (5), the shoot-through duty ratio d_{sh} is

$$d_{sh} = T_{sh}/T \le (1-m) \tag{6}$$

According to (1), the inductor current in the active state can be derived as

$$i_L(t) = i_L(t_0) - \frac{1}{L_1}\int_{t_0}^{t}[U_{C1}(t) - U_{in}(t)]dt \tag{7}$$

where $i_L(t_0)$ is the initial value of the inductor current in the active state. According to the current equations of the node N_1 and N_2 in Fig. 2(a), the diode current is equal to the sum of the currents of the inductor L_1 and the capacitor C_2, and the current of the inductor L_2 is equal to the sum of the dc-side current i_{dc} and the current of the capacitor C_2. Therefore, the diode current can be derived as

$$i_{VD} = 2i_L - i_{dc} \tag{8}$$

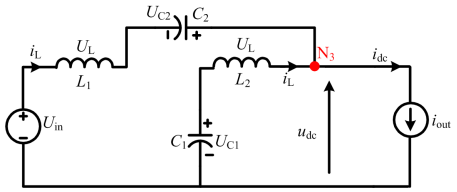

FIGURE 3. Equivalent circuit of qZSI in the abnormal state.

where i_{dc} is related to the three-phase output currents of qZSI, the cycle of which is much longer than the switching cycle of qZSI. Thus, i_{dc} is almost unchanged in one switching cycle. The diode current decreases with the decrease of the inductor current. By substituting (7) into (8), the diode current is

$$i_{VD}(t) = 2i_L(t_0) - i_{dc} - \frac{2}{L_1}\int_{t_0}^{t}[U_{C1}(t) - U_{in}(t)]dt \tag{9}$$

The diode current must be greater than zero in the active state. Otherwise, the equivalent circuit of the qZSI will change, causing the abnormal state. Fig. 3 shows the equivalent circuit of qZSI in the abnormal state. The capacitor C_1, the inductor L_2, and the load constitute a new loop, so the dc-link voltage is equal to the sum of the inductor voltage and the capacitor voltage, which can be expressed as

$$U_{dc} = U_{C1} + U_L \tag{10}$$

The dc-source, the inductor L_1, the capacitor C_2, and the load constitute a loop. The currents of the inductors L_1 and L_2 flow through the node N_3 and merge into i_{dc}, which can be expressed as

$$2i_L = i_{dc} \tag{11}$$

B. DC-LINK VOLTAGE SAG IN THE ABNORMAL STATE

In the abnormal state, as the inductor current remains almost unchanged in one switching cycle according to (11), the shoot-through duty ratio increases and the inductor voltage decreases to zero. The dc-link voltage is boosted to a higher value than its normal range in the duration of the continuous diode current and drops in the duration of the discontinuous diode current.

For convenience of comparison, the waveforms of the diode current, the dc-link voltage, and the inductor current are shown in Fig. 4 when the qZSI works in the normal and abnormal state. In Fig. 4 (b), the diode current decreases rapidly and then interrupts during $t_2 \sim t_3$. According to (11), the inductor current is equal to half of the dc-side current during $t_2 \sim t_3$, which can not abruptly change. Thus, the inductor is neither charged nor discharged during $t_2 \sim t_3$. This period of time is not the shoot-through time or the non-shoot-through time anymore, so the proportion of the shoot-through time will rise in the switching cycle, which can be rewritten as

$$d'_{sh} = \frac{T_{sh}}{T - T_{drop}} = \frac{d_{sh}}{1 - d_{drop}} \tag{12}$$

where T_{drop} and d_{drop} are the time and duty ratio of $t_2 \sim t_3$, respectively. The shoot-through duty ratio d'_{sh} in the abnormal

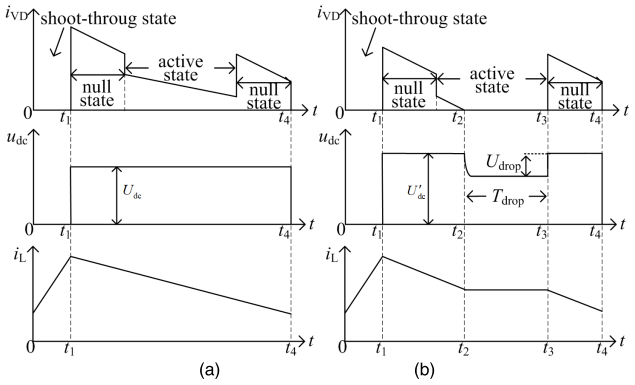

FIGURE 4. Waveforms of diode current, dc-link voltage, and inductor current in the (a) normal state and (b) abnormal state.

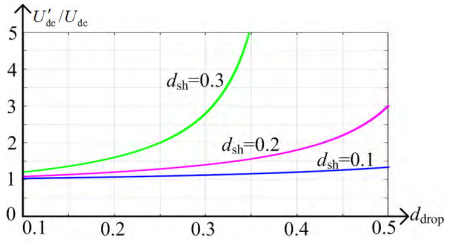

FIGURE 5. DC-link voltages with different d_{sh}.

state is actually higher than d_{sh} in the normal state. Therefore, the dc-link voltage U'_{dc} of the abnormal state is higher than that of the normal state U_{dc} during $t_1 \sim t_2$ and $t_3 \sim t_4$, which can be expressed as

$$U'_{dc} = \frac{1}{1-2d'_{sh}} U_{in} \tag{13}$$

$$\frac{U'_{dc}}{U_{dc}} = \frac{1\text{-}2d_{sh}}{1-2d_{sh}/(1-d_{drop})} \tag{14}$$

According to (14), the dc-link voltages with different d_{sh} are drawn in Fig. 5. Along with the increase of d_{drop}, the dc-link voltage becomes higher and higher. When $d_{drop} = 0.5$ and $d_{sh} = 0.2$, the dc-link voltage of the abnormal state is 3 times higher than that of the normal state. When $d_{drop} = 0.35$ and $d_{sh} = 0.3$, the dc-link voltage of the abnormal state is 5 times higher than that of the normal state. It is concluded that the amplitude of the dc-link voltage becomes uncontrollable. The excessive high dc-link voltage may destroy the inverter, threatening its safety and reliability.

In Fig. 4 (b), as the inductor current is fixed during $t_2 \sim t_3$, the inductor voltage drops to zero. According to (10), the dc-link voltage is equal to the voltage of the capacitor C_1, causing the dc-link voltage sag. The amplitude of the dc-link voltage sag U_{drop} can be derived as

$$U_{drop} = U'_{dc} - U'_{C1} = \frac{d'_{sh}}{1-2d'_{sh}} U_{in} \tag{15}$$

$$\frac{U_{drop}}{U'_{dc}} = d'_{sh} \tag{16}$$

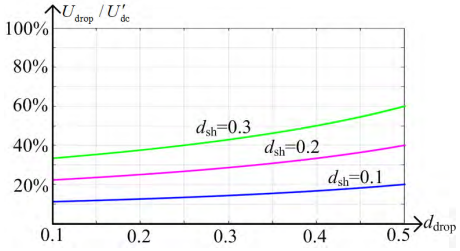

FIGURE 6. Sag degree of dc-link voltage.

It can be seen from (16) that the dc-link voltage drops d'_{sh} times, which is pictured in Fig. 6. When $d_{sh} = 0.1$, 0.2 and 0.3, the dc-link voltage drops 11%∼21%, 22%∼40%, and 33%∼60%, respectively.

The dc-link voltage sag results in the overshoot and instability of the dc-link voltage and the distortion of the output voltage and current. Hence, the safety and control performance of inverter are reduced, which is confirmed in the simulation and experimental results. Moreover, the normal work of many kinds of loads is influenced by the dc-link voltage sag. For example, if the load of qZSI is AC motor, the control principle of the voltage-frequency will not work in the speed control because the ratio of voltage-frequency is not constant under the unstable dc-link voltage. Therefore, large torque ripple is caused. When the qZSI works with the photovoltaic system, the maximum power point tracking will be inaccurate because the output power calculation is influenced by the unstable dc-link voltage.

C. INFLUENCE FACTORS OF DC-LINK VOLTAGE SAG IN THE ABNORMAL STATE

As the dc-link voltage sag is caused by the diode current interruption, the influence factors of the dc-link voltage sag are the average inductor current, the inductor current ripple, and the dc-side current according to (8). By analyzing these factors, we can come up with a solution to improve the diode current so that the dc-link voltage sag can be suppressed.

1) AVERAGE INDUCTOR CURRENT

The input power of qZSI P_{in} is equal to the output power P_{out}, which can be expressed as

$$P_{in} = U_{in} I_L = \frac{m^2 U_{in}^2 \cos\alpha}{2(1-2d_{sh})^2\sqrt{R^2+(\omega L)^2}} = P_{out} \tag{17}$$

where I_L is the average inductor current; α is the impedance angle; ω is the angular frequency of phase current. In (17), the input power is equal to the product of the dc source voltage and the inductor current, and the output power is calculated as per the dc-link voltage and the load. By solving (17), the average inductor current can be obtained as

$$I_L = \frac{P_{out}}{U_{in}} = \frac{m^2 U_{in} \cos\alpha}{2(1-2d_{sh})^2\sqrt{R^2+(\omega L)^2}} \tag{18}$$

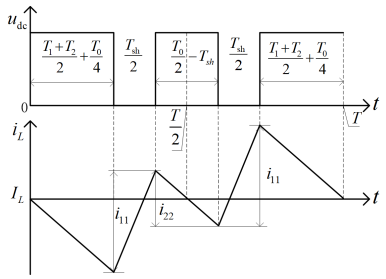

FIGURE 7. Instantaneous inductor current ripples of ZSVM1.

2) INDUCTOR CURRENT RIPPLE

The inductor current ripple of ZSVM1 in one switching cycle is shown in Fig. 7. The shoot-through time is divided into two equal parts, which are symmetric about $T/2$.

The instantaneous inductor current ripples $i_{1x}(x = 1, 2)$ of ZSVM1 in one switching cycle are given by

$$\begin{cases} i_{11} = \dfrac{U_{C1}}{L_1}\dfrac{T_{sh}}{2} = 6\,k\,(1 - d_{sh}) \\ i_{12} = \dfrac{U_{C1} - U_{in}}{L_1}\left(\dfrac{T_0}{2} - T_{sh}\right) \\ \qquad = 6\,k\left|m\cos\left(\theta - \dfrac{\pi}{6}\right) - 1 + 2\,d_{sh}\right| \end{cases} \tag{19}$$

where $k = (d_{sh}U_{in}T)/[12L_1(1\text{-}2d_{sh})]$. In (19), i_{11} and i_{12} represent the inductor current ripples in the shoot-through state and the non-shoot-through state, respectively. As the T_0 is related to θ, i_{12} is the function of θ.

According to (19), the inductor current ripple in the first sector can be expressed as

$$i_1 = 2i_{11} - i_{12}, 0 \le \theta \le \pi/3 \tag{20}$$

3) DC-SIDE CURRENT ANALYSIS

Since the dc-side current flows through the quasi Z-source network into the three-phase load, it can be solved by analyzing the change rules of the three-phase output currents. Thus, the three-phase output currents in the first sector are analyzed as an example.

i_a, i_b, and i_c are the three-phase output currents. When i_b is less than zero and the active vector V_1 is applied, the switches S_1, S_2 and S_6 are turned on. i_{dc} flows from S_1 into S_2 and S_6. Thus, i_{dc} is equal to i_a. When V_2 is applied, the switches S_1, S_2 and S_3 are turned on. i_{dc} flows from S_1 into S_2. However, i_b flows from S_1 into the upper freewheeling diode of B-phase bridge arm. Thus, i_{dc} is equal to i_c.

As i_b increases, it will be greater than zero. When the active vector V_1 is applied, i_{dc} flows from S_1 into S_2. Thus, i_{dc} is equal to i_a. When V_2 is applied, i_{dc} flows from S_1 and S_3 into S_2. Thus, i_{dc} is equal to i_c.

According to the analysis above, the dc-side current i_{dc} in one switching cycle is

$$i_{dc} = \begin{cases} |i_a|\,(vector = T_1, i_b < 0) \\ |i_c|\,(vector = T_2, i_b < 0) \\ |i_a|\,(vector = T_1, i_b > 0) \\ |i_c|\,(vector = T_2, i_b > 0) \end{cases} \tag{21}$$

In (21), i_{dc} is changed with the active vectors and i_b. Furthermore, i_{dc} is related to the switching state. For example, when only the upper switch of A-phase bridge arm is turned on among the three upper switches of inverter, i_{dc} will be equal to i_a. According to (21), i_{dc} in the sector becomes

$$\begin{aligned} i_{dc} &= \max(|i_a|, |i_c|) \\ &= \begin{cases} |i_a| = \left|\dfrac{mU_{in}\cos\varphi}{\sqrt{3}(1 - 2d_{sh})\sqrt{R^2 + (\omega L)^2}}\right| (i_b < 0) \\ |i_c| = \left|\dfrac{mU_{in}\cos(\varphi - \frac{4}{3}\pi)}{\sqrt{3}(1 - 2d_{sh})\sqrt{R^2 + (\omega L)^2}}\right| (i_b > 0) \end{cases} \end{aligned} \tag{22}$$

where φ *is* the phase angle of the output current. In (22), i_{dc} in the sector is a piecewise function, which is related to φ. i_a and i_c can be derived based on the dc-link voltage and load.

According to the Clarke transformation, the reference voltage of SVM (U_α) maintains the same phase angle θ with A-phase voltage. The A-phase current lags behind A-phase voltage for the impedance angle α degree. Thus, the relationship between θ and φ can be derived as

$$\theta = \varphi + \alpha \tag{23}$$

By substituting (23) into (22), (22) can be simplified as

$$i_{dc} = \begin{cases} |i_a| = \left|\dfrac{mU_{in}\cos(\theta - \alpha)}{\sqrt{3}(1 - 2d_{sh})\sqrt{R^2 + (\omega L)^2}}\right|, \\ \qquad 0 < \theta < \dfrac{\pi}{6} + \alpha \\ |i_c| = \left|\dfrac{mU_{in}\cos(\theta - \alpha - \frac{4}{3}\pi)}{\sqrt{3}(1 - 2d_{sh})\sqrt{R^2 + (\omega L)^2}}\right|, \\ \qquad \dfrac{\pi}{6} + \alpha < \theta < \dfrac{\pi}{3} \end{cases} \tag{24}$$

In (24), i_{dc} is the function of θ. In (20), the inductor current ripple is also the function of θ. Unifying the variable θ in the two equations is very convenient for analyzing the reason of the dc-link voltage sag.

The influence factors of the dc-link voltage sag have been discussed deeply. According to (8), (18), (20), and (24), the diode current should be increased in the active state in order to prevent the dc-link voltage sag, which requires large average inductor current, small dc-side current, and small inductor current ripple. Unfortunately, the average inductor current and the dc-side current are directly decided by the load and the dc source voltage that can not be changed. However, the inductor current ripple can be reduced by modifying the control strategy. In the next section, an improved control strategy is proposed to suppress the dc-link voltage sag, preventing the occurrence of the abnormal state.

III. IMPROVED SVM STRATEGY M-ZSVM1 TO SUPPRESS DC-LINK VOLTAGE SAG

In ZSVM1, the discharging time of inductor is too long in the switching cycle, leading to large inductor current ripple. Therefore, the diode current declines too much and is

prone to interrupt. In this paper, an improved SVM strategy is proposed to suppress the dc-link voltage sag of the qZSI, namely M-ZSVM1. In the proposed strategy, the shoot-through time is divided into two equal parts. The position of the shoot-through state is rearranged to ensure that the discharging and charging inductor current ripples are equal. Thus, the inductor current ripple is greatly reduced. The inductor and diode currents do not dramatically decline in the active state, avoiding the diode current interruption. The qZSI can work properly without dc-link voltage sag under wide load range. The stable dc-link voltage is provided for the load through applying the proposed strategy, improving the safety and reliability of the qZSI. Furthermore, the proposed strategy can be applied not only in the qZSI but also in the ZSI and other improved ZSI such as switched inductor ZSI, Trans-ZSI, and T-ZSI because they are the same family topology of the impedance source inverter which all have the problem of the dc-link voltage sag under light load.

In this section, the improved SVM strategy of suppressing dc-link voltage sag is firstly presented. Secondly, the diode currents and the load power ranges of the proposed strategy and ZSVM1 are compared to show the strong abilities of suppressing the dc-link voltage sag in the proposed strategy. Thirdly, the power loss and efficiency of the proposed strategy are discussed.

A. IMPROVED SVM STRATEGY–M-ZSVM1

In order to analyze the principle of suppressing the dc-link voltage sag, the relationship of the diode current and inductor current ripple is firstly given. Then, the shoot-through strategy with the minimum inductor current ripple is proposed to suppress the dc-link voltage sag.

The discharging inductor current ripple of ZSVM1 in $T_1/2+T_2/2+T_0/4$ in Fig. 7 can be moved from the beginning of the switching cycle to the end, as shown in Fig. 8. That the inductor current rapid increases during $0\sim t_3$ and substantial declines during $t_3 \sim t_4$ results in large inductor current ripple in the switching cycle. In Fig. 8, the inductor current fluctuates near its average value, so the inductor current can be expressed by the average inductor current and the inductor current ripple as per (18) and (20), which is given as follows

$$i_{\mathrm{L}} = I_{\mathrm{L}} - \frac{i_1}{2} \tag{25}$$

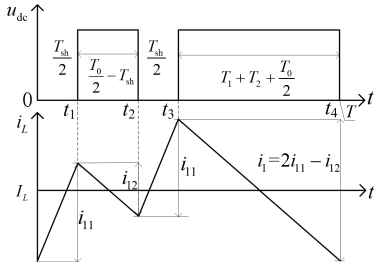

FIGURE 8. Equivalent inductor current ripple of ZSVM1.

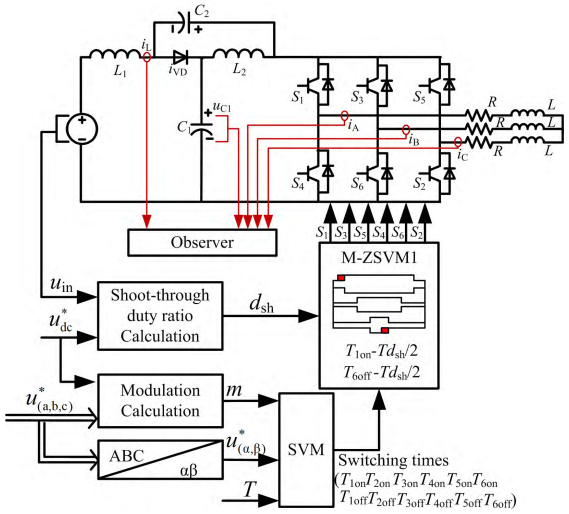

FIGURE 9. Control block diagram of the proposed strategy.

According to (8), the diode current gets the minimum value when the inductor current gets the minimum value. Thus, by substituting (25) into (8), the relationship between the diode current and the inductor current ripple is

$$i_{\mathrm{VD}} + i_1 = 2I_{\mathrm{L}} - i_{\mathrm{dc}} \tag{26}$$

In (26), the average inductor current I_{L} and the dc-side current i_{dc} all remain constant in the switching cycle, thus the sum of the diode current and the inductor current ripple is fixed in the switching cycle. If the inductor current ripple is too large, the diode current will be too small to prevent the diode current interruption in the active state. Therefore, reducing inductor current ripple is an effective way to prevent diode current interruption and suppress dc-link voltage sag.

The control block diagram of the proposed strategy is given in Fig. 9. Firstly, the references should be calculated. The shoot-through duty ratio d_{sh} is calculated due to (3). The modulation index m is derived due to the references of dc-link voltage $u_{\mathrm{dc}}*$ and output voltage $u_{(\mathrm{a,b,c})}*$. The reference of output voltage on $\alpha\beta$ axes $u_{(\alpha,\beta)}*$ is obtained by using the Clarke transformation. Secondly, as the input of space vector pulse width modulation (SVM), $u_{(\alpha,\beta)}*$, m, and control cycle T are used to generate six PWM control signals. Thirdly, the shoot-through time is calculated for inserting the shoot-through state into the PWM control signals.

The changed inserting position of the shoot-through state in the proposed strategy is shown in Fig. 10. In Fig. 10(a), the shoot-through states are inserted into the first half of the switching cycle before $T_1/2$ and the second half of the switching cycle before $T_2/2$. In Fig. 10(b), the shoot-through states are inserted into the first half of the switching cycle after $T_2/2$ and the second half of the switching cycle after $T_1/2$. Although the positions of the shoot-through state in Fig. 10(a) and 10(b) are different, their inductor current ripples are the same, as shown in Fig. 10(c) and (d). According to the principle of the volt-second balance, the charging inductor current ripple i_{M11} is equal to the discharging inductor current

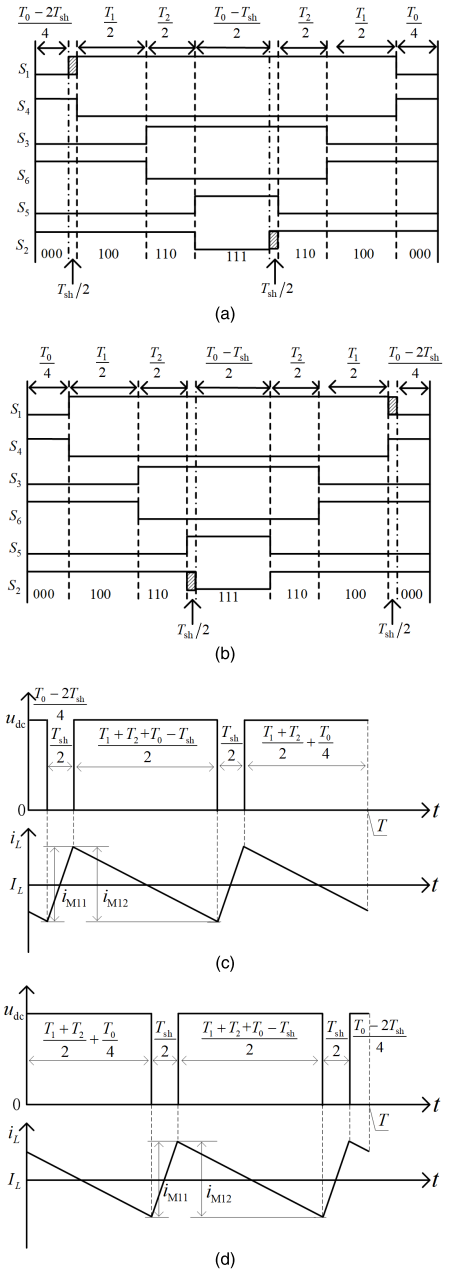

FIGURE 10. Switching sequences and inductor current ripples of the proposed strategy. Switching sequences of (a) Case I and (b) Case II. Inductor current ripples of (c) Case I and (d) Case II.

ripple i_{M12}, which can be calculated by

$$\begin{cases} i_{M11} = T_{sh}U_{C1}/2L_1 = 6k(1-d_{sh}) \\ i_{M12} = (T_1+T_2+T_0-T_{sh})(U_{in}-U_{C1})/2L_1 \\ \qquad = 6k(1-d_{sh}) \end{cases} \tag{27}$$

The two shoot-through states of the proposed strategy are reasonably distributed, thus the inductor current ripple of M-ZSVM1 is significantly reduced compared with that of ZSVM1. According to (26), the diode current of M-ZSVM1 will increase greatly compared with that of ZSVM1.

In order to insert the two equal shoot-through states, the switching time of the switches S_1 and S_2 have to be calculated and changed in the proposed strategy. However, only the switching time of S_2 need to be modified in ZSVM1 because of the symmetric switching sequence. Thus, the calculation of switching time is more complicated than ZSVM1. Besides, the asymmetric switching sequence of the proposed strategy may bring few harmonics, but the amplitude of harmonics is very small as the time of shoot-through state is very short.

B. COMPARISON OF M-ZSVM1 AND ZSVM1 FOR SUPPRESSING DC-LINK VOLTAGE SAG

In order to analyze the ability of suppressing dc-link voltage sag, the diode currents and load power ranges of M-ZSVM1 and ZSVM1 are compared under different shoot-through duty ratios and modulation indices.

According to (8), (18), (24), (20), and (27), the diode currents of M-ZSVM1 and ZSVM1 are calculated by

$$i_{VDM1} = \frac{\sqrt{3}m\cos\alpha(2P_{out} - U_{in}i_{M1}) - 2P_{out}(1-2d_{sh})f_u}{\sqrt{3}mU_{in}\cos\alpha} \tag{28}$$

$$i_{VD1} = \frac{\sqrt{3}m\cos\alpha(2P_{out} - U_{in}i_1) - 2P_{out}(1-2d_{sh})f_u}{\sqrt{3}mU_{in}\cos\alpha} \tag{29}$$

where $i_{M1} = 12mk\cos(\theta\text{-}\pi/6) - 6k(1-d_{sh})$ and

$$f_u = \begin{cases} \cos(\theta-\alpha), & 0 < \theta < \dfrac{\pi}{6}+\alpha \\ \cos\left(\theta-\alpha+\dfrac{4}{3}\pi\right), & \dfrac{\pi}{6}+\alpha < \theta < \dfrac{\pi}{3} \end{cases}$$

In (28) and (29), if the minimum values of i_{VDM1} and i_{VD1} are lower than zero, the diode current will be interrupted. The minimum values of the diode currents of M-ZSVM1 and ZSVM1 are pictured in Fig. 11 by using the qZSI parameters (shown in section IV).

In Fig. 11(a), the diode current of M-ZSVM1 is continuous in the modulation index range of 0.5 to 0.8, which 3 times wider than that of ZSVM1. In Fig. 11(b), the diode currents of M-ZSVM1 and ZSVM1 both increase a lot when d_{sh} increases from 0.1 to 0.2. The modulation range of M-ZSVM1 without the diode current interruption is changed from 0.5∼0.8 to 0.3∼0.8. However, the modulation range of ZSVM1 without diode current interruption is 0.68∼0.8 that changes a little. This proves that the increased d_{sh} does

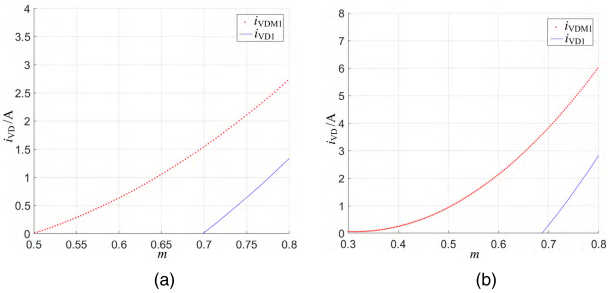

FIGURE 11. Minimum diode currents of M-ZSVM1 and ZSVM1 when (a) $d_{sh} = 0.1$ and (b) $d_{sh} = 0.2$.

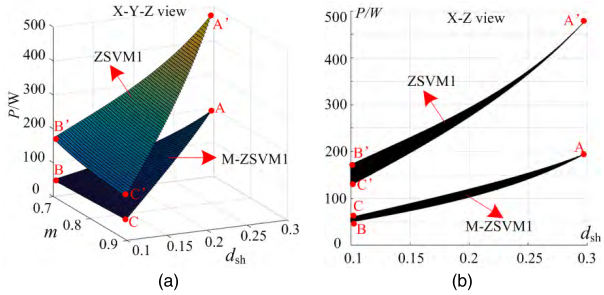

FIGURE 12. Critical condition of dc-link voltage sag in M-ZSVM1 and ZSVM1. (a) X-Y-Z view. (b) X-Z view.

nothing with suppressing the dc-link voltage sag in ZSVM1, but it has remarkable effects in M-ZSVM1. From the above analysis, M-ZSVM1 has stronger ability to suppress dc-link voltage sag than ZSVM1, ensuring the normal work of qZSI.

The load power range is another verification of suppressing dc-link voltage sag. By substituting (18), (24), (20), and (27) into (8), the load power ranges of M-ZSVM1 and ZSVM1 without dc-link voltage sag are calculated by

$$P_{M1} = \frac{\sqrt{3}mU_{in}i_{M1}\cos\alpha}{2\sqrt{3}m\cos\alpha + 2(2d_{sh}-1)f_u} \tag{30}$$

$$P_1 = \frac{\sqrt{3}mU_{in}i_1\cos\alpha}{2\sqrt{3}m\cos\alpha + 2(2d_{sh}-1)f_u} \tag{31}$$

In (30) and (31), P_{M1} and P_1 are the critical conditions of the dc-link voltage sag in M-ZSVM1 and ZSVM1, respectively. The load powers of M-ZSVM1 and ZSVM1 should be greater than P_{M1} and P_1, respectively. Otherwise, the dc-link voltage will drop. By substituting the qZSI parameters (shown in section IV) into (30) and (31), P_{M1} and P_1 are pictured in different d_{sh} and m, as shown in Fig. 12(a). Fig. 12(b) shows the X-Z view of Fig. 12(a), in which the axis of modulation index becomes a point. As d_{sh} and m must satisfy (6), P_{M1} and P_1 form two triangular surfaces (ABC and A'B'C'). The vertexes 'A' and 'A'' of the two triangles are at the high power, and the other points 'B', 'B'', 'C', and 'C'' of the two triangles are at the low power. The load power ranges of M-ZSVM1 and ZSVM1 without the dc-link voltage sag are the areas above the two triangular surfaces. When $m = 0.7$ and $d_{sh} = 0.3$, P_{M1} and P_1 are equal to 191W and 471W, respectively. The load powers from 191W-471W can be used in M-ZSVM1, but it can not be used in ZSVM1. When $m = 0.7$ and $d_{sh} = 0.1$, P_{M1} and P_1 are equal to 49W and 172W, respectively. When $m = 0.9$ and $d_{sh} = 0.1$, P_{M1} and P_1 are equal to 59W and 131W, respectively. Therefore, P_{M1} is 0.28 times of P_1 at least and 0.46 times of P_1 at most. P_{M1} is all lower than P_1, so M-ZSVM1 broadens the load power range. The load power area between the triangular surfaces of M-ZSVM1 and ZSVM1 (AA'BB'CC') is the broadened area of M-ZSVM1.

C. POWER LOSS AND EFFICIENCY

The power losses and efficiencies of the proposed strategy and ZSVM1 are calculated by using the method in [26] and [27]. As the proposed strategy and ZSVM1 have the same times and duration of shoot-through state, the power losses and efficiencies of the two strategies are the same when dc-link voltage does not drop. The total power loss consists of inverter switches power loss and quasi Z-source network power loss. The efficiency can be calculated as per the relationship between input power and power loss of the qZSI.

1) INVERTER SWITCHES POWER LOSS

a: SWITCHING LOSS

The switching loss of the MOSFET includes the turn on/off loss and the reverse recovery loss of the anti-parallel diode. In the non-shoot-through state, there is

$$\begin{cases} P_{s\_NST} = P_{s\_NST\_a} + P_{s\_NST\_b} + P_{s\_NST\_c} \\ P_{s\_NST\_a} = 2[\frac{3}{\pi}\int_0^{\frac{\pi}{3}}(U_{dc}|i_a|\frac{tri+tfu}{2}f_s)d\omega t + \frac{Q_{rr}U_{dc}f_s}{2} \\ \qquad \pi\int_0^{\frac{\pi}{3}}(U_{dc}|i_a|\frac{tru+tfi}{2}f_s)d\omega t] \\ P_{s\_NST\_b} = 2[\frac{3}{\pi}\int_0^{\frac{\pi}{3}}(U_{dc}|i_b|\frac{tri+tfu}{2}f_s)d\omega t + \frac{Q_{rr}U_{dc}f_s}{2} \\ \qquad +\frac{6}{\pi}\int_0^{\frac{\pi}{3}}(U_{dc}|i_b|\frac{tru+tfi}{2}f_s)d\omega t] \\ P_{s\_NST\_c} = 2[\frac{3}{\pi}\int_0^{\frac{\pi}{3}}(U_{dc}|i_c|\frac{tri+tfu}{2}f_s)d\omega t + \frac{Q_{rr}U_{dc}f_s}{2} \\ \qquad +\frac{6}{\pi}\int_0^{\frac{\pi}{3}}(U_{dc}|i_c|\frac{tru+tfi}{2}f_s)d\omega t] \end{cases} \tag{32}$$

where tri is the current rise time; tfu is the voltage fall time; tru is the voltage rise time; tfi is the current fall time; Q_{rr} is the reverse recovery charge. They are available in the datasheet. P_{s_NST} is the total switching loss of non-shoot-through state including the switching loss of each bridge arm ($P_{s\_NST\_a}$, $P_{s\_NST\_b}$, and $P_{s\_NST\_c}$).

In the shoot-through state, the current flowing through the switches is $2I_L$. The switching loss is derived as

$$P_{s\_ST} = U_{dc}(2I_L)\frac{tri+tfu+tru+tfi}{2}f_s + \frac{3}{2}Q_{rr}U_{dc}f_s \tag{33}$$

b: CONDUCTION LOSS

The conduction loss consists of the switch loss in forward conduction and the conduction loss of freewheeling diode, which are caused by the voltage drop of switching devices. In the non-shoot-through state, there are

$$\begin{cases} P_{con\_NST} = \sum_{x=a,b,c}(P_{conup\_NST\_x} + P_{condown\_NST\_x}) \\ P_{conup\_NST\_x} = \frac{3}{\pi}\int_0^{\frac{\pi}{3}}(R_{DS(on)}i_x^2\frac{T_x}{T})d\omega t \\ \qquad +\frac{3}{\pi}\int_0^{\frac{\pi}{3}}[(u_{D0}|i_x| + R_D i_x^2)(1-\frac{T_x}{T}-d_{sh})]d\omega t \\ P_{condown\_NST\_x} = \frac{3}{\pi}\int_0^{\frac{\pi}{3}}(R_{DS(on)}i_x^2(1-\frac{T_x}{T}-d_{sh}))d\omega t \\ \qquad +\frac{3}{\pi}\int_0^{\frac{\pi}{3}}[(u_{D0}|i_x| + R_D i_x^2)\frac{T_x}{T}]d\omega t \end{cases} \tag{34}$$

where $R_{DS(on)}$ is the drain-source on-state resistance of the MOSFET; u_{D0} is the on-state zero-current voltage; R_D the

on-state resistance of the anti parallel diode. i_x $(x = a, b, c)$ are three-phase currents; T_x $(x = a, b, c)$ are the turn on time of the three upper switches; P_{con_NST} is the total conduction loss of non-shoot-through state including the conduction loss of upper and lower switches ($P_{conup\_NST\_x}$ and $P_{condown\_NST\_x}$). When the upper switch is turned on, the lower switch of the same phase bridge arm is turned off. Therefore, the forward conduction time of the upper switch, T_x, is the same as the freewheeling time of the upper anti-parallel diode. The analysis for the case when the lower switch is turned on is similar to the previous analysis.

In the shoot-through state, the upper and lower switches of same phase bridge arm are tuned on, so that the current flowing through the switches is twice of the inductor current. Thus, the conduction loss in shoot-through state can be expressed as

$$P_{con\_ST}=2[R_{DS(on)}(2I_L)^2 d_{sh}^2] \tag{35}$$

2) POWER LOSS OF QUASI Z-SOURCE NETWORK

The total quasi Z-source network power loss (P_{ZSN}) includes the power losses of the two inductors (P_{ZSN_L}), the two capacitors (P_{ZSN_C}), and the diode (P_{ZSN_VD}). They are calculated as follows

$$\begin{cases} P_{ZSN} = P_{ZSN\_L} + P_{ZSN\_C} + P_{ZSN\_VD} \\ P_{ZSN\_L} = 2d_{sh}^2 I_L^2 r_L + 2(1\text{-}d_{sh})^2 I_L^2 r_L \\ P_{ZSN\_C} = 2d_{sh}^2 I_L^2 r_C + 2(1\text{-}d_{sh})^2 (I_L - I_{dc})^2 r_C \\ P_{ZSN\_VD} = (1 - d_{sh})^2 (2I_L - I_{dc})^2 U_f \end{cases} \tag{36}$$

where r_L is the equivalent series resistance of the inductors; r_C is the equivalent series resistance of the capacitors; U_f is the forward voltage of the diode.

3) EFFICIENCY

After obtaining the power loss, the efficiency is equal to the subtraction between the input power and the power loss, which can be express as

$$\eta = \frac{P_{in} - P_{con\_NST} - P_{con\_ST} - P_{s\_NST} - P_{s\_ST} - P_{ZSN}}{P_{in}} \tag{37}$$

By using the above formulas and the devices parameters in the experiment, the power loss of the qZSI with the proposed strategy is calculated at different load powers. As shown in Fig. 13, the total power loss reduces with the decrease of the load power. The power losses of the inverter switches and the quasi Z-source network all account for nearly half of the total loss. In the power loss of the quasi Z-source network, the power loss of the diode is the biggest. Additionally, the power loss of ZSVM1 will be the same as the proposed strategy if the dc-link voltage does not drop.

IV. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

To verify the strong ability of suppressing dc-link voltage sag of the proposed strategy, a three-phase *RL*-load of qZSI is built in MATLAB/Simulink. Simulations of the proposed strategy and ZSVM1 are conducted under the light load. Simulation parameters are given in TABLE 1.

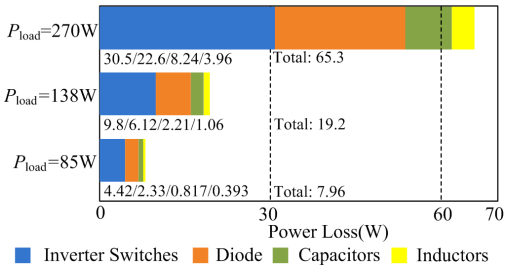

FIGURE 13. Power loss distribution of qZSI.

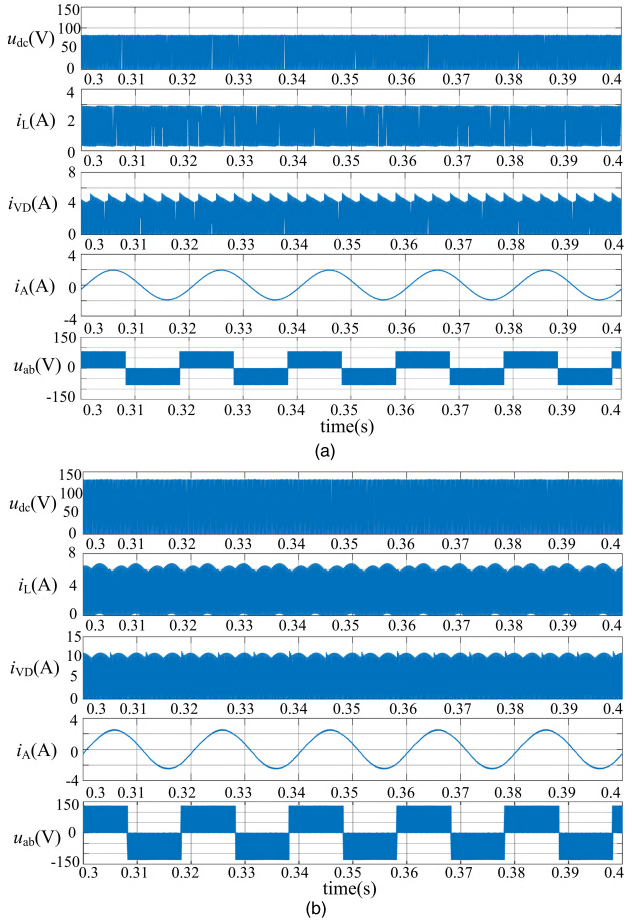

FIGURE 14. Simulation results of dc-link voltage, inductor current, diode current, output current, and line voltage in line period when load power is 85W. (a) M-ZSVM1. (b) ZSVM1.

TABLE 1. Simulation and experimental parameters.

parameter	symbol	value
dc source voltage	U_{in}	50 V
qZSI inductance	L_1=L_2	500 μH
qZSI capacitance	C_1=C_2	560 μF
impedance angle	α	π/10
switching cycle	T	200μs
ac output frequency	f	50Hz
modulation index	m	0.6
shoot-through duty ratio	d_{sh}	0.2

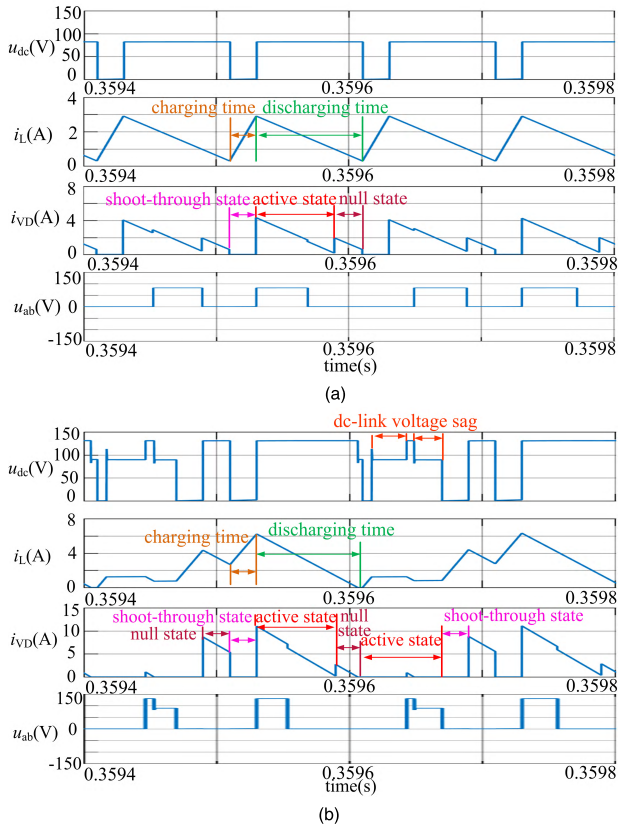

FIGURE 15. Simulation results of dc-link voltage, inductor current, diode current, and line voltage in switching period when load power is 85W. (a) M-ZSVM1. (b) ZSVM1.

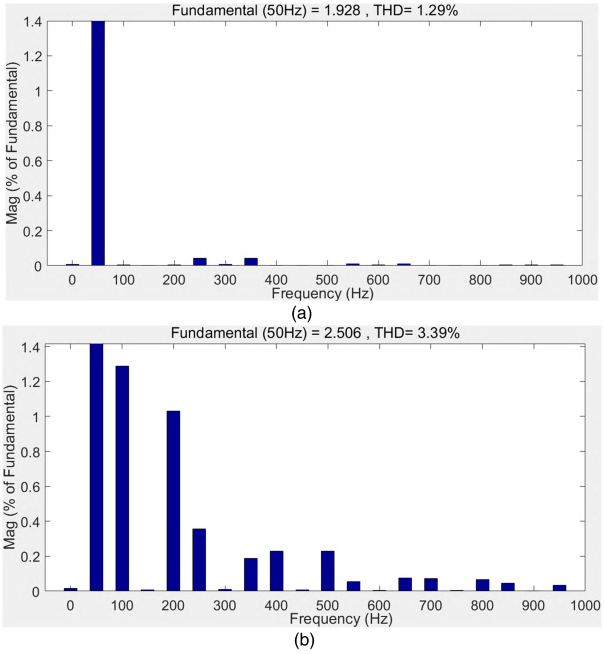

FIGURE 16. Harmonic spectrum for output current. (a) M-ZSVM1. (b) ZSVM1.

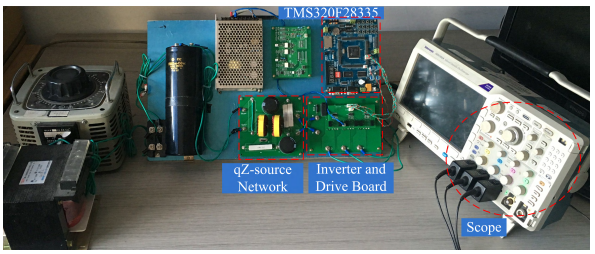

FIGURE 17. qZSI experimental platform.

According to the load power ranges of M-ZSVM1 and ZSVM1 in (30) and (31), the dc-link voltage will drop if the load power of ZSVM1 is lower than 337W, but the proposed strategy can work properly. Therefore, the simulations are made at the load power of 85W to compare the ability of suppressing the dc-link voltage sag of M-ZSVM1 and ZSVM1.

Fig. 14 shows the simulation waveforms of the dc-link voltage, the inductor current, the diode current, the output current, and the line voltage of M-ZSVM1 and ZSVM1 in the line period. Fig. 15 shows their waveforms in the switching cycle. In Fig. 14, the dc-link voltage, the peak line voltage, and the output current of ZSVM1 are apparently higher than those of M-ZSVM1. In Fig. 15(a), the qZSI works very well. The dc-link voltage is 0V in the shoot-through state and 82V in the null and active states. The average inductor current is 1.65A, and the inductor current fluctuates from 0.3A to 3A. The charging inductor current ripple is equal to the discharging inductor current ripple each time. Moreover, the diode current decreases from 4A to 0.4A in the active state and null state, which is continuous all the time. The peak line voltage is equal to the peak dc-link voltage 82V. The proposed strategy can prevent the diode current interruption and suppress the dc-link voltage sag effectively.

In Fig. 15(b), the diode current of ZSVM1 is interrupted in the active and null states. The time of the diode current interruption accounts for nearly 35% of the switching cycle. Meanwhile, the dc-link voltage drops dramatically. The peak dc-link voltage is boosted to 131V in the duration of the continuous diode current, which is 1.58 times higher than one without dc-link voltage sag. In the duration of the discontinuous diode current, the dc-link voltage drops from 131V to 90V. The line voltage is distorted seriously.

Fig. 16 shows the harmonic spectrums of the output currents of M-ZSVM1 and ZSVM1. The THD is around 1.29% in M-ZSVM1, and these harmonics are all less than 0.05%. However, the THD is around 3.39% in ZSVM1. The second, fourth, and fifth harmonics are 1.29%, 1%, and 0.36%, respectively.

B. EXPERIMENTAL RESULTS

The qZSI experimental platform is also built to validate the feasibility and correctness of the proposed strategy. The controller is based on the TMS320F28335 digital signal processor. Six MOSFETs, IRFPS37N50A, are employed as the power switch devices of the main circuit, as shown in Fig. 17. The experimental parameters are the same as the simulation parameters except the load power and modulation index.

In order to compare the ability of suppressing dc-link voltage sag of M-ZSVM1 and ZSVM1, three groups of

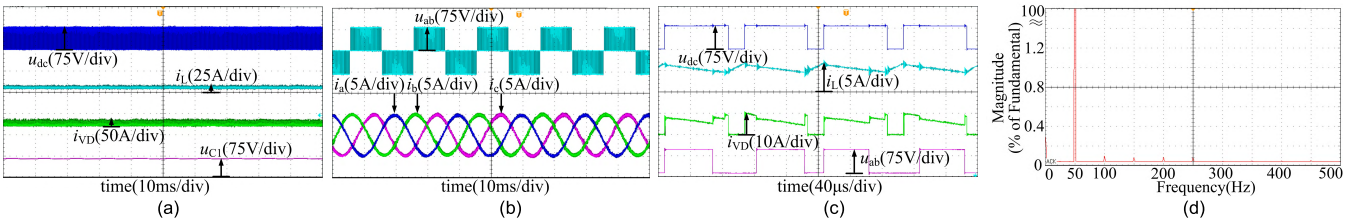

FIGURE 18. Experimental waveforms of u_{dc}, i_L, i_{VD}, u_{C1}, i_a, i_b, i_c, and u_{ab} in (a) and (b) line period and (c) switching period, and (d) harmonic spectrum for output current of M-ZSVM1 when load power is 270W.

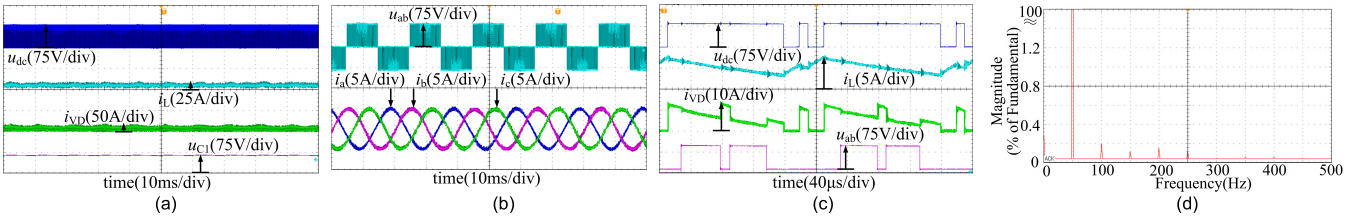

FIGURE 19. Experimental waveforms of u_{dc}, i_L, i_{VD}, u_{C1}, i_a, i_b, i_c, and u_{ab} in (a) and (b) line period and (c) switching period, and (d) harmonic spectrum for output current of ZSVM1 when load power is 270W.

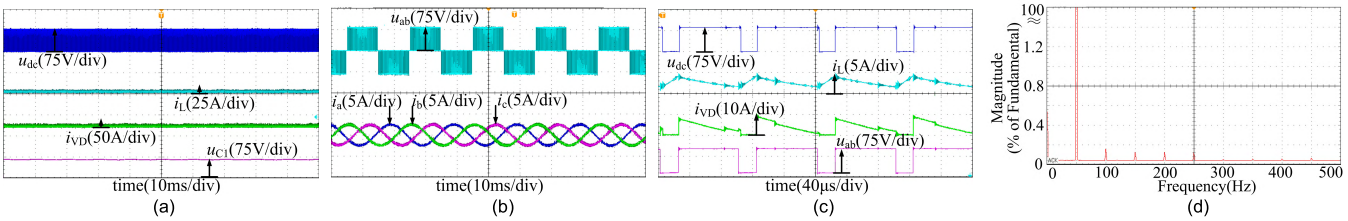

FIGURE 20. Experimental waveforms of u_{dc}, i_L, i_{VD}, u_{C1}, i_a, i_b, i_c, and u_{ab} in (a) and (b) line period and (c) switching period, and (d) harmonic spectrum for output current of M-ZSVM1 when load power is 138W.

TABLE 2. Load power in the experiment.

Load power	d_{sh}	m
270W	0.2	0.8
138W	0.2	0.8
85W	0.2	0.6

experiments are made at different load powers which are summarized in TABLE 2.

The experimental waveforms of the dc-link voltage u_{dc}, the inductor current i_L, the diode current i_{VD}, the capacitor voltage u_{C1}, the line voltage u_{ab}, the three-phase output currents, and the harmonic spectrum for the output current of M-ZSVM1 and ZSVM1 are given in each experiment of 270W, 138W and 85W, respectively.

When the load power is 270W, Fig. 18 and 19 show the experimental waveforms of M-ZSVM1 and ZSVM1, respectively. In Fig. 18, the peak dc-link voltage, the capacitor voltage, the peak line voltage, and the peak output current of M-ZSVM1 are about 83V, 63V, 83V, and 5A, respectively. The harmonics of the output currents of M-ZSVM1 are all less than 0.2%. In Fig. 19, the peak dc-link voltage, the capacitor voltage, the peak line voltage, and the peak output current of ZSVM1 are about 82V, 62V, 82V, and 5A, respectively. The harmonics of the output current of ZSVM1 are also all less than 0.2%. However, the minimum diode current of M-ZSVM1 4A is larger than that of ZSVM1 2A, which indicates that ZSVM1 is more likely to cause the dc-link voltage sag.

When the load power decreases to 138W, Fig. 20 and 21 show the experimental waveforms of M-ZSVM1 and ZSVM1, respectively. In Fig. 20, the peak dc-link voltage, the capacitor voltage, the peak line voltage, and the peak output current of M-ZSVM1 are about 86V, 66V, 86V, and 2.7A, respectively. The minimum diode current is 1.6A, which is greater than zero in the active state and null state all the time. Therefore, the dc-link voltage sag does not happen, and the harmonics of the output current are all less than 0.2%. In Fig. 21, the diode current has decreased to zero before the end of the non-shoot-through state, causing the dc-link voltage sag. According to the analysis of part B of section II, the peak dc-link voltage and output current with dc-link voltage sag are higher than those without dc-link voltage sag. Therefore, the peak dc-link voltage of ZSVM1 is boost to 97V, and the peak output current increases to 3.1A, which is higher than that of M-ZSVM1. During the time of

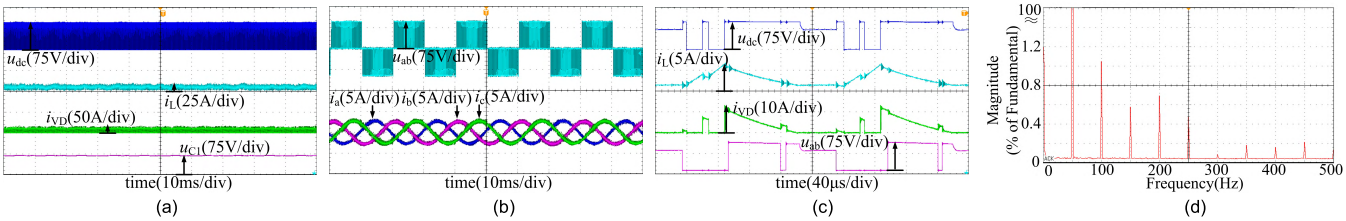

FIGURE 21. Experimental waveforms of u_{dc}, i_L, i_{VD}, u_{C1}, i_a, i_b, i_c, and u_{ab} in (a) and (b) line period and (c) switching period, and (d) harmonic spectrum for output current of ZSVM1 when load power is 138W.

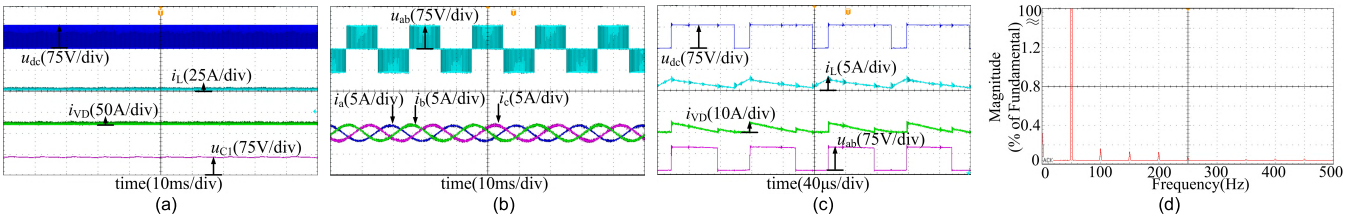

FIGURE 22. Experimental waveforms of u_{dc}, i_L, i_{VD}, u_{C1}, i_a, i_b, i_c, and u_{ab} in (a) and (b) line period and (c) switching period, and (d) harmonic spectrum for output current of M-ZSVM1 when load power is 85W.

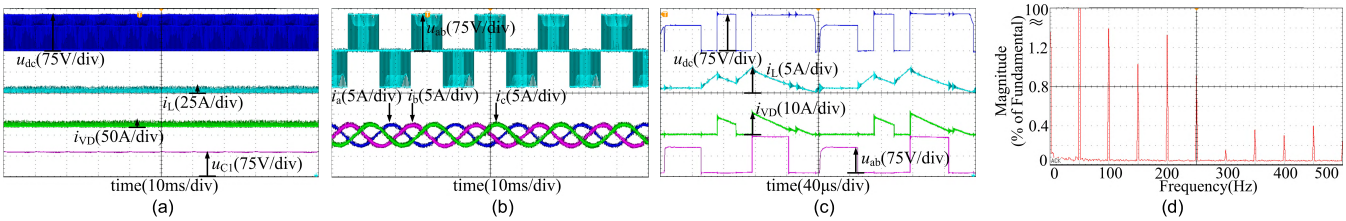

FIGURE 23. Experimental waveforms of u_{dc}, i_L, i_{VD}, u_{C1}, i_a, i_b, i_c, and u_{ab} in (a) and (b) line period and (c) switching period, and (d) harmonic spectrum for output current of ZSVM1 when load power is 85W.

the diode current interruption, the dc-link voltage drops from 97V to 73V, causing the distortion of the line voltage u_{ab} and output current. The line voltage drops from 97V to 73V. The second, third, fourth, and fifth harmonics of the output current increase to 1%, 0.52%, 0.64% and 0.44%, respectively.

When the load power decreases to 85W, Fig. 22 and 23 show the experimental waveforms of M-ZSVM1 and ZSVM1, respectively. In Fig. 22, the peak dc-link voltage, the capacitor voltage, the peak line voltage, and the peak output current of M-ZSVM1 are about 83V, 63V, 83V, and 2A, respectively. Although the output power of the qZSI decreases a lot, the minimum diode current is also greater than zero. In Fig. 22 (d), the magnitude of the fundamental components of the output current is 100%, and the harmonics of the output current are all less than 0.2%. In Fig. 23, the diode current interrupts for a long time, and the dc-link voltage drops seriously. For this reason, the peak dc-link voltage of ZSVM1 is boosted to 130V, and the peak output current increases to 2.6A, which is higher than that of M-ZSVM1. The waveform of the line voltage is similar to that of the dc-link voltage. The peak line voltage is not a constant. Sometimes it is 130V and sometimes is 89V. The distorted line voltage produces large harmonics in the output current. In Fig. 23 (d), the second, third, fourth, and fifth harmonics of the output current increases to 1.52%, 1%, 1.28% and 0.88%, respectively. Therefore, the experiment results verify that the dc-link voltage sag not only causes unstable dc-link voltage and output voltage of qZSI but also distorts the output current. Moreover, the conclusion that the proposed strategy has strong ability to suppress the dc-link voltage sag under light load is validated.

The experiment results are summarized in TABLE 3. There are two differences between M-ZSVM1 and ZSVM1. The first difference is that the qZSI works properly in M-ZSVM1 at different load powers, and low THD is in the output current. However, the THD of the output currents of ZSVM1 increases with the decrease of the load power. The second difference is that the dc-link voltage is all stable in different load powers in M-ZSVM1. However, the dc-link voltage fluctuation becomes more and more serious with the decrease of the load power in ZSVM1.

Additionally, the efficiencies of the proposed strategy and ZSVM1 are measured and pictured in Fig. 24. The efficiency of the proposed strategy is 88% at load power of 85W, 84.8% at load power of 138W, and 74.9% at load power of 270W. The efficiency of ZSVM1 is 85.9% at load power of 85W,

TABLE 3. Summary of experimental results.

Experimental results / Load powers	M-ZSVM1				ZSVM1			
	Peak dc-link voltage	Peak line voltage	Peak output current	THD	Peak dc-link voltage	Peak line voltage	Peak output current	THD
270W	82V	82V	5A	1.5%	82V	82V	5A	1.6%
138W	85V	85V	2.7A	1.52%	73V~97V	73V~97V	3.1A	5.5%
85W	83V	83V	2A	1.55%	89V~135V	89V~135V	2.6A	7.6%

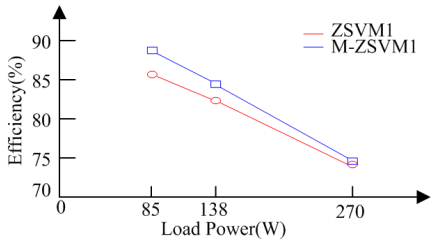

FIGURE 24. Efficiencies of the proposed strategy and ZSVM1.

82.4% at load power of 138W, and 74.8% at load power of 270W. Although the efficiencies of the two strategies reduce with the increase of the load power, the efficiency of the proposed strategy are apparently higher than that of ZSVM1 at 85W and 138W for the reason that the dc-link voltage drops in ZSVM1.

V. CONCLUSION

In order to solve the problem of the dc-link voltage sag of qZSI under the light load, the reason, harm, and influence factor of the dc-link voltage sag are analyzed in this paper. Then, a new ZSVM strategy is proposed to suppress the dc-link voltage sag. The principle and realization of the proposed strategy are given in detail. The diode current and the load power range of the proposed strategy are analyzed and compared with those of ZSVM1. The results indicate that the proposed strategy can keep the diode current continuous and enhance the ability of suppressing the dc-link voltage sag for qZSI under the light load. Therefore, the qZSI can work properly under wide load range, improving the safety and reliability of the qZSI. When the qZSI is applied to drive the AC motor drive system, the photovoltaic power system, and other control system, a stable dc-link voltage is provided through using the proposed strategy, ensuring the normal work of these systems. Furthermore, the proposed strategy can be also applied to ZSI and other improved ZSI to suppress the dc-link voltage sag.

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