IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received April 14, 2019, accepted May 3, 2019, date of publication May 8, 2019, date of current version May 24, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2915677

A Suppressing Method for Spur Caused by Amplitude Quantization in DDS

SHENG TANG, CHANGLONG LI, AND YUQING HOU
School of Information Science and Technology, Northwest University, Xi'an 710127, China

Corresponding author: Yuqing Hou (houyuqin@nwu.edu.cn)

This work was supported in part by the Natural Science Basic Research Plan in Shaanxi Province of China under Program 2018JM1025, in part by the Open Fund of Key Laboratory of Precision Navigation and Timing Technology of National Time Service Center under Grant 2014PNTT04, and in part by the National Natural Science Foundation of China under Program 11403018.

ABSTRACT Direct digital synthesis (DDS) technology is widely used in navigation, communications, aerospace, and other fields. Due to the technical limitations in the process of DDS digitization, the output spectrum of DDS is inevitably spurious. In order to meet the requirement of the pure frequency reference signal for modern instrument or equipment, it is necessary to correctly analyze the spur of DDS and effectively suppress it. In this paper, the causes of the spur in traditional DDS are analyzed, and a piecewise linear approximation method is proposed to suppress the amplitude quantization spur of DDS. In order to verify the effectiveness of the proposed spurious suppression method in this paper, the MATLAB simulation is carried out and a field programmable gate array (FPGA) hardware platform for DDS is developed. The simulation and actual test results prove the feasibility of this method. In the limited storage space, this method improves the accuracy of amplitude quantization, reduces spurs, and enhances the accuracy of synthetic frequency.

INDEX TERMS Direct digital synthesis, spurious suppression, amplitude quantization, FPGA.

I. INTRODUCTION

Frequency synthesis refers to the process of synthesizing discrete frequencies with the same index from a reference source with better frequency stability and accuracy. The circuit system that realizes frequency synthesis is called frequency synthesizer. As an important part of modern electronic instrument or equipment, frequency synthesizer must meet the requirements of high purity, high accuracy, high stability and low noise.

The main methods of frequency synthesis in the contemporary era are direct analog frequency synthesis, indirect frequency synthesis and direct digital frequency synthesis [1]–[6]. Direct analog frequency synthesis is a method that generates frequencies by adding, subtracting and dividing one or more frequency reference sources using frequency doubling, frequency dividing and mixing methods. This method is characterized by short frequency conversion time and low phase noise. However, the generated frequency is obtained by using a large number of frequency doubling, frequency division and mixing, which makes the direct analog frequency synthesizer bulky, spurious and high power consumption. Indirect frequency synthesis mainly refers to Phase Locked Loop (PLL) frequency synthesis. This method uses phase feedback and phase-locked technology in frequency synthesis. A large number of harmonic or combined frequencies are generated by mixing and dividing the harmonic generators, and then the frequency of Voltage Controlled Oscillator (VCO) is locked on a certain harmonic or combined frequency by phase-locked loop, and the required frequency output is indirectly generated by VCO. This method has many advantages, such as high output frequency, low phase noise, good spurious suppression. However, the traditional PLL frequency synthesizers adopt closed-loop control, so their circuit structure complicated and very inconvenient to debug them, and it is difficult to achieve output frequency continuously adjustable.

With the development of digital technology and the improvement of circuit integration, direct digital frequency synthesis technology has emerged. Direct digital frequency DDS technology was first proposed by Tierney in 1971. Its principle is to sample signal waveforms at a very small phase interval, calculate the amplitude of signal waveforms corresponding to the corresponding phase rotation, and store

The associate editor coordinating the review of this manuscript and approving it for publication was Abdel-Hamid Soliman.

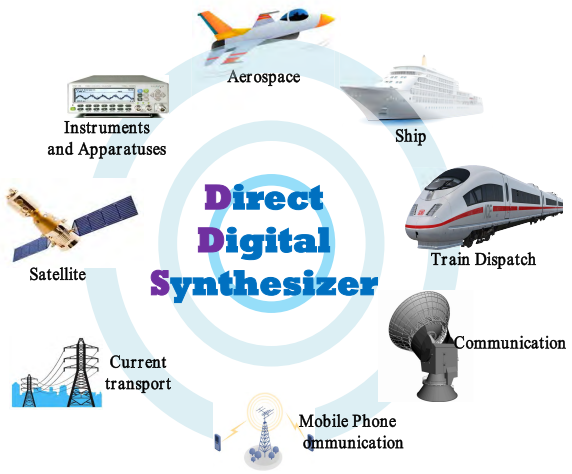


FIGURE 1. Application of DDS.

them in the Read Only Memory (ROM). In the process of frequency synthesis, the phase of waveform signal is obtained by digital phase accumulation, and the phase amplitude is converted. Compared with the traditional frequency synthesis technology, DDS has the advantages of short frequency conversion time, high frequency resolution, easy integration, high reliability and easy debugging [7]–[10]. With the continuous improvement of DDS technology, its application fields are more and more extensive, such as aerospace, surveying and mapping, guidance, satellite positioning and high-speed communications and other high-tech fields, just as shown in Fig.1 [11]–[14].

There are usually two ways to design and implement frequency synthesizer based on DDS technology, using DDS chip or FPGA [6]–[8], [14]–[16]. Chip-based frequency synthesizers can achieve higher integration. But because both of the external pins and internal structure of DDS chip are fixed, the frequency resolution usually cannot be changed. So it cannot meet the high accuracy and flexibility requirements of some special equipment or engineering. As a semi-customized circuit in the field of Application Specific Integrated Circuits (ASIC), FPGA not only solves the shortcomings of customized circuits, but also overcomes the shortcomings of the limited number of gate circuits of the original Programmable Logic Device (PLD). It breaks the traditional process of ''design-chip-package'' and can build digital circuits with different functions on a chip. The function of high integration, high flexibility and re-writing capability of FPGA has expanded its application field. DDS circuit modules such as phase accumulator, waveform memory and angle-to-amplitude converter can be constructed flexibly by using FPGA. Although there are differences in structure and performance indicators, the two frequency synthesizers follow the same principle. The basic principle is that the frequency tuning words are accumulated in turn under the control of the system clock, and the phase addresses are obtained. The expected frequency is synthesized by looking

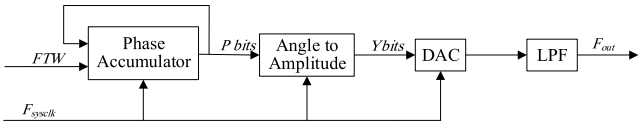


FIGURE 2. Block diagram of traditional DDS method.

up the table. Spurious signals are inevitably introduced in their process of synthesizing frequency.

However, some practical projects and systems (just as shown in Fig.1) usually require lower spurious frequency synthesizers to generate their reference frequency signals. Therefore this paper summarizes the sources of spurs of DDS, deeply analyses the amplitude quantization spur, and proposes a spurious suppression method based on piecewise linear approximation to improve the purity of the output signal of DDS frequency synthesizer.

II. DDS SPURIOUS ANLYSIS

When traditional DDS realizes frequency synthesis, the frequency tuning word input to the phase accumulator is accumulated in turn under the system clock, and the instantaneous value of the waveform is synthesized by means of lookup table [10], [15]. As shown in Fig.2, the method produces a time series of digital words at the output of the accumulator that increases linearly until the accumulator rolls over at its maximum value of 2^C. Hence, the accumulator output has a fixed modulus 2^C. Due to the limitation of the amount of memory in the synthesizer, the phase address intercepts the high P bits of the accumulator output value, which reduces the complexity of frequency synthesis. In other words, only the Most Significant Bit (MSB) is applicable. But it also reduces the range of phase addresses. Phase addresses range is usually from 0 to (2^P-1). The accumulator output sequence range 0 to (2^P-1) maps to one revolution on the unit circle, that is, it linearly maps binary values from 0 to (2^P-1) to radian angles from 0 to 2π. This mapping arrangement allows the angle-to-amplitude converter to translate the P-bits words to Y-bits amplitude values in a very efficient manner, and finally a low-pass filter is used to obtain a desired sinusoidal signal. The Y-bits digital amplitude sequence signal output from the angle-to-amplitude converter is transformed into an analog signal by a Y-bit Digital to Analog Converter (DAC) circuit, and finally a low-pass filter is used to obtain a desired sinusoidal signal. The above mentioned angle-to-amplitude conversion process depends on the following equation:

$$x = A\sin(\frac{2k\pi}{2^P}) \tag{1}$$

where A is the maximum amplitude, P is the number of bits taken from the accumulator, k is the binary value of those bits at any given instant, x is the amplitude value corresponding to the address at a given time.

The following equation expresses the sinusoidal frequency output from a traditional accumulator-based DDS:

$$F_{out} = \frac{FTW}{2^C}F_{sysclk} \tag{2}$$

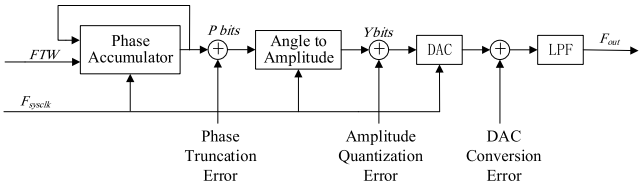


FIGURE 3. Sources of DDS spurs.

where F_{out} is the synthesized frequency, F_{sysclk} is the sampling frequency, FTW is the frequency turning words, and it is usually $FTW < 2^{C-1}$. And DDS can be regarded as a digital frequency divider, which can output sinusoidal wave with resolution of $F_{sysclk}/2^C$ and lower than the sampling frequency of the system. That is to say, every sampling frequency period, DAC will output a point, and $2^C/FTW$ points form a period of output frequency. So we can conclude that the core operation of the DDS is essentially a digital process.

Because of its inherent digital characteristics, there are a lot of spurious components in its output signal [15]–[20]. The generation sources of DDS spurious signals mainly include phase truncation error, amplitude quantization error and DAC conversion error, just as shown in Fig.3.

(1) Phase truncation error. In order to improve the frequency accuracy of DDS, a phase accumulator with higher bit width is usually a better choice. But this choice will consume a lot of ROM resource. A certain number of digits are usually omitted and reserved to P bits (MSB only) to reduce the complexity of the angle-amplitude conversion module. The subsequent problem is that truncation errors emerge. In order to comprehensively consider the contradiction between phase address truncation and resource of FPGA chip, the number of phase accumulator bits in this paper is 32 bits. In order to save storage space, the high 16 bits of the output value of the phase accumulator is the phase address P. The DAC chip used in this paper is 16 bits, so the magnitude Y stored in ROM is 16 bits.

(2) Amplitude quantization error. The ideal simulated sine wave should be a smooth continuous curve with infinite resolution. In ideal ROM storage, there should be infinite storage points. The dense discrete points are approximate to an analog sine wave. These sine amplitudes are expressed in binary numbers, but the limited ROM storage space and the limited resolution in DAC must be quantized, which will lead to quantization errors. A lot of experiments show that the spur caused by the quantization error will be improved by about 6 dB for each additional bit of DDS amplitude quantization. Therefore, improving the storage mode of ROM quantization can effectively improve the quality of DDS frequency synthesis.

(3) DAC conversion error. The digital signal synthesized in the FPGA chip needs to be converted into analog signal by DAC. In this process, the main factors affecting the signal quality are the nonlinearity of DAC, limited resolution, burst spike pulse, digital noise feed through and conversion rate, which distort the output signal of DDS and introduce errors.

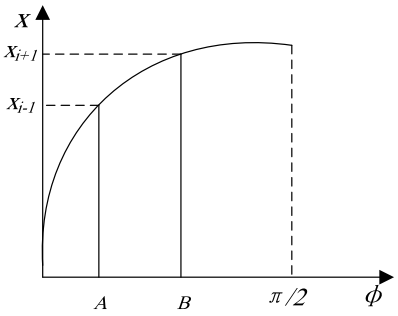


FIGURE 4. Traditional DDS phase-to-amplitude conversion diagram.

Phase truncation error, amplitude quantization error and DAC conversion error are the main factors affecting the spectral purity of traditional DDS synthesized frequency signals. In addition, the high swing rate of digital signal in the chip of FPGA can produce instantaneous noise coupled to the output of DAC. The stray of the system clock will be amplified into the frequency signal by frequency multiplication. The unreasonable PCB wiring can also lead to spurious signals.

In order to meet the requirement of pure frequency reference signal for modern instruments and equipment, It is necessary to study stray suppression methods. At the same time, based on the above analysis, we can know that the spurious suppression of DDS can adopt different methods for different error sources. In this paper, we focus on the spurs caused by amplitude quantization, and devote ourselves to the research of its suppression method.

Among the many factors that lead to spurious in DDS frequency synthesis, the reason of amplitude quantization spurious is the digitization of analog signals. The digital signal loses some sine wave information. As shown in Fig. 4, phase-to-amplitude conversion is performed after 1/4 quantization of sinusoidal wave amplitude. In traditional DDS, the frequency control words are accumulated under the control of the clock signal. If the phase address of the accumulator output is the phase address stored in ROM, it corresponds to the accuracy amplitude, such as point A or B in Fig.4, which corresponds to the amplitude x_{i-1} or x_{i+1}. At this time, the signal synthesized by DDS will not introduce amplitude quantization spurious. If the output address of the accumulator is not stored in the ROM, for example, the phase address falls between AB of Fig. 4, then there is no corresponding amplitude in the ROM. In this case, traditional DDS usually adopts the approach of adjacent approximation. That is to say, the expected amplitude value is replaced by the corresponding amplitude value of A (or B). And then the amplitude quantization error cannot be avoided.

III. SPURIOUS SUPPRESSION BASED ON PIECEWISE LINEAR APPROXIMATION

Just as mentioned above, magnitude quantization error not only affects the spectral purity of the synthesized frequency, but also has an important impact on the accuracy of the synthesized frequency. Therefore, this paper propose a spurious

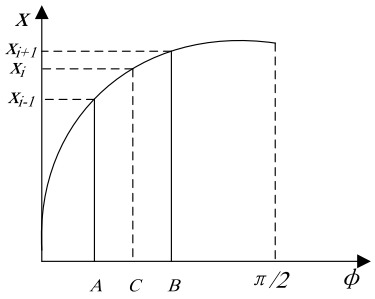


FIGURE 5. A model for median value calculation.

suppression method based on piecewise linear approximation to improve the quantization degree when the storage capacity of ROM is unchanged. Under the control of the clock, the output value of the phase register represents the phase of the sinusoidal function. Not all sinusoidal samples are stored. The high P bits in the accumulator are used for ROM addressing, while the other $d = N - m(m$ denotes the low m bits rounded in the accumulator) is used for correlative calculation of the amplitude approximation method.

The method can be briefly divided into two steps. First, median amplitude value calculation based on trigonometric function to reduce phase-to-amplitude conversion error. Secondly, Secondly, piecewise linear approximation further improves the accuracy of amplitude quantization.

A. MEDIAN VALUE CALCULATION

The sinusoidal signal can be expressed as:

$$x_i = A\sin(\frac{2\pi f}{f_s}i) \quad (i = 1, 2, 3\cdots) \tag{3}$$

Among them, x_i is the amplitude of the ith sampling of DDS, A is the maximum amplitude, f is the output frequency, f_s is the sampling frequency. From the formula, we can get that:

$$x_{i+1} + x_{i-1} = 2x_i\cos(\frac{2\pi f}{f_s}) \tag{4}$$

In the above formula, x_{i+1} is the last point of the corresponding amplitude of two adjacent phase addresses in ROM (just as the amplitude of point B in Fig.5). x_{i-1} is the preceding point of the corresponding amplitude of two adjacent phase addresses in ROM (just as the amplitude of point A in Fig.5). The median x_i (just as the amplitude of point C in Fig.5) can be obtained from the following formula:

$$x_i = \frac{x_{i+1} + x_{i-1}}{2\cos(\frac{2\pi f}{f_s})} \tag{5}$$

This method improves the magnitude quantization of ROM by a simple algorithm, which is equivalent to doubling the original quantization. It not only reduces the error caused by amplitude quantization, but also improves the accuracy of the output signal. The model is shown in Fig. 5.

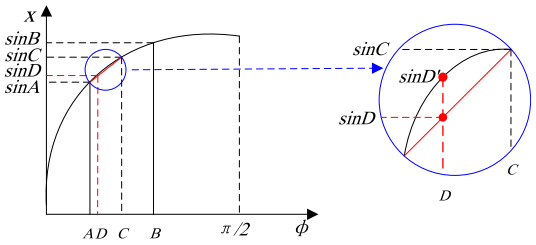


FIGURE 6. A model for piecewise linear approximation.

B. PIECEWISE LINEAR APPROXIMATION

In a phase-to-amplitude conversion process, if the sampling address falls in section AB as shown in Fig.6, the corresponding magnitude quantization has three results: (1) If the sampling address is a point in A or B, the corresponding exact amplitude can be obtained by looking up ROM tables. (2) If the sampling address is a point in C, the corresponding amplitude can be obtained by median value calculation mentioned above. (3) The sampling address is between AC or BC. In this case, there is no corresponding value stored in ROM. It can only be replaced by A, B or C, which will lead to remarkable errors. If an approximate value of the corresponding amplitude of the address is obtained by using a linear function in the corresponding sinA-sinC or sinC-sinB segments, the sinusoidal amplitude can be expressed more accurately, and the magnitude quantization error can be reduced. As shown in Fig. 6, if the address is D between AC, the approximate amplitude sin$D$ can be obtained as follows:

$$\sin D = \sin A + (\sin C - \sin A) \times \Delta x \tag{6}$$

where sin$A$ is the storage value in ROM, sin$C$ is the calculated median value, Δx is a phase offset, sin$D$ is the approximation value corresponding to the actual sampling address D when synthesizing frequency. Although there is still an estimation error of (sinD' − sin$D$) relative to the ideal magnitude quantization value sinD', the improvement of quantization accuracy is obvious, just as shown in Fig.6.

The value in the phase registers at any instant reads:

$$D = FTW \times (i - 1) \tag{7}$$

where i is the number of clock cycles, and $D[(N-1):0]$ represents an N-bit word with bit $(N\text{-}1)$ as it MSBs and bit 0 as its Least Significant Bit (LSB). The notation is used in Verilog hardware description language. The phase angle of every sinusoid sample to be interpolated is calculated by formula (8) and the interpolated value is given by formula (9) [16].

$$D = \left(\frac{\pi}{2}\right) \times \left(\frac{D_i[(N-1:0)]}{2^N}\right) \tag{8}$$

$$\sin D = \sin A + \frac{\sin C + \sin A}{2^{d-1}} \times (D[d-2:0]) \tag{9}$$

In other words, the d LSBs of the phase register output D indicates the relative position of the interpolated sample from the preceding stored sample. They therefore also represent the number of clock cycles required for the value in the phase

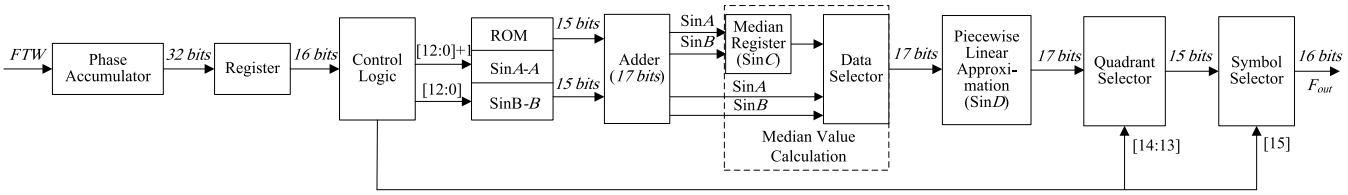


FIGURE 7. The block diagram of spurious suppression method based on piecewise linear approximation.

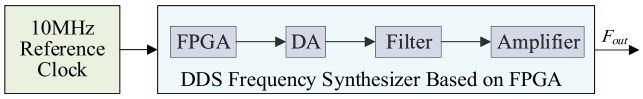


FIGURE 8. Block diagram of DDS frequency synthesizer based on FPGA.

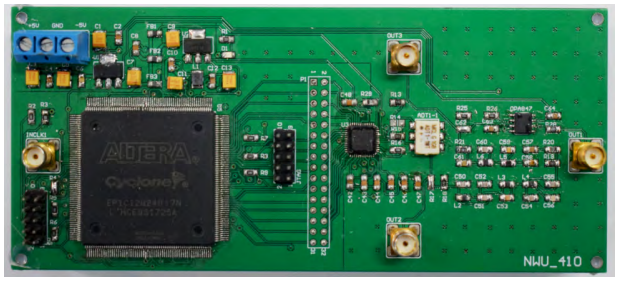
register to change from A to B. The output of the ROM has a word length and hence amplitude resolution of y bits. In order to be more consistent with the actual hardware language description, the two ends of the above formula are multiplied by 2^{d-1}.

$$\sin D = (\sin C - \sin A) \times (D[d-2:0]) + \sin A \ll (d-1) \tag{10}$$

Summarizing the above contents, the spurious suppression method based on piecewise linear approximation can be briefly described as Fig.7. Incidentally, the final output digital amplitude of synthesized frequency signal is 16 bits, which is to match the bit width of the subsequent digital analog converter.

IV. DEVELOPMENT OF DDS FREQUENCY SYNTHESIZER BASED ON FPGA

In order to verify the effectiveness of the proposed spurious suppression method based on piecewise linear approximation, this paper designs and implements a DDS frequency synthesizer based on FPGA. Thanks to the flexible programmability of FPGA, the traditional DDS method and the spurious suppression method based on piecewise linear approximation can be burned into the DDS platform alternately, and then the comparative experiment can be carried out conveniently. The frame structure of frequency synthesizer based on FPGA is shown in the Fig. 8, which specifically consists of the reference clock module, the FPGA module, the DAC module, the filter module and the amplification driver module. The circuit board of the DDS frequency synthesizer based on FPGA is shown as Fig.9(a), whose size is about 142mm $\times$ 62 mm. The reference clock module uses the SRS company's rubidium atomic clock PRS10 as shown in Fig.9(b). The output of the atomic clock is a 10 MHz sinusoidal wave with amplitude of 0.7V. In order to meet the requirement of frequency synthesizer for higher sampling clock, the 10MHz signal output by the rubidium atomic clock is multiplied to 100MHz by the PLL in the FPGA. The module of FPGA is EP1C12Q240I7 of Altera's hurricane series. The digital logic circuits such as phase accumulator and phase-to-amplitude converter are designed and implemented in EP1C12Q240I7. The spurious suppression method



(a)

(b)

FIGURE 9. Photograph of DDS frequency synthesizer and its clock reference. (a) DDS frequency synthesizer based FPGA. (b) Rubidium atomic clock PRS10.

based on piecewise linear approximation is realized under the drive of 100 MHz system clock. The DAC module uses 16-bit parallel input DAC chip MAX5885 of Maxim Company. It has the characteristics of high stability and low noise. It can convert the digital waveform output by EP1C12Q240I7 into analog waveform output. The filter module is designed to filter out clutter and other interfering signals in the output waveform of the DAC module. It uses a seventh-order elliptic filter to improve the quality of the synthesized waveform. The amplifier driver module is designed and implemented by TI's ultra-low noise integrated operational amplifier OPA847, which makes the device have a large driving capability, and the output synthesized frequency signal has an amplitude of not less than 3 Vpp under a load of 50 Ω.

V. EVALUATION EXPERIMENTS

Practice is the sole criterion for testing truth. This paper evaluates the effectiveness of the proposed DDS method from the following aspects. Meanwhile, the parameters of DDS are set to the same value for the purpose of ensuring of the objectivity of the evaluation results, both in the traditional

TABLE 1. DDS parameter setting in the experiments.

Parameter name	Set value
FTW	32 bits
Phase Accumulator	32 bits
F*sysclk*	100 MHz
P	16 bits
Y	16 bits
DAC	16 bits

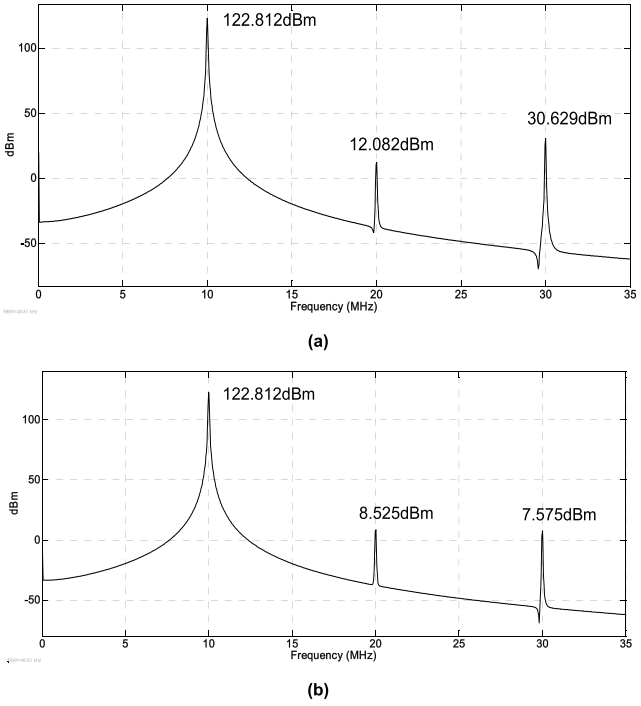


FIGURE 10. Simulation comparison of spurious suppression effect. (a) Traditional method. (b) The proposed method.

method (as shown in Fig.2) and the proposed method (as shown in Fig.7), as shown in Table 1.

A. SPURIOUS SUPPRESSION

In order to verify the spurious suppression effectiveness of the proposed method based on piecewise linear approximation, both of simulation and actual test are carried out in this paper.

In the following experiments, 10MHz is selected as the synthetic frequency, and Matlab simulations are implemented firstly. Due to the limitation of DDS frequency synthesizer's storage resource, the traditional DDS method (as shown in Fig.2) often adopts the strategy of adjacent amplitude replacement in the process of amplitude quantization. This rough treatment will inevitably lead to obvious spurious phenomenon, just as shown in Fig.10(a). Obviously, the main frequency intensity is about 122dBm, the corresponding second harmonic intensity is about 12dBm and the third harmonic intensity is about 30dBm. Spurious suppression ratio is usually used as an evaluation index of suppression effect in frequency synthesis. The spurious suppression ratio is usually defined as the strength difference between the main signal and its spur. As can be seen from Fig.10(a),

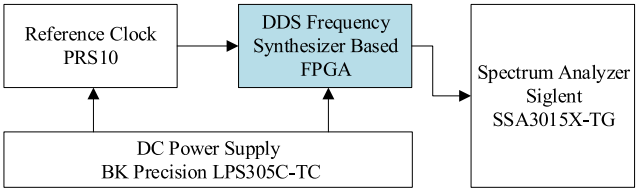


FIGURE 11. Block diagram of the actual test platform.

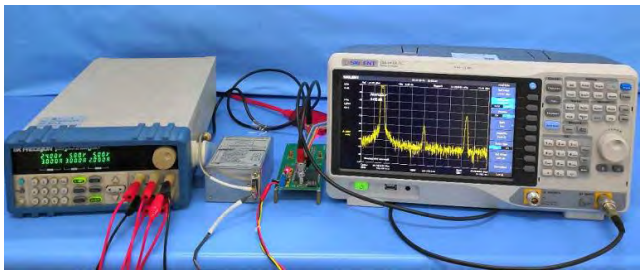


FIGURE 12. Photograph of the actual test platform.

the spurious suppression ratio of the traditional DDS method to the second harmonic is about 110dBm, and to the third harmonic is about 92dBm. Correspondingly, the Fig.10(b) shows the simulation result of the proposed spurious suppression method based on piecewise linear approximation. Obviously, the main frequency intensity is the same about 122dBm, the corresponding second harmonic intensity is about 9dBm, and the third harmonic intensity is about 8dBm. And the spurious suppression ratio of the new method to the second harmonic is about 113dBm, and to the third harmonic is about 114dBm. The simulation results show that the new method proposed in this paper has better spurious suppression effect.

The actual test platform mainly includes DC power supply, rubidium atomic clock PRS10, DDS frequency synthesizer based on FPGA, spectrum analyzer and several coaxial cables, just as shown in Fig.11 and Fig.12. The PRS10 rubidium atomic clock is selected as the system reference clock to output 10MHz standard reference frequency signal. The reference frequency signal is multiplied upto 100MHz by the PLL in the FPGA in order to meet the requirement of frequency synthesizer for higher sampling clock. And the spectrum analyzer is SIGLENT SSA3015X-TG, which undertakes the task of measuring the effect of spurious suppression.

As shown in Fig.13, the actual test results show that the main frequency intensity of the DDS frequency synthesizer based on FPGA output is about −3dBm, the corresponding second harmonic intensity is about −61dBm and the third harmonic intensity is about −49dBm when traditional DDS method is executed. And the spurious suppression ratio of the traditional DDS method to the second harmonic is about 58dBm, and to the third harmonic is 46dBm. When the DDS frequency synthesizer based on FPGA executes the proposed spurious suppression method based on piecewise linear approximation, the main frequency intensity of its output is about −15dBm, the corresponding second harmonic intensity is about −88dBm and the third harmonic intensity

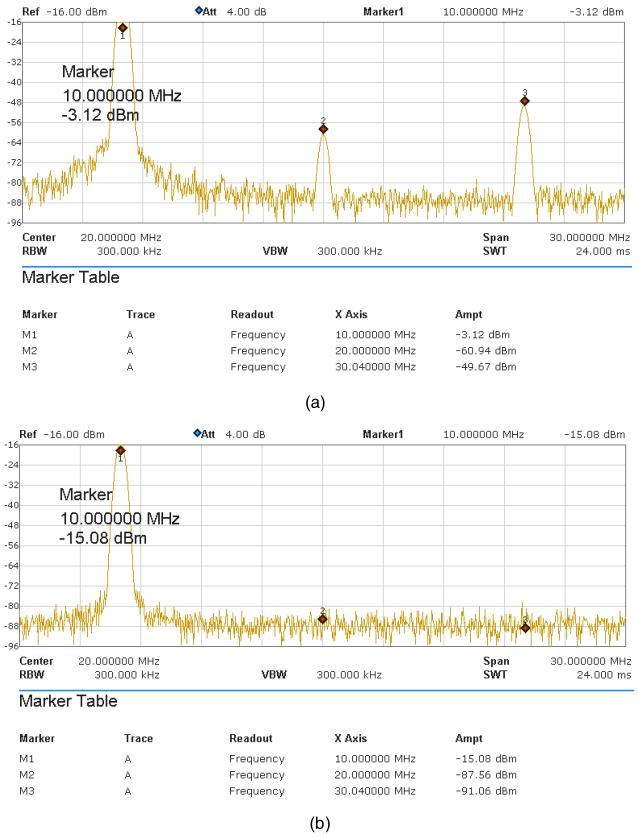


FIGURE 13. Actual test comparison of spurious suppression effect. (a) Traditional method. (b) The proposed method.

is about −91dBm. And the spurious suppression ratio of the new method to the second harmonic is about 73dBm, and to the third harmonic is 76dBm. The actual test results show that the new method proposed in this paper has better spurious suppression effect too.

Summarizing the above experiments, it is obvious that both of the Matlab simulation and the actual test results show that the new method proposed in this paper has better spurious suppression effect. Meanwhile, we can see that the proposed spurious suppression method based on piecewise linear approximation obtains better spurious suppression index in Matlab simulation rather than in actual test. That is due to the Matlab simulation is executed in very ideal conditions. But in the real circuit implementation, besides amplitude quantization, there are many unexpected factors that can lead to the increase of initial harmonics, such as reference clock noise, digital switch spurs, and so on. Perhaps they are the reasons why the actual test results do not match the simulation results very well.

B. ACCURACY AND STABILITY

In order to evaluate the proposed DDS method more comprehensively, the accuracy and stability of the output signal of the frequency synthesizer are measured. Frequency stability is the random fluctuation degree of frequency within a unit time interval, which represents the ability to maintain frequency. Allan variance is used as the mathematical representation of

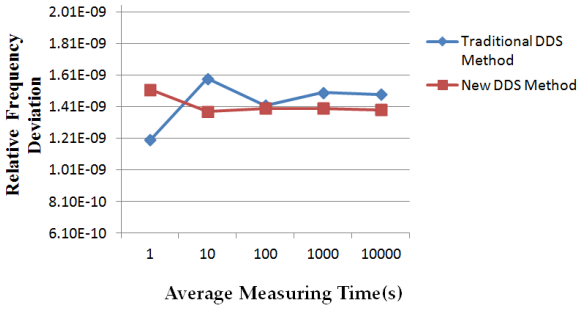


FIGURE 14. Frequency accuracy of the DDS frequency synthesizer based FPGA output.

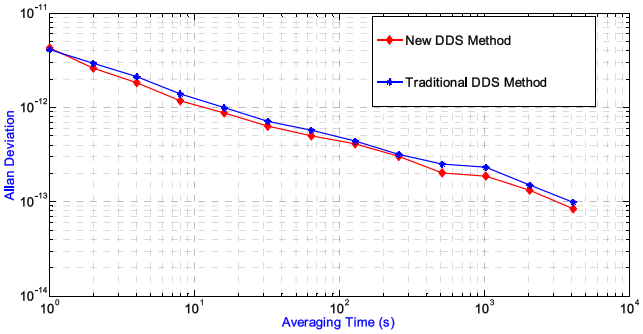


FIGURE 15. Frequency stability of the DDS frequency synthesizer based FPGA output.

TABLE 2. Comparison of resource consumption.

FPGA resource consumption	Traditional method	Proposed method
Device	Cyclone EP1C12Q240I7	Cyclone EP1C12Q240I7
Total logic elements	295/12060 (2%)	1104/12060 (9%)
Total pins	19/173 (11%)	19/173 (11%)
Total memory bits	122880/239616 (51%)	180275/239616 (75%)
Total PLLs	1/2 (50%)	1/2 (50%)

frequency stability. Just as shown in Fig.14, the accuracies of the output signals of the frequency synthesizer executing two methods are similar. But as shown in Fig.15, when the proposed spurious suppression method based on piecewise linear approximation is implemented, the stability of the output signal of the frequency synthesizer is slightly better.

C. RESOURCE CONSUMPTION

When evaluating different kinds of DDS methods, FPGA resource consumption should not be ignored. Therefore, this paper separately counts the logical resource consumption of DDS frequency synthesizer when it executes the traditional method and the new method, just as shown in Table 2. Obviously, when the proposed spurious suppression method based on piecewise linear approximation and the traditional method are executed by the same FPGA Cyclone EP1C12Q240I7, they consume the same pin and PLL resources. Meanwhile, the proposed method consumes a little more logic element

and memory resources than the traditional method. But, the benefits of sacrificing these logic element and memory resources are remarkable. That is, more pure spectrum and frequency stability.

VI. CONCLUSION

This paper introduced the basic principle and implementation of traditional DDS method. Starting from the inherent characteristics of DDS implemented by FPGA, the paper deeply analyzed the causes of various spurs introduced in the process of DDS synthesis frequency.

In order to suppress the amplitude quantization spur of DDS, this paper proposed a new spurious suppression method based on piecewise linear approximation. This method improves the quantization degree of amplitude and reduces the stray caused by quantization. Both of the Matlab simulation and the actual test results show that the new method proposed in this paper has better spurious suppression effect. At the same time, the new method can make the frequency synthesizer output more stable. And it is expected to provide technical reference for time-frequency generation and maintenance engineering.

It is undeniable that there is still much room for improvement in the proposed method, such as:

(1) Optimization of algorithm implementation process, which will further save the logic and memory resources in FPGA.

(2) Further refinement of linear approximation processes, which will further improve the accuracy of phase-amplitude conversion and further reduce spurs.

(3) Combining other stray suppression methods. Different kinds of spurious suppression methods can play a role in different stages of frequency synthesis. For example, the spurious suppression methods for phase truncation.

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SHENG TANG received the Ph.D. degree in measurement technique and instrument from the University of Chinese Academy of Sciences, in 2013. He is currently a Senior Engineer with the School of Information Science and Technology, Northwest University, China. His main research interests include the design and implementation of intelligent instruments, and meters.

CHANGLONG LI is currently pursuing the M.S. degree in circuits and systems with the School of Information Science and Technology, Northwest University, Xi'an, China. He is studying about circuits and signal processing. His main research interest is to improve the quality of DDS frequency synthesized signals based on the advantages of applying FPGA.

YUQING HOU received the M.S. degree in electronics from the Xi'an Institute of Optics and Precision Mechanics, CAS, Xi'an, in 1990. She is currently a Professor with the School of Information Sciences and Technology, Northwest University. Her current research interests include intelligent instrument, digital signal processing, and so on.