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Exploring Memristor Multi-Level Tuning Dependencies on the Applied Pulse Properties via a Low Cost Instrumentation Setup

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ABSTRACT Deeper understanding of memristive behavior is the only safe way towards maximum exploitation of the favorable properties and the analog nature of this new device technology in innovative applications. This can be achieved through experimental hands-on experience with real devices. However, lab experiments with memristors are a challenging step, especially for the uninitiated. In this direction, this paper presents some important considerations to carry out reliable measurements using an experimental setup composed of *off-the-shelf* components and an affordable data acquisition system. We specifically show how a transimpedance amplifier can be used to protect the memristor from damage via current compliance limiting, and allow full control over the voltage drop on its terminals. Using the proposed setup, a set of key experiments were carried out on commercial memristors from *Knowm Inc.*, revealing fundamental dependencies of memristor state-tuning properties on the characteristics of the applied pulses and the initial conditions of the devices.

INDEX TERMS Digilent AD2, feedback ammeter, instrumentation, Knowm, memristor, multi-level memory, resistive switching, ReRAM, transimpedance amplifier.

I. INTRODUCTION

The existence of the fourth fundamental circuit element, the memristor (short for ''memory resistor''), was postulated by Chua in 1971 [1]. Today the term memristor usually refers to any resistive switching (RS) device that complies with a set of certain properties known as ''fingerprints'' [2]. Unprecedented attention on this device technology has been drawn since 2008 after the first demonstration of the well-known TiO_2-based memristor by Hewlett-Packard Laboratories (HP Labs) [3], who managed to connect the nature of such devices with Chua's 1971 theory (although the hysteretic RS property of oxides sandwiched between metal electrodes was known from the '60s [4], [5]). Owing to their plasticity, analog nature, and (in most cases) nonvolatility, memristors constitute an emerging trend in modern electronics [6], representing a promising technology with several applications including memory [7], adaptive and learning circuits [8], [9], sensing [10] and computing [11].

The HP Labs invention in 2008 was soon followed by the identification of additional material compounds which can be the basis of memristive devices and a wide variety of such materials are being studied [12]. While this technology is continuously evolving/maturing, some commercially available memristors were released by *Knowm Inc*. [13] bringing this technology closer to researchers that might not have access to fabrication facilities. As typically happens with all new electronic device technologies, modeling and simulation are the first steps to exploring general attributes [14], verifying theoretical aspects and studying innovative application prospects [15]. Lab experiments with fabricated memristors are the next challenging step. An important barrier in this direction is usually the lack of state-of-the-art equipment to realize reliable experimental measurements. Additionally, the parasitics and the still important memristor device variability [16] cause hesitation on the inexperienced researchers

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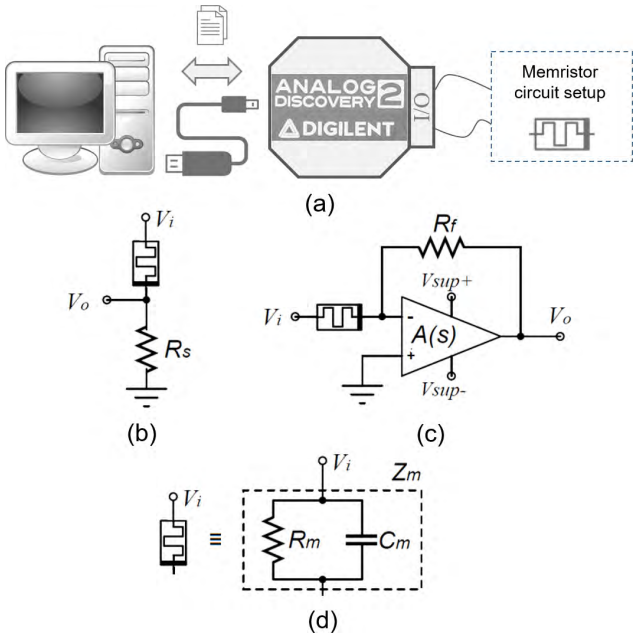

FIGURE 1. (a) Overview of the experimental setup which comprises the portable Digilent AD2 instrument connected via USB cable to a computer, and the memristor circuit in the final stage. (b) The memristor-resistor voltage divider. (c) The feedback ammeter circuit. (d) For proper analysis of the setup, the memristor was modeled as the equivalent impedance Z_m of the resistance R_m (memristance) and a parasitic capacitance C_m as in [22] and [23]. Moreover, the op-amp was modeled as a single pole and a defined open-loop low-frequency gain, inferred from the Gain Bandwidth product in the datasheet.

not only about the quality of the devices under test, but also about the strategy followed and the setup used to carry out the experiments. In order to affordably get around highly expensive instrumentation equipment, the first ad-hoc characterization tools for memristor technology are currently being developed [17]. Measuring the memristor behavior accurately with low cost equipment will do more to promote memristor science around the world than almost anything else.

In this context, building upon preliminary results presented in [18], the work reported here contributes with the design and development of a low cost experimental measurement and data acquisition setup, which facilitates gaining valuable hands-on experience on memristor characterization. Such setup suggests connecting the memristor to the inverting input of the op-amp used to implement a transinpedance amplifier (thereinafter called feedback ammeter - FA) to enable: (i) controlling the voltage drop on the memristor terminals, (ii) measuring the current through it (via current to voltage conversion), and (iii) adjusting the compliance current to protect the memristor from damage. We analyze the functional properties, versatility and performance of this setup, which was designed in keeping with a certain model of the target device [see Fig. 1(d)] and the desired parameters to obtain (i.e. the memristance as a function of the measured current and the applied input voltage.) Moreover, we compared the FA-based solution to the simpler memristor-resistor voltage divider approach, frequently used for current limiting and measuring [19], [20]. Finally, experimental results revealing fundamental dependencies of the switching behavior of memristors on the applied pulse amplitude, duration, and the initial conditions of the devices, are presented. Owing to the practical nature of the presented material and the accessibility of the suggested hardware, this work creates a solid basis for several researchers in the field to study further the dynamic behavior of memristors, expand experimentation beyond research labs, and push forward *R&D* on this emerging device technology.

II. EXPERIMENTAL SETUP

A. LAB EQUIPMENT CONSIDERATIONS

Owing to the fast switching towards the low resistive state (LRS or simply ON state), especially in filamentary memristors [21], current limiting (also known as compliance current) is crucial for device protection and longer endurance/lifetime. The simplest current limiting approach is via a series resistor R_s [see Fig. 1(b)]. The resulting voltage divider between the known R_s and the memristor is also used to compute the current through the device by measuring the voltage drop V_0 across R_s, to have a constant update of the memristance in all moments during every experiment.

However, assuming the same resistor is permanently connected to the memristor for constant state measurement during switching, selecting an R_s value good enough to properly sense any memristance level might not be easy. Moreover, owing to the resulting voltage divider, the voltage drop across the memristor changes while its state changes during the switching process. Because of this, it is difficult to determine if any specific behavior observed is attributed to device intrinsic characteristics or it was caused by the voltage re-distribution during switching (henceforth called ''voltage divider effect'').

As far as probe compensation is concerned, most probes in measuring equipment permit compensating the inductance added by the wires. However, memristive devices are time variant, meaning that any compensation done at the beginning of an experiment could become inadequate throughout the experiment due to the continuous change of the memristance and the effect of any parasitic capacitance. Of course, this might not be an issue when working at low frequencies, but at high frequencies or pulse inputs, the lack of compensation could be a problem. This is especially important when using voltage and current to compute the memristance, since ringing could affect the computation. In short, in order to deal with such situations, the selected target experimental setup should preferably comply with the following requirements:

- Protect the memristor by limiting the flowing current;
- Allow a direct control over the voltage drop on the memristor terminals;
- Permit measuring current and voltage simultaneously to get continuous update of the state of the memristor;
- Support high-frequency and pulsed input signals.

B. THE FEEDBACK AMMETER COMPARED TO THE MEMRISTOR-RESISTOR VOLTAGE DIVIDER FOR DEVICE CHARACTERIZATION

The overall measurement setup is presented in Fig. 1(a). The circuits shown in Fig. 1(b) and Fig. 1(c) are used alternately as ''memristor circuit setup'' in Fig. 1(a). Their V_i and V_o nodes are directly connected to the function generator and the digital oscilloscope, respectively, of the Digilent *Analog Discovery* 2 (AD2) [24], a modern, low-cost multi-function instrumentation and data acquisition tool, configured to provide the input voltage $V_{\rm i}$ and to monitor the output voltage $V_{\rm o}$. The objective is to compute the memristance in all moments as a function of the flowing current and the voltage applied to the memristor. However, having constantly a resistor in series with the memristor, as shown in Fig. 1(b), affects its behavior due to the voltage-divider effect.

Therefore, in keeping with the requirements mentioned previously, we suggested instead the feedback ammeter [25] shown Fig. 1(c), to guarantee an invariable voltage drop on the memristor (owing to the virtual ground), to sense the current in a non-invasive manner (by measuring the output voltage) and, at the same time, to protect the memristor limiting the current up to a certain and configurable value. A similar strategy for current limiting using a supply voltage regulator can be found in [26]. Such circuit generates a virtual ground so that the memristor under-test sees at its terminals only the input voltage V_i and ground. By measuring the output voltage $V_{\rm o}$, given a known feedback resistor R_f, the current through the device can be computed effectively for the whole memristance range. Additionally, this topology allows configuring the maximum current by tuning the supply voltage $V_{\rm sup}$ of the op-amp. So, via the feedback analysis, the $V_{\rm sup}$ required to limit the current up to a specific maximum value ($I_{\rm max}$) is:

$$V_{\rm sup} = \pm R_f I_{\rm max} \tag{1}$$

However, $I_{\rm max}$ is not a hard current limit as it depends on R_f and on the op-amp saturation near the rails. In fact, when the maximum current is reached and $V_{\rm o}$ saturates in either of the supply voltage rails of the op-amp, the current through the memristor is given by:

$$I_m = -\frac{V_o}{R_m + R_f} + \frac{V_i}{R_m + R_f} \tag{2}$$

Assuming $R_f \gg R_m$ at the end of the SET ($\rm R_{OFF} \rightarrow R_{ON}$ switching) process, and with constant $V_{\rm o} = V_{\rm sup}$, it turns out that $I_{\rm max}$ grows linearly with $(1/R_f)V_{\rm i}$, i.e. $I_{\rm max}$ increases with $V_{\rm i}$ but the rate is made negligible by selecting properly the R_f. This is illustrated in Fig. 2 where we demonstrate such current limiting property. It can be noticed that once $V_{\rm o}$ has saturated during the SET process, the current I_m through the memristor keeps increasing beyond $I_{\rm max}$ but at a much lower pace, as requested, while the voltage drop seen by the memristor (i.e. the difference between the input voltage and that at the inverting input $V_{\rm i}$-$V_{\rm inv}$) is kept almost constant.

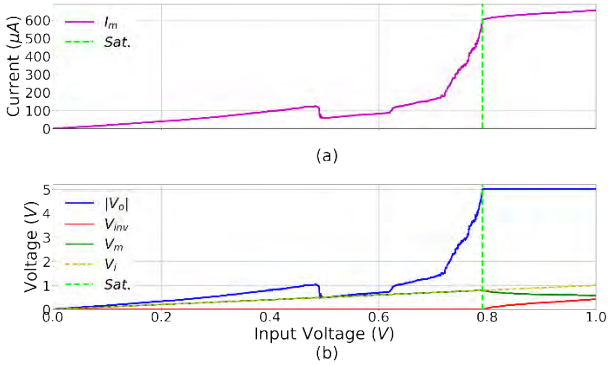

FIGURE 2. Current limiting property of the feedback ammeter in a SET process of a memristor by *Knowm Inc.* The graphs show (a) the evolution of the current through the memristor with input voltage and (b) the voltage in all nodes of interest during the application of an increasing positive input voltage ramp $V_{\rm i}$. $V_{\rm inv}$ is the voltage at the inverting input of the op-amp which, after saturation, it increases with $V_{\rm i}$ to keep constant the voltage drop on the memristor ($V_{\rm m} = V_{\rm i}$- $V_{\rm inv}$). $R_{\rm f} = 8.3{\rm k}\Omega$ and $|V_{\rm sup}| = 5$V. The vertical dashed line is a guide to the eye, indicating the saturation point.

Considering the component selection, as far as the op-amp is concerned: (a) it should ideally not present a ''phase reversal'' when one of its inputs is driven to one of the supply voltages (i.e. saturation). In such a case, the output may slew to the opposite polarity from what is expected, which could lead to memristance calculation faults. (b) It should be a ''rail to rail'' opamp, making easier the calculation of the required $V_{\rm sup}$ for a desired $I_{\rm max}$, defined by (1). (c) It should preferably operate at a wide range of supply voltages, so as to enable a wide range of possible $I_{\rm max}$ values. Some additional features are: the *gain-bandwidth product* (GBWP), which describes the op-amp behavior with frequency. However, since experiments on memristors rarely involve too high frequency input signals, GBWP is not really a critical parameter for this setup. Finally, the *offset voltage*, which represents the voltage difference caused by a variation between bias currents on the two inputs, owing to the fact that the input impedance is not infinite; it is a parameter found in the datasheet that can be measured and compensated, if necessary. Everything considered, the impact of any nonidealities of the components to the measurements is taken into account collectively while computing the average measurement error for the entire memristance range [18].

In order to compare experimentally the two alternative topologies, both circuits shown in Fig. 1(b) and Fig. 1(c) were prototyped on PCBs that connect directly to the AD2 instrument. This way, any inductance owing to the connection wires was eliminated. In all measurements, the memristors used were BS-AF-W discrete self-directed-channel bipolar devices [27], developed and commercialized in 16-pin ceramic DIP packages by *Knowm Inc*. [13].

Figure 3(a) shows a picture of the experimental setup with the voltage divider PCB, whereas Fig. 3(b) shows typical *i-v* hysteresis loops highlighting the expected fingerprints of memristors, i.e. the fact that the *i-v* loops are always pinched at the origin and that their lobes shrink with increasing

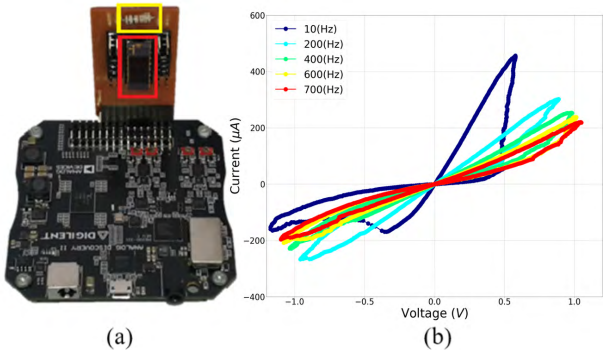

FIGURE 3. (a) The experimental setup based on Fig. 1(a) with a PCB corresponding to Fig. 1(b). The red square shows the DIP 16 *Knowm Inc.* memristor package, whereas the yellow square shows the series resistor R_S. (b) *i-v* hysteresis loops for different frequencies of the applied symmetric triangular input signal with $R_S = 2\text{k}\Omega$ and 1.5-V input amplitude. In every subsequent cycle, a different frequency was used. The horizontal axis shows the voltage drop on the memristor V_m, not V_i.

frequency of the applied signal. The snapback phenomenon in the *i-v* graphs is attributed to the voltage divider effect.

Likewise, Fig. 4(a) is a picture of the experimental setup with the feedback ammeter. The PCB includes a feedback resistor R_f and the MIC 7122YMM op-amp, which we preferred for its wide V_{sup} range support, that is also compatible with the ±5V voltage supply given by the Digilent AD2 (it was used to provide V_{sup} to the op-amp). This op-amp has a typical offset of 0.5 mV which can reach up to 9 mV. For instance, if we apply a 200-mV input pulse, in worst case the offset could cause a 4.5% read error, whereas for the amplitude values we used the measurement error was only 0.25%. The larger the input voltage, the lower the read error percentage. Figure 4(b) shows *i-v* hysteresis loops corresponding to those shown in Fig. 3(b), while limiting the current at 800μA. Although the particular frequency values are not important, their selection is relevant to the amplitude of the applied input voltage. Likewise, Fig. 4(c) shows similar *i-v* hysteresis loops when different I_{max} limits were set by modifying the programmable voltage output of AD2, thus proving the configurable current-limiting property. Generally, we observe that in Fig. 3(b) the maximum current achieved is much lower due to the fact that the voltage drop on the device during switching cannot be kept fixed. Moreover, driving and operating the op-amp out of its linear region is of course not an objective, as the circuit will behave differently and measurements will be influenced. So, while processing the measurement data for the time when the op-amp is saturated, we keep the last memristance value before saturation starts and the first one after saturation ends, and assume that memristance change is linear in-between these values.

It should be also considered that, while the input voltage is always acquired directly from the AD2, the current is computed via measuring V_{o}, which has a different transfer function in each circuit. So, in order to better capture the circuits' performance and limitations, we performed an analysis while modeling the memristor as an equivalent impedance Z_{m} of the resistance R_{m} (memristance) and a parasitic capacitance C_{m} [see Fig. 1(d)], owing to the MIM structure (likewise in [22], [23].) The objective was to identify up to what frequency the measurements were not affected by C_{m} and/or the opamp pole. For both circuits shown in Fig. 1(b) and Fig. 1(c), the transfer function can be computed assuming a constant Z_m for the memristor. In the case of the feedback ammeter, the op-amp was approximated as a single-pole system with time constant τ and open-loop gain A_{ol} [28] (values estimated from information in the datasheet). The transfer function for the feedback ammeter is:

$$\frac{\text{V}_\text{O}(s)}{\text{V}_\text{i}(s)} = \frac{A_{ol} \cdot R_f \cdot (1 + sC_mR_m)}{R_{ss} \cdot \left(1 + sC_m \cdot R_{pp}\right) \cdot (1 + s\tau) + A_{ol} \cdot R_m} \tag{3}$$

where $R_{ss} = R_m + R_f$ and $R_{pp} = R_f||R_m$ (|| means parallel connection). On the other hand, for the voltage divider it is:

$$\frac{\text{V}_\text{O}(s)}{\text{V}_\text{i}(s)} = \frac{R_m}{R_m + R_s} \frac{1 + sC_mR_m}{1 + sC_m(R_m||R_s)}. \tag{4}$$

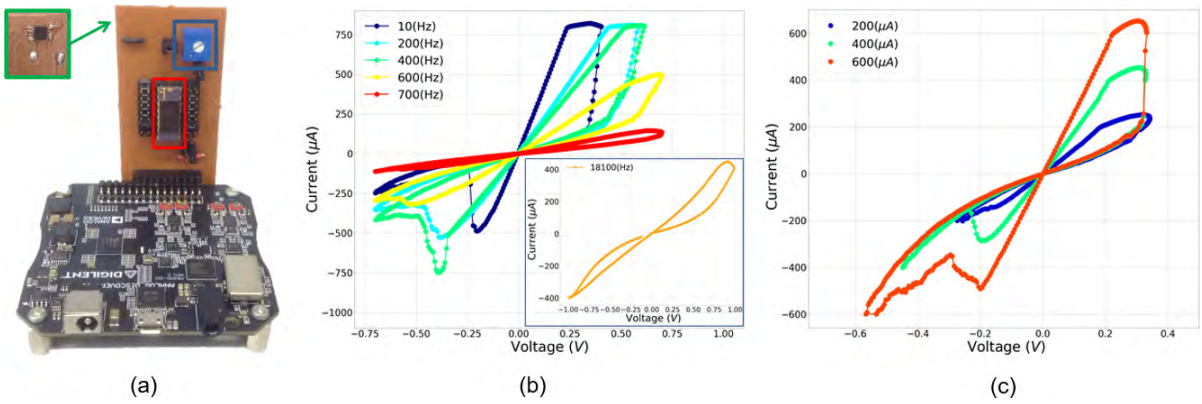

FIGURE 4. (a) The experimental setup of Fig. 1(a) with a PCB corresponding to Fig. 1(c). The red square shows the slot where a DIP 16 *Knowm Inc.* memristor package is connected. The green square shows the op-amp (located at the back side of the PCB) which, together with the feedback resistor in the blue square (a potentiometer) make the feedback ammeter that is connected to the Digilent AD2. (b) *i-v* hysteresis loops for different frequencies of the applied symmetric triangular input $V_i(t)$ with amplitude 0.7V. Current was limited to $I_{\text{max}} = 800\mu$A. For each subsequent cycle a different frequency was used. The inset shows an *i-v* taken for a much higher frequency signal and 1-V amplitude. (c) *i-v* loops for different current limits I_{max}, for input voltage $V_i(t) = 0.75\sin(2\pi ft)$ and $f = 100$Hz. After every cycle, the V_{sup} was configured to set the new I_{max}. In (b) and (c) the horizontal axis shows the voltage drop on the memristor V_m, not V_i.

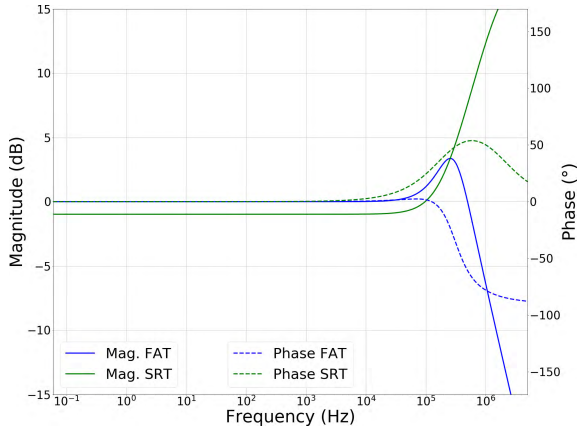

FIGURE 5. Bode plot for the transfer function of the feedback ammeter topology (FAT) (3) and the series resistor topology (SRT) (4), assuming a constant Z_m. Parameters used: $R_m = 8.3\text{k}\Omega$, $C_m = 100\text{pF}$ (which was purposely set nearly 3× the real measured C_m, to give us a safer margin), $R_f = 8.3\text{k}\Omega$, $A_{ol} = 100000$, $\tau = 4\text{ms}$, and $R_s = 1\text{k}\Omega$. A BK Precision 5491B multimeter was used to calibrate the AD2 instrument and also to measure precisely and set the R_f resistance via a potentiometer.

Based on (3) and (4), the frequency response of both systems was studied. The used parameter values were either measured, found in the datasheet, or estimated in the range of real measured values, for consistency. After performing a sensitivity analysis while probing several R_m values, it was figured out that R_m did not affect significantly the system behavior. Therefore, we assumed a fixed R_m within the memristance range of the target devices, selecting $R_\text{m} = R_\text{f} = 8.3\text{k}\Omega$ to leave gain at 0dB. Figure 5 shows the respective Bode plot. It can be seen that the output response is not significantly affected unless high frequency signals are applied. Of course, if Z_m increases, then the amplification will possibly affect lower frequency inputs.

In short, the experimental results showed that the series resistor R_s affects the memristance evolution, something that does not happen with the feedback ammeter approach. The latter allows configurable current limiting in a noninvasive way (i.e. without a series resistor.) It is worth mentioning also that a properly selected value for the fixed series resistor R_s to serve for current limiting is not necessarily a good value for current sensing as well. According to [29], a small R_s would be enough for current limiting, having also a positive impact on device endurance, whereas for current sensing the optimum R_s depends on the R_m range and on the target application requirements (e.g. the geometric mean of the high resistive state (HRS) and the low resistive state (LRS) was recommended in [30] for binary readout). In our experiments R_s value was selected by trial and error to maximize the achieved R_m window). All in all, while the memristor-resistor voltage divider topology is generally a rather good choice for current limiting and possibly for state programing purposes, according to results in [19] and [20], the suggested feedback ammeter topology results better for the characterization of memristors, since current sensing and current limiting are both achieved simultaneously and in a noninvasive way.

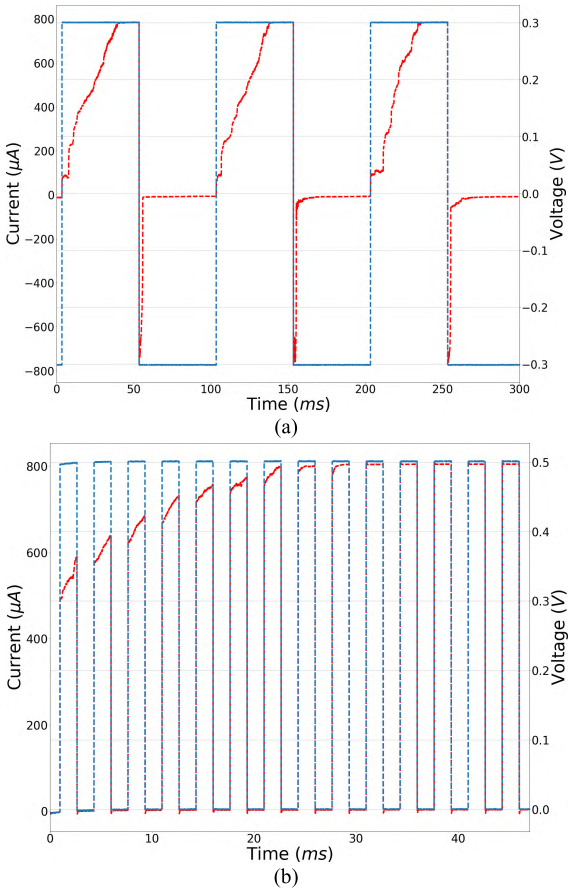

FIGURE 6. Current response (red line) under the application of different pulsing protocols, involving square pulse inputs of constant amplitude and duration (blue line). (a) Wide-enough SET-RESET pulses for binary switching. (b) A series of narrower SET pulses applied consecutively to achieve multi-level programming. Current limiting is observed as the latter saturates at 800μA for a specific V_{sup} given by (1).

So next we proceed with more experimental results obtained using only the feedback ammeter topology.

III. EXPERIMENTAL RESULTS ON MULTI-LEVEL STATE TUNING OF MEMRISTORS

The ability to control/program the state of the memristor with good precision is a very desirable property, both for memory and computing applications. Therefore, next we focus on measurements with pulsed SET/RESET inputs applied to *Knowm Inc*. memristors, aiming to analyze the impact of the pulse properties (amplitude, duration, polarity) on the device state, as well as the dependence of the switching process on the initial condition of the device.

A. MULTI-LEVEL TUNING EXPLORATION

Figure 6 shows the device behavior under two different pulsing protocols. More specifically, in Fig. 6(a) we used 50-ms wide and 0.3-V high square SET pulses, each one applied after a negative RESET pulse. The pulses were selected purposely wide-enough to observe how conductance constantly changed while the input voltage was kept constant, until the I_max current was reached. In fact, by such

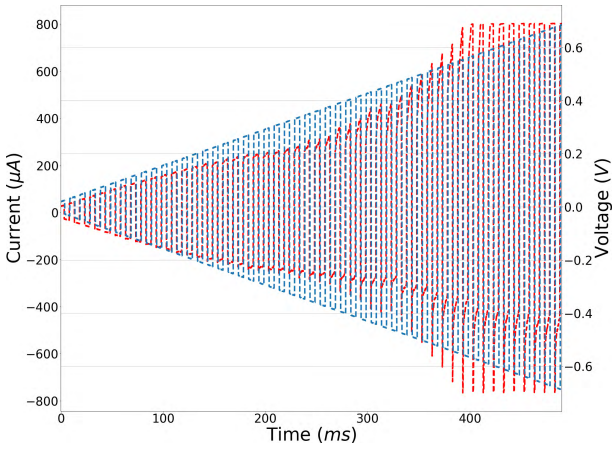

FIGURE 7. Amplitude sweep of 5ms-wide 50Hz SET-RESET square pulses of gradually increasing amplitude (blue line) ranging between 20mV and 700mV. The current (red line) starts to change significantly near 250ms, when the voltage amplitude exceeds 0.4V, and finally saturates at 800μA.

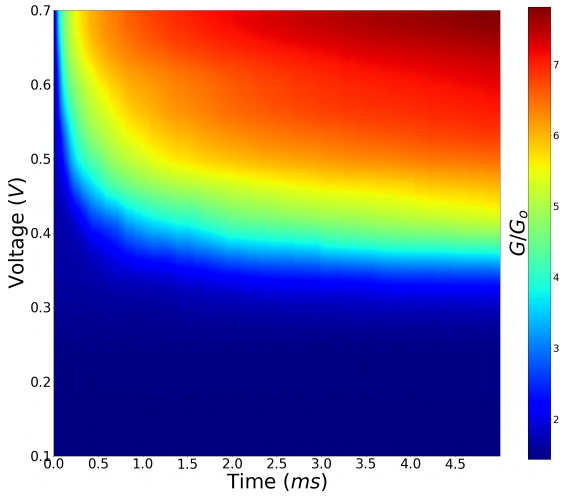

FIGURE 8. Dependence of conductance evolution on the amplitude and the width of the applied SET voltage pulse. The memristor was first initialized with precision around 8.5kΩ according to algorithm proposed in [31]. Then a 5-ms wide pulse of a specific amplitude was applied. Pulse amplitudes ranged between 0.1V and 0.7V, incrementing by 0.04V. For each amplitude, the experiment was repeated 10 times and the mean values of the conductance (normalized to the quantum conductance $G_o = 77.5$uS [32]) are shown (interpolated) in a color representation.

conductance change, it can be aspired that narrower pulses of similar amplitude, if applied consecutively, can enable multi-level memristance tuning. The latter is precisely shown in Fig. 6(b) where a series of 5ms-wide and 0.5V-high SET pulses were applied, with 5ms pulse separation and without intermediate RESET step. It can be observed that current increases gradually, proving that memristance changes in an incremental manner. This property is very much desirable when multi-level switching is required in applications such as multi-level resistive memories and synaptic electronics in neuromorphic computing. Hence, the proposed setup allows multi-level memristance tuning measurements.

In Fig. 7 we further elaborate on this by gradually increasing the amplitude of the input square waveform to highlight the change-rate dependence on it. State change-rate is observed much higher at higher amplitudes, as expected from similar results in the literature (here above 0.4V). Based on this experiment, given a specific pulse width, the end-user can select the pulse amplitude which satisfies their application requirements. When the input signal frequency increases, more consecutive pulses of a certain amplitude are required to cause the same amount of change in the device state.

B. SEARCH FOR TUNING EFFECT DEPENDENCIES ON THE APPLIED PULSE CHARACTERISTICS

By observing experimental results about memristor characterization, published in several relevant works in the literature, it can be concluded that tuning the state of memristors is generally a function of the amplitude and duration of the applied voltage pulse.

In this direction, Fig. 8 aims to reveal the dependencies of conductivity change on these two variables, namely pulse *duration* and *amplitude*. More specifically, a multi-step precise RESET process (according to the programing algorithm proposed in [31]) took place before each experiment to make sure the device was always left in a very similar starting point and thus to mitigate any later dependence of the results on initial conditions. Then, a 5-ms wide SET pulse of a specific amplitude was applied and the time-evolution of the conductance was monitored. The same experiment was repeated for several different amplitude values.

By observing Fig. 8 (the conductance evolution is read horizontally from left to right for a specific amplitude selected in the vertical axis) we notice that there is a distinguishable separation (approximately at 0.35V) between voltage amplitudes that hardly affect the device state and those that have a more immediate impact. The *Knowm Inc*. bipolar memristors used in this work demonstrate threshold-based incremental switching behavior. For instance, pulses with amplitudes higher than 0.6V would serve better for binary switching, even for a small selected pulse-width. On the other hand, amplitudes closer to 0.4V could permit analog tuning, whereas pulses of amplitude less than 0.3V can be used to sense the device state without affecting it. Such absolute values mentioned here may be slightly different from device to device due to variability and dependence on the prior forming process. Overall, the final achieved state depends not only on the selected pulse amplitude but also on its duration; pulses of lower amplitude need more time to drive the device to a specific state.

Therefore, Fig. 9 aims to further uncouple the effect of the two involved variables of interest for both polarities. Likewise in [33], the dependence of conductance change on the pulse *amplitude* was first studied. To this end, a sequence of fixed-width pulses of increasing amplitude were applied. On the other hand, a fixed amplitude was used while varying the pulse *duration* to steer our study towards dependencies on this variable. After the application of every such pulse, the conductance was read and stored. Results for the SET

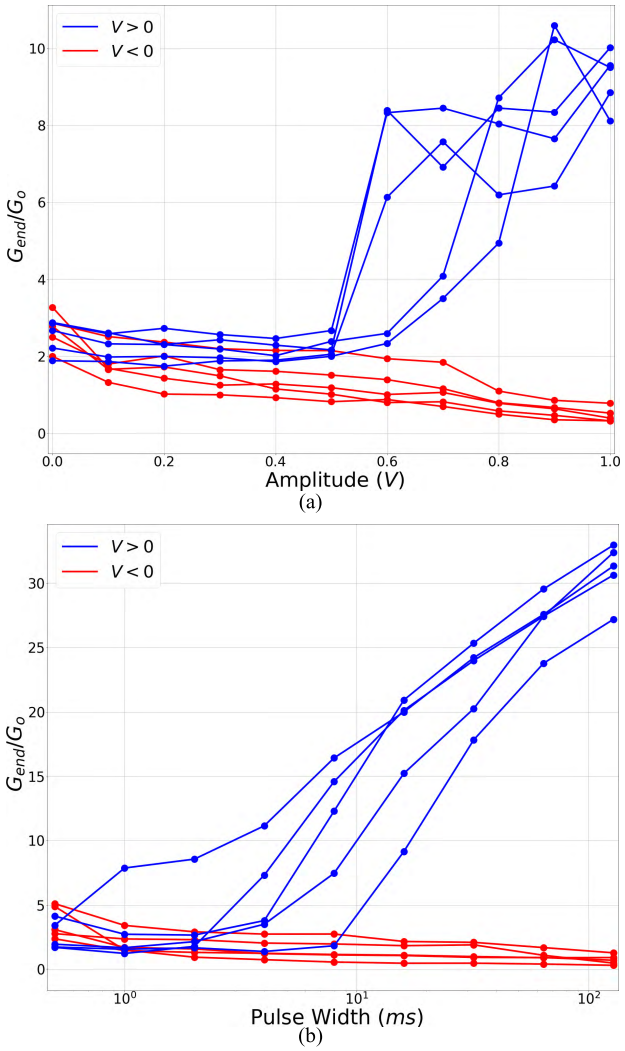

FIGURE 9. Final conductance (normalized to G_o) as a result of the application of a specific pulse train. (a) A sequence of 10 SET (blue lines)/RESET (red lines) pulses of fixed width (10ms) and increasing amplitude (by |0.1|V) were applied. (b) A sequence of 10 SET (blue lines)/RESET (red lines) pulses of fixed amplitude (0.5V) and increasing duration (by 0.2ms) were applied. After every pulse the conductance was stored. The experiment was repeated 5 times.

process are in line with the results shown previously in Fig. 7 and Fig. 8. Unless the pulse amplitude exceeds 0.4V, there is no significant effect on the device state. However, it is further proved that there is no hard voltage threshold; in fact, even when applying a SET pulse of just 0.5V, which according to Fig. 9(a) should not have a great impact to the device state within the first 10ms, eventually the final achieved conductance can be quite high if the applied pulse is kept long enough, as observed in Fig. 9(b). As far as the RESET process is concerned, conductance decreased gradually at a fairly constant pace as the state approached the HRS, regardless of the pulse characteristics. We underline here that owing to device-to-device variability and dependence on the forming process, although the results in Fig. 9(a) are qualitatively in line with those in previous figures such as

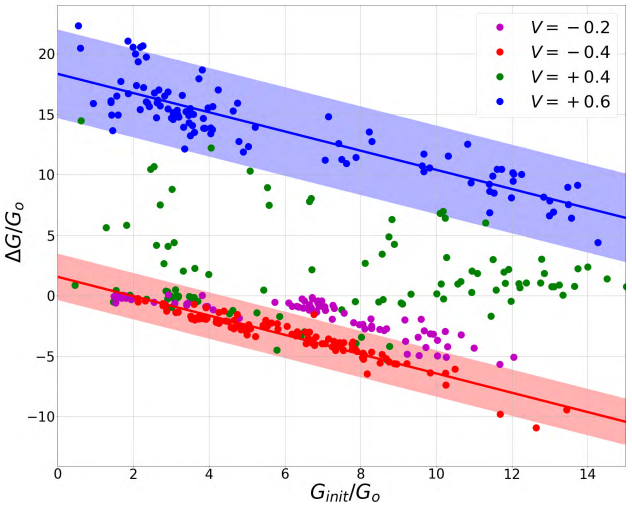

FIGURE 10. Conductance change after the application of a specific pulse, depending on the initial condition/state of the device (both magnitudes are shown normalized to G_o.) 100 points are shown for every different amplitude of the applied 2-ms wide SET or RESET pulse. A simple linear regression was fit to all cases (only two are shown for clarity) and two standard deviations (2σ) are shown with a brighter tone, as a guide to the eye.

Fig. 8, the switching time scale is quite different, without loss of generality.

C. SEARCH FOR TUNING EFFECT DEPENDENCIES ON THE INITIAL CONDITIONS OF THE MEMRISTOR

Given the conductance evolution results observed in the previous figures, we searched for dependencies of the change rate on the initial state/condition of the memristor. Figure 10 shows the trends in the dependence of the conductance change ΔG on the initial conductance (state) G_{init} when a pulse of specific amplitude and duration was applied. 100 measurements were taken on the same device for each one of the four different pulse amplitudes. For each measurement, the memristor was initialized using a pulse whose amplitude was randomly selected within a specific range, to distribute G_{init} along the desired spectrum of values shown in Fig. 10. The G_{init} was read by applying a 1-ms wide and 0.12-V high pulse. Next a 2-ms wide SET or RESET pulse of a specific amplitude was applied and the conductance was finally read again with the same read pulse to compute the difference ΔG.

By observing Fig. 10, we conclude that there are some patterns of conductivity change, providing us with useful information for multi-level tuning requirements. SET change is higher/lower when G_{init} is lower/higher, whereas the opposite relation is observed for the RESET change. Moreover, the higher the amplitude of the applied pulse, the higher the ΔG caused on the device. These observations are valid in the whole dynamic range of conductance. So, after the application of a specific voltage pulse, the final state of the memristor is clearly affected by its initial state. This is quite an important characteristic being omitted by behavioral device models of the literature and window functions are normally necessary

to incorporate such switching properties [34]. Furthermore, by observing these statistics shown in Fig. 10 we notice that a simple linear equation could provide a very good approximation of the final state of the device, given an initial state and specific properties of the applied programming pulse. In other words, given a specific G_{init} and a desired G_{final}, this analysis reveals that there is a particular pulse (or a series of consecutive pulses) which can result in the required transition $G_{init} \rightarrow G_{final}$ and the pulse characteristics could be theoretically predicted with quite good precision. In our case, the precision is better for the RESET process as the dispersion of the obtained data is much smaller.

IV. CONCLUSION

A low-cost, yet complete and flexible instrumentation solution for characterizing memristors was presented, exploiting the properties of the well-known feedback ammeter on memristor measurements. We achieved: direct control over the voltage drop on the device, current-sensing in a non-invasive way with good precision in the entire dynamic memristance range, and configurable current limiting (compliance). Experimental results from measurements on commercial memristor devices from *Knowm Inc*. revealed dependencies of memristance switching behavior not only on the properties of the applied pulsing protocol (amplitude, duration) but also on the initial condition of the device. Such information presented altogether in this work, results useful to the end-user working on memristor device modeling or planning to use memristor devices in memory, computing or learning applications. Multi-level tuning is considered to be a pre-requisite for synaptic devices within neuromorphic architectures. The experiments in this paper cover input pulses of frequencies up to a few kHz. However, to study memristor as synthetic synapse, high frequency signal generation of up to 10s of MHz frequency is desirable. The used topology as well as all the conducted experiments were thoroughly discussed in the paper, in an attempt to facilitate comprehension of memristive behavior and motivate researchers and enthusiasts to expand experimentation beyond the labs and dare implement/test memristor application ideas in hardware.

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