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A 0.5-V Fully Synthesizable SAR ADC for On-Chip Distributed Waveform Monitors

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ABSTRACT This paper presents a fully synthesizable successive-approximation-register (SAR) analog-to-digital converter (ADC) for on-chip distributed waveform monitoring in a low-power system-on-chip (SoC). All blocks in the proposed ADC are designed using only standard digital cells, enabling an auto-generation based on regular digital design tools. Therefore, the proposed ADC provides enhanced portability and reusability which facilitate integration into various functional blocks requiring testing and diagnosis. To implement the SAR ADC, a synthesizable voltage digital-to-analog converter (VDAC) and a rail-to-rail hybrid comparator are proposed in this paper. An inherited nonlinearity of the standard-cell-based VDAC is compensated by a histogram-based soft calibration which can be easily embedded in a waveform reconstruction module. In addition, an oversampling technique with a redundant error correction method is employed to realize the fully synthesizable design without a sample-and-hold (S/H) circuit. The proposed ADC was fabricated in 28-nm CMOS technology, occupying an active area of 0.002 mm^2. The ADC achieves 5.39-bit effective-number-of-bit (ENOB) at 500-kS/s sampling rate. The power consumption of the ADC is 92.2 μW with a supply voltage of 0.5 V.

INDEX TERMS Analog-to-digital converter, comparator, digital-to-analog converter, on-chip oscilloscope, redundant error correction, standard-cell-based design, successive-approximation register, synthesizable design.

I. INTRODUCTION

As system-on-chips (SoCs) integrate more functional blocks, various circuit and system issues that influence the operation of the SoCs have emerged such as signal integrity, power integrity, and malfunction [1]. Because those issues not only degrade the performance of the functional blocks but also cause a malfunction of the entire SoC, it is important to discover any abnormally operating circuit during testing and validation processes. Therefore, the demand for an on-chip waveform monitor to diagnose SoCs has increased [1]–[3]. The waveform monitors reported in the prior studies were mainly focused on high-speed signaling [2] or power delivery diagnosis [4]. However, as the demand for SoCs in internet-of-things (IoT) applications has grown, an on-chip waveform monitor specialized for the IoT applications has become necessary in accordance with the SoCs. Because many IoT applications require a low-voltage operation [5]–[7] rather than high resolution or high bandwidth, the waveform monitor has to operate with the low supply voltage. In addition, a distributed waveform monitoring system is needed because of the difficulty in implementing an analog signal buffer that can be operated with the low supply voltage. Thus, a compact active area with enhanced portability and reusability are important for realizing the distributed structure and reducing both the design time and the manufacturing cost [8]. Therefore, a synthesizable digital implementation of the on-chip waveform monitor has been preferred to satisfy those requirements.

Fig. 1 shows the conceptual diagram of the proposed waveform monitoring system. The on-chip distributed monitors

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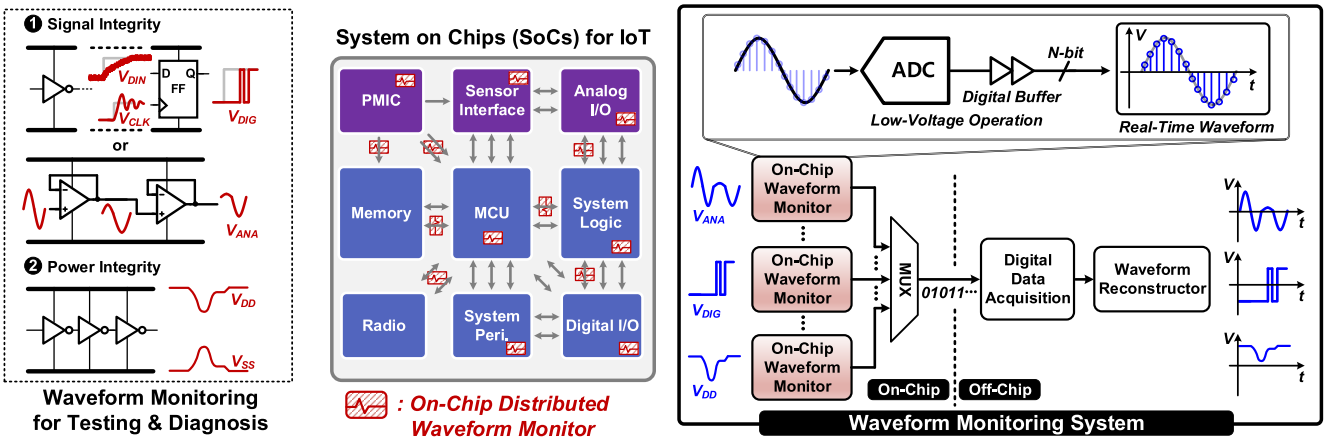


FIGURE 1. Conceptual diagram of the on-chip distributed waveform monitoring system for testing and diagnosis of system-on-chips (SoCs).

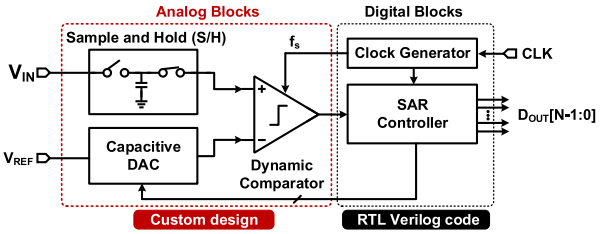


FIGURE 2. Block diagram of the conventional SAR ADC structure.

transmit waveform data in digital format to an off-chip reconstruction module through a multiplexer, which facilitates the integration of multiple modules with a limited number of input/output (I/O) pins. The off-chip processing module reconstructs the on-chip signal waveforms from the acquired digital data. For the digital implementation of the on-chip waveform monitors, it is essential to realize an analog-to-digital converter (ADC) in a synthesizable digital design within a compact area. Because analog circuits in a conventional ADC structure are difficult to implement using only standard digital cells, synthesizable ADC designs from the prior studies were based on a stochastic flash ADC [9]–[13]. By synthesizing thousands of comparators based on standard digital cells, the stochastic flash ADC converts an analog input into a quantized digital output using Gaussian distribution of the comparator offset. The stochastic flash ADC provides portability and reusability owing to the synthesizable design, but the required number of comparators for improving resolution is increased exponentially, occupying large silicon area. The large power consumption by a lot of comparators and post-processing blocks is also problem to be used for the waveform monitors. Hence, an optimized ADC structure for the on-chip distributed waveform monitors is required instead of the stochastic flash ADC.

Among several ADC structures, a successive-approximation-register (SAR) ADC is a feasible structure for the synthesizable design. A conventional SAR ADC structure has a capacitive digital-to-analog converter (DAC), a comparator, and a SAR controller as shown in Fig. 2. The SAR controller is usually synthesized from a register-transfer-level (RTL) Verilog code. Hence, standard-cell-based designs of the DAC and comparator are required to realize the synthesizable SAR ADC. Although the capacitive DAC (CDAC) enables the energy-efficient operation of the SAR ADC, it is difficult to implement the synthesizable CDAC based on the standard digital cells. Therefore, other DAC structures should be investigated for the synthesizable design. In the case of the comparator, a NAND-based synthesizable implementation was examined in several previous studies [10], [11], but the narrow input common-mode range needs improvement for use in the on-chip waveform monitors. Besides the DAC and comparator, an ADC implementation without a sample and hold (S/H) circuit is challenging problem. Unlike the stochastic flash ADC, the SAR ADC needs S/H operation during the successive-approximation procedure. Because of the difficulty in implementing a synthesizable S/H circuit, another conversion method would be needed so that the S/H circuits would not have to be implemented.

This paper demonstrates a fully synthesizable SAR ADC for the on-chip distributed waveform monitoring systems. The proposed ADC is based on the SAR architecture which can reduce the active area significantly compared to that of the stochastic flash ADC. A standard-cell-based voltage DAC and hybrid comparator are proposed to realize both the synthesizable design and the low-voltage operation. By embedding the compensation of the DAC nonlinearity into the waveform reconstruction process, this paper reduces the overhead area and power consumption caused by the ADC calibration block. For the fully synthesizable design, the proposed ADC excludes the use of the S/H circuits and employs an oversampling technique with a redundant error correction, which reduces conversion error induced from the time-varying input signal.

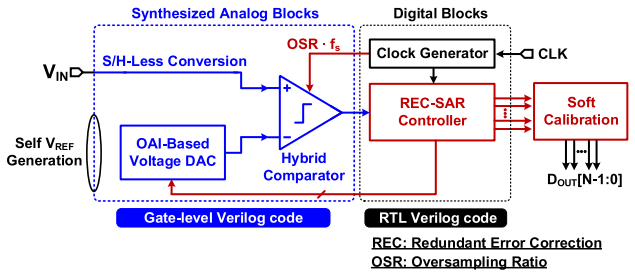


FIGURE 3. Block diagram of the proposed synthesizable SAR ADC structure.

The organization of this paper is as follows. Section II presents the overall architecture of the proposed SAR ADC. A detailed design of the synthesizable voltage DAC and hybrid comparator is explained in Section III. Then, Section IV describes the implementation of the proposed SAR ADC. The measurement results of the fabricated ADC are explained in Section V, and Section VI concludes this paper.

II. PROPOSED ARCHITECTURE OF SYNTHESIZABLE SAR ADC

The overall architecture of the proposed SAR ADC is shown in Fig. 3. The SAR ADC has a similar structure as the conventional SAR ADC in Fig. 2, but three key features of the proposed ADC enable the fully synthesizable design: 1) synthesizable voltage DAC and hybrid comparator, 2) a soft calibration for the ADC nonlinearity, and 3) an S/H-less successive approximation scheme that uses an oversampling technique and a redundant error correction (REC). Considering the waveform monitoring applications, the proposed ADC is implemented with a single-ended structure. In addition, the ADC operates without any external reference voltage or bias current, which further improves the portability.

To implement the synthesizable DAC, a voltage DAC (VDAC) is proposed and employed in the ADC instead of the conventional CDAC. The VDAC is made up of OR-AND-Invert (OAI) logic gates available in the standard digital-cell library, and the overall VDAC is defined as a gate-level Verilog code. Hence, the VDAC can be generated using regular digital design tools. The proposed ADC employs a binary-weighted 7-bit VDAC. This paper also proposes a synthesizable hybrid comparator based on NAND and NOR logic gates, which provides an extended input range compared to the conventional NAND-based comparator [10], [11]. Hence, the synthesizable VDAC and hybrid comparator provide a wide conversion range of the ADC and empower the waveform monitor to detect a full range of arbitrary waveforms.

However, the synthesizable ADC shows a nonlinear transfer characteristic because the VDAC exhibits a non-uniform voltage step. An on-chip calibration logic using an extra DAC unit can improve the linearity, but the integrated calibration logic increases the number of control signals and active area of the ADC. Considering the waveform monitoring

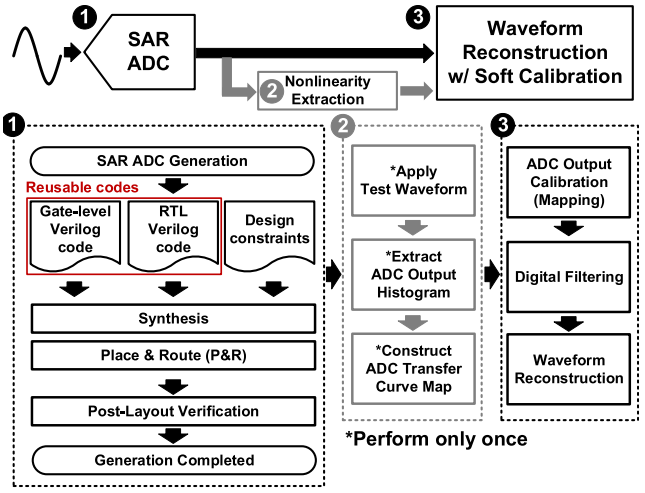


FIGURE 4. Design flow and calibration process of the proposed SAR ADC.

applications that use an off-chip waveform reconstruction block, it is more efficient to incorporate the ADC calibration in the waveform reconstruction process. Therefore, this paper proposes a soft calibration process that can be embedded in the waveform reconstruction block. The soft calibration process performs a remapping of the output digital word based on an estimated nonlinear transfer characteristic of the ADC, providing a linearity-improved waveform reconstruction.

To realize the fully synthesizable design, the proposed ADC adopts an S/H-less successive approximation scheme. The absence of S/H operation causes a conversion error because the input signal can be varied at each successive-approximation step. To reduce the input signal variation during the conversion, the proposed ADC increases the conversion rate to higher than the Nyquist rate in the same manner as the oversampling technique [14]. The oversampling technique shortens the time window for each SAR conversion step, which can reduce the maximum input variation during the time window. In addition, the proposed ADC incorporates the redundant error correction step in the successive approximation process. Even if the varied input signal causes a wrong decision in the previous step, the error correction step tracks the input signal variation and minimizes the conversion error by correcting the wrong decision.

The design flow of the proposed SAR ADC is shown in Fig. 4. The core circuits of the VDAC and the hybrid comparator are generated from gate-level Verilog codes and other digital circuits are synthesized from RTL Verilog codes. The synthesizable ADC descriptions are converted to a physical layout through a place and route (P&R) process using the standard digital design tools. Afterwards, a post-layout verification is performed to validate the synthesized designs. The nonlinear transfer characteristic of the ADC can be extracted by applying a test input signal to the fabricated ADC at the beginning of operation. A histogram of the ADC output can be constructed by applying a triangular input

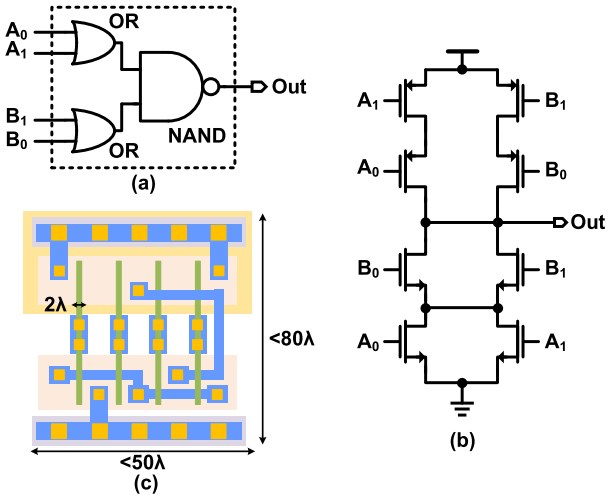
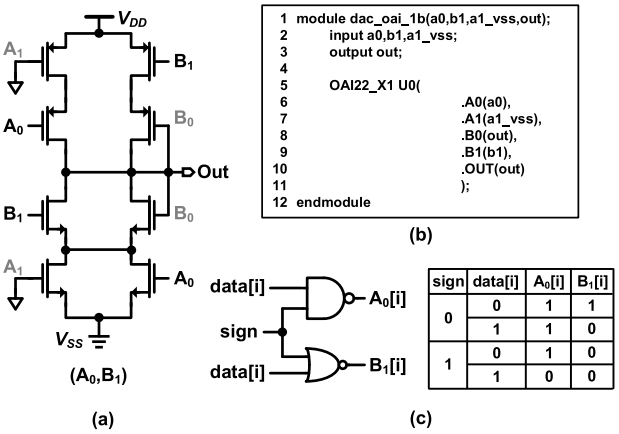


FIGURE 5. (a) Block diagram, (b) schematic, and (c) layout of an OAI22 logic gate in standard digital-cell library.



sign	data[i]	A_0[i]	B_1[i]
0	0	1	1
	1	1	0
1	0	1	0
	1	0	0

FIGURE 6. (a) Schematic of OAI22-based VDAC unit cell, (b) gate-level Verilog code of VDAC unit cell, and (c) input control logic for each bit cell.

signal, and the ADC nonlinearity curve can be extracted from the histogram. Once the nonlinearity curve of the ADC is established, the waveform monitor system reconstructs the measured waveforms continuously by mapping the ADC output onto the nonlinearity curve. Because the nonlinearity of the ADC mainly results from the deterministic cause of the VDAC, the calibration process is performed only once at the beginning of the system operation.

III. SYNTHESIZABLE DAC AND COMPARATOR

A. SYNTHESIZABLE VOLTAGE DAC

The proposed VDAC is designed using OAI22 logic gates which are available in most standard digital-cell libraries. The block diagram and schematic of the OAI22 logic gate are shown in Fig. 5. Two OR gates and a single NAND gate are combined, and total eight transistors constitute the OAI22 logic gate. Assuming a minimum channel length is defined as 2λ, the unit layout size of the OAI22 logic gate is approximated about $4000\lambda^2$, as shown in Fig. 5(c). When the 2λ is about 30 nm, the estimated active area of the binary-weighted 7-bit VDAC is smaller than 0.001 mm^2, which is a highly area-efficient design compared to the design of thousands of comparators in the stochastic flash ADC.

Fig. 6(a) shows configurations of the OAI22 logic gate for the implementation of the VDAC. Among the four input terminals, A_1 and B_0 terminals are tied to zero (or ground) and *Out* node, respectively. The gate-level Verilog code of the OAI22 configuration is described in Fig. 6(b). Depending on sign bit (MSB) and each data bit, the A_0 and B_1 are generated using NAND and NOR gates, respectively. All possible A_0 and B_1 cases are shown in the table in Fig. 6(c). According to the control data, the OAI22 logic gate can be configured to three operational modes. Fig. 7 shows each operational mode depending on the control data. When the control data pair (A_0, B_1) is set to (1,1) for decreasing *Out*, all PMOS

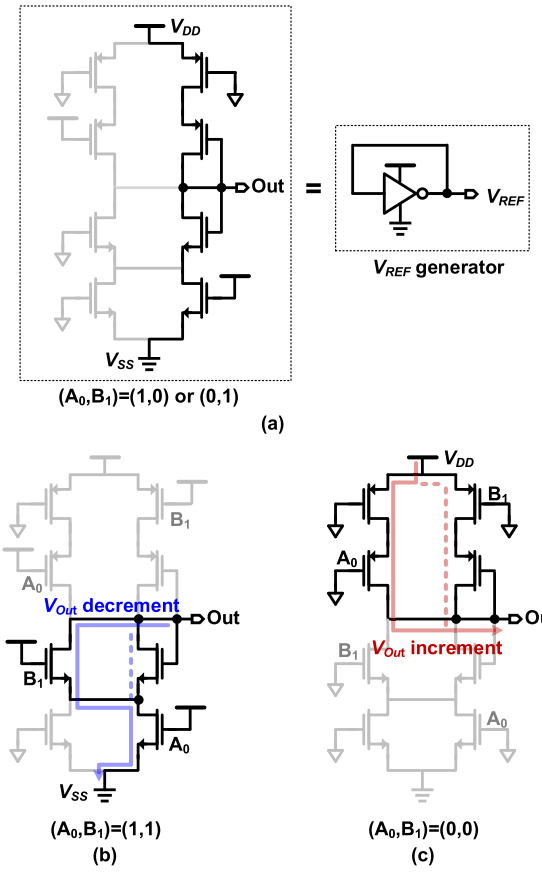


FIGURE 7. OAI22-based VDAC configurations according to input control data of (a) $(A_0, B_1) = (1, 0)$ or $(0, 1)$, (b) $(A_0, B_1) = (1, 1)$, and (c) $(A_0, B_1) = (0, 0)$.

transistors providing a voltage charging path from V_{DD} to *Out* are deactivated, and the OAI22 logic gate decreases the DAC output voltage. On the contrary, when the control data pair is set to (0,0), all NMOS transistors providing a voltage discharging path from *Out* to V_{SS} are deactivated, and the OAI22 logic gate increases the DAC output voltage. Other control conditions of (1,0) or (0,1) make the OAI22 logic

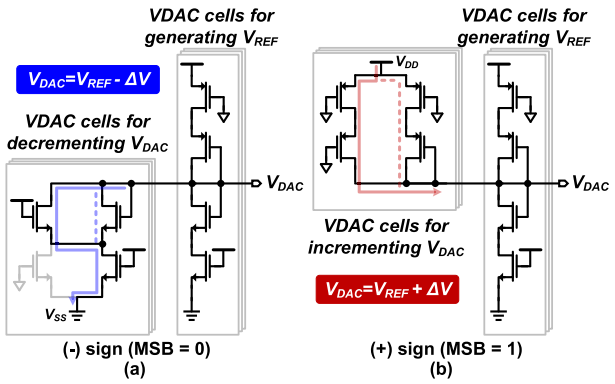


FIGURE 8. Summarized operation of OAI22-based VDAC unit cell with (a) MSB = 0 and (b) MSB = 1.

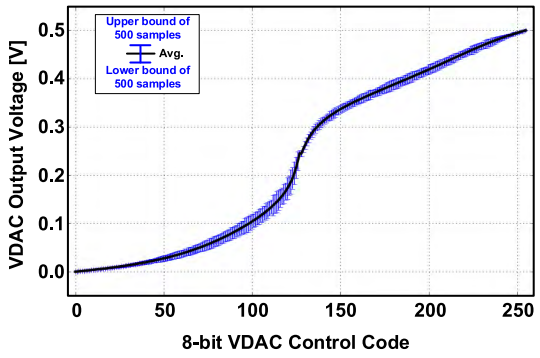


FIGURE 9. Monte Carlo mismatch simulation of VDAC transfer characteristic with 500 trials.

gate generate a reference voltage V_{REF}. Therefore, the DAC output voltage is determined by a ratio between the numbers of OAI22 logic gates configured as the reference generator mode and charging or discharging modes.

The summarized DAC operation of the OAI22 logic gate is shown in Fig. 8. Depending on the sign bit, the OAI22-based VDAC unit cell provides a bipolar operation. In case of the (−) sign data (MSB = 0), each OAI22 operates as either the NMOS discharging logic or the reference voltage generator. Then, the DAC output voltage V_{DAC} is adjusted by the complementary switching between the two configurations in the range from V_{SS} to V_{REF}. In the same manner, in the case of the (+) sign data (MSB = 1), V_{DAC} is controlled by the complementary configurations between the PMOS charging logic and the reference voltage generator in the range from V_{REF} to V_{DD}. Therefore, the bipolar operation of the VDAC provides a rail-to-rail output range from V_{SS} to V_{DD}.

The proposed SAR ADC employs a 7-bit VDAC that can provide an 8-bit resolution owing to the bipolar operation. The 8-bit resolution of the VDAC was determined with consideration for bit losses by the non-ideal effects from the rail-to-rail operation and the automated layout process. Fig. 9 shows the Monte Carlo simulation results of the VDAC according to an 8-bit control code with a supply voltage of 0.5 V. The VDAC shows a nonlinearity which mainly results from the non-uniform voltage steps of the OAI22-based VDAC units rather than a mismatch effect, and this nonlinearity is inevitable in the synthesized DACs [12], [15]. Nevertheless, the nonlinearity of the VDAC is a static characteristic that can be calibrated easily. In addition, the proposed VDAC guarantees the monotonic increment and decrement in the rail-to-rail range, which is much extended from the DACs in [12], [15], [16]. Hence, this paper achieves both the synthesizable design and wide output range by employing the proposed VDAC.

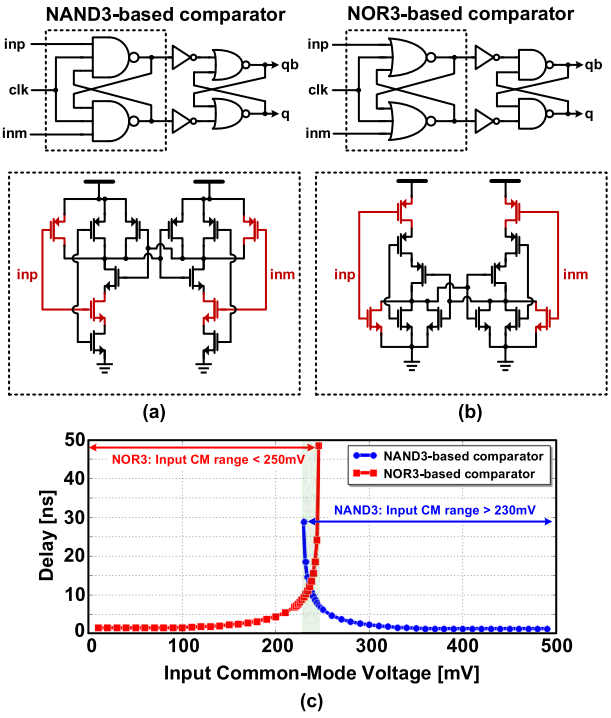


FIGURE 10. Schematics of (a) a NAND3-based comparator and (b) a NOR3-based comparator. (c) Simulated propagation delays of each comparator versus input common-mode (CM) voltage.

B. SYNTHESIZABLE HYBRID COMPARATOR

The stochastic flash ADC in [10], [11] employed a synthesizable comparator made up of NAND3 logic gates as shown in Fig. 10(a). Because the input voltages are applied to both NMOS and PMOS transistors simultaneously, the NAND3-based comparator has a narrow input common-mode (CM) range above half V_{DD} [12]. For example, when a low input CM voltage near V_{SS} is applied to the comparator, the input NMOS transistors turn off and the comparison between two input voltage cannot be performed normally. Hence, the NAND3-based comparator alone cannot support a rail-to-rail input CM voltage range. On the contrary, as shown in Fig. 10(b), the synthesizable comparator made up of NOR3 logic gates provides a narrow input CM range below half V_{DD}, which is a complementary range against the NAND3-based comparator. For the input CM voltage above half V_{DD}, the input PMOS transistors turn off and

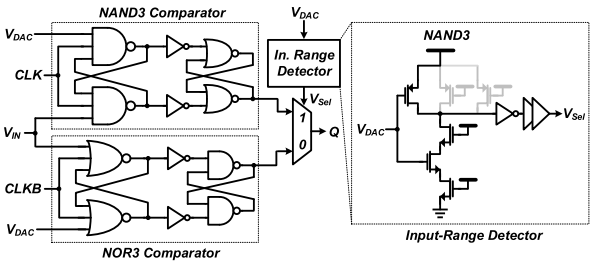


FIGURE 11. Schematic of the proposed hybrid comparator.

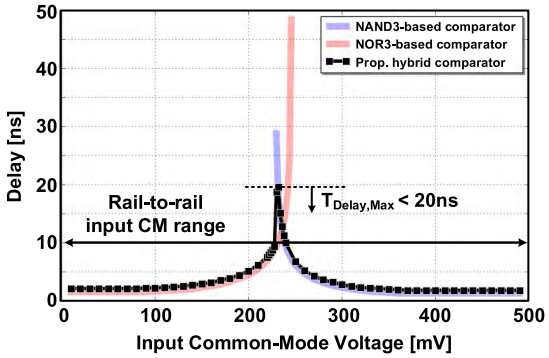


FIGURE 12. Simulated propagation delay of the proposed hybrid comprator versus input common-mode (CM) voltage.

the comparator fails to compare the two input voltages. Fig. 10(c) shows the simulated propagation delay of the two synthesizable comparators with a 0.5-V supply voltage. The NAND3-based comparator and NOR3-based comparator exhibit a contrasting input CM range with an overlapped range around half V_{DD}. Therefore, rather than the use of single NAND3-based comparator or NOR3-based comparator, employing both the NAND-based comparator and the NOR-based comparator simultaneously [17] can provide the rail-to-rail input CM range of the ADC.

The proposed hybrid comparator is shown in Fig. 11. The hybrid comparator is composed of a NAND3-based comparator, a NOR3-based comparator, a 2-to-1 multiplexer, and an input-range detector. All blocks in the hybrid comparator are implemented with the standard digital cells, supporting the synthesizable design. The input-range detector determines which comparator is used for the input voltage comparison according to V_{DAC}. The input range detector is designed using the NAND3 logic gate which is the same as the NAND3-based comparator. If the V_{DAC} is higher than logical threshold voltage of the NAND3, the NAND3-based comparator is used for executing the comparison. Otherwise, the NOR3-based comparator performs the comparison. Because both comparators have the overlapped input range, the input range detector is robust to the non-ideal effects such as an offset or detection error by random noise. The simulated input CM range of the proposed hybrid comparator is shown in Fig. 12. The rail-to-rail input CM range is achieved owing

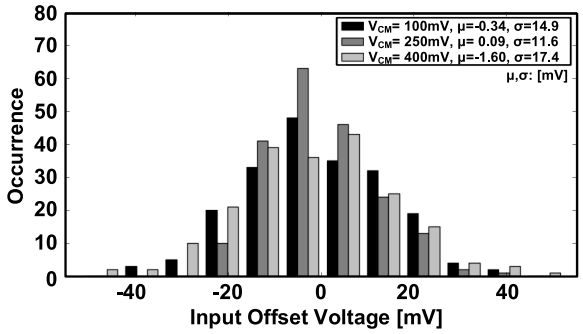


FIGURE 13. Monte Carlo simulation results of input offset voltage of the proposed hybrid comparator versus input common-mode (CM) voltage.

to the hybrid structure. Although the multiplexing structure adds an additional propagation delay of less than 1 ns, the maximum propagation delay is significantly reduced to less than 20 ns because of the input-dependent switching between the two complementary comparators. Fig. 13 shows the Monte Carlo simulation results of the input offset voltage of the proposed hybrid comparator. Compared to the synthesized comparators in [10]–[12], the proposed hybrid comparator shows smaller input offset voltage over the rail-to-rail CM range.

IV. IMPLEMENTAION OF SYNTHESIZABLE SAR ADC

A. SAR ADC IMPLEMENTATION

Fig. 14 shows the implementation of the proposed SAR ADC. All blocks in the SAR ADC are synthesized and generated automatically using the standard digital design tools. The 7-bit binary-weighted VDAC generates V_{DAC} for the successive-approximation procedure. Each bit of the VDAC is composed of the OAI22-based unit cells, and the VDAC decoder controls the bipolar operation of the VDAC based on the 8-bit SAR control signals. The hybrid comparator performs a comparison between V_{DAC} and V_{IN}. Then, the following SAR controller conducts the successive-approximation procedure according to the decision of the hybrid comparator. The clock signals used in the ADC are generated in the clock generator.

To realize the fully synthesizable design, the proposed SAR ADC compares two input voltages, V_{IN} and V_{DAC}, without employing S/H operation. Since V_{IN} varies continuously during each conversion process, the S/H-less comparison results in a conversion error induced by the variation in V_{IN}. Assuming that the input signal with a frequency of f_{sig} is expressed as $v_{in}(t) = \alpha sin(2\pi f_{sig} t) + \beta$, the maximum input voltage variation $\Delta v_{in,max}$ for sampling rate of f_s can be derived as

$$\Delta v_{in,max} = 2\alpha\pi \frac{f_{sig}}{f_s}. \quad (1)$$

According to (1), increasing the sampling rate f_s can reduce the maximum variation $\Delta v_{in,max}$ during each conversion period. Fig. 15 shows the maximum input voltage variation

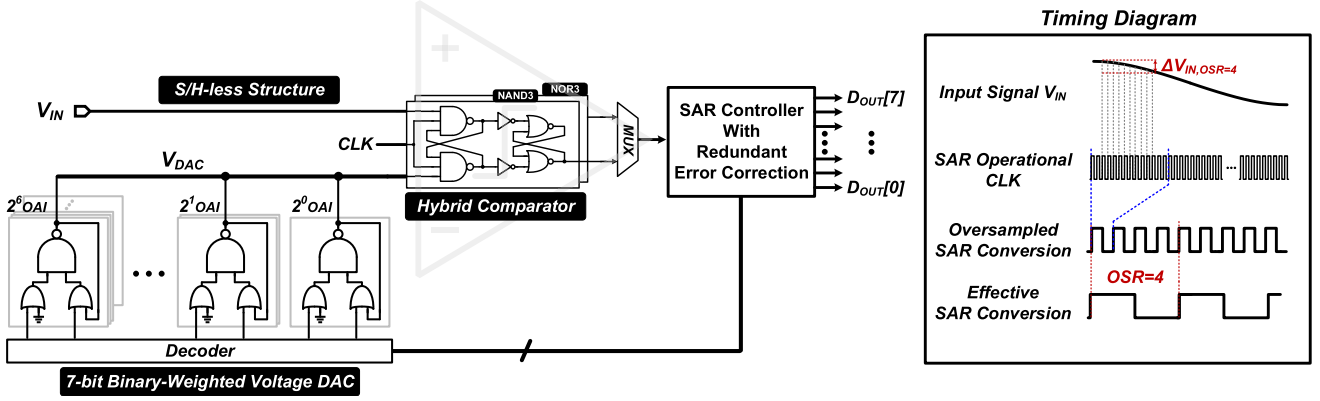


FIGURE 14. Block diagram and timing diagram of the proposed SAR ADC.

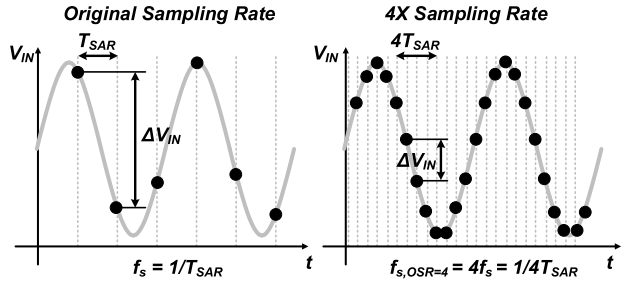


FIGURE 15. Conceptual maximum input signal variation depending on use of oversampling technique.

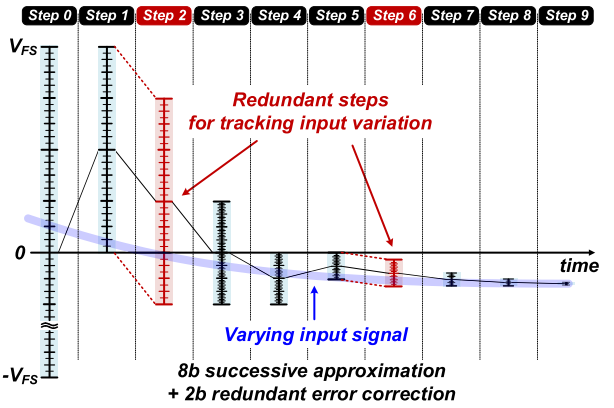


FIGURE 16. Proposed successive approximation procedure with two redundant-error-correction steps.

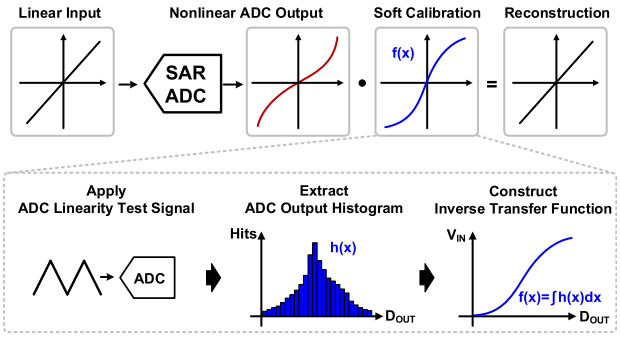


FIGURE 17. Overall waveform reconstruction procedure embedding the soft calibration.

according to an oversampling ratio (OSR). The oversampling technique reduces each conversion period T_{SAR} by the amount of the OSR, and the maximum input variation is also reduced in accordance with the conversion period. Therefore, this paper employs the oversampling SAR structure [14], [18] to minimize the conversion error caused by the S/H-less structure.

In addition to the oversampling technique, the proposed ADC incorporates the redundant error correction (REC) steps into the successive-approximation process. Fig. 16 shows the proposed SAR controller operation. Two redundant steps for tracking the input signal variation are added to the conventional successive-approximation process in the same manner with a binary-scaled error compensation in [19]. For evenly spaced error compensation steps, the two REC steps are inserted at the third step and seventh step, respectively. The redundant steps have same decision range with those in the previous steps, and the ADC can track the input signal variation by shifting the VDAC output voltage level.

B. SOFT CALIBRATION PROCESS

As explored in Section III, the synthesized ADC exhibits the nonlinear transfer characteristics. Hence, this paper proposes a soft calibration process that compensates for the ADC nonlinearity, as shown in Fig. 17. Before a beginning of the monitoring operation, the nonlinear characteristic of the ADC is extracted by applying a low-frequency triangular input signal with a rail-to-rail swing range. Then, a normalized histogram $h(x)$ for the number of hits per ADC output code can be established which corresponds to a derivative of the inverse transfer characteristic of the ADC. Therefore, the ADC inverse transfer function $f(x)$ can be estimated by integrating the histogram function $h(x)$. Once the inverse

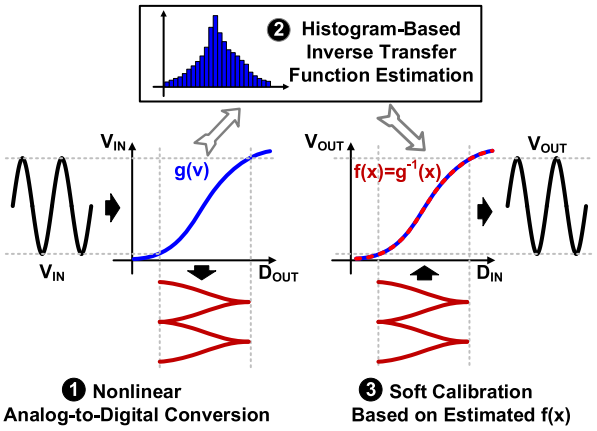


FIGURE 18. Conceptual soft calibration process with a sinusoidal input signal.

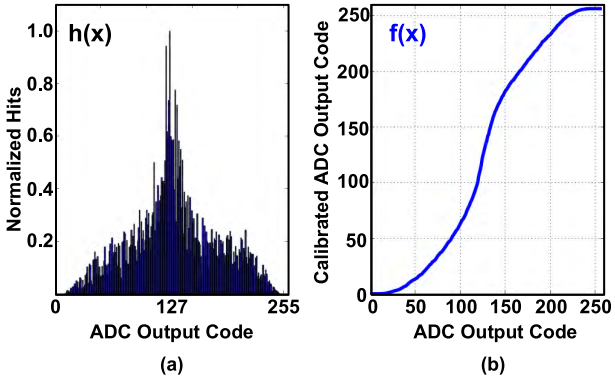


FIGURE 19. (a) Measured ADC output histogram with a triangular input signal and (b) estimated inverse transfer function.

transfer function $f(x)$ is constructed, the compensation process only performs a mapping of the raw ADC output x onto the estimated $f(x)$. The overall calibration can be conducted in the software-level waveform reconstruction process after the acquisition of the ADC output word. Hence, a complex digital logic or hard-wired control block is not required for the calibration.

Fig. 18 shows the conceptual soft calibration process with a sinusoidal input signal V_{IN}. According to the nonlinear transfer characteristic $g(v)$ of the ADC, the sinusoidal input applied to the ADC is converted to the nonlinear digital output word D_{OUT}. To compensate for the nonlinear conversion, the calibration process extracts an inverse function $f(x) = g^{-1}(x)$ of the ADC transfer characteristic through the histogram-based estimation as described in Fig. 17. Then, the inverse function $f(x)$ calibrates the raw output word D_{OUT}, and the on-chip waveform signal V_{OUT} is reconstructed based on the calibrated D_{OUT}. Fig. 19 shows the soft calibration example using the measured data. The histogram function $h(x)$ for the ADC output was constructed by applying a triangular input signal. Then, inverse transfer function $f(x)$ were established by integrating $h(x)$. At this time,

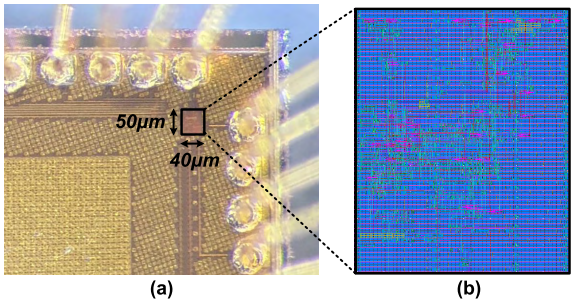


FIGURE 20. (a) Die micrograph and (b) layout of the fabricated ADC.

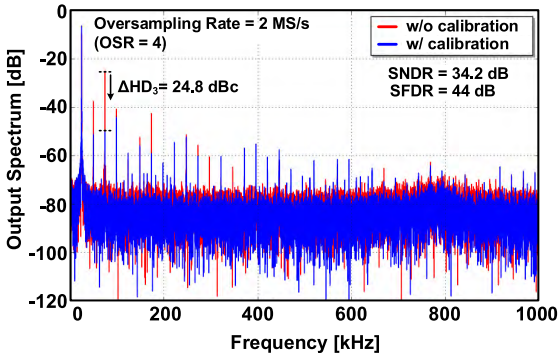


FIGURE 21. Measured output spectrum with a 24.8-kHz input signal.

the output of $f(x)$ is set to calibrated digital code considering the code-mapping process in the calibration. Because the proposed soft calibration mainly compensates for the deterministic nonlinearity caused by the VDAC, the identical $f(x)$ can be used repeatedly in the waveform reconstruction. Thus, the calibration procedure for extracting $f(x)$ is performed only once at the beginning of the system operation.

V. MEASUREMENT RESULTS

The proposed ADC was fabricated in 28-nm CMOS process. Fig. 20 shows the die micrograph of the fabricated ADC. The proposed ADC occupies an active area of 0.002 mm^2, which provides much improved area efficiency compared to the conventional synthesizable ADCs. The proposed ADC operates with a supply voltage of 0.5 V and consumes 92.2 μW. The effective sampling rate of the ADC is 500 kS/s with an oversampling ratio (OSR) of four. The ADC calibration process is embedded in a waveform reconstruction module, which is performed only once at the beginning of the measurement.

Fig. 21 shows the measured output spectrum of the fabricated ADC. When a sinusoidal input signal of 24.8 kHz was applied to the ADC, the measured SNDR and SFDR were 34.2 dB and 44 dB, respectively. Compared to the performance without the soft calibration, the third-order harmonic distortion HD_3 is reduced by 24.8 dBc, and the SNDR is improved by 19.4 dB. Fig. 22 shows the measured SNDR versus the input amplitude. With an input signal

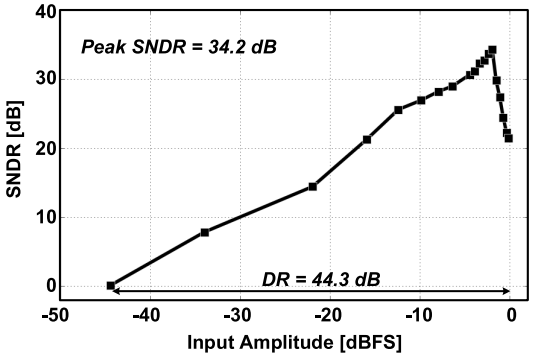


FIGURE 22. Measured SNDR versus input signal amplitude.

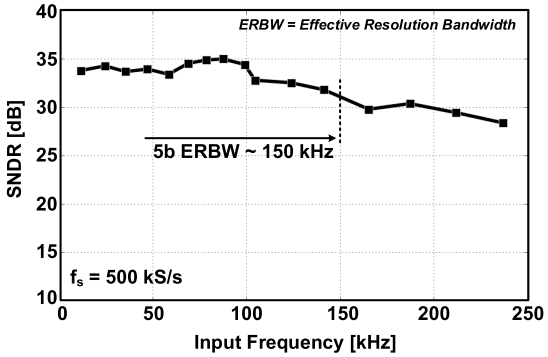


FIGURE 23. Measured SNDR versus input signal frequency.

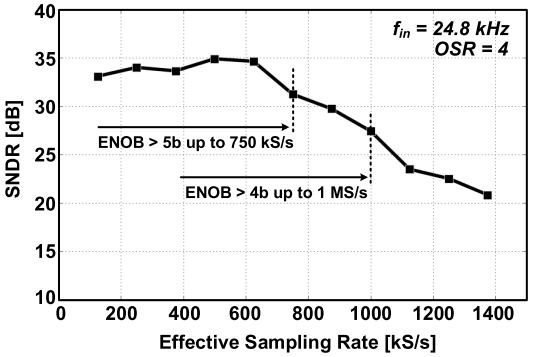


FIGURE 24. Measured SNDR versus sampling rate with an oversampling ratio (OSR) of four.

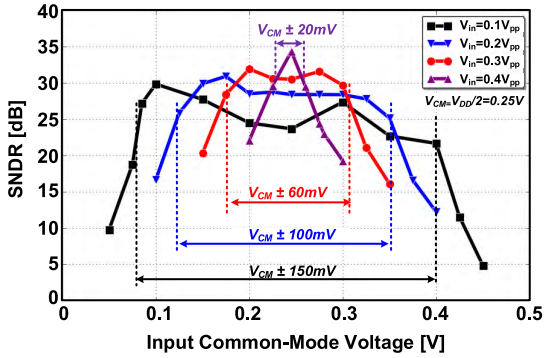


FIGURE 25. Measured SNDR versus input common-mode voltage depending on input signal swing.

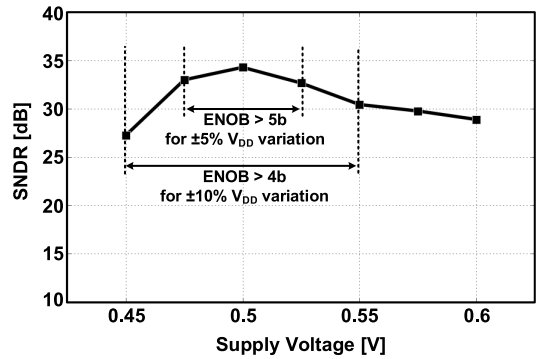


FIGURE 26. Measured SNDR versus supply voltage variation.

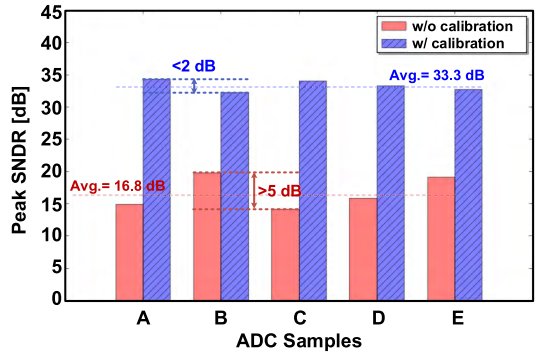


FIGURE 27. Measured SNDR deviation in five fabricated ADC samples.

frequency of 24.8 kHz, the proposed ADC achieves a peak SNDR of 34.2 dB and a dynamic range (DR) of 44.3 dB. Fig. 23 shows the measured SNDR versus the input signal frequency. The ADC maintains an effective-number-of-bit (ENOB) of 5 bit at input signal frequencies up to 150 kHz. Even if the input signal frequency is higher than 150 kHz, the ADC provides an ENOB greater than 4 bit. The measured SNDR according to the effective sampling rate are shown in Fig. 24. With an OSR of four and an input signal frequency of 24.8 kHz, the 5-bit ENOB is sustained up to 750 kS/s. Although a higher sampling frequency can reduce the maximum input voltage variation as shown in (1), the effective sampling rate is limited by the propagation delay of the synthesized hybrid comparator. For this reason, the measured SNDR decreases with a sampling rate higher than 750 kS/s.

Fig. 25 shows the measured SNDR versus the input CM voltage. The rail-to-rail operation of the VDAC and the extended input range of the hybrid comparator facilitate the wide conversion range of the ADC regardless of the input CM voltage, which enables the versatile waveform measurements. The effect of the supply voltage variation on the ADC performance is shown in Fig. 26. With an effective sampling rate of 500 kS/s and an input signal frequency of 24.8 kHz,

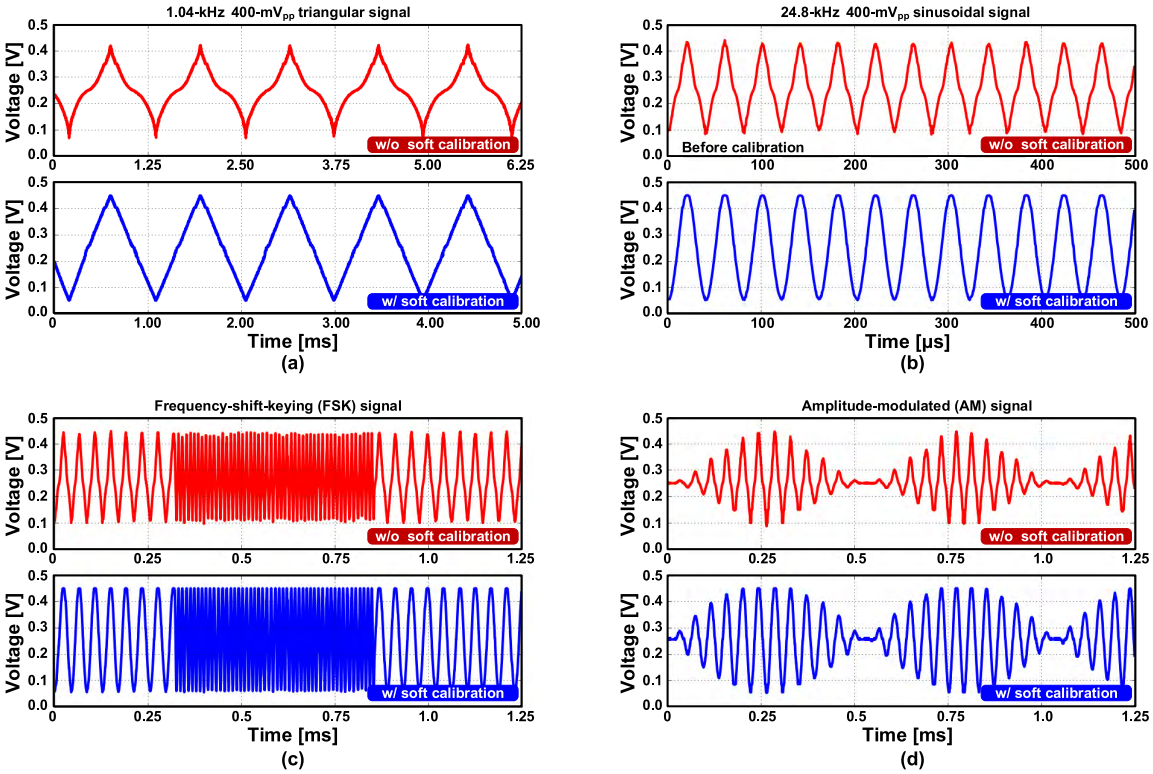


FIGURE 28. Measured waveforms using the fabricated ADC with (a) a 1.04-kHz triangular input signal, (b) a 24.8-kHz sinusoidal input signal, (c) a frequency-shift-keying (FSK) input signal, and (d) an amplitude-modulated (AM) input signal.

TABLE 1. Performance summary and comparison to prior synthesizable ADCs.

	This Work	[9]	[10]	[11]	[12]	[13]
Type	SAR	Stochastic Flash	Stochastic Flash	Stochastic Flash	Stochastic Flash	Stochastic Flash
Process	28 nm	90 nm	180 nm	90 nm	130 nm	65 nm
Active Area	0.002 mm^2	0.04 mm^2	0.43 mm^2	0.18 mm^2	0.51 mm^2	0.756 mm^2
Normalized Area*	1	1.94	5	8.5	11.5	70
Supply Voltage	0.5 V	1.2 V	0.9 V	1.2 V	0.7 V	0.9 V
SNDR	34.2 dB	24 dB	33.6 dB	35.9 dB	34.9 dB	39 dB
Sampling Rate (F_s)	500 kS/s	1500 MS/s	8 MS/s	210 MS/s	140 MS/s	100 MS/s
Power Consumption	0.092 mW	23 mW	0.631 mW	34.8 mW	17.3 mW	33 mW
Normalized Input Range**	0.8	0.04	0.16	0.12	0.57	0.24
# of Segments***	127 (DAC) + 2 (CMP)	63 (CMP)	7,680 (CMP)	2,047 (CMP)	2,040 (CMP)	8,190 (CMP)
Figure-of-Merit+	4.39	1.18	2.02	3.25	2.72	4.53
Need Analog References?	No	No	Yes	No	No	Yes
Fully Synthesizable Design?	Yes	No	No	Yes	Yes	No

* Normalized area = $\frac{\text{active area}}{0.002\ mm^2} \cdot \left(\frac{28\ nm}{\text{process}}\right)^2$.

\+ Figure-of-Merit (FoM) = $\frac{\text{Power}}{2^{\text{ENOB}} \cdot F_s}$ [pJ/Conv].

** Single-ended input range normalized to supply voltage.

*** Segments: Synthesized comparators (CMP) and DAC units.

the ADC sustains a 5-bit ENOB against a supply voltage variation of ±5%, which is sufficient robustness considering that the target SoC applications usually employ a fine-grained power management unit [20]. Even if the supply voltage is varied up to ±10%, the ADC can maintain an ENOB greater than 4 bit. Fig. 27 shows the SNDR deviation in

five fabricated ADC samples. Before the calibration process, the five ADC samples shows SNDR lower than 20 dB with a deviation larger than 5 dB. On the contrary, after the calibration process, the ADCs provide an SNDR higher than 32 dB with a reduced deviation of lower than 2 dB. Therefore, the on-chip distributed waveform monitor based on the proposed ADC can provide a uniform performance even in the presence of process variation.

The measured waveforms using the proposed ADC are shown in Fig. 28. To verify the capability of versatile waveform measurement empowered by the proposed ADC, (a) a 1.04-kHz triangular input signal, (b) a 24.8-kHz sinusoidal input signal, (c) a frequency-shift-keying (FSK) input signal, and (d) an amplitude-modulated (AM) input signal were applied to the ADC. Each input waveform was acquired by the fabricated ADC and reconstructed with the soft calibration process.

Table 1 shows the performance summary and comparison to the prior studies. This paper realizes a fully synthesizable SAR ADC differentiated from the conventional stochastic flash ADCs, providing the smallest normalized area. The ADC also provides a normalized input range of 0.8 which is the widest range among the synthesizable ADCs. In addition, the ADC operates with a low supply voltage of 0.5 V which is the lowest operational voltage. The proposed ADC achieves a peak SNDR of 34.2 dB at an effective sampling rate of 500 kS/s which is optimized for probing a low-frequency signal in the low-voltage SoC applications.

VI. CONCLUSIONS

This paper describes the design of a fully synthesizable SAR ADC for an on-chip distributed waveform monitor. To realize the synthesizable design of an SAR ADC, a synthesizable VDAC and a rail-to-rail hybrid comparator are proposed in this paper. A histogram-based soft calibration that can be embedded in a waveform reconstruction module compensates for the nonlinearity of the ADC caused by the synthesized VDAC. An oversampling technique with a redundant error correction realizes the fully synthesizable design without an S/H operation. The fabricated ADC achieved an ENOB of 5.39 bit at 500 kS/s sampling rate as well as compact area of 0.002mm^2, and a probing capability for various waveforms has also been demonstrated through the measurements. By designing all blocks in the ADC with standard digital cells, the proposed ADC enhances portability and reusability, which facilitates the integration into various functional blocks. In addition, the synthesizable design of the ADC enables the efficient migration to other processes without additional design burden.

REFERENCES

[1] K. Noguchi and M. Nagata, "An on-chip multichannel waveform monitor for diagnosis of systems-on-a-chip integration," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 15, no. 10, pp. 1101–1110, Oct. 2007.

[2] Y. Zheng and K. L. Shepard, "On-chip oscilloscopes for noninvasive time-domain measurement of waveforms in digital integrated circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 11, no. 3, pp. 336–344, Jun. 2003.

[3] Y. Araga, T. Hashida, and M. Nagata, "An on-chip waveform capturing technique pursuing minimum cost of integration," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May/Jun. 2010, pp. 3557–3560.

[4] T. Hashida and M. Nagata, "An on-chip waveform capturer and application to diagnosis of power delivery in SoC integration," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 789–796, Apr. 2011.

[5] M. Taghadosi, L. Albasha, N. A. Quadir, Y. A. Rahama, and N. Qaddoumi, "High efficiency energy harvesters in 65nm CMOS process for autonomous IoT sensor applications," *IEEE Access*, vol. 6, pp. 2397–2409, 2018.

[6] Y.-H. Hwang, Y. Song, J.-E. Park, and D.-K. Jeong, "A 0.6-to-1V 10k-to-100kHz BW 11.7b-ENOB noise-shaping SAR ADC for IoT sensor applications in 28-nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2018, pp. 247–248.

[7] J.-E. Park, Y.-H. Hwang, and D.-K. Jeong, "A 0.4-to-1 V voltage scalable $\sum\Delta$ ADC with two-step hybrid integrator for IoT sensor applications in 65-*nm* LP CMOS," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 64, no. 12, pp. 1417–1421, Dec. 2017.

[8] M.-J. Seo, Y.-J. Roh, D.-J. Chang, W. Kim, Y.-D. Kim, and S.-T. Ryu, "A reusable code-based SAR ADC design with CDAC compiler and synthesizable analog building blocks," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 65, no. 12, pp. 1904–1908, Dec. 2018.

[9] T. Sundstrom and A. Alvandpour, "Utilizing process variations for reference generation in a flash ADC," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 56, no. 5, pp. 364–368, May 2009.

[10] S. Weaver, B. Hershberg, P. Kurahashi, D. Knierim, and U. Moon, "Stochastic flash analog-to-digital conversion," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 11, pp. 2825–2833, Nov. 2010.

[11] S. Weaver, B. Hershberg, and U.-K. Moon, "Digitally synthesized stochastic flash ADC using only standard digital cells," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 1, pp. 84–91, Jan. 2014.

[12] A. Fahmy, J. Liu, T. Kim, and N. Maghari, "An all-digital scalable and reconfigurable wide-input range stochastic ADC using only standard cells," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 62, no. 8, pp. 731–735, Aug. 2015.

[13] M.-K. Jeon, W.-J. Yoo, C.-G. Kim, and C. Yoo, "A stochastic flash analog-to-digital converter linearized by reference swapping," *IEEE Access*, vol. 5, pp. 23046–23051, 2017.

[14] P. Harpe, E. Cantatore, and A. van Roermund, "11.1 An oversampled 12/14b SAR ADC with noise reduction and linearity enhancements achieving up to 79.1dB SNDR," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 194–195.

[15] W. Deng *et al.*, "A fully synthesizable all-digital PLL with interpolative phase coupled oscillator, current-output DAC, and fine-resolution digital varactor using gated edge injection technique," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 68–80, Jan. 2015.

[16] K. Seong, W.-C. Lee, B. Kim, J.-Y. Sim, and H.-J. Park, "All-synthesizable current-mode transmitter driver for USB2.0 interface," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 2, pp. 788–792, Feb. 2017.

[17] O. Aiello, P. Crovetti, and M. Alioto, "Fully synthesizable, rail-to-rail dynamic voltage comparator for operation down to 0.3 V," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2018, pp. 1–5.

[18] Y.-S. Shu, L.-T. Kuo, and T.-Y. Lo, "An oversampling SAR ADC with DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2928–2940, Dec. 2016.

[19] C.-C. Liu *et al.*, "A 10b 100MS/s 1.13mW SAR ADC with binary-scaled error compensation," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 386–387.

[20] J.-E. Park and D.-K. Jeong, "A fully integrated 700mA event-driven digital low-dropout regulator with residue-tracking loop for fine-grained power management unit," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2018, pp. 231–232.

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