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Design of Highly Linear Broadband Continuous Mode GaN MMIC Power Amplifiers for 5G

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ABSTRACT In this paper, we present a design approach for broadband harmonic-tuned monolithic microwave integrated circuit (MMIC) power amplifiers (PAs). Two harmonic matching networks are proposed for the realization of continuous class-B and class-F modes in an integrated PA. A design procedure is developed for integrated PAs using these matching networks to achieve high linearity, broadband operation, and compact chip area, in the presence of parasitic components and the physical limitations of the MMIC process. Two proof-of-concept fully integrated PAs are implemented in a 0.25-μm GaN-on-SiC process. Output power of 34.2–36.4 dBm with 40% to 49% power-added efficiency (PAE) is achieved in 4.2–7.0 GHz (51.6% fractional bandwidth), from the continuous class-B PA with only 1.5-mm^2 chip area. Furthermore, the continuous class-F PA achieves 36.2 dBm output power and 52% PAE at 5.0 GHz. The PAs are also characterized using QAM signals with wide bandwidth, in order to evaluate their performance for 5G wireless applications. For a 64-QAM signal with 100-MHz bandwidth and 8 dB peak-to-average power ratio (PAPR), the continuous class-B PA achieves 29.3 dBm average output power, 28% average PAE, and −25 dB (5.5%) error vector magnitude (EVM). The continuous class-F PA, tested using a 200 MHz 256 QAM signal with 8.5 dB PAPR, provides an average output power of 28.5 dBm, average PAE of 27%, and −28 dB (4%) EVM, without any pre-distortion.

INDEX TERMS 5G, broadband amplifier, continuous mode, GaN, harmonic tuned, monolithic microwave integrated circuit (MMIC), power amplifier (PA).

I. INTRODUCTION

The fifth generation (5G) wireless network is under development as a platform for a new era of connectivity. 5G is expected to offer higher capacity, lower latency, ubiquitous coverage, and improved energy efficiency. The small cell and massive multi-input multi-output (MIMO) base stations are employed in 5G wireless networks to further increase data capacity and improve quality of service. These size-constrained systems need high levels of integration. Furthermore, complex modulated signals, e.g., high-order QAM, of wide bandwidth are used to enable high data-rate transmission demanded by the emerging applications while maintaining the spectrum efficiency. Therefore, highly linear broadband power amplifiers (PAs) with compact chip area are essential components for such applications.

GaN technology with impressive output power capability has become popular in recent years. Initially, discrete GaN HEMTs were adopted in high-power applications, and then GaN monolithic microwave integrated circuit (MMIC) technologies opened up opportunities for system miniaturization [1]. In 5G, it is expected that GaN MMIC PAs would be extensively deployed in cellular base stations to reduce size and enhance system integration [2]. Consequently, it is essential for MMIC implementations to develop low-loss and compact circuitry in order to ensure high efficiency and broad bandwidth in the presence of parasitic components and physical limitations of the process. Furthermore, the current density limitation of metal layers and parasitic inductive coupling between adjacent structures make it challenging to develop a compact layout structure for MMIC PAs [3]–[10].

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Harmonic tuning can enhance efficiency of the PA, but it is usually performed using quarter-wavelength transmission lines or lumped-element resonance circuits that limit the bandwidth [11], [12]. The continuous-mode [13] enables broadband operation of harmonic-tuned PAs by extending the design space for the fundamental and harmonic load impedances. It can also improve the PA efficiency by properly exploiting the nonlinearity of transistor's drain-source capacitance [14], [15].

Linearity of the PA becomes more critical when dealing with high-order modulated signals which are prone to both amplitude and phase distortions. GaN HEMT devices suffer from *soft gain compression*, which degrades the PA linearity. Furthermore, wide modulation bandwidths used in 5G impose more stringent linearity requirements on the PA [16]–[18]. Conventional linearization techniques based on digital pre-distortion (DPD) and post-processing face implementation challenges for wideband modulated signals, e.g., hardware complexity and power consumption are increased. Furthermore, in massive MIMO arrays, the output power per PA is significantly reduced which leaves a small power budget for the DPD hardware, while different nonlinear behavior of the PAs prevents from effectively adopting the DPD for linearization. Therefore, it is desirable to design highly linear and efficient PAs directly at the circuit level.

In this paper, we present a systematic approach for designing highly efficient broadband harmonic-tuned MMIC PAs. New harmonic matching networks are proposed for continuous-mode class-B and class-F PAs. Detailed theoretical analysis and design procedures are disclosed along with a linearity improvement approach used for mitigating AM-AM and AM-PM distortions of the PAs. Experimental results show that the proposed PAs can simultaneously achieve high efficiency and high linearity when excited by wideband high-order modulation signals of 5G applications. The rest of the paper is organized as follows. In Section II, two harmonic matching networks are proposed for realization of the continuous class-B and class-F modes in an integrated PA. In Section III, a design procedure is developed for integrated PAs using these matching networks to achieve high efficiency, broadband operation, and compact chip area. Moreover, considering nonlinearity of the transistor's transconductance and gate-source capacitance, a design approach is used to mitigate the AM-AM and AM-PM distortions of the PA. Two GaN MMIC PAs are designed using the proposed harmonic matching networks. Measurement results are given in Section IV, where high-order QAM signals with wide bandwidth are used to evaluate linearity of the PAs for 5G wireless applications. This is followed by concluding remarks in Section V.

II. BROADBAND HARMONIC MATCHING NETWORKS

A. CONSIDERATIONS FOR MMIC IMPLEMENTATION

The broadband harmonic matching is usually achieved by using high-order networks in *discrete-component* circuit implementations. However, simple networks with low loss and compact chip area are essential for MMIC PAs. For some conventional PA classes, e.g., class-E and class-F, there are popular harmonic matching network structures [12], [19], [20], while for continuous modes such networks are still under development. Here, we present two networks for the realization of the continuous class-B and continuous class-F modes in MMIC PAs.

The continuous class-B mode is defined by the following optimum load impedance at the fundamental and second-harmonic frequencies

$$Z_L(f) = (1 + j\gamma)R_{opt} \tag{1}$$

$$Z_L(2f) = -j\frac{3\pi}{8}\gamma R_{opt}, \tag{2}$$

while the optimum load impedance at higher-order harmonics is a short circuit. R_{opt} denotes the optimum load resistance of the transistor and $-1 \leq \gamma \leq 1$ [13]. On the other hand, in the continuous class-F mode, the optimum load impedances are given by [14]

$$Z_L(f) = \left(\frac{2}{\sqrt{3}} + j\gamma\right) R_{opt} \tag{3}$$

$$Z_L(2f) = -j\frac{7\sqrt{3}\pi}{24}\gamma R_{opt} \tag{4}$$

$$Z_L(3f) = \infty. \tag{5}$$

Theoretical efficiency of the PA in these modes is given by $\pi/4 \approx 78.5\%$ and $\pi/2\sqrt{3} \approx 90.7\%$, respectively. These operation modes provide extended design spaces for harmonic load impedances and facilitate the realization of broadband harmonic-tuned PAs.

The realization of continuous modes in broadband MMIC PAs entails dealing with several issues.

1) The required purely reactive second-harmonic impedance condition cannot be achieved over a broad bandwidth. In discrete circuits, this condition is satisfied using high-order matching networks, which usually is impractical in integrated circuits because of the chip area, parasitics and insertion loss limitations.
2) The third-harmonic open-circuit impedance for the continuous class-F mode cannot be achieved due to limited quality factor of integrated passive components.
3) The optimum load reactance in the second-harmonic frequency band should maintain a constant ratio with respect to the reactance in the fundamental frequency band, i.e., $X_L(2f)/X_L(f) \approx -1.18$ in the continuous class-B and ≈ -1.59 in the continuous class-F, a requirement that is difficult to maintain over a broad bandwidth.
4) In order to maximize the PA efficiency, it could be rather beneficial to use a harmonic matching network with a low insertion loss in the fundamental frequency band, rather than trying to achieve the near perfect optimum load impedances. Therefore, the three conditions discussed above are not really essential to achieve high efficiency over a broad bandwidth.

5) The on-chip inductors and transmission lines should be designed with a compact footprint, a requirement that usually degrades their quality factor and increases their parasitic components. This leads to trade-off between bandwidth/efficiency and chip area of the PA.

These issues should be considered in choosing the circuit structure of the harmonic matching network and its physical implementation. In the following, we investigate the two circuits proposed for the continuous class-B and continuous class-F operation.

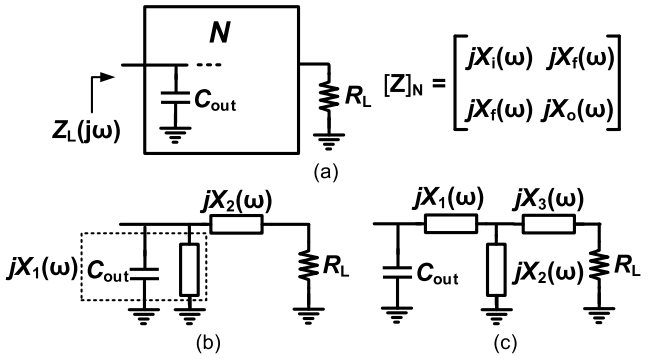

FIGURE 1. (a) General matching network design problem for harmonic-tuned PAs. (b) *L* network. (c) *T* network.

B. GENERAL PROBLEM OF MATCHING NETWORK DESIGN

The general problem of matching network design for harmonic-tuned PAs can be considered as shown in Fig. 1(a). A passive reactive network including the output-referred parasitic capacitance C_{out} of the transistor is used to transform the load resistance into the optimum load impedance $Z_L = R_{opt}$ of the transistor in the fundamental ($\omega_L \leq \omega \leq \omega_H$) and harmonic frequency bands. The impedance transformation ratio, $ITR = R_{opt}/R_L$, the input quality factor, $Q_i = \omega_0 R_{opt} C_{out}$, and the fractional bandwidth, $(\omega_H - \omega_L)/\omega_0$, are the main parameters of this matching network design problem. Here, ω_0 denotes center of the frequency band $\omega_0 = \sqrt{\omega_L \omega_H}$. Moreover, the parameter $-1 \leq \gamma \leq 1$ is an extra degree of freedom that extends the design space for optimum impedances. The network can be synthesized using circuit simulators, but such approach cannot provide insights into the circuit operation and usually does not lead to low-loss compact-size circuits that are essential for MMIC implementation.

We derive the conditions that this two-port network should meet in terms of its impedance parameters. Assuming that the network is lossless and reciprocal, its impedance parameters can be described as

$$[Z]_N = \begin{bmatrix} jX_i(\omega) & jX_f(\omega) \\ jX_f(\omega) & jX_o(\omega) \end{bmatrix}. \quad (6)$$

It can be shown that the impedance presented to the transistor is derived as

$$Z_L(j\omega) = \left(\frac{X_f^2}{X_o^2 + R_L^2}\right) R_L + j\left(X_i - \frac{X_f^2 X_o}{X_o^2 + R_L^2}\right). \quad (7)$$

The real part of the load impedance in the fundamental frequency band has the most significant effect on the output power. Therefore, the primary condition that should be satisfied, e.g., for the continuous class-B operation, can be written as follows

$$H_1(\omega) \equiv \left(\frac{X_f^2(\omega)}{X_o^2(\omega) + R_L^2} \frac{R_L}{R_{opt}}\right) \rightarrow 1, \ \omega_L \leq \omega \leq \omega_H. \quad (8)$$

This transfer function should be small in the second-harmonic frequency band, i.e., $H_1(\omega) \rightarrow 0$, $2\omega_L \leq \omega \leq 2\omega_H$. These conditions can be controlled by two parameters $X_f(\omega)$ and $X_o(\omega)$. A more practical condition for the second-harmonic band can be considered as $Re[Z_L(j\omega)] \ll Im[Z_L(j\omega)]$, which can be written as

$$H_2(\omega) \equiv \left(\frac{X_f^2(\omega)[X_o(\omega) + R_L]}{X_i(\omega)[X_o^2(\omega) + R_L^2]}\right) \ll 1, \ 2\omega_L \leq \omega \leq 2\omega_H. \quad (9)$$

This condition can be satisfied by making $X_i(\omega)$ or $X_o(\omega)$ large or ensuring a small $X_f(\omega)$ in the second-harmonic band, using appropriate resonance circuits. It should be noted that at sufficiently high frequencies, the input impedance of the two-port network is dominated by the output parasitic capacitance, i.e., $Z_L(j\omega) \approx 1/j\omega C_{out}$, hence the condition (9) can be met independently.

Moreover, the imaginary part of the load impedance should satisfy the conditions given by (1) and (2). In practice, the condition in the fundamental frequency band is achieved by keeping the load impedance inside the constant $Q \leq 1$ area of the Smith chart. In the second-harmonic band, the imaginary part should be within the high-efficiency area of Smith chart, which can be derived using harmonic load-pull simulations, and usually covers a large area of the Smith chart, e.g., lower half circle.

For the continuous class-F mode, an open-circuit impedance at the third-harmonic frequency is required. From (7), it can be achieved if $X_i(3\omega_0) \rightarrow \infty$ and or $X_f(3\omega_0) \rightarrow \infty$. Therefore, the network structure should have some resonant circuits at $3\omega_0$ which appear in the impedance parameters $X_i(\omega)$ and or $X_f(\omega)$.

Two representative circuit structures that can be considered as the matching network are shown in Fig. 1(b) and Fig. 1(c). We investigate these circuits for the realization of the continuous class-B and continuous class-F modes, respectively.[1]

C. PROPOSED NETWORK FOR CONTINUOUS CLASS-B OPERATION

For the *L* network of Fig. 1(b), the impedance parameters are given by $X_i = X_f = X_1$ and $X_o = X_1 + X_2$. It is assumed that $R_{opt} > R_L$, which is usually the case for GaN transistors.[2] Using the conditions (1) and (7) while assuming

[1] These circuits can be extended to multi-section networks in order to achieve wider bandwidth. In such cases, analyses that will be presented in the following can be applied to each section

[2] For large transistors where $R_{opt} < R_L$, the *L* network should be modified to have a reactance in parallel with the load impedance.

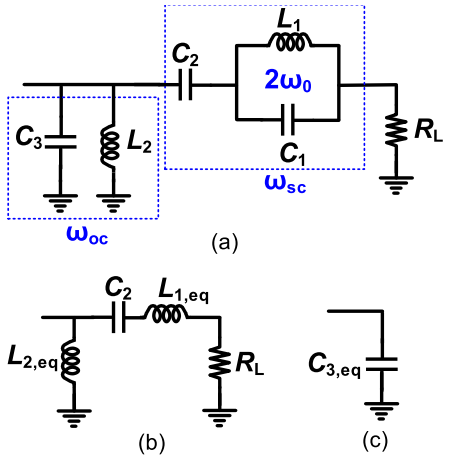

FIGURE 2. (a) Harmonic matching network proposed for the continuous class-B operation. Equivalent circuit at (b) fundamental and (c) second-harmonic frequencies.

$\gamma = 0$ at the center of fundamental frequency band, the two reactances $X_1(\omega_0)$ and $X_2(\omega_0)$ can be determined. Moreover, the condition (9) can be satisfied if $X_2(2\omega_0) \to \infty$. It should be noted that these results, derived at the center of the band, can only be used as guidelines for initial circuit design.

We propose the circuit shown in Fig. 2(a) for the continuous class-B operation. This network has some interesting features that make it attractive for the MMIC implementation. This is based on a modified minimum inductor bandpass filter structure [21], [22], that requires the minimum inductance compared to the conventional bandpass filters. Moreover, this network can provide sharper transition from the passband to stop-band that helps to realize a reactive impedance in the second-harmonic frequency band. The capacitor C_3 includes the transistor's drain-source parasitic capacitance, while the inductor L_2 acts as the drain bias feed.

The resonant frequencies of the LC networks are chosen such that the circuit can provide required load impedances at the fundamental and second-harmonic frequencies. The second-harmonic signal is further suppressed by the network $L_1||C_1$ which operates as an open-circuit at $2\omega_0$ ($X_2 \to \infty$). The frequency response of the load impedance can be controlled by the open-circuit frequency of $L_2||C_3$, $\omega_{oc} = 1/\sqrt{L_2C_3}$, and the short-circuit frequency of the series branch, $\omega_{sc} = 1/\sqrt{L_1(C_1 + C_2)}$. In the following, we explore the circuit behavior at fundamental and second-harmonic frequencies.

At the fundamental frequency, the parallel shunt branch can either operate as an inductor or capacitor depending on its resonance frequency ω_{oc}. We choose $\omega_0 < \omega_{oc} < 2\omega_0$, to achieve an inductive reactance at the fundamental and a capacitive reactance at the second-harmonic. It can be shown that the equivalent inductance of this network at ω_0 is $L_{2,eq} = L_2/[1-(\omega_0/\omega_{oc})^2]$. Moreover, the network $L_1||C_1$ acts as an equivalent inductance of $L_{1,eq} = (4/3)L_1$. Therefore, equivalent circuit of the network is derived as the circuit shown in Fig. 2(b). This can provide a resistive-inductive impedance for an initial value of $\gamma > 0$ [see (1)]. The circuit elements can be chosen to achieve an impedance with constant real part over the bandwidth, while the imaginary part changes from an inductive to a capacitive reactance as γ varies from a positive toward a negative value.

At the second-harmonic frequency, the resonator $L_1||C_1$ acts as an open-circuit and this leads to a reactive load impedance. The parallel branch operates as an equivalent capacitance of $C_{3,eq} = [1-(\omega_{oc}/2\omega_0)^2]C_3$ at $2\omega_0$ [Fig. 2(c)]. This can provide the capacitive load impedance for an initial value of $\gamma > 0$ [see (2)].

D. PROPOSED NETWORK FOR CONTINUOUS CLASS-F OPERATION

For the T network of Fig. 1(c), the impedance parameters are derived as

$$X_i = \frac{X_1 + X_2}{1 - \omega C_{out}(X_1 + X_2)} \tag{10}$$

$$X_f = \frac{X_2}{1 - \omega C_{out}(X_1 + X_2)} \tag{11}$$

$$X_o = X_3 + \frac{X_2(1 - \omega C_{out}X_1)}{1 - \omega C_{out}(X_1 + X_2)}. \tag{12}$$

In the second-harmonic frequency band, there are three options to meet the condition (9); $X_f = 0$ which leads to $X_2 = 0$, $X_i \to \infty$ resulting in $1 - \omega C_{out}(X_1 + X_2) = 0$, or $X_o \to \infty$ which requires $X_3 \to \infty$. Moreover, the open-circuit requirement at the third-harmonic frequency can be achieved if $1 - \omega C_{out}(X_1 + X_2) = 0$.

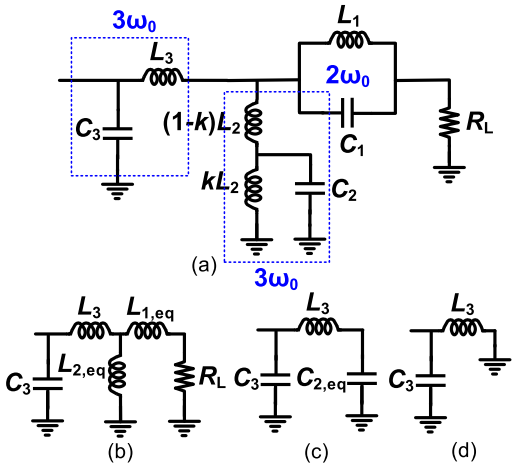

FIGURE 3. (a) Harmonic matching network proposed for the continuous class-F operation. Equivalent circuit at (b) fundamental, (c) second-harmonic, and (d) third-harmonic frequencies.

Using these insights, we propose the circuit shown in Fig. 3(a) to realize the continuous class-F mode. In this circuit, the capacitor C_3 includes the transistor's drain-source parasitic capacitance, while the inductor L_2 acts as the drain bias feed. The resonant frequencies are chosen such that the circuit can provide the required load impedances at the fundamental and harmonic frequencies. Moreover, the network

$L_1||C_1$ prevents the second-harmonic signal from reaching the output ($X_3 \rightarrow \infty$). The parallel branch composed of C_2 and the two parts of L_2 has a short-circuit impedance at $\omega_{sc} = 1/\sqrt{k(1-k)L_2C_2}$ and an open-circuit impedance at $\omega_{oc} = 1/\sqrt{kL_2C_2}$. The short-circuit frequency is adjusted at the third-harmonic frequency, i.e., $\omega_{sc} = 3\omega_0$, and as a result, the third-harmonic signal is suppressed at the output. The open-circuit frequency can be used to control behavior of the impedance at the fundamental and second-harmonic frequencies. It can be shown that the parallel branch appears as an inductor for $\omega < \omega_{oc}$ and as a capacitor for $\omega > \omega_{oc}$. We choose $\omega_0 < \omega_{oc} < 2\omega_0$ to achieve an inductive reactance at fundamental and a capacitive reactance at the second-harmonic. Using the conditions set on ω_{sc} and ω_{oc}, it can be shown that the parameter k should be chosen within the range $5/9 < k < 8/9$. In the following, we investigate the circuit operation at the fundamental and harmonic frequencies.

In the fundamental frequency, $L_1||C_1$ acts as an equivalent inductance of $L_{1,eq} = (4/3)L_1$, while the parallel branch appears as an inductance $L_{2,eq}$. Therefore, the network is simplified as the circuit shown in Fig. 3(b). The inductive T network can transform the load resistance to an impedance with the real part of the fundamental load impedance, $(2/\sqrt{3})R_{opt}$, and can provide an inductance to transform the capacitor C_3 reactance to the imaginary part of the optimum load impedance, γR_{opt}.

In the second-harmonic frequency, $L_1||C_1$ appears as an open-circuit and leads to a reactive load impedance. The parallel branch operates as an equivalent capacitance of $C_{2,eq}$. The equivalent circuit shown in Fig. 3(c), can provide the reactive second-harmonic load impedance given by (4).

In the third-harmonic frequency, the parallel branch appears as a short-circuit. Therefore, the equivalent circuit shown in Fig. 3(d) would be $L_3||C_3$ which acts as an open-circuit at $3\omega_0$ to meet the condition (5).

It should be noted that in the proposed design approach for the circuits of Fig. 2 and Fig. 3, the resonant frequencies are chosen to obtain a simplified description for the circuit operation. In practice, the resonant frequencies can be allowed to deviate in some extent from these theoretical values to enable a broadband operation. Moreover, there are some effects neglected in the theory, such as harmonic generation by nonlinear drain-source and gate-source capacitances of the transistor [15] as well as the gate-drain capacitance feedback effects. Therefore, the harmonic matching network should be further optimized using a nonlinear transistor model to include such effects.

III. PA CIRCUIT DESIGN

A. TRANSISTOR SIZE AND BIAS SELECTION

The PAs are designed using a 0.25-μm GaN-on-SiC technology from WIN Semiconductors. The drain bias voltage is set at the process maximum voltage of 28 V. The transistor size is selected based on the desired output power level. Using load-pull simulations and the process design kit (PDK), a transistor size of 8×125 μm is chosen that can provide about 36 dBm output power at 5.0 GHz.

The soft gain compression behavior of GaN HEMT appears especially detrimental for QAM signals as every symbol experiences dislocation, while a conventional gain compression only affects high-power symbols close to the constellation corners. This raises the error vector magnitude (EVM) of the output signal resulting from aggregated errors in all the symbols. Among several mechanisms that contribute to nonlinearity of the PA, nonlinearity of the transconductance $g_m(V_{gs})$ and gate-source capacitance $C_{gs}(V_{gs})$ usually dominate the AM-AM and AM-PM distortions, respectively [23]. As shown in Fig. 4, using proper quiescent bias current, these nonlinearities can significantly be reduced to improve the EVM for QAM signals. Since EVM is dependent on both AM-AM and AM-PM distortions, the optimum quiescent bias current is somewhere between the current levels for minimum nonlinearity of transconductance and gates-source capacitance. The simulation results indicate that a quiescent bias current around 15–30 mA can be considered as the optimum for linear operation.

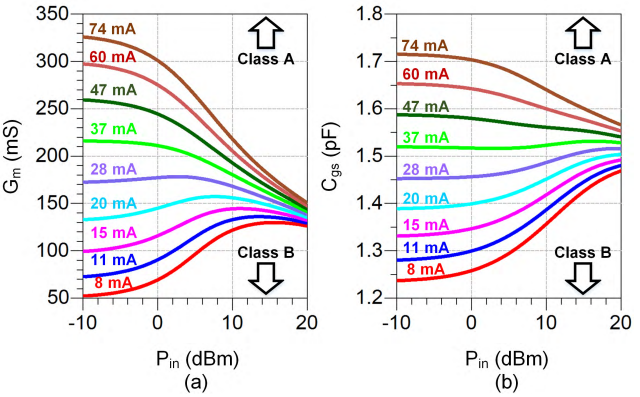

FIGURE 4. Average (a) transconductance and (b) gate-source capacitance of the GaN HEMT versus input power for different quiescent bias currents.

As the transistor is biased at class-AB, its drain current waveform deviates from the half-wave sinusoid. Therefore, theories of continuous class-B and class-F should be modified. It can be shown that the optimum load resistance for the conduction angle of α is derived as

$$R_{opt}(\alpha) = \frac{1-\cos(\alpha/2)}{\alpha - \sin(\alpha)}\pi R_{opt}, \tag{13}$$

where R_{opt} is the optimum load resistance in the class-B [13]. In the class-AB, $\pi < \alpha < 2\pi$, and $R_{opt}(\alpha)$ varies within $0.93R_{opt}$ to R_{opt}. Therefore, the optimum fundamental load impedance is practically independent of the quiescent bias current. The efficiency at peak power is mainly determined by the optimum load resistance and supply voltage, and thus is insensitive to the gate bias voltage. However, the back-off efficiency which is even more important for signals with high peak-to-average power ratio (PAPR), slightly degrades by increasing the bias current. The optimum

second- and third-harmonic load impedances are also modified by the conduction angle, but these have a minor effect on the efficiency.

B. CONTINUOUS CLASS-B PA

A 4–7 GHz continuous class-B PA is designed using the developed approach. For the selected transistor, the optimum load resistance and drain-source parasitic capacitance are derived as 70 Ω and 0.5 pF, respectively. The output matching network is designed using the circuit of Fig. 2. The circuit components of the synthesized network are approximately given by $L_{1,2} \approx$ [1.7 1.4] nH and $C_{1,2,3} \approx$ [0.50 0.15 0.59] pF. Thus, $f_{oc} \approx 5.5$ GHz and $f_{sc} \approx 4.9$ GHz, which are close to $f_0 \approx 5.3$ GHz, while the resonant frequency of $L_1||C_1$ is close to $2f_0 \approx 10.6$ GHz. Then the circuit is tuned and optimized to compensate for parasitic and coupling effects in the layout. The design of a compact layout for the output matching network is challenging as several criteria including optimum load impedances, insertion loss, electromigration current limit, and bandwidth should be considered. In this design, the inductors are realized as the meandered microstrip transmission line using stacked two metal layers.

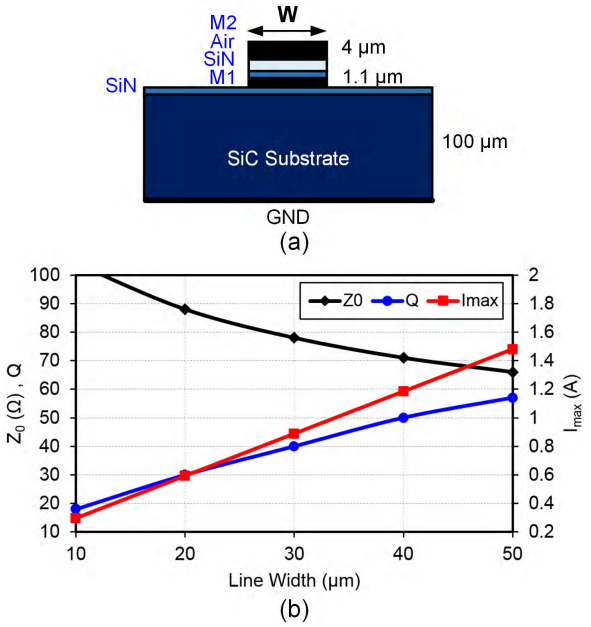

FIGURE 5. (a) Physical structure of the transmission lines in the GaN process. (b) Characteristic impedance, quality factor (at 5 GHz), and electromigration current limit of the transmission lines versus their width. The transmission lines are constructed as the microstrip structure with stacked double-metal over a 100-μm SiC substrate.

The characteristic impedance, quality factor (at 5 GHz), and electromigration current limit of the transmission lines versus their width are shown in Fig. 5. In the circuit of Fig. 2, L_2 should pass the drain bias current with $I_{dc,max} \approx 300$ mA, thus its metal width should be chosen wider than 10 μm to meet the current density limit. Using wider lines, higher quality factors can be achieved, but this increases parasitic capacitances and the chip area. Since the inductors are implemented as meandered lines, their parasitic components can limit bandwidth of the PA. Especially, the drain bias feed has significant effects on the bandwidth of broadband amplifiers [24], [25]. Therefore, extensive EM simulations are performed to minimize such effects. A line width of 25 μm is selected based on the insertion loss, current density limit, and chip area. The quality factor of the inductors implemented as meandered transmission lines is estimated as 25 at 5 GHz. The capacitors are implemented using the MIM structure with the capacitance density of 215 pF/mm^2. The load impedance presented by the designed harmonic matching network to intrinsic drain of the transistor and its insertion loss are shown in Fig. 6. The continuous class-B operation is nearly fully achieved with the parameter γ varying from 0.58 to −0.59. The insertion loss is maintained lower than 1 dB over 4.2–7.0 GHz, with a minimum of 0.44 dB achieved at center of the band, 5.3 GHz.

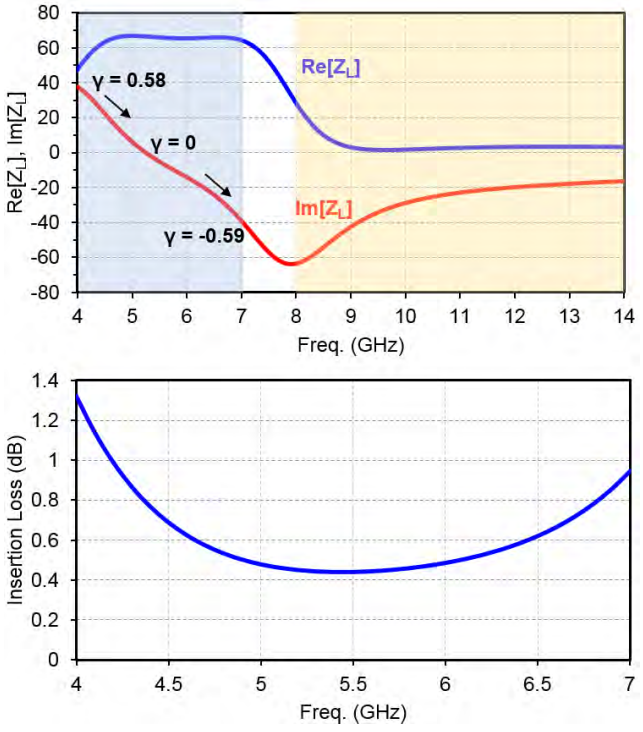

FIGURE 6. Load impedance (at the intrinsic drain node) and insertion loss of the output matching network in the continuous class-B PA. The fundamental and second harmonic frequency bands are highlighted.

Next, an input matching network is designed to transform the source resistance into the optimum source impedance of transistor over the bandwidth. The PA circuit schematic is shown in Fig. 7. The resistors are included in the input matching network to ensure low-frequency stability of the transistor.

The PA, driven with input power of 24 dBm, delivers 34.8–36.4 dBm output power, 43–54% drain efficiency (DE), and 40–50% PAE over 4.0–7.0 GHz. These results are achieved with a fixed input power, which is not optimum for all frequencies. It should be noted that higher efficiency can

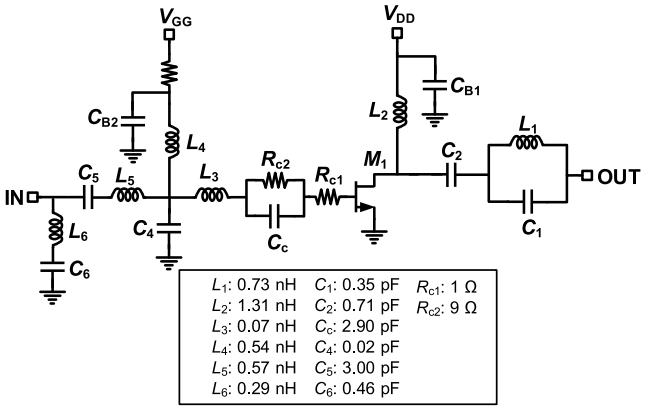

FIGURE 7. Circuit schematic of the continuous class-B PA.

be achieved if the PA is designed for a narrower bandwidth, because (1) the output matching network would have lower insertion loss, and (2) the load impedance can be maintained closer to the optimum points in the fundamental and second-harmonic frequency bands.

C. CONTINUOUS CLASS-F PA

A 4–6 GHz continuous class-F PA is designed using the proposed technique. The transistor is biased at 26 mA quiescent current (see Fig. 4) and 28 V supply voltage. The output matching network is designed using the circuit of Fig. 3. The same design considerations mentioned before are applied to this network. The inductors L_2 and L_3 pass the drain bias current and their width should be chosen to meet the current density limit. The main components of the output matching network are estimated as $L_{1,2,3} = [0.47\ 1.30\ 0.26]$ nH, $C_{1,2,3} = [0.54\ 0.30\ 0.50]$ pF, and $k = 0.72$. The resonant frequencies of $L_1||C_1$, $L_3||C_3$, open- and short-circuit frequencies of the parallel branch are derived as 2.0, 2.8, 1.9, and 3.6 times the center frequency of 5 GHz, respectively. These are close to the theoretical values and ranges selected in the design phase. A line width of 20 μm is chosen for L_1 and L_3, while L_2 is implemented using slightly wider line of 25 μm. The quality factors of the inductors are estimated as $Q_{1,2,3} = [19\ 23\ 15]$, at 5 GHz. The load impedance presented by the designed harmonic matching network and its insertion loss are shown in Fig. 8. The continuous class-F operation is nearly fully achieved with the parameter γ varying from 0.43 to -0.48. As discussed in Section II-A, an open-circuit impedance is not necessary over all the third-harmonic bandwidth to achieve high efficiency. The insertion loss reads 0.5–1.1 dB over the target bandwidth 4.0–6.0 GHz.

The input matching network is designed using a slightly different approach compared to the previous PA to further improve the linearity. It is designed to provide impedance matching and have a low quality factor in order to mitigate conversion of the transistor's input capacitance nonlinearity into AM-PM distortion [18], [26]. The designed input matching network exhibits an input impedance of $52.1+j2.3\ \Omega$ ($S_{11} \approx -30$ dB) at 5.0 GHz, which has a very low

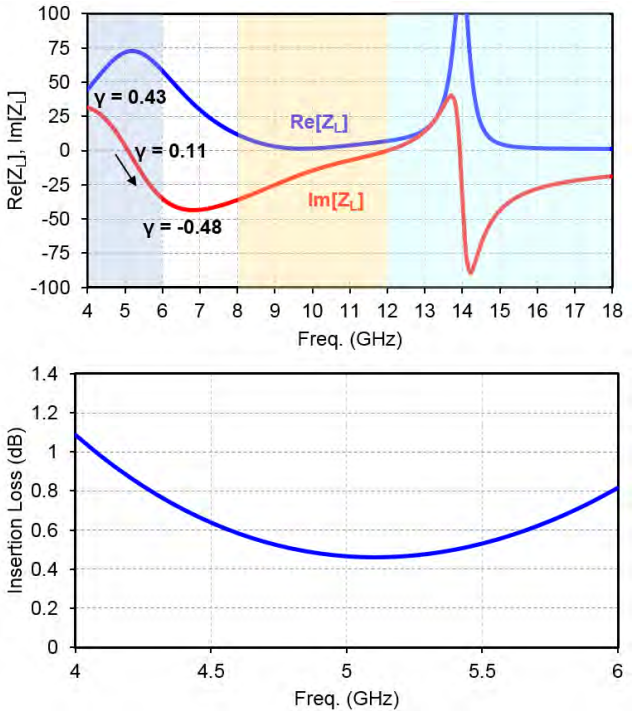

FIGURE 8. Load impedance (at the intrinsic drain node) and insertion loss of the output matching network in the continuous class-F PA. The fundamental and harmonic frequency bands are highlighted.

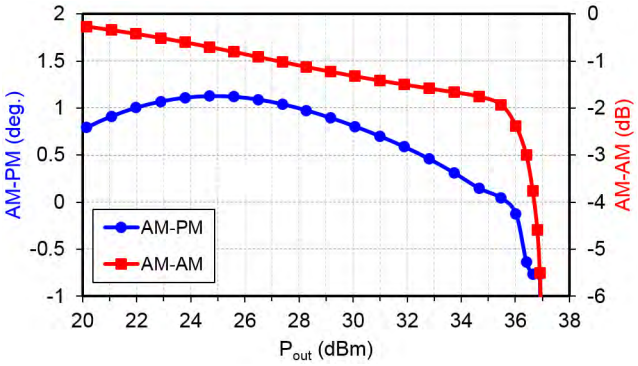

FIGURE 9. Simulated AM-AM and AM-PM distortions of the continuous class-F PA at 5.0 GHz.

quality factor. The quality factor remains lower than 0.3 over 500 MHz bandwidth around 5.0 GHz, which helps to achieve a good linearity for wideband QAM signals.

The PA circuit schematic is shown in Fig. 10. The PA is fully integrated on chip, including output and input matching networks, dc block capacitors, bias feed inductors, and decoupling capacitors. The PA simulation results indicate 36.4 dBm output power, 60% DE, 57% PAE, and 13.4 dB gain at 5.0 GHz. Simulated AM-AM and AM-PM distortions versus output power are shown in Fig. 9. The AM-PM is $-0.6°$ at 3-dB gain compression and remains lower than 1.1° within a 20-dB output power range.

IV. MEASUREMENT RESULTS

The PA chips, shown in Fig. 11, are implemented in a 0.25-μm GaN-on-SiC process from WIN Semiconductors.

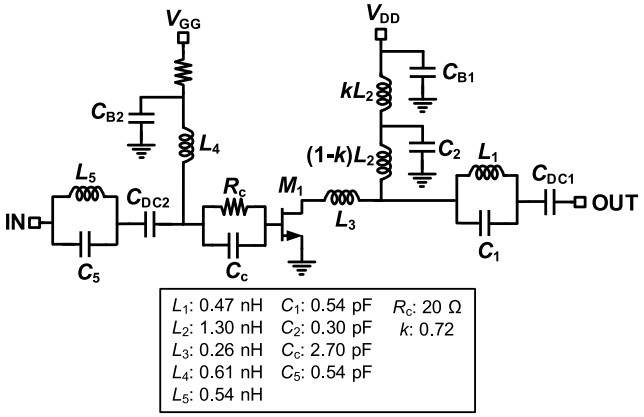

FIGURE 10. Circuit schematic of the continuous class-F PA.

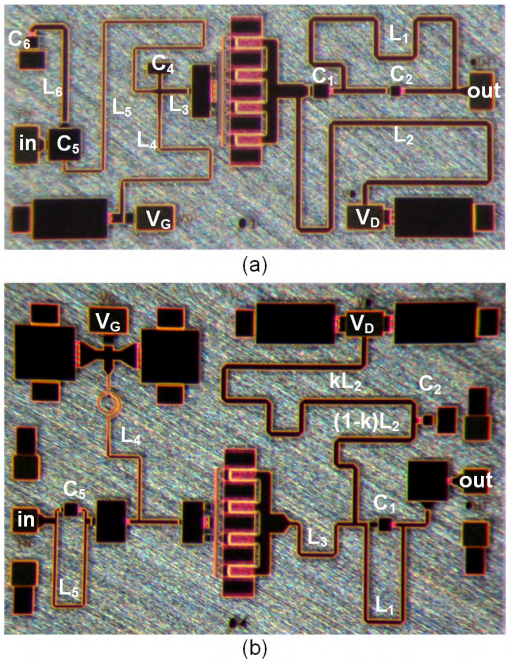

FIGURE 11. Chip micrograph of (a) continuous class-B PA (1.8 mm × 0.85 mm) and (b) continuous class-F PA (1.8 mm × 1.2 mm).

The HEMT devices feature maximum drain bias voltage of 28 V and breakdown voltage of 120 V. Their unity current gain frequency f_T and the maximum frequency of oscillation f_{max} are 25 and 75 GHz, respectively. The process offers two metal layers, TaN thin film and GaN epi resistors, MIM capacitors, and through backside vias for grounding. For measurements, the PA chip is attached to test PCB using a conductive epoxy and is wire-bonded to bias and RF traces on the board.

A. CONTINUOUS CLASS-B PA

The PA chip shown in Fig. 11(a) occupies 1.53 mm^2. The PA is biased at $V_{GS} = -2.4$ V and $V_{DS} = 28$ V, consuming 16 mA bias current from the supply.

1) CW MEASUREMENTS

In Fig. 12, output power, DE, PAE, and gain are shown versus frequency, at input power of 24 dBm. It is noticed

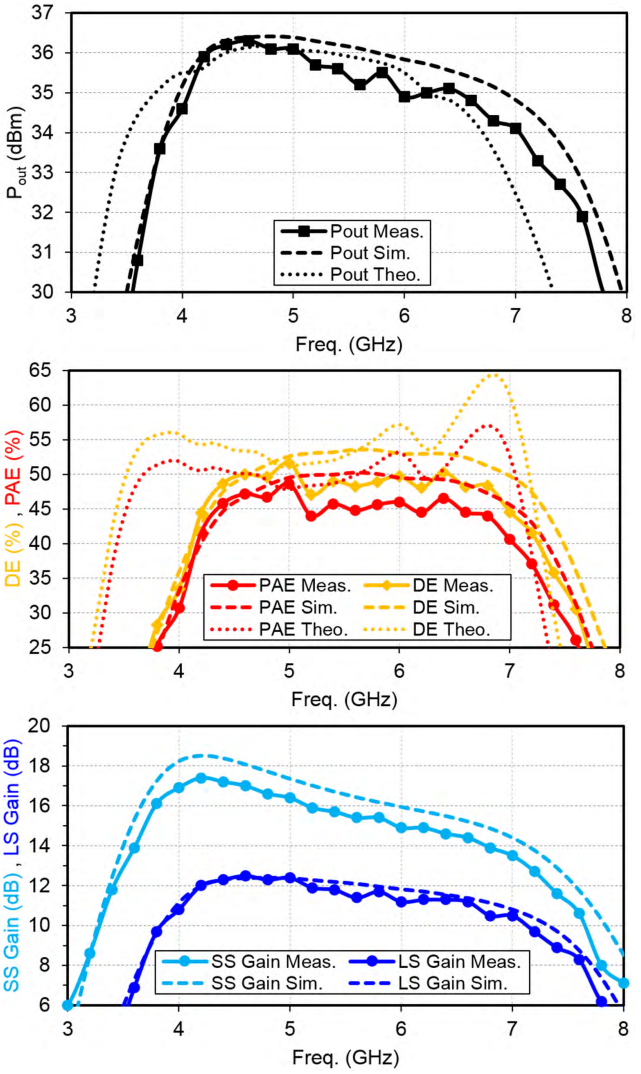

FIGURE 12. Output power, DE, PAE, and gain (small-signal and large-signal) versus frequency at input power of 24 dBm (continuous class-B PA).

that the expected bandwidth is almost fully covered. The PA achieves 34.1–36.3 dBm output power, 40–49% PAE, and 10.5–12.4 dB power gain in 4.2–7.0 GHz bandwidth. The ripples in the output power and efficiency versus frequency are mainly caused by frequency dependent responses of the matching networks and variations of the loss in the measurement setup, e.g., cables, connectors, and attenuator. The input power should be increased in higher frequencies where power gain is lower, to improve output power and efficiency. The maximum deviation from simulations occurs at 6.0 GHz, where the output power and PAE are respectively dropped by 1.1 dB and 11%. Theoretical results for output power and DE/PAE are also included for comparison. These results are obtained using the developed theories as initial design point using ideal circuit elements and further optimized to achieve a broadband response.

In Fig. 13, power gain, DE, and PAE, at 5.0 GHz, are shown versus output power. The gain is almost constant at low

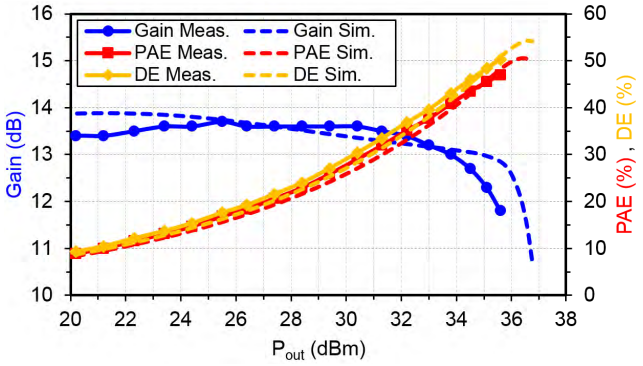

FIGURE 13. Power gain, DE, and PAE versus output power at 5.0 GHz (continuous class-B PA).

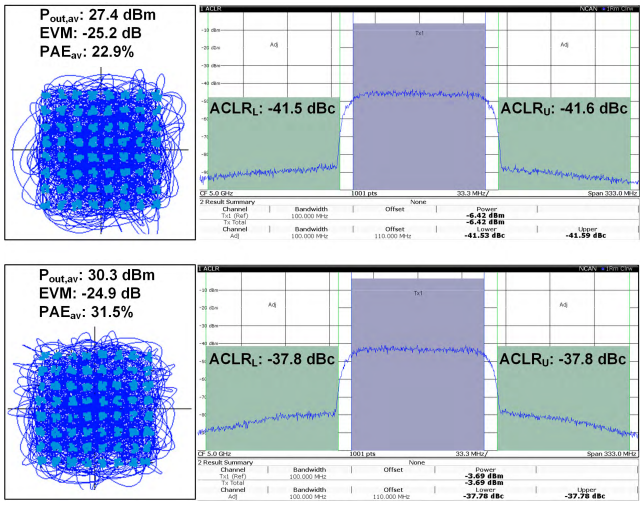

FIGURE 14. Measured output constellation and spectrum at two output power levels for a 100-MHz 64-QAM signal with 8 dB PAPR at 5.0 GHz (continuous class-B PA).

power levels, indicating that the soft gain compression, specific to GaN devices, has been well mitigated using the proper quiescent bias current. The output power of 35.6 dBm and DE/PAE of 50/47% are achieved at 1-dB gain compression.

2) MODULATED-SIGNAL MEASUREMENTS

The modulation measurements are performed using R&S SMW200A vector signal generator and R&S FSW43 vector signal analyzer. The root raised cosine (RRC) filtering is applied on the modulated signals to limit their spectral bandwidth.

In Fig. 14, measured output constellation and spectrum are shown for a single-carrier 100-MHz 64-QAM signal with 8 dB PAPR at 5.0 GHz. The results are shown at two output power levels to demonstrate their effects on efficiency and linearity. At 27.4 dBm average output power, an average PAE of 22.9% is achieved, with EVM and ACLR of −25.2 dB and −41.5 dBc, respectively. By increasing the output power to 30.3 dBm, the average PAE is improved to 31.5%, while the linearity metrics are degraded to −24.9 dB EVM and −37.8 dBc ACLR.

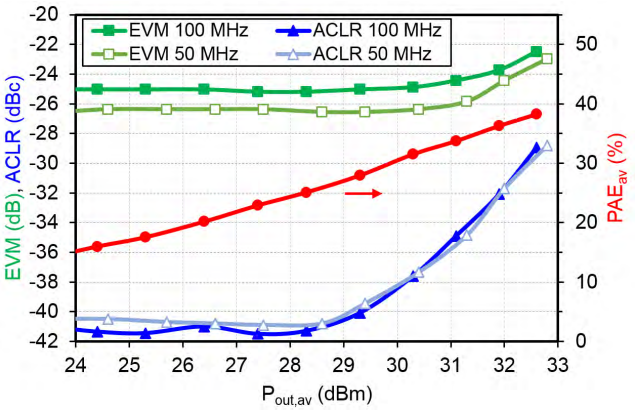

FIGURE 15. Measured EVM, ACLR, and average PAE versus the average output power. The results are shown for a 50/100-MHz 64-QAM signal with 7.9/8 dB PAPR at 5.0 GHz (continuous class-B PA).

In Fig. 15, EVM, ACLR, and average PAE are shown versus the average output power. The average of ACLR at the lower and upper channels is reported here. The results are shown at two modulation bandwidths of 50 and 100 MHz. The average PAE is the same in both cases. The EVM and ACLR start to increase with the output power from $P_{out,av} \approx 28$ dBm, which considering the 8 dB PAPR is around the onset of gain compression. To achieve EVM < -25 dB at 100-MHz modulation bandwidth, the PA can provide 29.3 dBm average output power, 28% average PAE, and −40 dBc ACLR. For 50-MHz modulation bandwidth, higher output power and PAE of 31.5 dBm and 37% can be achieved, but ACLR increases to −34 dBc.

B. CONTINUOUS CLASS-F PA

The PA chip shown in Fig. 11(b) occupies 2.16 mm^2. The PA is biased at $V_{GS} = -2.35$ V and $V_{DS} = 28$ V, consuming 26 mA bias current from the supply.

1) CW MEASUREMENTS

In Fig. 16, the output power, DE, PAE, and gain versus frequency are shown at input power of 23 dBm. The output power 1-dB bandwidth is 4.4–6.0 GHz. In Fig. 17, the power gain, DE, and PAE versus output power are shown at 5.0 GHz. The maximum DE/PAE of 55/52% is achieved with output power of 36.2 dBm at 2-dB gain compression. The gain behavior versus output power confirms proper bias condition to mitigate the AM-AM distortion of the PA. The difference between measured and simulated results is relatively small. It is noted that the efficiency of the continuous class-F PA is not much higher than that of the continuous class-B PA as theoretically expected. This can be attributed to the long charging and discharging times of the large device used, which leads to deviation from the optimum class-F operation. Moreover, the class-F PA is less driven into compression which also affects the efficiency. Nevertheless, the class-F PA exhibits higher gain and linearity.

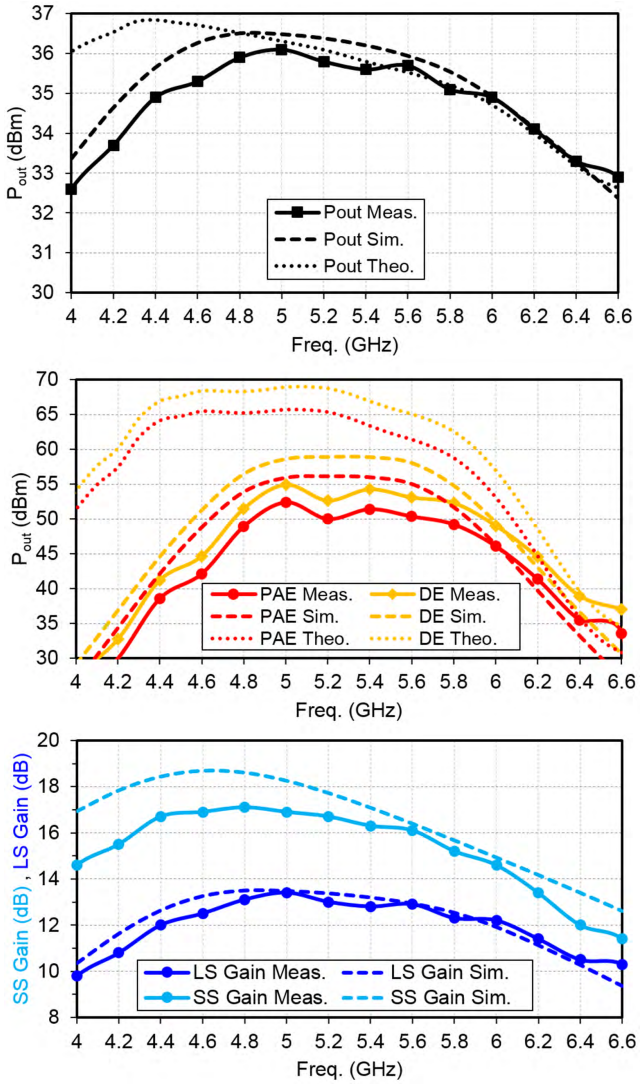

FIGURE 16. Output power, DE, PAE, and gain (small-signal and large-signal) versus frequency at 23 dBm input power (continuous class-F PA).

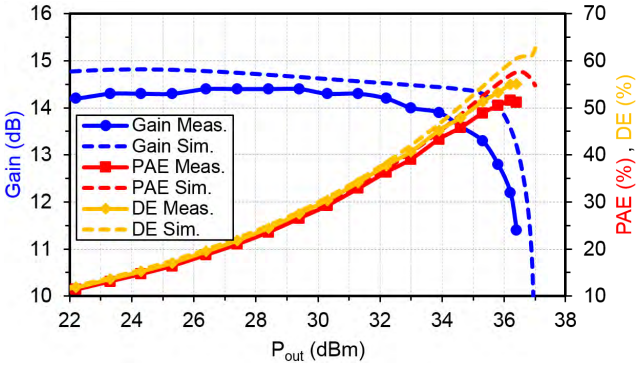

FIGURE 17. Power gain, DE, and PAE versus output power at 5.0 GHz (continuous class-F PA).

2) MODULATED-SIGNAL MEASUREMENTS

The PA performance is evaluated using single-carrier 64-QAM and 256-QAM signals with 8.2 dB and 8.5 dB PAPR, respectively. The effect of quiescent bias current on the EVM is checked to investigate the proposed linear design approach. As shown in Fig. 18, the minimum EVM is achieved at 23 mA current, which is close to the 26 mA chosen in the design. It is noticed that the EVM could be significantly degraded, e.g., by 5–8 dB, if the transistor was biased in the class-B with zero quiescent bias current.

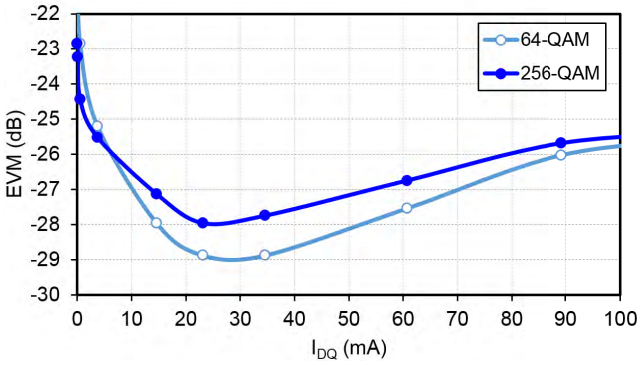

FIGURE 18. Measured EVM versus the quiescent bias current for 200-MHz 64-QAM and 256-QAM signals at 5.0 GHz (continuous class-F PA). The average output power is maintained fixed at 28 dBm.

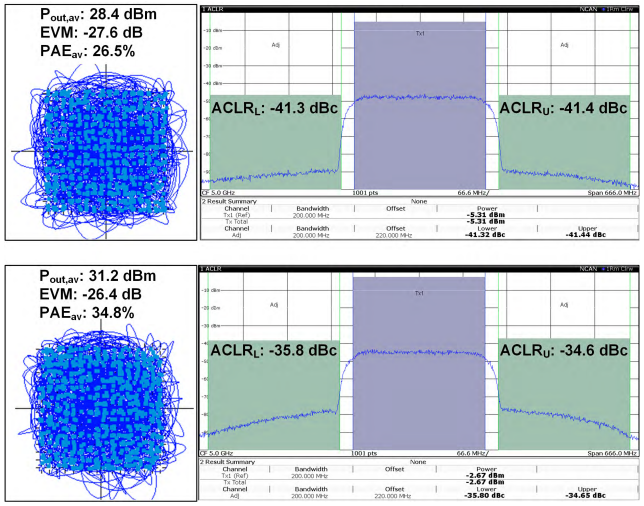

FIGURE 19. Measured output constellation and spectrum at two output power levels for a 200-MHz 256-QAM signal with 8.5 dB PAPR at 5.0 GHz (continuous class-F PA).

The measured output signal constellation and spectrum for 200-MHz 256-QAM at two output power levels are shown in Fig. 19. At average output power of 28.4 dBm, the EVM of −27.6 dB can be achieved with average PAE of 26.5%. The PAE can be improved to 34.8% by increasing the output power by 2.8 dB, with the EVM slightly degraded to −26.4 dB. Furthermore, the ACLR increases by about 6–7 dB, while mismatch between the lower and upper channels increases from 0.1 dB to 1.2 dB. The required EVM depends on the modulation scheme and bit error rate (BER). Theoretically, assuming that the error power spectral density is given by the additive white Gaussian noise (AWGN) and equally distributed among all constellation points, for a 256-QAM signal the signal-to-noise ratio (SNR) should be 19 dB to maintain an average BER of 10^{-3} [27].

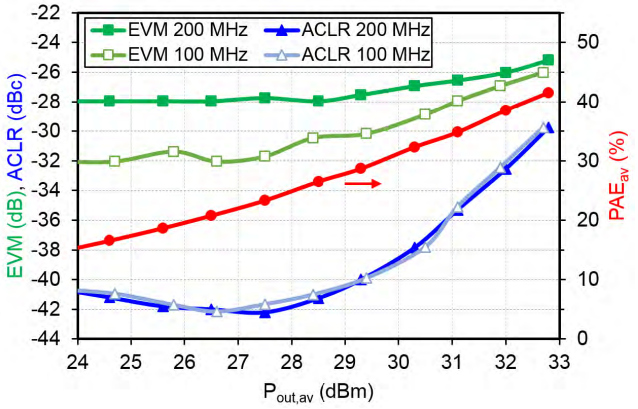

FIGURE 20. Measured EVM, ACLR, and average PAE versus the average output power (continuous class-F PA). The results are shown for a 256-QAM signal with 100/200 MHz modulation bandwidth and 8.2/8.5 dB PAPR at 5.0 GHz.

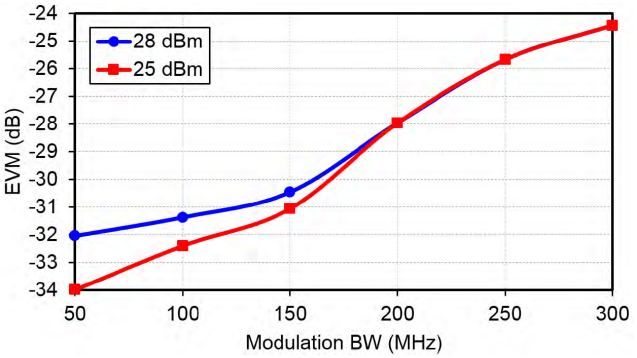

FIGURE 21. Measured EVM versus the modulation bandwidth for 256-QAM signal at 5.0 GHz (continuous class-F PA). The average output power is maintained fixed at 25/28 dBm.

Using SNR $\approx$ 1/EVM^2, this translates to the EVM requirement of -19 dB. In practice, other factors cause unequal distribution of the error power, e.g., larger AM-AM and AM-PM of the PA at higher power points in the constellation (Fig. 19). Therefore, the required EVM should be specified by a standard considering the application scenario.

In Fig. 20, the EVM, ACLR, and average PAE are shown versus average output power. The EVM is highest for the 200-MHz modulation bandwidth, but the difference diminishes at the high output power levels. An EVM of -28 dB can be achieved with 28.5 dBm average output power and 27% average PAE at 200-MHz modulation bandwidth; these values are improved to 31.1 dBm and 35% at 100-MHz modulation bandwidth.

In Fig. 21, the EVM is shown versus modulation bandwidth. The EVM slightly degrades when the modulation bandwidth increases from 50 MHz to 150 MHz. Beyond this range, the EVM raises more sharply with the modulation bandwidth. When the modulation bandwidth is narrow, e.g., 50 MHz, the EVM is higher at 28 dBm average output power because of gain compression. However, at wide modulation bandwidth, e.g., $>$ 150 MHz, the difference between EVM values become negligible, indicating that EVM is dominated by dynamic nonlinear effects.

C. COMPARISON AND DISCUSSION

In Table 1, performance of the PAs is compared with high-efficiency GaN MMIC PAs. It should be noted that most of the GaN MMIC PAs reported in the literature are targeted for applications where the linearity is not a primary concern. Here, we have included some recent publications with wideband modulated-signals measurements. Furthermore, the efficiency of PAs presented in this paper are measured at only 1–2 dB gain compression to maintain linearity, hence are lower than the efficiency at saturation. A wide modulation bandwidth in the range of 100–200 MHz (and beyond) is used here to evaluate performance of the PAs for 5G applications.

The continuous class-B PA achieves high efficiency over a broad bandwidth (51.6% fractional bandwidth),

TABLE 1. Comparison of high-efficiency GaN MMIC PAs.

	This Work I	This Work II	[7]	[8]	[9]	[10]
Freq. (GHz)	4.2–7.0	4.6–6.0	4.9–5.9	6.4–8.3	6.8–7.2	4.9–5.9
P_{out} (dBm)	34.2–36.4	34.7–36.2	37–37.7	36–36.6	37.7–38.0	34.6–36.1
DE (%)	44–52	45–54	50–58	40–50	62–67	62–79
PAE (%)	40–49	42–52	48–55	36–47	58–64	49–61
Gain (dB)	10.6–12.4	12.2–13.4	28.5–31.7	10–12	12.2–13.5	8–12
Modulation	64-QAM	256-QAM	256-QAM	256-QAM	256-QAM	256-QAM
Mod. BW (MHz)	100	100/200	80	7	60	80
PAPR (dB)	8	8.2/8.5	11.25	7.4	7	—
Carrier Freq. (GHz)	5.0	5.0	5.7	7.0	7.0	5.2
EVM (dB)	-25	-28	-32	—	—	-32
$P_{out,av}$ (dBm)	29.3	31.1/28.5	30.6	28.7	32	28
PAE_{av} (%)	28	35/27	27	26	30	30
Chip Area (mm^2)	1.53	2.16	4.7	7.8	9.0	2.42
GaN Process	0.25 μm	0.25 μm	0.25 μm	0.25 μm	0.25 μm	0.25 μm

while featuring the most compact chip area. It exhibits a competitive average PAE of 28% for a 100-MHz 64-QAM signal with 8 dB PAPR. The continuous class-F PA also exhibits high efficiency and compact chip area. Using the proposed approaches to achieve high linearity, i.e., input matching network with low quality factor to mitigate AM-PM distortion and optimum quiescent bias current determined based on the EVM measurements, the PA can accommodate a 200-MHz 256-QAM signal with −28 dB EVM and 27% average PAE.

V. CONCLUSION

A design approach is developed here for broadband monolithic microwave integrated circuit (MMIC) power amplifiers (PAs). Two output matching network circuits are proposed for realization of the continuous class-B and continuous class-F modes in integrated PAs. Furthermore, to achieve high linearity, a biasing approach is adopted based on nonlinearity of the transistor's transconductance and gate-source capacitance. Using the developed techniques, two MMIC PAs are designed and implemented in a GaN-on-SiC process. The fabricated PAs achieve high efficiency, broad bandwidth, and compact chip area. Their performance evaluated using QAM signals with wide modulation bandwidth, 100–200 MHz, indicate promising results for sub-6 GHz 5G wireless communications.

REFERENCES

[1] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A review of GaN on SiC high electron-mobility power transistors and MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1764–1783, Jun. 2012.

[2] D. Schnaufer and B. Peterson, "GaN: A critical technology for 5G," Qorvo, Greensboro, NC, USA, White Paper, Dec. 2016. [Online]. Available: http://www.qorvo.com/resources/d/qorvogallium-nitiride-gan-a-critical-technology-for-5g-white-paper

[3] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, and N. Rorsman, "A wideband and compact GaN MMIC Doherty amplifier for microwave link applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 922–930, Feb. 2013.

[4] S. Rezaei, L. Belostotski, F. M. Ghannouchi, and P. Aflaki, "Integrated design of a class-J power amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1639–1648, Apr. 2013.

[5] G. Nikandish and A. Medi, "A design procedure for high-efficiency and compact-size 5–10-W MMIC power amplifiers in GaAs pHEMT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 2922–2933, Aug. 2013.

[6] Y. Xu *et al.*, "A scalable large-signal multiharmonic model of AlGaN/GaN HEMTs and its application in C-band high power amplifier MMIC," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 8, pp. 2836–2846, Aug. 2017.

[7] B. Liu, M. Mao, C. C. Boo, P. Choi, D. Khanna, and E. A. Fitzgerald, "A fully integrated class-J GaN MMIC power amplifier for 5-GHz WLAN 802.11ax application," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 5, pp. 434–436, May 2018.

[8] R. Quaglia, V. Camarchia, M. Pirola, J. J. M. Rubio, and G. Ghione, "Linear GaN MMIC combined power amplifiers for 7-GHz microwave backhaul," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 11, pp. 2700–2710, Nov. 2014.

[9] R. Giofrè, P. Colantonio, and F. Giannini, "A design approach to maximize the efficiency vs. linearity trade-off in fixed and modulated load GaN power amplifiers," *IEEE Access*, vol. 6, pp. 9247–9255, Feb. 2018.

[10] B. Liu, M. Mao, D. Khanna, P. Choi, C. C. Boon, and E. A. Fitzgerald, "A highly efficient fully integrated GaN power amplifier for 5-GHz WLAN 802.11ac application," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 5, pp. 437–439, May 2018.

[11] F. Giannini and L. Scucchia, "A complete class of harmonic matching networks: Synthesis and application," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 3, pp. 612–619, Mar. 2009.

[12] G. Nikandish, E. Babakrpur, and A. Medi, "A harmonic termination technique for single- and multi-band high-efficiency class-F MMIC power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 5, pp. 1212–1220, May 2014.

[13] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Boston, MA, USA: Artech House, 2006.

[14] N. Tuffy, L. Guan, A. Zhu, and T. J. Brazil, "A simplified broadband design methodology for linearized high-efficiency continuous class-F power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1952–1963, Jun. 2012.

[15] J. Moon, J. Kim, and B. Kim, "Investigation of a class-J power amplifier with a nonlinear C_{out} for optimized operation," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 11, pp. 2800–2811, Nov. 2010.

[16] H. T. Dabag, B. Hanafi, O. D. Gürbüz, G. M. Rebeiz, J. F. Buckwalter, and P. M. Asbeck, "Transmission of signals with complex constellations using millimeter-wave spatially power-combined CMOS power amplifiers and digital predistortion," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 7, pp. 2364–2374, Jul. 2015.

[17] M. Vigilante and P. Reynaert, "A wideband class-AB power amplifier with 29–57-GHz AM–PM compensation in 0.9-V 28-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1288–1301, May 2018.

[18] S. Shakib, H.-C. Park, J. Dunworth, V. Aparin, and K. Entesari, "A highly efficient and linear power amplifier for 28-GHz 5G phased array radios in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3020–3036, Dec. 2016.

[19] S. Gao, "High efficiency class-F RF/microwave power amplifiers," *IEEE Microw. Mag.*, vol. 7, no. 1, pp. 40–48, Feb. 2006.

[20] Z. Popovic and J. A. Garcia, "Microwave class-E power amplifiers: A brief review of essential concepts in high-frequency class-E PAs and related circuits," *IEEE Microw. Mag.*, vol. 19, no. 5, pp. 54–66, Jul. 2018.

[21] H. Watanabe, "On the circuit with a minimum number of coils," *IRE Trans. Circuit Theory*, vol. CT-7, no. 1, pp. 77–78, Mar. 1960.

[22] A. Taslimi and K. Mouthaan, "Design of optimized minimum inductor bandpass filters," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 2, pp. 484–495, Feb. 2017.

[23] L. Cotimos Nunes, P. M. Cabral, and J. C. Pedro, "AM/AM and AM/PM distortion generation mechanisms in Si LDMOS and GaN HEMT based RF power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 799–809, Apr. 2014.

[24] C. Campbell *et al.*, "A wideband power amplifier MMIC utilizing GaN on SiC HEMT technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2640–2647, Oct. 2009.

[25] G. Nikandish and A. Medi, "Unilateralization of MMIC distributed amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3041–3052, Dec. 2014.

[26] S. Golara, S. Moloudi, and A. A. Abidi, "Processes of AM-PM distortion in large-signal single-FET amplifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 245–260, Feb. 2017.

[27] K. Cho and D. Yoon, "On the general BER expression of one- and two-dimensional amplitude modulations," *IEEE Trans. Commun.*, vol. 50, no. 7, pp. 1074–1080, Jul. 2002.

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