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Generalized Circuit Topology of Qn-Hybrid-NPC Multilevel Converter With Novel Decomposed Sensor-Less Modulation Method

MOSTAFA ABARZADEH[1,2], (Member, IEEE), AND KAMAL AL-HADDAD[1], (Fellow, IEEE)
[1]Department of Electrical Engineering, École de technologie supérieure (ÉTS), University of Quebec, Montreal, QC H3C 1K3, Canada
[2]Electrical Engineering Faculty, Sahand University of Technology, Tabriz, Iran

Corresponding author: Mostafa Abarzadeh (m_abarzadeh@ieee.org)

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ABSTRACT In this paper, a novel generalized circuit topology of the n-time quadrupled-hybrid-neutral-point-clamped (Qn-HNPC) converter and a new decomposed sensor-less modulation method are proposed to multiply the number of output voltage levels of the 5L-HNPC converter with a less number of components. The Qn-HNPC converter is realized by applying *n* number of the proposed voltage-level multiplier modules (VLMMs) to the 5L-HNPC converter. Hence, the number of output voltage levels is n-time quadrupled in the attained Qn-HNPC converter, whereas a less number of components, as well as, low cost and size, are added to the main 5L-HNPC converter. Moreover, a novel generalized decomposed sensor-less modulation method is introduced to decompose the main 5L-HNPC and the proposed VLMMs reference signals in the attained Qn-HNPC converter. Consequently, only four low-voltage and low-power switches operate at switching frequency, whereas the remaining devices commutate at the low or fundamental frequency. Furthermore, employing the proposed modulation method in the attained Qn-HNPC converter causes self-balancing of all the capacitors voltage, doubling the first switching harmonic cluster frequency of the output voltage, as well as a remarkable decrease in the control complexity, the stored energy, and the size of the VLMMs capacitor. The presented simulation and experimental results verify the performance and viability of the proposed Qn-HNPC converter topology, as well as, the suggested decomposed modulation method.

INDEX TERMS Capacitor voltage self-balancing, components reduction, decomposed modulation method, multilevel inverter, n-time quadrupled-hybrid-neutral-point-clamped (Qn-HNPC) converter, neutral-point-clamped (NPC) converter, voltage level multiplier module (VLMM).

I. INTRODUCTION

Increasing trends toward applying multilevel converters (MLC) to renewable energy conversion systems and other industrial applications necessitate improvement of the MLCs configurations and modulation methods. MLCs have emerged as promising state-of-the art technology for the high-power and high-voltage power electronic converters. Generating multilevel staircase output voltage results in switching frequency reduction, decreased loss, lower dv/dt and harmonic contents, as well as amended electromagnetic interference (EMI) of the MLCs. Major types of the MLCs are classified as the neutral-point-clamped (NPC), the cascaded H-bridge (CHB), the flying capacitor (FC), and the modular multilevel (MM) converters [1]–[9].

A proper operation of power electronic converters as well as industrial drives is required to meet the harmonic limit mandated by the stringent standards. Hence, the higher number of output voltage levels is demanded in MLCs to fulfill the relevant stringent standards. However, excessive number of components such as dc-link capacitors and clamping diodes in the NPC converters, isolated dc power supplies in the CHB converters, and flying capacitors in the FC converters are required by increasing the number of output voltage levels. Furthermore, control and modulation methods of the traditional MLCs are more arduous at the higher number of output voltage levels [6]–[10].

Recently, the hybrid multilevel inverters have been proposed as promising solutions for overcoming these

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drawbacks [5]–[17]. A static ground power unit (SGPU) based on the 25-level hybrid Active-NPC (ANPC) converter, which consists of the 5L-ANPC converter and the suggested submodule has been proposed in [8]. However, it requires three isolated power supplies to provide 25-level output voltage. In [14], a 13-level three-phase hybrid multilevel converter (HMC) based on the combination of the FC and CHB converters has been introduced. In the suggested HMC, the blocking voltage of the semiconductors of augmented CHB is equal to the nominal voltage of the converter. Hence, this is not applicable for the high voltage MLCs. In [15], a 9-level hybrid cascaded multilevel inverter (HCMLI) which consists of the presented improved four-level submodule and full-bridge converter has been proposed. Even though the HCMLI provides 9-level output voltage, it requires four isolated power supplies. 9-level and 11-level hybrid ANPC converters comprising the 5L-ANPC converter and the low-voltage and low-power h-bridge have been proposed in [10] and [16], respectively for SGPU applications. In [18], optimized topologies for the symmetrical and asymmetrical cascaded multilevel converters have been presented. The proposed optimized modules are cascaded to provide higher number of voltage levels. However, the suggested topologies comprise at least four isolated power supplies and it only can be used in single-phase configuration. In [19], A three-stage 18-level three-phase hybrid inverter circuit which comprises three hybrid high, medium, and low voltage inverter stages with trinary ratio in dc-link voltages as well as its switching method has been proposed. Very high-resolution stacked multilevel inverter topologies for adjustable speed drives have been proposed in [20]–[22]. Three 17-level inverters, which has been developed by cascading a FC inverter with three capacitor fed H-bridges have been stacked to form the 49-level MLC. However, it needs to three isolated power supplies and numerous semiconductors and capacitors for generating the 49 voltage levels as well as sophisticated and complicated capacitors voltage controllers. In [23] and [24], a 27-level and 23-level asymmetrical MLC have been proposed using three h-bridge stages with trinary ratio in the dc-link voltages, respectively. They require three isolated power supplies, which have been provided by the high-frequency dc-link. Generally, the binary or trinary ratios for the dc-link capacitors or isolated power supplies are used for asymmetric cascaded h-bridge and hybrid converters. By using the ratio of asymmetry more than trinary, the MLC cannot generate some levels of the output voltage [25], [26]. Accordingly, the proposed hybrid configurations in the literature require numerous isolated dc-power supplies with various voltages or numerous bulky and costly capacitors by increasing the number of output voltage levels. Hence, it leads to increase cost, size, and complexity of the control and modulation method as well as decrease the modularity of the mentioned converters.

Hence, this paper proposes a novel generalized circuit topology of Qn-HNPC converter and its new decomposed sensor-less modulation method to remarkable increase the number of output voltage levels. The Qn-HNPC converter is formed by augmenting n number of the proposed VLMM submodules at the output of the 5L-HNPC. converter. The proposed VLMM sub-modules generate additional minor voltage levels between the major voltage levels of the 5L-HNPC converter, which results in quadrupling the number of output voltage levels by augmenting each VLMM at the output of the 5L-HNPC. In addition, the proposed VLMM operates at low voltage and low power. The quaternary ratio ($1 : \frac{1}{4} : \frac{1}{16} : \ldots$) of the dc-link power supplies is used in the proposed Qn-HNPC converter. Moreover, the maximum power distribution ratio (PDR) of the first VLMM dc-power supply is only 8 % of the total required power of converter. Accordingly, the output voltage quality of the attained Qn-HNPC converter is remarkably improved by multiplication of the output voltage levels whereas the low extra cost and size are imposed on the main 5L-HNPC converter and the number of components such as power supplies, semiconductors, and capacitors is significantly decreased. Furthermore, employing the suggested modulation method leads to decomposing the main 5L-HNPC converter and the proposed VLMMs reference signals, as well as remarkable improvement of the output voltage frequency spectrum. Hence, the size, cost, and complexity of the attained Qn-HNPC converter are significantly reduced and less-component converter is achieved. Moreover, the proposed decomposed modulation method causes self-balancing of all the capacitors voltage in Qn-HNPC converter, and remarkable decrease in size and stored energy of the capacitors in the proposed VLMMs.

This paper is organized as follows. In section II, the circuit topology of the proposed 21L quadrupled-HNPC (Q-HNPC) converter and its suggested sensor-less decomposed modulation method are presented. In section III, comparison of the proposed 21L Q-HNPC converter with the other MLC topologies is described. Section IV presents the generalized circuit topology of the proposed Qn-HNPC converter and generalized sensor-less decomposed modulation method. The 41L three-phase Q-HNPC converter is introduced in section V. In sections VI and VII, simulation and experimental results are performed. Finally, the conclusion is presented in section VIII.

II. CIRCUIT TOPOLOGY OF THE PROPOSED 21L Q-HNPC CONVERTER AND THE SUGGESTED SENSOR-LESS DECOMPOSED MODULATION METHOD

A. THE PROPOSED VLMM

The suggested VLMM is a low voltage and low power submodule to generate minor voltage levels between the main 5L-HNPC voltage levels. The proposed VLMM comprises two low frequency and four high frequency switches, one capacitor and one isolated dc source. Moreover, a new sensor-less modulation method is suggested for the VLMM to guarantee the capacitor voltage self-balancing, and decrease the capacitor size by factor of f_{SW}/f_1 where f_{SW} is switching

frequency and f_1 is fundamental frequency. Hence, the cost, size and start-up charging time of the VLMM is notably decreased, also the VLMM power density is remarkably increased by employing the proposed sensor-less modulation method.

B. ONE-STAGE MULTIPLICATION OF THE OUTPUT VOLTAGE LEVEL NUMBER: THE 21L Q-HNPC CONVERTER

The proposed 21L Q-HNPC converter is formed by augmenting one low voltage and low power VLMM submodule at the output of the 5L-HNPC converter. The proposed 21L Q-HNPC configuration is depicted in Figure 1. As shown in Figure 1, by augmenting one low voltage and low power VLMM to the 5L-HNPC, the number of 5L-HNPC output voltage levels is quadrupled and the 21L Q-HNPC converter is attained. As presented in Figure 1, the quaternary ratio of the main dc-link power supply is used in the proposed 21L Q-HNPC converter. In the 21L Q-HNPC converter, the 5L-HNPC module operates at nominal voltage (E) and low frequency (f_1) in which all of the power switches operate at $E/2$ with f_1 frequency. In addition, the augmented VLMM works at low voltage ($E/4$) in which two switches operate at only $E/4$ with $5 \times f_1$ frequency, and four switches work at only $E/8$ with switching frequency. Thus, only four very low-voltage switches operate at switching frequency and the number of high frequency switches is substantially reduced in the attained 21L Q-HNPC converter. Then, the high-efficiency, and high-frequency silicon carbide metal-oxide-semiconductor field-effect transistors (SiC-MOSFET) can be used for the proposed VLMM. Moreover, due to low frequency operation of the main 5L-HNPC and two switches of the VLMM, it is possible to use the gate turn-off thyristor (GTO) instead of the insulated gate bipolar transistor (IGBT) especially for high power applications, which leads to remarkable decrease in cost, size and complexity of the attained 21L Q-HNPC converter.

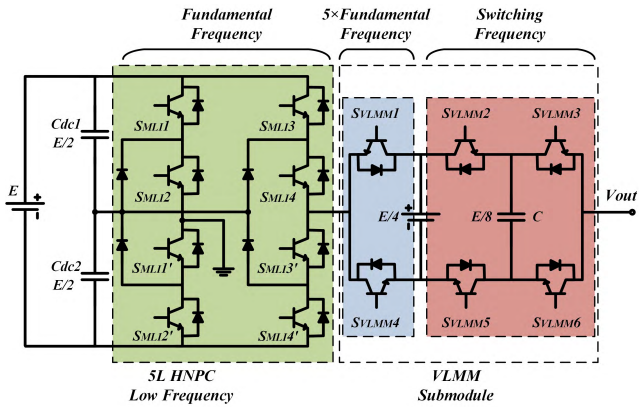

FIGURE 1. One Stage Multiplication of the 5L-HNPC Output Voltage Level Number: The proposed 21L Q-HNPC converter.

C. THE PROPOSED MODULATION METHOD FOR VLMM WITH CAPACITOR VOLTAGE SELF-BALANCING AND MINIMUM CAPACITOR VALUE CALCULATION

Figure 2 depicts the proposed modulation method for the VLMM submodule. The suggested modulation method comprises four combined level shifted and phase shifted triangular carriers and logic gates to generate switching signals of the VLMM submodule power switches. First, a zero-crossing comparator (Z_C) is used to detect positive and negative half cycle of the VLMM input reference signal ($V_{ref-VLMM}$) and to control (S_{VLMM1}, S_{VLMM4}) at $5 \times f_1$ frequency. Z_C and (S_{VLMM1}, S_{VLMM4}) are expressed as

$$Z_C = \begin{cases} 1, & V_{ref-VLMM} \geq 0 \\ 0, & V_{ref-VLMM} < 0 \end{cases} \quad (1)$$

$$S_{VLMM1} = \overline{S_{VLMM4}} = Z_C \quad (2)$$

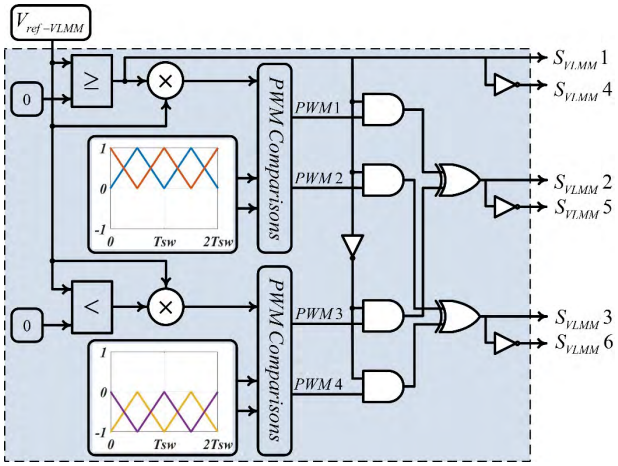

FIGURE 2. Block diagram of the proposed modulation method for the VLMM.

is ON when $Z_C = 1$ and OFF when $Z_C = 0$. Then, $V_{ref-VLMM}$ is intersected with four triangle carrier signals where the positive and negative half cycle of $V_{ref-VLMM}$ is intersected with two positive and two negative phase-shifted triangle carrier signals, respectively. Both of the positive and negative phase-shifted carrier signals are shifted by π. Thus, the outputs of the four PWM comparisons ($PWM1$, $PWM2$, $PWM3$, $PWM4$) are applied to two logic form equations to provide corresponding gate signals of the VLMM power switches. The logic equations for providing (S_{VLMM2}, S_{VLMM5}) and (S_{VLMM3}, S_{VLMM6}) switching signals are

$$S_{VLMM2} = \overline{S_{VLMM5}} = (PWM1 \cdot Z_C) \oplus (PWM3 \cdot \overline{Z_C}) \quad (3)$$

$$S_{VLMM3} = \overline{S_{VLMM6}} = (PWM2 \cdot Z_C) \oplus (PWM4 \cdot \overline{Z_C}) \quad (4)$$

where $\oplus$ and $\cdot$ are logic XOR and AND gates.

The charging and discharging of the VLMM capacitor is balanced in each switching period by employing the proposed modulation method. Therefore, in each switching period, the quantities of the charge and discharge are equal which

leads to self-balancing of the VLMM capacitor voltage. As a result, the sensor-less voltage balancing of dc capacitor is obtained in the proposed VLMM submodule. Moreover, the VLMM capacitor size is decreased by factor of f_{SW}/f_1. It is worth mentioning that $V_{ref-VLMM}$ is a non-sinusoidal signal generated by the proposed decomposed modulation method for the 21L Q-HNPC converter. $V_{ref-VLMM}$ provides minor voltage levels between the major voltage levels of the main 5L-HNPC converter. The generated $V_{ref-VLMM}$ reference signal and the switching pattern generation using the proposed modulation method for the VLMM are presented in Figure 3.

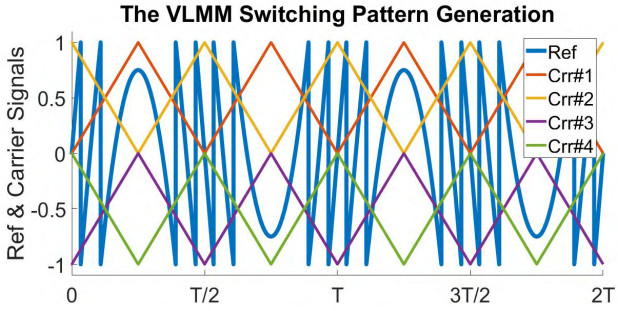

FIGURE 3. The generated $V_{ref-VLMM}$ reference signal and the switching pattern generation using the proposed modulation method for the VLMM.

As presented in Figure 3, the VLMM capacitor is charged and discharged based on non-sinusoidal and periodic reference signal provided by the suggested decomposed modulation method. In order to balance the capacitor voltage to desired value, the quantity of charge and discharge (Q_{charge} and $Q_{discharge}$) should be equal in each switching period (T_C). The VLMM capacitor charging and discharging states are shown in Figure 4.

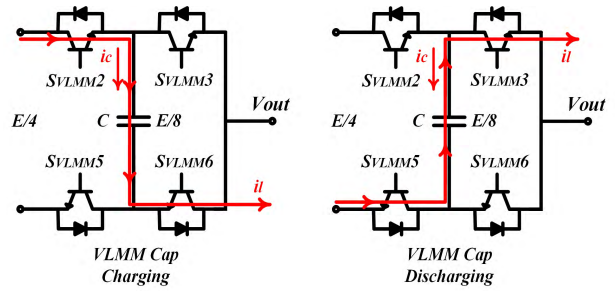

FIGURE 4. Charging and discharging states of the VLMM dc capacitor.

As illustrated in Figure 4, the relation between the load current (i_l), Q_{charge}, $Q_{discharge}$, and T_C is expressed as

$$i_l = {dq}/{dt} \tag{5}$$

$$dt = \frac{\left|T_C - t_{on-S_{VLMM}3}\right|}{2} - \frac{\left|T_C - t_{on-S_{VLMM}2}\right|}{2} \tag{6}$$

$$dq = Q_{discharge} - Q_{charge} = \frac{\left|T_C - t_{on-S_{VLMM}3}\right|}{2} \cdot i_l - \frac{\left|T_C - t_{on-S_{VLMM}2}\right|}{2} \cdot i_l \tag{7}$$

$$dq = \frac{\left|t_{on-S_{VLMM}3} - t_{on-S_{VLMM}2}\right|}{2} \cdot i_l \tag{8}$$

Therefore, the VLMM capacitor is balanced when $t_{on-S_{VLMM}3} = t_{on-S_{VLMM}2}$. The VLMM capacitor is charged and discharged with switching frequency (f_{SW}) and $t_{on-S_{VLMM}3} = t_{on-S_{VLMM}2}$ is guaranteed by applying the proposed modulation method. Hence, The VLMM capacitor is automatically balanced to half of the VLMM dc power supply and sensor-less VLMM capacitor voltage balancing is achieved. The VLMM capacitor current is calculated as

$$i_C(t) = C \times \frac{dv}{dt} \rightarrow i_C = C \times \frac{V_{ripple}}{\Delta t_c} \tag{9}$$

where C is the VLMM capacitor value, V_{ripple} is the VLMM capacitor voltage ripple, Δt_c is duration of the VLMM capacitor charge and discharge in each PWM period, and i_C is the VLMM capacitor current. Hence, Δt_c is expressed as

$$\Delta t_c = \frac{1 - \left|V_{ref-VLMM}\right|}{2f_{SW}} \tag{10}$$

Thus, by employing the VLMM proposed modulation method and considering the fact that $V_{ref-VLMM}$ is a non-sinusoidal reference signal, Δt_c is calculated as

$$\Delta t_c = \begin{cases} \left(1 - \left|V_{ref} - 0.8\right|\right)/(2 \times f_{SW}), & 0.6 \le V_{ref} \le 1 \\ \left(1 - \left|V_{ref} - 0.4\right|\right)/(2 \times f_{SW}), & 0.2 \le V_{ref} < 0.6 \\ \left(1 - \left|V_{ref}\right|\right)/(2 \times f_{SW}), & -0.2 \le V_{ref} < 0.2 \\ \left(1 - \left|V_{ref} + 0.4\right|\right)/(2 \times f_{SW}), & -0.6 \le V_{ref} < -0.2 \\ \left(1 - \left|V_{ref} + 0.8\right|\right)/(2 \times f_{SW}), & -1 \le V_{ref} < -0.6 \end{cases} \tag{11}$$

In (11), the charging and discharging periods of the proposed VLMM capacitor are balanced in each switching period by employing the suggested modulation method. Figure 5 depicts the relationship between Δt_c, the VLMM capacitor current ($i_C(t)$), and its mean value in one fundamental period. As presented in Figure 5, by employing the proposed modulation method, the VLMM capacitor is charged and discharged in each switching period and its average current in each switching and one fundamental period is zero. Hence, The VLMM capacitor is automatically balanced and sensor-less VLMM capacitor voltage balancing is attained.

The VLMM minimum required capacitor value is calculated based on Δt_c in (11). Considering (10) and (11), the maximum value of Δt_c as worst-case scenario is expressed as

$$(\Delta t_c)_{\max} = \frac{1}{2f_{SW}} \tag{12}$$

Hence, the minimum required VLMM capacitor value for the desired V_{ripple}, load current peak value of I_{peak}, and switching frequency of f_{SW} is defined as

$$C_{VLMM-\min} = \frac{I_{peak}}{V_{ripple} \times 2f_{SW}} \tag{13}$$

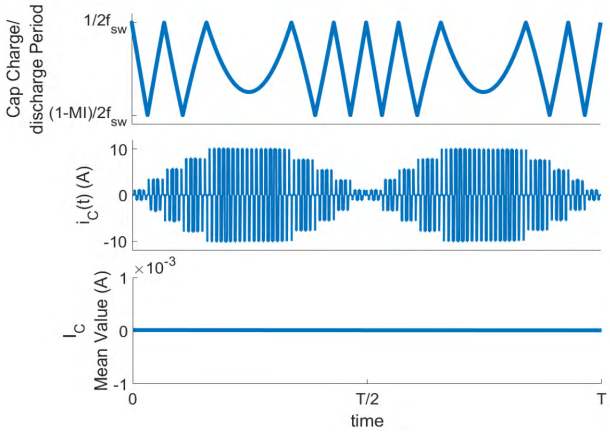

FIGURE 5. Relationship between Δt_C, the VLMM capacitor current ($i_C(t)$), and its mean value (I_C) in one fundamental period by employing proposed decomposed modulation method in the VLMM.

Considering (13), the proposed VLMM capacitor can be adjusted by modifying f_{SW} in which by increasing f_{SW}, the required VLMM capacitor is decreased.

D. THE PROPOSED SENSOR-LESS DECOMPOSED MODULATION METHOD FOR THE 21L Q-HNPC CONVERTER

The proposed sensor-less decomposed modulation method for the 21L Q-HNPC converter is presented in Figure 6. As depicted in Figure 6, a new switching method is employed to generate the main 5L-HNPC and augmented low-voltage VLMM switching signals from the input sinusoidal reference signal. Various steps of the proposed decomposed modulation method for the 21L Q-HNPC converter are as follows

1) The input $5 \times V_{ref}(t) = 5 \times MI \times \sin(\omega_r t)$ reference signal is decomposed to the major voltage levels for the 5L-HNPC and the minor voltage levels for the proposed VLMM. The $5 \times V_{ref}(t)$ compared to -3, -1, $+1$, $+3$ levels by employing the PWM comparisons. As shown in Figure 6, sum of the PWM comparisons outputs provides the low-frequency five-level staircase $V_{ref-HNPC}$ reference signal.
2) The attained $V_{ref-HNPC}$ is applied to the 5L-HNPC switching states table to generate corresponding switching signals of the 5L-HNPC converter. The switching states table of the 5L-HNPC is illustrated in Table 1. Hence, the output voltage of the 5L-HNPC converter is a staircase voltage with peak-to-peak voltage of $2E$ and fundamental frequency. Accordingly, all of ($S_{MLI}1$, $\overline{S_{MLI}1}$), ($S_{MLI}2$, $\overline{S_{MLI}2}$), ($S_{MLI}3$, $\overline{S_{MLI}3}$), and ($S_{MLI}4$, $\overline{S_{MLI}4}$) power switches operate at fundamental frequency.
3) The proposed VLMM reference signal is calculated as

$$V_{ref-VLMM} = 5 \times V_{ref}(t) - V_{ref-HNPC} \qquad (14)$$

Therefore, the augmented low-voltage VLMM $V_{ref-VLMM}$ reference signal provides minor voltage levels between the major voltage levels of the main 5L-HNPC. Then, $V_{ref-VLMM}$ is applied to the VLMM suggested modulation method to generate switching signals for ($S_{VLMM}1$, $S_{VLMM}4$), ($S_{VLMM}2$, $S_{VLMM}5$), and ($S_{VLMM}3$, $S_{VLMM}6$). The VLMM proposed modulation method is presented and described in part C and Figure 2.

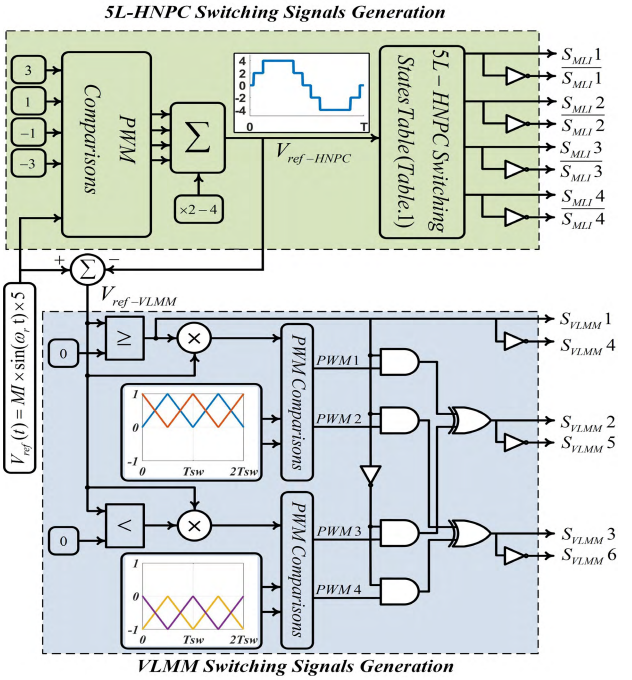

FIGURE 6. Block diagram of the proposed modulation method for the 21L Q-HNPC converter.

TABLE 1. The 5L-HNPC possible switching states table.

$V_{ref-HNPC}$	$S_{MLI}1$	$S_{MLI}2$	$S_{MLI}3$	$S_{MLI}4$	$V_{out-HNPC}$
4	1	1	0	0	E
2	1	1	0	1	$E/2$
	0	1	0	0	
0	1	1	1	1	0
	0	1	0	1	
	0	0	0	0	
-2	0	1	1	1	$-E/2$
	0	0	0	1	
-4	0	0	1	1	$-E$

The 21L Q-HNPC converter input reference signal ($5 \times V_{ref}$) as well as the decomposed reference signals of the 5L-HNPC converter ($V_{ref-HNPC}$), and the proposed VLMM submodule ($V_{ref-VLMM}$) are presented in Figure 7.

III. COMPARISON OF THE PROPOSED 21L Q-HNPC CONVERTER WITH OTHER MLC TOPOLOGIES

The comparison of the proposed 21L Q-HNPC converter with the traditional MLCs such as NPC, CHB, FC, SM and

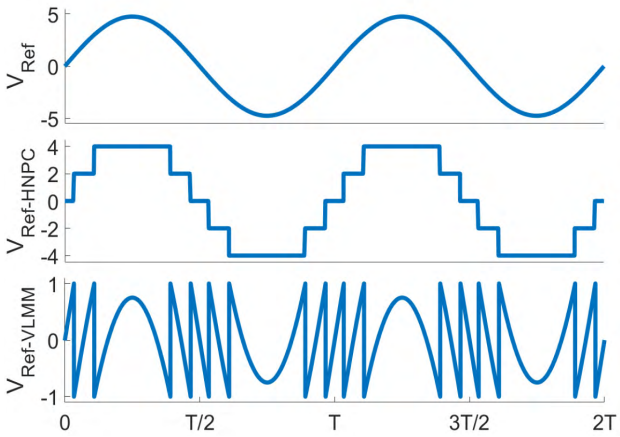

FIGURE 7. The 21L Q-HNPC input reference (V_{ref}), and the generated $V_{ref-HNPC}$ and $V_{ref-VLMM}$ reference signal by employing the proposed decomposed modulation method.

ANPC converters for generating the 21-level output voltage from various aspects are illustrated in Tables 2 and 3. Table 2 presents the comparison between the proposed 21L Q-HNPC and the other MLCs from aspects of the number of low frequency (LF) and high frequency (HF) switches, diodes, capacitors and isolated dc sources. As illustrated in Table 2, the number of HF and LF switches as well as the number of diodes, isolated dc sources and capacitors are remarkably decreased by augmenting the proposed VLMM submodule to the 5L-HNPC converter. The additional minor voltage levels are generated between the major voltage levels of the main 5L-HNPC by utilizing the proposed VLMM, which results in quadrupling the number of output voltage levels.

TABLE 2. Comparison of the proposed 21L Q-HNPC with the NPC, CHB, FC, SM, and ANPC converters from aspect of the number of components.

Type of MLI	No. of HF Switches	No. of LF Switches	No. of Diodes	No. of Caps	No. of DC Sources
NPC	40	-	380	20	1
CHB	40	-	-	-	10
FCM	40	-	-	19	2
SM	40	-	-	20	2
ANPC	20	4	-	11	1
Q-HNPC	4	10	4	3	2

Moreover, Table 3 illustrates the voltage rating of the isolated dc sources, capacitors, and HF and LF switches for the proposed Q-HNPC converter and the other MLCs for providing the 21 level output voltage. As presented in Table 3, in the proposed 21L Q-HNPC converter, only the low-voltage part operates at switching frequency whereas the high-voltage part works at fundamental or low frequency. This improvement causes remarkable decrease in emanated electromagnetic interference (EMI), switching noises and losses as well as increase the efficiency of the proposed 21L Q-HNPC converter.

TABLE 3. Comparison of the proposed 21L Q-HNPC with the NPC, CHB, FC, SM, and ANPC converters from aspect of the voltage ratings of devices.

Type of MLI	DC Sources Voltage (p.u.)	HF Switches Voltage (p.u.)	LF Switches Voltage (p.u.)	Caps Voltage (p.u.)
NPC	1	0.05	-	0.05
CHB	0.1	0.1	-	No Cap
FCM	1	0.05	-	From 0.05 to 0.95
SM	1	0.05	-	From 0.05 to 0.45
ANPC	1	0.05	0.5	From 0.05 to 0.45
Q-HNPC	0.8 (HNPC) 0.2 (VLMM)	0.1 (VLMM)	0.4 (HNPC) 0.2 (VLMM)	0.1 (VLMM)

Hence, the output voltage quality of the attained 21L Q-HNPC converter is remarkably ameliorated by multiplication of the output voltage levels whereas the low cost and size are imposed on the 5L-HNPC and the number of components such as power supplies, semiconductors, and capacitors is significantly decreased.

IV. GENERALIZED CIRCUIT TOPOLOGY OF THE PROPOSED Qn-HNPC CONVERTER AND THE GENERALIZED SENSOR-LESS DECOMPOSED MODULATION METHOD

A. TWO-STAGE MULTIPLICATION OF THE OUTPUT VOLTAGE LEVEL NUMBER: THE 85-LEVEL Q2-HNPC CONVERTER

The 85-level Q2-HNPC converter is depicted in Figure 8. It consists of the main 5L HNPC converter and 2 proposed VLMM submodules. The proposed decomposed modulation method for the 85L Q2-HNPC converter is presented in Figure 9. As shown in Figure 9, the suggested modulation method is applied to decompose the reference signals of the main 5L HNPC converter and 2 augmented low-voltage and low-power VLMM submodules from the input sinusoidal signal. First, the suggested modified reference voltage waveform generator is used to provide modified reference waveform from input $MI \times \sin(\omega_r t)$ reference signal. Then, the modified reference waveform is decomposed to major voltage levels for the main 5L HNPC converter and minor voltage levels for 2 proposed VLMM submodules. The suggested main 5L HNPC converter major level detector is used to detect low-frequency and high-voltage major voltage levels ($V_{ref-Main-MLI}$). Thus, the achieved $V_{ref-Main-MLI}$ reference signal provides major voltage levels of the proposed 85L Q2-HNPC converter output voltage. Moreover, the augmented low-voltage VLMMs reference signals provide minor voltage levels between major voltage levels of the main 5L HNPC con-

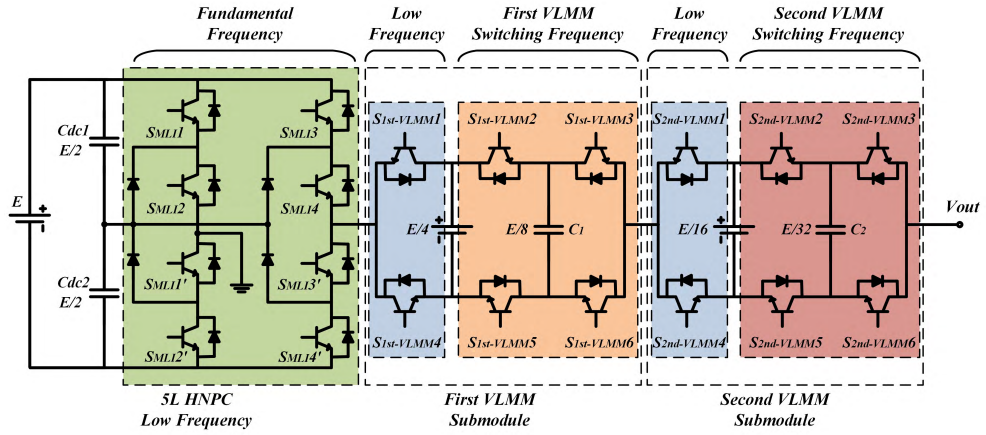

FIGURE 8. Circuit topology of the proposed 85L Q2-HNPC converter.

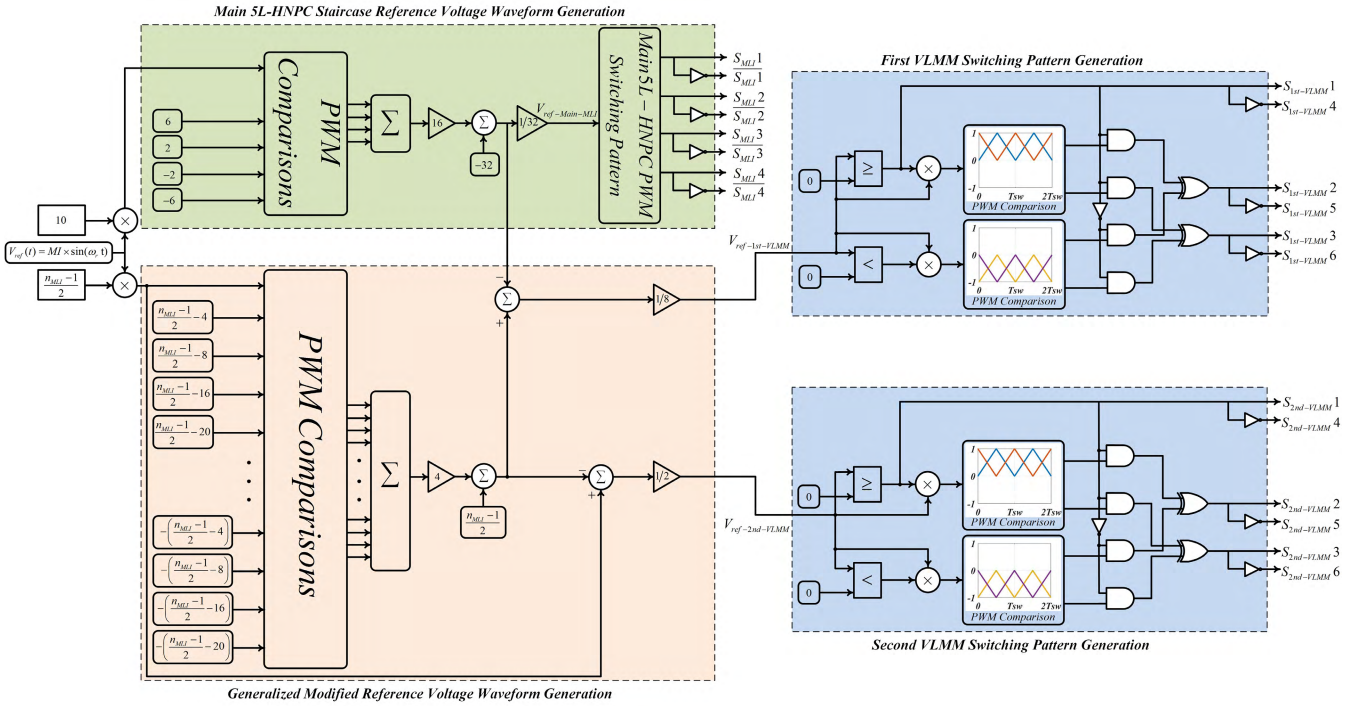

FIGURE 9. The generalized proposed decomposed switching pattern for 85L Q2-HNPC and generalized Qn-HNPC converters.

verter. The attained $V_{ref-1st-VLMM}$ and $V_{ref-2nd-VLMM}$ reference signals generate low-voltage minor voltage levels of the 85L Q2-HNPC output voltage. Finally, the obtained $V_{ref-Main-MLI}$ is applied to the main 5L HNPC switching pattern generator to provide ($S_{MLI}1$, $\overline{S_{MLI}1}$), ($S_{MLI}2$, $\overline{S_{MLI}2}$), ($S_{MLI}3$, $\overline{S_{MLI}3}$), and ($S_{MLI}4$, $\overline{S_{MLI}4}$) switching signals. Similarly, $V_{ref-1st-VLMM}$ and $V_{ref-2nd-VLMM}$ reference signals are applied to each VLMM proposed switching pattern generator, which is described in part C of section II, to provide ($S_{1st-VLMM}1$, $S_{1st-VLMM}4$), ($S_{1st-VLMM}2$, $S_{1st-VLMM}5$), and ($S_{1st-VLMM}3$, $S_{1st-VLMM}6$) switching signals for the first VLMM, as well as ($S_{2nd-VLMM}1$, $S_{2nd-VLMM}4$), ($S_{2nd-VLMM}2$, $S_{2nd-VLMM}5$), and ($S_{2nd-VLMM}3$, $S_{2nd-VLMM}6$) switching signals for the second VLMM.

B. GENERALIZED CIRCUIT TOPOLOGY OF THE PROPOSED Qn-HNPC CONVERTER

In this part, the generalized topology of the Qn-HNPC converter is proposed. The proposed Qn-HNPC converter consists of one 5L HNPC converter as the main MLC and n number of the suggested VLMM submodules. The n VLMM submodules are augmented to the main 5L HNPC converter output to remarkably increase the number of output voltage

levels. The number of the attained Qn-HNPC output voltage levels is expressed as

$$N_{Qn-HNPC} = 5 \times 4^n + 4^{n-1} + 4^{n-2} + \cdots + 1 \quad (15)$$

where $N_{Qn-HNPC}$ is the number of output voltage levels of the attained Qn-HNPC and n is the number of augmented VLMM submodules. Based on (15), the number of output voltage levels of the Qn-HNPC is remarkably increased by augmenting n number of the VLMM submodules. For example, the number of output voltage levels of the Q2-HNPC by augmenting two VLMM submodules is obtained as

$$N_{Q2-HNPC} = 5 \times 4^2 + 4^1 + 1 = 85 \quad (16)$$

Similarly, the number of output voltage levels of the Q3-HNPC by augmenting three VLMM submodules is obtained as

$$N_{Q3-HNPC} = 5 \times 4^3 + 4^2 + 4^1 + 1 = 341 \quad (17)$$

Moreover, in the proposed Qn-HNPC, the main 5L HNPC converter operates at converter nominal voltage (E) and fundamental frequency (low frequency) whereas the first augmented VLMM works at low voltage which is $\frac{E}{4^1}$ and low frequency, and also the second augmented VLMM operates at $\frac{E}{4^2}$ and low frequency. Similarly, the $(n-1)^{\text{th}}$ augmented VLMM operates at $\frac{E}{4^{(n-1)}}$ and low frequency and the n^{th} augmented VLMM operates at $\frac{E}{4^n}$ and switching frequency. Hence, only the n^{th} augmented VLMM commutates at switching frequency whereas the main 5L HNPC converter and other $n-1$ VLMMs operate at low frequency. The proposed n number of the low-voltage and low-power VLMM submodules generate additional minor voltage levels between major voltage levels of the main 5L HNPC converter which causes notable increase the number of the Qn-HNPC converter output voltage levels. Furthermore, all components of the augmented VLMM submodules operate at low voltage and low power. The dc-link voltage and power of the applied low-voltage and low-power VLMM submodules are only a fraction of the main 5L HNPC converter dc-link voltage and power. Accordingly, the output voltage quality of the Qn-HNPC converter is remarkably amended by notable increase in number of the output voltage levels whereas the low extra cost and size are added to the main 5L HNPC converter.

V. 41L THREE-PHASE CONFIGURATION OF THE PROPOSED Q-HNPC CONVERTER

The three-phase configuration of the proposed Q-HNPC converter is presented in Figure 10. As shown in Figure 10, it consists of three single-phase 21L Q-HNPC converters. Each single-phase Q-HNPC converter requires the main dc power supply with PDR of 33 % and the VLMM auxiliary dc power supply with PDR of only 2.6 %. In the three-phase Q-HNPC converter, the output phase voltage has 21 levels and the output line voltage has 41 levels. Hence, by augmenting the low-voltage and low-power VLMM submodules to the 5L HNPC converter, very high resolution 41L three-phase Q-HNPC is obtained.

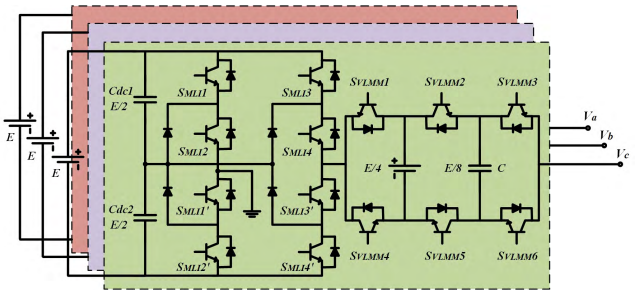

FIGURE 10. Three-phase configuration of the proposed Q-HNPC converter.

TABLE 4. Main parameters of the simulated proposed 21L Q-HNPC, 41L three-phase Q-HNPC, and 85L Q2-HNPC converters.

Parameters	Value
Fundamental frequency	$f = 50\,Hz$
RL load	$R = 40\,\Omega, L = 20\,mH$
21L Q-HNPC & Each phase of the 41L three-phase Q-HNPC	
Main 5L HNPC dc-link	$E = 200V$
VLMM submodule dc-link	$E_{VLMM} = 50V$
HNPC dc capacitors	$C_{dc1} = C_{dc2} = 1200\,\mu F$
VLMM switching frequency	$f_{SW} = 5\,kHz$
VLMM capacitor	$C = 680\,\mu F$
85L Q2-HNPC	
Main 5L HNPC dc-link	$E = 200V$
First VLMM submodule dc-link	$E_{1st-VLMM} = 50V$
Second VLMM submodule dc-link	$E_{2nd-VLMM} = 12.5V$
HNPC dc capacitors	$C_{dc1} = C_{dc2} = 1200\,\mu F$
First VLMM capacitor	$C_1 = 800\,\mu F$
First VLMM switching frequency	$f_{SW-1st-VLMM} = 10\,kHz$
Second VLMM capacitor	$C_2 = 680\,\mu F$
Second VLMM switching frequency	$f_{SW-2nd-VLMM} = 20\,kHz$

VI. SIMULATION RESULTS

The proposed 21L Q-HNPC, 41L three-phase Q-HNPC, and 85L Q2-HNPC converters have been simulated in MATLAB/Simulink platform to evaluate the feasibility and performance of the proposed topologies as well as their suggested sensor-less decomposed modulation methods. The 21L Q-HNPC, 85L Q2-HNPC, and 41L three-phase Q-HNPC converters as well as their switching pattern generation methods are presented in Figures 1, 6, 8, 9, and 10, respectively. The main parameters of the simulated 21L Q-HNPC, 41L three-phase Q-HNPC, and 85L Q2-HNPC converters are illustrated in Table 4.

Figure 11 presents the simulation results of the low frequency main 5L-HNPC and the high frequency VLMM submodule voltages as well as the proposed 21L Q-HNPC output

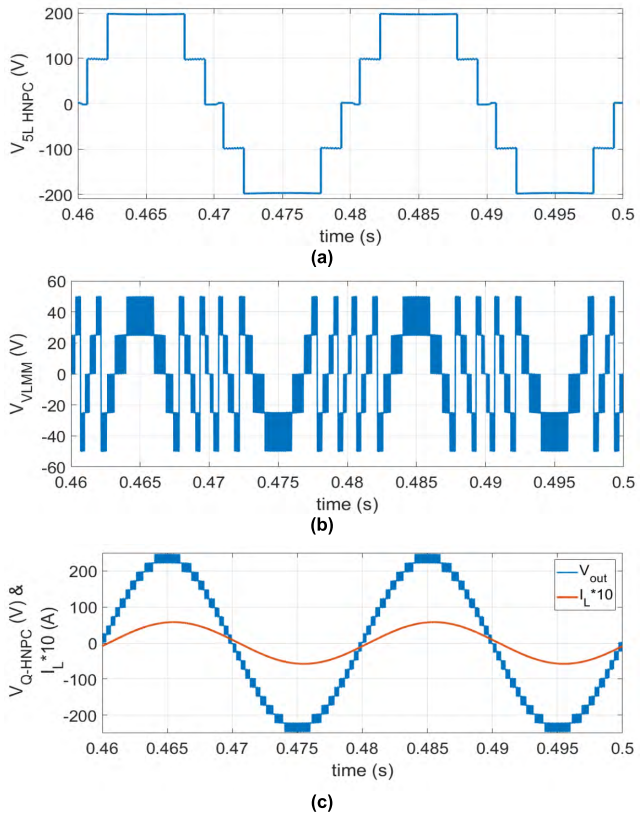

FIGURE 11. (a). The main 5L HNPC converter output voltage. (b). The augmented VLMM submodule output voltage. (c). The proposed 21L Q-HNPC output voltage and load current multiply by 10.

voltage and load current for $f_{SW} = 5\,kHz$ and $MI = 0.95$. As depicted in Figure 11. (a), the main 5L-HNPC operates at fundamental frequency with $400\,V$ peak-to-peak voltage. In addition, as shown in Figure 11. (b), the proposed VLMM submodule works at $f_{SW} = 5\,kHz$ with $100\,V$ peak-to-peak voltage. Hence, as presented in Figure 11. (c), the proposed 21L Q-HNPC output voltage has 21 levels with $500\,V$ peak-to-peak voltage. Furthermore, Figure 12 shows the FFT analysis of the proposed 21L Q-HNPC output voltage. As depicted in Figure 12, the output voltage THD is $6.25\,\%$ and the first switching harmonic cluster of the output voltage is around $10\,kHz$. With regards to Figure 12, by applying the proposed modulation method to the VLMM, the first switching harmonic cluster is shifted to twice of the switching frequency and odd multiples of the switching harmonic clusters are canceled and eliminated from the output voltage. Accordingly, the output voltage has switching harmonic clusters around the $k \times m \times f_{SW}$ where k is an integer number and $m = 2$ is the number of phase shifted carrier signals in the suggested switching pattern.

Figure 13 depicts the 21L Q-HNPC converter output voltage and load current during step load change from $R = 40\,\Omega, L = 20\,mH$ to $R = 10\,\Omega, L = 15\,mH$. As shown in Figure 13, the proposed 21L Q-HNPC converter has improved steady-state performance and fast dynamic

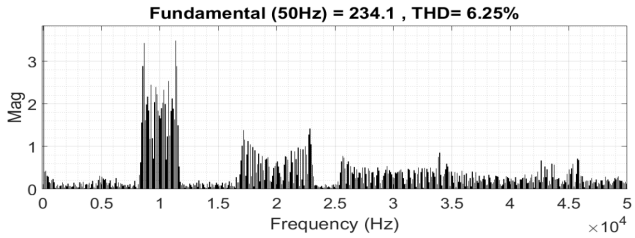

FIGURE 12. FFT analysis of the proposed 21L Q-HNPC output voltage.

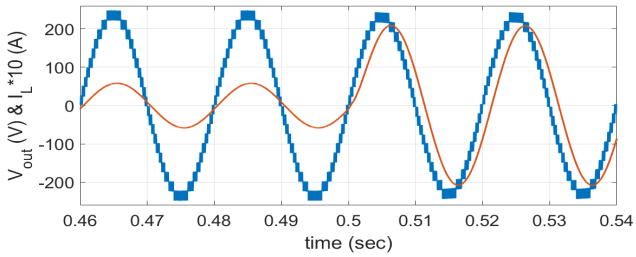

FIGURE 13. The proposed 21L Q-HNPC output voltage and load current multiply by 10 during step load change from $R = 40\,\Omega$, $L = 20\,mH$ to $R = 10\,\Omega$, and $L = 15\,$mH.

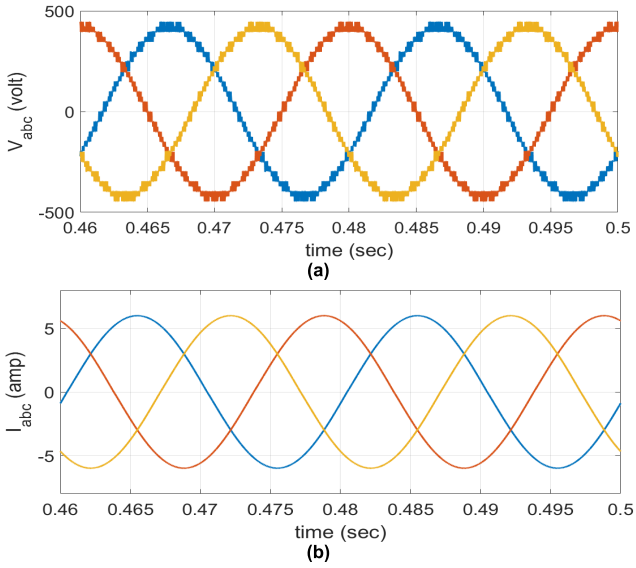

FIGURE 14. (a). The 41L three-phase Q-HNPC converter output line voltages. (b). The 41L three-phase Q-HNPC converter load current.

response during step load change with various load factors. Furthermore, the VLMM capacitor is self-balanced during step load change and sensor-less capacitor voltage balancing is obtained for various load conditions.

In addition, the output line voltages and load currents of the 41L three-phase Q-HNPC converter is presented in Figure 14. As depicted in Figure 14, the output line voltage has 41 levels and the load current is pure sinusoidal. Hence, the very high resolution three-phase converter is obtained.

Moreover, simulation results are presented to evaluate the performances of the proposed 85L Q2-HNPC converter and

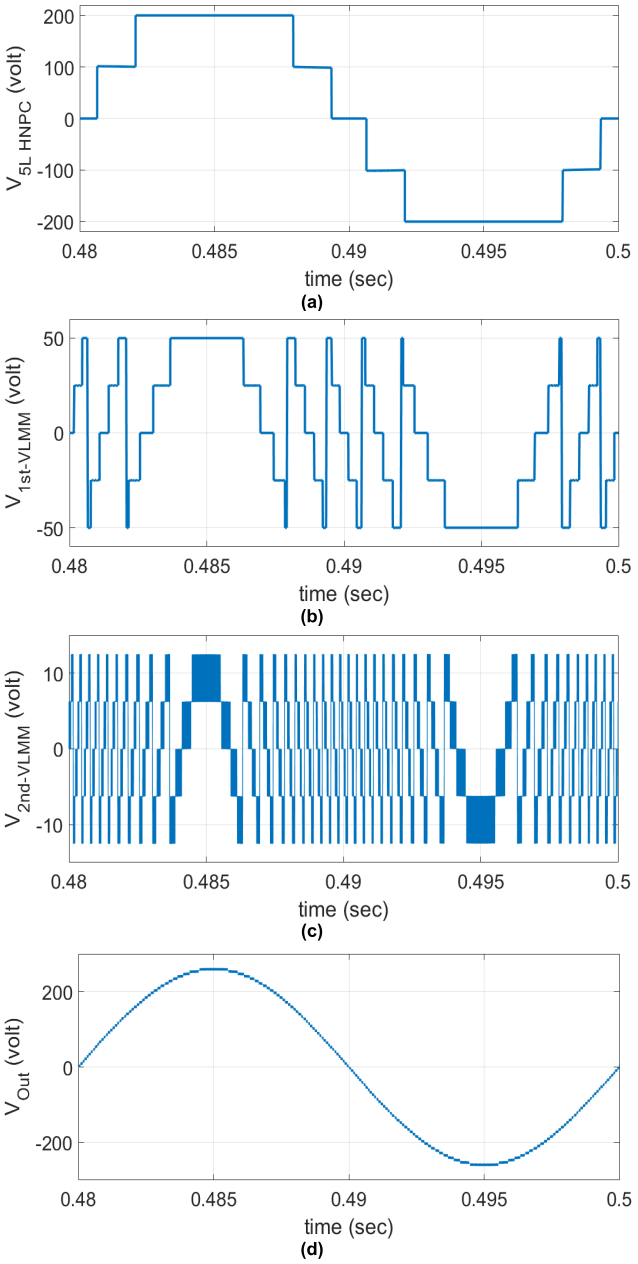

FIGURE 15. (a). The main 5L HNPC converter output voltage. (b). First augmented VLMM submodule output voltage. (c). Second augmented VLMM submodule output voltage. (d). The proposed 85L Q2-HNPC output voltage.

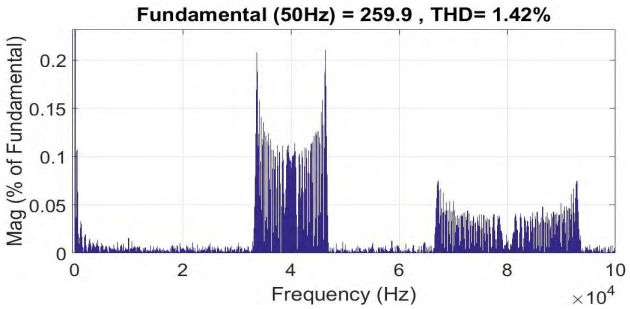

FIGURE 16. FFT analysis of the proposed 85L Q2-HNPC output voltage.

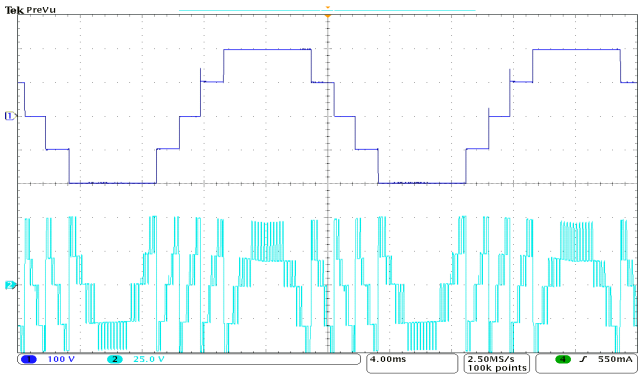

FIGURE 17. The main 5L-HNPC converter output voltage (Ch1: 100 V/div) and the proposed VLMM submodule output voltage (Ch2: 25 V/div).

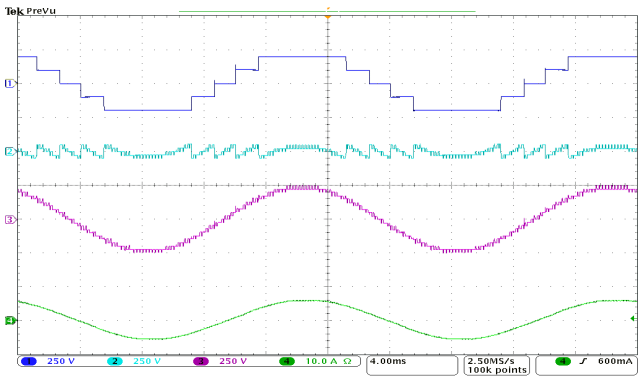

FIGURE 18. The main 5L-HNPC converter (Ch1: 250 V/div), the proposed VLMM submodule (Ch2: 250 V/div), the 21L Q-HNPC converter (Ch3: 250 V/div) output voltages, and the load current (Ch4: 10 A/div).

its suggested switching method. The main 5L HNPC converter output voltage, the first and second low-voltage and low-power VLMM submodules output voltages, as well as the output voltage of the 85L Q2-HNPC converter for $MI = 0.99$ are depicted in Figure 15. As presented in Figures 15. (a), (b) and (c), the main 5L HNPC converter commutates at 50 Hz with peak-to-peak voltage of 400 V whereas the first augmented low-voltage and low-power VLMM submodule operates at $f_{SW-1st-VLMM} = 10\,kHz$ with peak-to-peak voltage of 100 V and the second added very low-voltage and low-power VLMM submodule operates at $f_{SW-2nd-VLMM} = 20\,kHz$ with peak-to-peak voltage of 25 V. Figure 15. (d) illustrates the proposed 85L Q2-HNPC converter staircase output voltage with peak-to-peak voltage of 525 V. The 85L Q2-HNPC converter output voltage FFT analysis is presented in Figure 16. As shown in Figure 16, the output voltage THD is 1.42 % and the output voltage first switching harmonic cluster is around 40 kHz. Hence, the output voltage has switching harmonic clusters around the $k \times m \times f_{SW-2nd-VLMM}$ where k is an integer number and $m = 2$ is the number of phase shifted

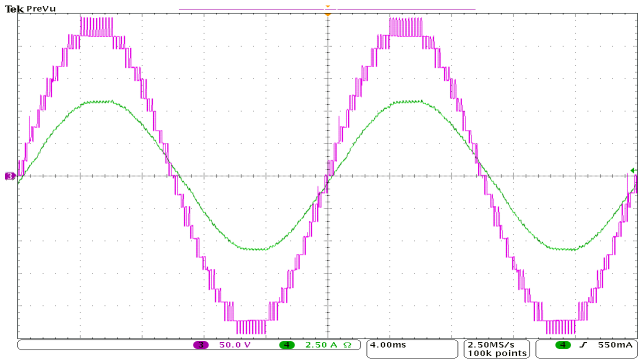

FIGURE 19. The proposed 21L Q-HNPC converter output voltage (Ch3: 50 V/div) and the load current (Ch4: 2.5 A/div).

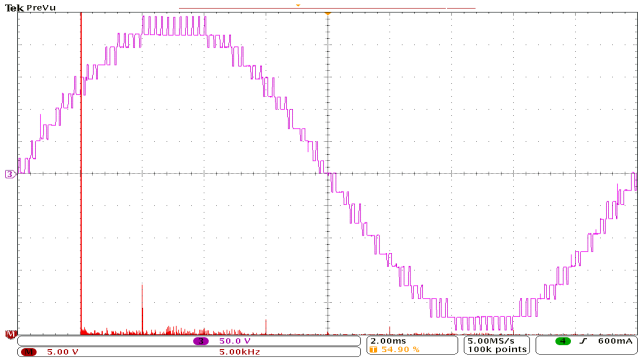

FIGURE 20. The proposed 21L Q-HNPC converter output voltage (Ch3: 50 V/div) and the output voltage FFT analysis (Math: vertical: 5.00 V/div, horizontal: 5.00 kHz/div).

carrier signals in the proposed modulation method for second VLMM submodule.

VII. EXPERIMENTAL RESULTS

The proposed 21L Q-HNPC converter has been implemented in the laboratory to evaluate the performance and feasibility of the proposed configuration as well as the suggested sensor-less decomposed modulation method. It comprises fourteen 700 V 58A APT70SM70B SiC MOSFETs and their driver boards. The VLMM carrier frequency is set to $f_{SW} = 2.5\,kHz$. In order to control the proposed 21L Q-HNPC converter, the dSpace 1103 real-time controller has been employed. All the experimental prototype components are presented in Table 4. Figure 17 presents the low frequency main 5L-HNPC, and the high frequency VLMM submodule output voltages. As depicted in Figure 17, the main 5L-HNPC commutates at $50\,Hz$ with $400\,V$ peak-to-peak voltage whereas the proposed VLMM submodule operates at $f_{SW} = 2.5\,kHz$ with $100\,V$ peak-to-peak voltage. Figure 18 depicts the main 5L-HNPC, the augmented VLMM, and the 21L Q-HNPC output voltages as well as the load current at RL load. Figure 19 shows the proposed 21L Q-HNPC converter output voltage and load current at RL load. Moreover, the staircase output voltage of the proposed 21L Q-HNPC converter as well as its FFT analysis are shown in Figure 20. As presented in Figure 20, the output voltage has the first switching harmonic cluster around $2 \times f_{SW} = 5\,kHz$. Hence, odd multiples of the VLMM switching frequency (f_{SW}) are eliminated from the output voltage frequency spectrum.

Hence, provided experimental and simulation results verifies the viability and feasibility of the proposed 21L Q-HNPC, 41L three-phase Q-HNPC, and 85L Q2-HNPC configurations as well as their suggested sensor-less decomposed modulation methods.

VIII. CONCLUSION

The novel generalized proposed circuit topology of Qn-HNPC converter and the suggested sensor-less decomposed modulation method were studied and analyzed. Moreover, the 21L Q-HNPC converter and its extended 85L Q2-HNPC converter topology as well as their sensor-less decomposed modulation methods were described and analyzed in detail. The main advantages of the proposed Qn-HNPC converters are as follows

- The number of output voltage levels of the attained Qn-HNPC converter is remarkably increased whereas the low extra cost and size are imposed on the main 5L HNPC converter.
- Only four low-voltage and low-power switches of the newly introduced VLMM submodule in the proposed Qn-HNPC converter operate at switching frequency and other semiconductor devices commutate at low or fundamental frequency.
- The maximum power distribution ratio (PDR) of the first VLMM dc-power supply is only 8 % of the nominal power for the 21L Q-HNPC and 85L Q2-HNPC converters, and the maximum PDR of the second VLMM dc-power supply is only 0.7 % of the nominal power for the 85L Q2-HNPC converter.
- The proposed modulation method for VLMM causes self-balancing of all the capacitors voltage, and notable decrease in stored energy and size of the capacitor in the proposed VLMM.
- The proposed switching method leads to eliminate odd multiples of switching frequency from the output voltage frequency spectrum.

Accordingly, aforementioned improvements have led to remarkable decrease in control complexity, notable reduction in capacitor size of the novel proposed VLMM, as well as substantial improvements of the Qn-HNPC converter performance and output voltage quality. Provided simulation and experimental results verify the performance and viability of the proposed Qn-HNPC converters as well as their suggested sensor-less decomposed modulation and control methods.

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MOSTAFA ABARZADEH (S'15–M'16) received the B.Sc., M.Sc., and Ph.D. degrees (Hons.) in electrical engineering from the Sahand University of Technology (SUT), Tabriz, Iran, in 2008, 2011, and 2016, respectively.

He was a Visiting Ph.D. Researcher with Aalborg University, Denmark, in 2015. Since 2016, he has been an Assistant Professor with the Electrical Engineering Faculty, SUT. He is currently a Postdoctoral Research Fellow with the Canada Research Chair in Electric Energy Conversion and Power Electronics, École de technologie supérieure (ÉTS), University of Quebec, Canada. He has authored or coauthored over 35 journal and conference papers and book chapters. He holds six patents, including one U.S. patent. His current research interests include topology, modeling, control, and modulation of power electronic converters, hybrid multilevel inverters, and applications of power electronics in renewable energy conversion, transportation electrification, power grid, and variable-speed motor drives.

Dr. Abarzadeh has been a member of the Iran's National Elites Foundation, since 2006. He was selected by the SUT as the Distinguished Student, in 2010 and 2012. He was a recipient of the Best Poster Presentation Award from the IEEE Energy Conversion Congress and Exposition (ECCE), in 2015.

KAMAL AL-HADDAD (S'82–M'88–SM'92–F'07) received the B.Sc.A. and M.Sc.A. degrees in electrical engineering from the University of Québec à Trois-Rivières, Canada, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from the Institute National Polytechnique, Toulouse, France, in 1988.

Since 1990, he has been a Professor with the Electrical Engineering Department, École de technologie supérieure (ÉTS), Montreal, QC, Canada, where he has been the Canada Research Chair in Electric Energy Conversion and Power Electronics, since 2002. He has supervised more than 100 Ph.D. and M.Sc.A. students working in the field of power electronics. He is a Consultant and has established very solid link with Canadian industries. He has coauthored more than 600 transactions and conference papers and two books. His research interests include high-efficient static power converters, active-hybrid power filters, grid connect, and multilevel converters, including modeling, control, and development of prototypes for various industrial applications. He is a member of the Academy of science, a Fellow of the Royal Society of Canada, and a Fellow Member of the Canadian Academy of Engineering. He was a recipient of the Dr.-Ing. Eugene Mittelmann Achievement Award. He was the IEEE IES President, from 2016 to 2017, and a IES Distinguished Lecturer.