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Surface Study of $Ge_2Sb_2Te_5$-Based Electrical Probe Memory for Educational Archival Storage

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ABSTRACT Surface roughness that is an inherent character of deposited films determines contact resistance at layer interfaces and thus may play a critical role in write and readout operations of phase-change electrical probe memory comprising multiple stacked layers. The surface roughness of different layered components was therefore simulated and their impact on resulting temperature, write/read current, and bit size was evaluated. It was revealed that using capping layer with larger root-mean-square and denser roughness significantly decreases the temperature and write/read current, and therefore forms a written bit embedded inside the active layer, while surface roughness of active layer, bottom electrode, and substrate have a negligible effect on electro-thermal characteristic and phase-transformation extent of the probe memory. To trigger optimum readout current and exempt from tip wear, probe tip was suggested to penetrate into the capping layer by 0.2 nm for the densest roughness of 3 nm root-mean-square.

INDEX TERMS Surface roughness, phase-change materials, electrical probe, crystallization, amorphization, readout.

I. INTRODUCTION

Prosperity of digitalize education associated with ubiquitous on-line journals/proceedings has created an 'Age of Big Data' in the field of education and thus triggered the amount of educational archival data increasing at a phenomenal rate. To match the growth rate of global archival data particularly in the field of education, storage capacity of conventional mass storage devices such as magnetic hard disk, optical disc, and Flash memory, is required to be enhanced significantly. However, due to their inherent physical limits [1]–[6], the prospect of conventional mass storage devices to outreach the growth rate of the global data remains dim, and this urgently necessitates the development of more innovative mass storage devices that simultaneously exhibit ultra-high recorded density, fast storage speed, and low energy consumption. Probe-based memory has been regarded as one of the best solutions to resolving above issue, thus delivering several prototypes. Compared with its compatriots, phase-change electrical probe memory was unanimously considered as one of the most promising candidates to fulfill above requirements [7]–[9].

Phase-change electrical probe memory usually consists of a nanoscale conductive probe and a storage media stack comprising a so-called phase-change layer (e.g., $Ge_2Sb_2Te_5$ media) sandwiched between a capping layer that protects phase-change layer from wear and oxidation, and a under layer that serves as a bottom electrode, deposited on silicon (Si) substrate. The recording operation of phase-change electrical probe memory is achieved by injecting a current pulse, via a conductive probe, into the phase-change media whose atomic structure can be rapidly and reversibly switched between a crystalline phase having a long range order and an amorphous phase having a short range order, due to the resulting Joule heating. The readout operation is realized by applying a low voltage potential, via a conductive probe, to the previously recorded region of phase-change media to detect the current variation depending on the large electrical resistivity contrast between the crystalline and amorphous phases. Figure 1 schematically shows the principles of phase-change electrode probe memory when operated in record and readout modes respectively.

As the write/read current is almost bounded inside a region directly underneath the probe, the device resolution drastically relies on the size of the probe tip, and using a probe with small diameter can therefore increase the storage density remarkably [10]. Additionally, the vigorous development of phase-change random access memory (PCRAM) during last two decades has demonstrated the several merits of

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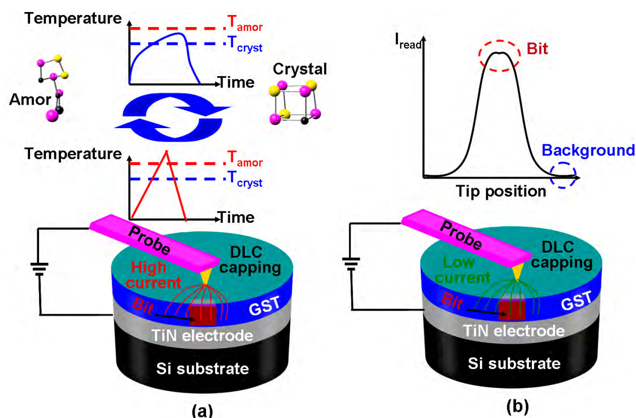

FIGURE 1. The schematic of phase-change electrical probe memory operated in (a) write mode, and (b) readout mode. The atomic structures of GST media in amorphous and crystalline phases, along with their reciprocal switching mechanisms, are depicted on top of (a), while the readout current with respect to the probe tip position is illustrated on top of (b).

phase-change materials (represented by $Ge_2Sb_2Te_5$, usually abbreviated as GST) including fast switching speed, low power consumption, and small feature size [11]–[13]. Thanks to this, phase-change probe memory that makes use of GST as the storage media has attained considerable attention from worldwide researchers, thus resulting in numerous fruitful achievements from both experimental and theoretical points of view [7]–[9], [14]–[16]. According to reported results, the write and readout performances of phase-change electrical probe memory were found to be strongly dependent of the geometrical and electro/thermal properties of the stacked layers, allowing for a design of an optimized media stack having a 10 nm GST layer sandwiched between a 2 nm diamond-like carbon (DLC) capping layer and a 40 nm titanium nitride (TiN) layer [15], [16]. It should be however noted that the interfaces of the stacked layers in previous work were assumed to be thoroughly smooth. This assumption is obviously contradictory to the practical observation owing to the existence of film surface roughness. The advent of surface roughness between adjacent stacked layers undoubtedly causes an incomplete layer contact and thus may strongly affect the current density and temperature distribution inside the storage layer, thereby bringing about adverse effects on phase-transformation kinetic. To address this omission, in this study we carried out detailed physically-realistic simulations of the write and readout operations of phase-change electrical probe memory by investigated the effect of surface roughness on the achievable phase-transformation extent and readout signals based on a sophisticated surface roughness model.

II. METHOD

Surface roughness shows the degree of unevenness of the film surface, thus playing an important role in determining the electrical/optical properties of the sample, particularly at adjacent layers interfaces.

As illustrated in Figure 2, the surface roughness of the DLC capping causes an insufficient contact between probe tip

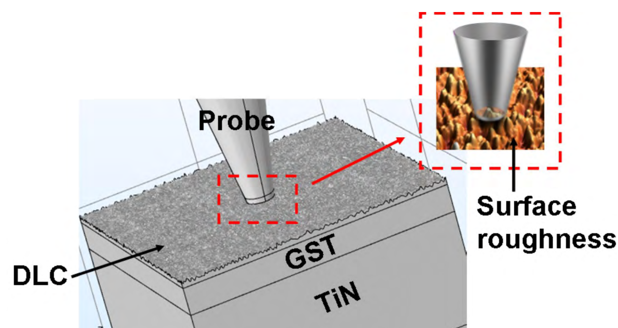

FIGURE 2. Schematic of surface roughness at probe-DLC capping interface.

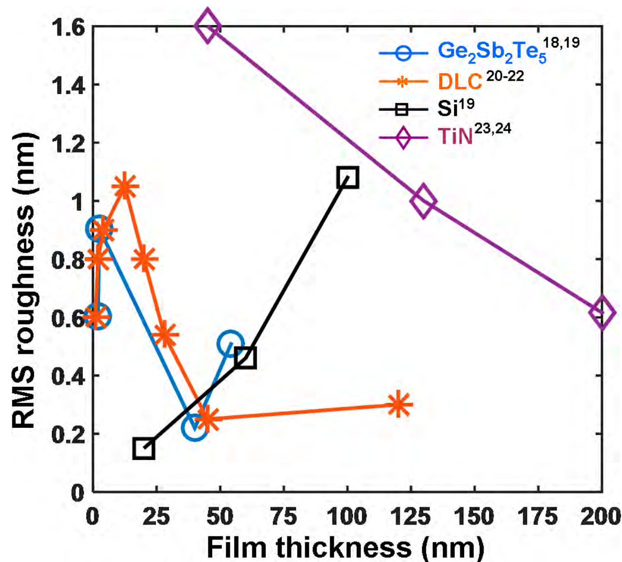

FIGURE 3. Measured rms roughness for different layers of phase-change electrical probe memory as a function of film thickness. Surface roughness of Si substrate does not correlate to its film thickness.

and DLC capping, rendering the write/readout current partly flow through the phase-change layer when compared with the smooth surface. This can significantly alter the electric field and temperature profiles inside the phase-change layer and affect the phase-transformation extent and the resulting readout signal. Prior to modeling the surface roughness impact, the values of surface roughness for different layers, usually denoted by root-mean-square (rms) that indicates an rms average distance of each grain hillock or pits deviating from a reference plane [17], needs to be carefully established, leading to Figure 3.

According to Figure 3, thin films employed for phase-change electrical probe memory exhibit various rms roughness, arising from several aspects such as media composition [25], film thickness [19], deposition techniques [21]–[24] and substrate temperature. In spite of these variations, the rms roughness for film thickness less than 200 nm (i.e. the maximum film thickness possibly adopted for phase-change electrical probe memory) ranges from 0.1 nm to 1.6 nm. As a result, rms roughness implemented in our model include both aforementioned experimentally

reported values and some arbitrarily chosen values to more comprehensively assess its influence on the write and readout performances of the phase-change electrical probe memory. The write model of phase-change electrical probe memory consists of the Laplace equation for the electrical process, the heat conduction equation for the thermal process, and the rate equation for the phase-transformation process respectively, giving rise to [10]:

$$\nabla \cdot (\sigma \cdot \nabla V) = 0, \quad (1)$$

$$\rho C_p \frac{\partial T}{\partial t} - k \cdot \nabla^2 T = \sigma |E|^2, \quad (2)$$

$$\frac{\partial \chi}{\partial t} = A_c (1-\chi)^n \exp(\frac{-E_c}{k_B T}), \quad (3)$$

where V is the electric potential, σ is the electrical conductivity, ρ is the density, C_p is the heat capacity, T is the temperature, k is the thermal conductivity, E is the electric field, χ is the crystal fraction, A_c is the pre-factor, n is the reaction order, E_c is the height of the energy barrier for crystallization, and k_B is the Boltzmann's constant. To simulate the crystallization process, eqns (1)-(3) are solved simultaneously to calculate the current density, temperature profile, and crystal extent inside the GST media, while the amorphization process is mimicked by solving eqns (1) and (2) simultaneously to provide the temperature and the cooling rate. The readout model comprises eqn (1) only that is solved to compute the current density as well as the readout current.

The advantageous storage capability of the GST media mainly arises from its well-known threshold switching behavior for which the amorphous GST with high resistance can be switched to a low resistance state once the applied voltage exceeds a so-called threshold voltage [26].To accurately mimic the threshold switching character, the electrical conduction of the amorphous GST is assumed to result from a combination of the transport of free carriers with 3D Poole-Frenkel emission of carriers from a two-center Coulomb potential, giving rise to [27]:

$$\sigma_{am} \approx \sigma_{LE} \cdot (E < E_t) + \sigma_{HE} \cdot (E \geq E_t), \quad (4)$$

where σ_{am} is the electrical conductivity of the amorphous GST, E is the electric field, Et is the critical electric field, defined by $\beta^2/(es)^2$ where β is the Pool-Frenkel constant, e is an electron volt, and s is the distance between the two coulombic centers, σ_{LE} and σ_{HE} are the electrical conductivity of the amorphous GST at low and high electric fields respectively, described by [28]:

$$\sigma_{LE} \approx \frac{2K\mu k_B T}{Es} \exp(\frac{-E_a}{k_B T}) \sinh(\frac{eEs}{2k_B T}), \quad (5)$$

$$\sigma_{HE} \approx K\mu e \frac{k_B T}{\beta E^{1/2}} (1 - \frac{k_B T}{\beta E^{1/2}}) \exp(-\frac{E_a - \beta E^{1/2} + \frac{\beta^2}{es}}{k_B T}), \quad (6)$$

where K is a pre-factor, $\mu = \mu_0 / \sqrt{1 + (\mu_0 E / v_{sat})^2}$ is the free carrier mobility with μ_0 as the low-field mobility and v_{sat} as the saturation velocity, E_a is the low-field temperature dependent activation energy, given by [28]:

$$E_a = E_{a_0} - \frac{aT^2}{b+T}, \quad (7)$$

where Ea_0, a, and b are constant values obtained from dedicated measurements in the ohmic regime. The electrical conductivity of the crystalline GST is assumed to be temperature-dependent only, defined by [16]:

$$\sigma_{cryst} \approx \sigma_{0cryst} \exp(-\frac{E_C}{k_B T}), \quad (8)$$

where σ_{0cryst} is a pre-factor, and E_c is the activation energy for crystallization. In this case, the electrical conductivity of the GST media during crystallization ($\sigma_{crystallization}$) and amorphization ($\sigma_{amorphization}$) simulations are modeled as:

$$\sigma_{crystallization} = \sigma_{cryst} \cdot \chi + \sigma_{am} \cdot (1-\chi), \quad (9)$$

$$\sigma_{amorphization} = \sigma_{am} \cdot condition\ 1 + \sigma_{cryst} \cdot condition\ 2, \quad (10)$$

where condition 1 = ($T > 620°C$)&($T_t < -37°C/ns$); condition 2 = ($T < 620°C$)||($T_t > -37°C/ns$); T_t is the cooling rate. The thermal conductivity of the GST media (K_{GST}) also depends on its structure and thus is depicted by:

$$K_{GST} = K_{cryst} \cdot \chi + K_{am} \cdot (1-\chi), \quad (11)$$

where K_{cryst} and K_{am} are thermal conductivities of crystalline and amorphous GST at room temperature respectively. During the simulations, the top of the probe was connected a write/readout pulse, and the bottom of the TiN electrode was maintained at ground potential. The temperature at both boundaries is set as room temperature. The surrounding boundaries of the media stack were realized with periodic boundary conditions to imitate the periodic structure. The calculations were performed using a commercial software package COMSOL MULTIPHYS^{TM} based on the finite-element method.

To create film surface roughness, a random number between 0 and 1 is generated through a random function with x and y coordinates as input arguments, whereby the product of this random number and a pre-defined rms value usually obtained from experimental measurements results in a surface roughness at specified position. Repeating such an operation over the whole surface (i.e., set x and y to cover the dimension of the entire surface) enables a roughness on the film surface everywhere. The height and the density of the created surface roughness can be easily adjusted by modifying the values of the pre-define rms constant and the maximum number of knots. The resulting surface roughness with different height and densities is schematically shown in Figure 4.

According to Figure 4, it is possible to create a thin film with any desired surface conditions by appropriately tailoring the modeling parameters. As a result, such a roughness modeling strategy is consolidated with the aforementioned write/read model to assess its influence on the write and readout performances of phase-change electrical probe memory, as detailed below.

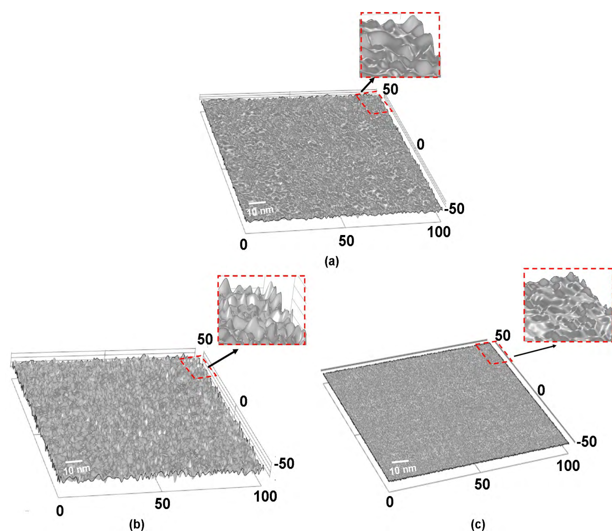

FIGURE 4. Simulated surface with a rms value of (a) 0.7 nm, (b) 1.7 nm, and (c) 0.7 nm with denser roughness.

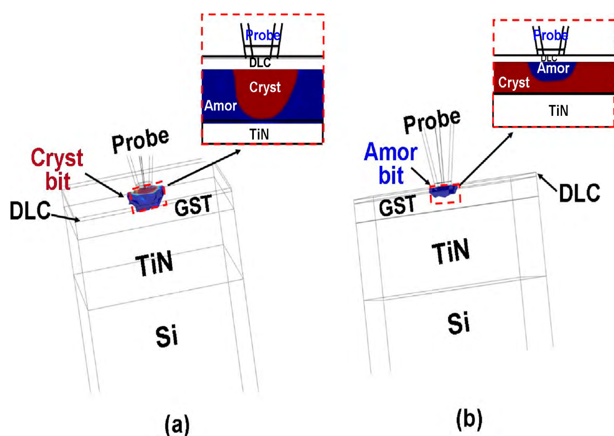

FIGURE 5. The formed (a) crystalline bit and (b) amorphous bit resulting from the proposed optimized media stack. The cross-sectional view of the resulting bits is displayed in insets.

III. RESULTS

The resulting crystalline and amorphous bits, obtained from the aforementioned electro-thermal and phase-change model based on the optimized media stack mentioned in section 1, is schematically shown in Figure 5.

Note that the crystallization pulse was chosen to be a 4 V of 200 ns (50 ns rise, 100 ns plateau, and 50 ns trailing), whereas the amorphization pulse is adjusted to be a 5 V of 170 ns (50 ns rise, 100 ns plateau, and 20 ns trailing) in order to achieved the desired temperature and the cooling rate. The silicon dioxide (SiO_2) encapsulated Si probe with platinum silicide (PtSi) at tip apex was implemented to reduce the energy consumption per bit, simultaneously alleviating the tip wear. Due to the resulting temperature profile, the formed crystalline bit exhibits a cylindrical shape that extends through the entire GST layer, while the amorphous bit has an approximately semi-elliptical shape located on top portion of the GST layer. Both cases lead to noticeable readout signals that can readily distinguish the written bits from surrounding background. However, such optimized outcomes arise from an assumption that simulated media stacks have thoroughly smooth surfaces, which is obviously contradictory to the experimental observations. Therefore, surface roughness is introduced into each layer of the media stack that includes Si substrate, TiN electrode, GST layer, and DLC capping, and thus to re-assess their respective role on the write performances of the probe memory device, elucidated in the following sections.

A. SURFACE ROUGHNESS OF SI SUBSTRATE AND TiN ELECTRODE

Si layer in phase-change electrical probe memory is usually performed as a wafer on which other functional films are deposited. As a result, it plays a minor role on determining the write/read performances of the probe device. To prove this, Si substrate with rms varying from 0 nm to 1.7 nm (arbitrarily chosen value) was introduced into the previous model, resulting in unnoticeable difference on induced temperature and readout signals. Additionally, the maximum temperature inside Si substrate seems to be independent of its surface roughness, and constantly remains at 20 °C. This is because its large thermal conductivity makes Si as a heat sink and varying the surface roughness can barely affect its internal temperature [29].

TiN layer that acts as a bottom electrode obviously plays a more important role for write and readout operations of the probe device than Si substrate. Therefore, influence of the surface roughness of TiN layer on phase-change kinetics and readout signals cannot be underestimated. To assess this, the maximum temperature at the bottom of the GST layer (directly underneath the tip, denoted as T_{max}) as well as the maximum write current (I_{max}) during the pulse period were measured according to different rms and roughness densities for both crystallization and amorphization processes, giving rise to Figure 6. Note that for density definition, the number of knot for the least density, intermediate density, and the most density, are set to be 10, 100, and 300, respectively.

Figure 6(a) clearly indicated that for a given roughness density, a larger TiN rms can slightly decrease the measured T_{max} and I_{max} during the crystallization process. This is likely due to a fact that a larger rms equivalently increases its layer thickness. Therefore, heat dissipation effect through the TiN bottom is more pronounced due to the large thermal conductivity of the TiN media (~12 $Wm^{-1}K^{-1}$) [30], thus causing a lower T_{max}. Such a TiN layer with increased thickness also enhances the entire device resistance and consequently reduces the write current with larger rms value. In spite of these variations, no remarkable decrements of T_{max} and I_{max} were observed when varying rms values from 0 nm to 3 nm, as for a TiN layer with an intermediately dense surface, T_{max} and I_{max} changes from 108 °C and 15.6 μA to 93 °C and 15.45 μA, respectively. This may be ascribed to the ultra-high electrical conductivity of the TiN media that offsets the influence of the increased thickness on device resistance, and therefore suppresses sharp changes of T_{max} and I_{max} for

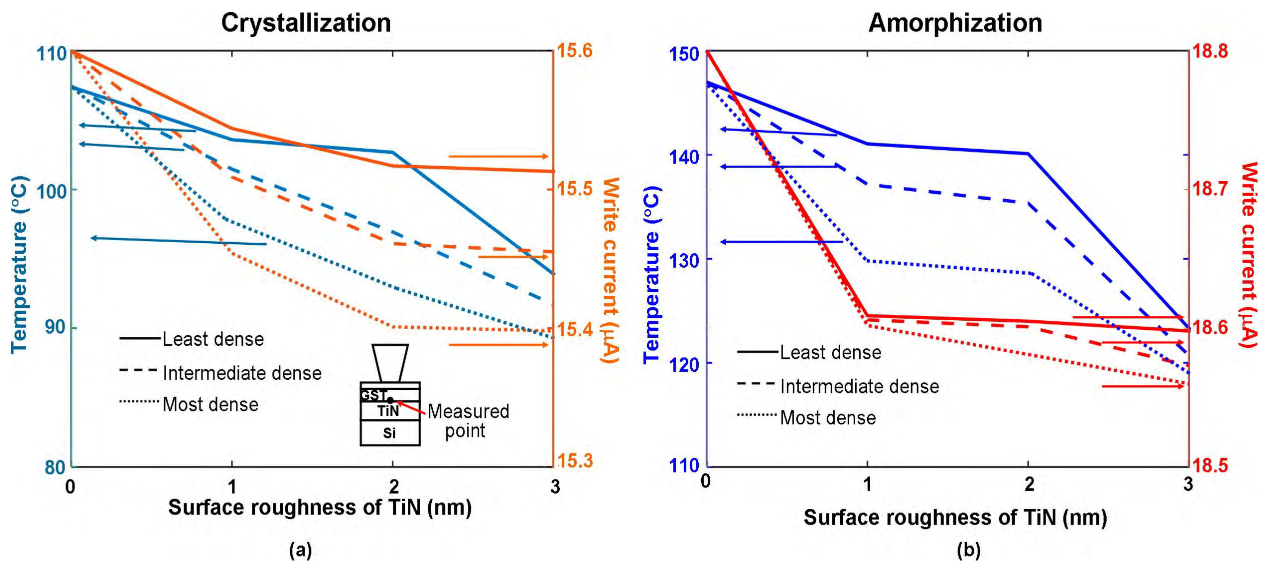

FIGURE 6. T_{max} **and** I_{max} **as a function of the TiN layer surface roughness for (a) crystallization and (b) amorphization processes. The surfaces of other layers are considered as completely smooth.**

different rms. It was also found that for a constant rms, a TiN layer with less dense roughness results in higher T_{max} and I_{max} than that with more dense roughness. This is probably because the increase of roughness density severely impairs the film smoothness at GST-TiN interface and thus increases the contact resistance, causing larger device resistance. As a result, I_{max} is decreased and this consequently reduces the generated Joule heating and lowers T_{max}. Due to the ultra-high electrical conductivity of TiN media, the decrement of T_{max} and I_{max} with respect to roughness density still remains low as they change from 105 °C and 15.53 μA to 98 °C and 15.45 μA for 1 nm rms. The dependence of T_{max} and I_{max} on TiN surface roughness for amorphization process (shown in Figure 6(b)) was analogous to crystallization case, as T_{max} and I_{max} were reduced by increasing either the rms value or roughness density. However, the calculated T_{max} and I_{max} during amorphization process for different rms and roughness density were higher than those for crystallization process, as they vary from 148 °C and 18.8 μA to 126 °C and 18.6 μA with rms ranging from 0 nm to 3 nm (the lease dense case), and from 125 °C and 18.6 μA to 120 °C to 18.57 μA between the lease dense and the most dense roughness (3 nm rms case). This can be readily owed to the higher electric pulse adopted for amorphization process.

In addition to write performance, the impact of TiN surface roughness on readout performance of phase-change electrical probe memory was also assessed according to readout current variations with respect to rms and roughness density, as shown in Figure 7. As can be seen from Figure 7, increasing rms results in a diminishing readout current for both readout configurations for a given surface roughness. This is expected as the presence of surface roughness equivalently increases the TiN layer thickness and thus reduces the readout current. As TiN layer plays a minor role in determining the entire device resistance, the readout current only varies from

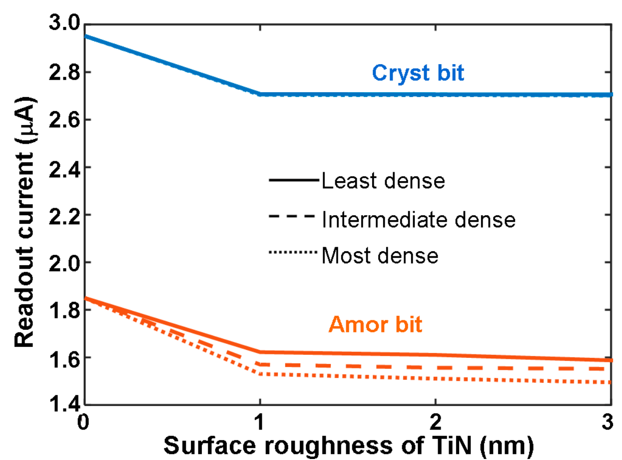

FIGURE 7. Readout current as a function of the TiN roughness rms and density for reading crystalline and amorphous bits from amorphous and crystalline background, respectively. The surfaces of other layers are considered as completely smooth.

2.95 μA to 2.8 μA for reading crystalline bit and from 1.8 μA to 1.6 μA for reading amorphous bit, respectively, for rms changing from 0 nm to 3 nm (the most dense case). On the other hand, the readout current experiences a slight decrease by increasing the roughness density. This may arise from a fact that the TiN surface with larger density generates more roughness at GST-TiN interface, and therefore brings about a more resistive surface. However, as the TiN media exhibits extremely low resistance, its influence on resulting readout current can be ignored.

B. SURFACE ROUGHNESS OF THE GST LAYER

The most critical component of phase-change probe memory is undoubtedly the GST film where phase transformation occurs. In this case, surface roughness of the GST layer may

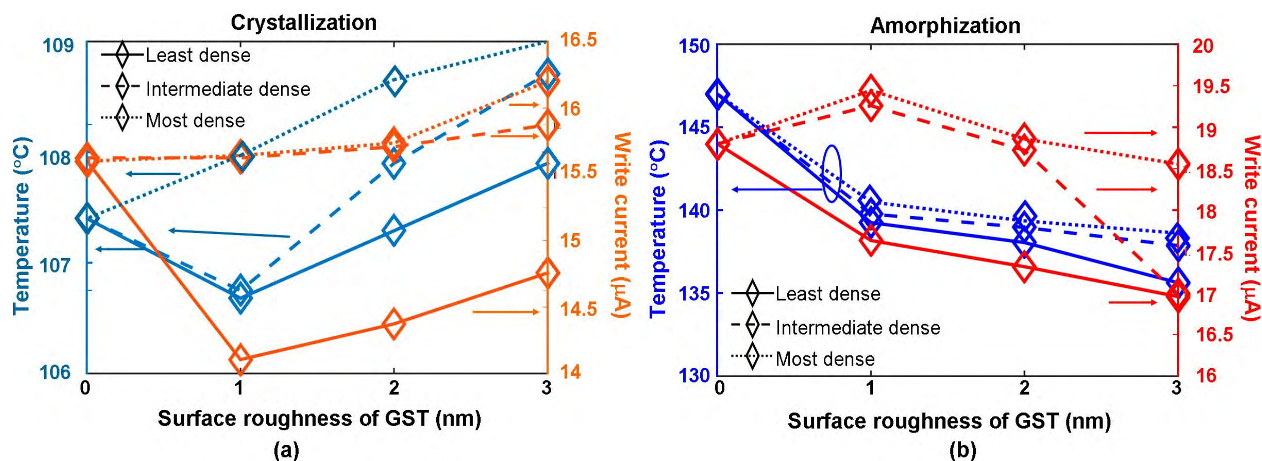

FIGURE 8. T_{max} **and** I_{max} **as a function of the GST layer surface roughness for (a) crystallization and (b) amorphization processes. The surfaces of other layers are considered as completely smooth.**

more pertain to the physical performances of entire device compared with Si substrate and TiN electrode. To demonstrate this, T_{max} and I_{max} as a function of rms and roughness density of the GST surface were calculated for both crystallization and amorphization processes, resulting in Figure 8.

According to Figure 8(a), for GST surfaces with the least dense and the intermediately dense roughness, T_{max} initially decreases when rms increases from 0 nm to 1 nm, and subsequently undergoes a gradual increase when rms continuously rises to 3 nm. Obviously the initial decrease on T_{max} from 0 nm to 1 nm is likely caused by the advent of surface roughness that increases the entire device resistance and thus reduces the generated joule heating. However, continuously increasing rms equivalently thickens the GST layer thickness, rendering the recorded bit further away from TiN electrode and Si substrate. As a result, heat diffusion through TiN electrode was somewhat circumvented by the thicker GST layer, thus slightly rising T_{max}. The TiN surface with the densest roughness evidently makes roughness repeated more frequently than two previous cases, and can more effectively suppress the heat diffusion effect. Therefore, T_{max} undergoes a slow increase with rms changing from 0 nm to 3 nm. I_{max} almost follows the magnitude-varying trend of T_{max} for roughness with different densities, which can be explained by aforementioned reasons. For a given rms, the denser roughness was found to exhibit larger T_{max} and I_{max} than the less dense roughness. This is because the advent of denser roughness makes DLC capping in contact with GST media more frequently, and thus lowers the resulting contact resistance, giving rise to larger I_{max} and T_{max}.

The effect of GST roughness on the write of amorphous bit is shown in Figure 8(b). Differing from Figure 8(a), T_{max} is actually decreased by increasing rms from 0 nm to 3 nm for a given roughness density. According to aforementioned speculations, rougher surface equivalently thicken the GST layer and effectively attenuates the joule heating escaping through the bottom electrode. However, thicker GST layer also implies a larger device resistance and this definitely

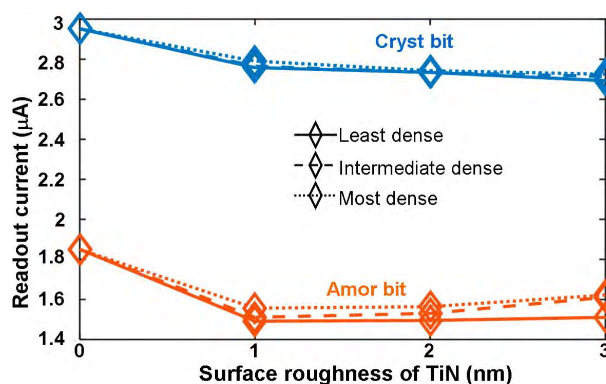

FIGURE 9. Readout current as a function of the GST roughness rms and density for reading crystalline and amorphous bits from amorphous and crystalline background, respectively. The surfaces of other layers are considered as completely smooth.

reduces I_{max}, which is reflected in Figure 8(b). The reduction on I_{max} clearly lowers joule heating and T_{max}. Hence, it seems that the decrease of I_{max} plays a more critical role in determining T_{max} than the impact of heat diffusion, thereby causing a continuous decrease on T_{max}. Similar to crystallization case, implementing denser roughness enables larger T_{max} and I_{max} for a given rms. Despite these variations, the influence of the GST roughness on I_{max} and T_{max} remains weak, as the maximal increment of I_{max} and T_{max} are 2 μA and 2.5° C for crystallization, and 2.5 μA and 8 °C for amorphization, respectively. The GST media presents a fairly high electrical conductivity (particularly for crystalline phase) [31], which attenuates its impact on entire device resistance and the resulting I_{max}. Additionally, due to its low thermal conductivity, the generated joule heating cannot easily diffuse through the bottom electrode, and hence maintain T_{max} at constant point [32].

Similar to the TiN case, the read of previously written bits inside surrounding background is also investigated for different rms and roughness densities of GST surface, as depicted in Figure 9. It is indicated in Figure 9 that the GST layer

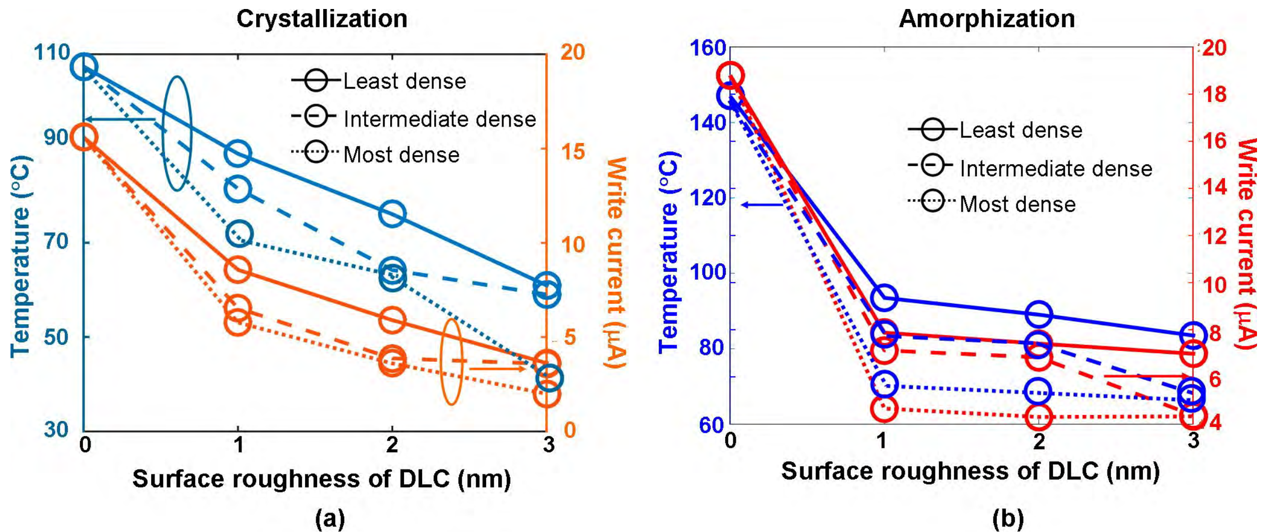

FIGURE 10. Tmax and Imax as a function of the DLC layer surface roughness for (a) crystallization and (b) amorphization processes. Other layer surfaces (i.e., GST, TiN, and Si) are considered completely smooth.

with larger rms slightly reduces the readout current due to the equivalently larger thickness which enhances the entire device resistance. For a given rms, using GST layer with denser roughness results in a gradual increase on readout currents for both configurations. This can be ascribed to a hypothesis that the GST roughness with larger density actually keeps DLC capping more frequently in contact with the GST media, and this makes the GST surface more resemble the originally smooth interface than that with smaller density. Due to the weak contribution to the entire resistance, only negligible variation of I_{max} and T_{max} arising from the GST roughness is observed.

C. SURFACE ROUGHNESS OF THE DLC LAYER

DLC capping layer is the sole component of phase-change electrical probe memory that has a direct contact with the probe tip where the write/read current is applied. Therefore, the surface roughness of DLC capping may contribute to the contact resistance at tip-DLC interface dramatically and has a non-negligible effect on the resulting temperature and write/read signals inside device. To testify this speculation, T_{max} and I_{max} were first calculated with respect to various rms and roughness densities of the DLC layer, giving rise to Figure 10.

According to comparisons among Figures 8(a), 9(a) and 10(a), DLC surface roughness undoubtedly brings about far stronger effect on T_{max} and I_{max} than TiN electrode and Si substrate, as T_{max} and I_{max} change from 108 °C and 15.6 μA to 46 °C and 2 μA, respectively, when rms and roughness density of DLC surface are set from 0 nm and 'least dense' to 3 nm and 'most dense', respectively. Due to the existence of surface roughness, the bottom of probe tip cannot entirely contact with the DLC surface, which causes large contact resistance at tip-DLC interface, and substantially reduces I_{max}. The decreased current generates smaller joule heating and further lowers T_{max}. Similar to previous cases, larger rms results in a lower T_{max} and I_{max} for a given density. However, varying rms of DLC roughness leads to more pronounced T_{max} and I_{max} decrements than rms of TiN electrode and Si substrate. For instance, increasing rms of DLC surface with the intermediate roughness from 0 nm to 3 nm reduces T_{max} and I_{max} from 108 °C and 15.6 μA to 59 °C and 3.6 μA, respectively. This is because the entire device resistance is majorly dominated by the DLC capping because of its fairly high resistivity and thin thickness. As a consequence, rising rms that equivalently thickens the layer thickness in fact makes the whole device more resistive, and therefore degrades T_{max} and I_{max}. Another key observation is that for a given rms, increasing DLC roughness density exhibits noticeable reduction on T_{max} and I_{max} compared with TiN and Si cases. Obviously the presence of larger roughness density yields more points contact at tip-DLC interface than surfaces contact, and thus rises up the contact resistance, which inversely decreases T_{max} and I_{max}.

The influence of DLC surface roughness on T_{max} and I_{max} during amorphization process is analogous to crystallization case. Increasing rms and density of DLC roughness from 0 nm and 'least dense' to 3 nm and 'most dense' alters T_{max} and I_{max} from 147° C and 18.8 μA to 65 °C and 4.32 μA, respectively. Additionally, T_{max} and I_{max} are both reduced by increasing either rms or roughness density. Reasons for these are similar to aforementioned crystallization cases and thus not repeated here. However, more eminent T_{max} and I_{max} decrements during amorphization are found than its crystallization counterpart, particularly when rms values vary from 0 nm and 1 nm, probably ascribed to the higher pulse magnitude required for amorphization.

Figure 11 shows readout currents as a function of rms and roughness densities of the DLC layer for both configurations. As clearly illustrated in Figure 11, readout current initially

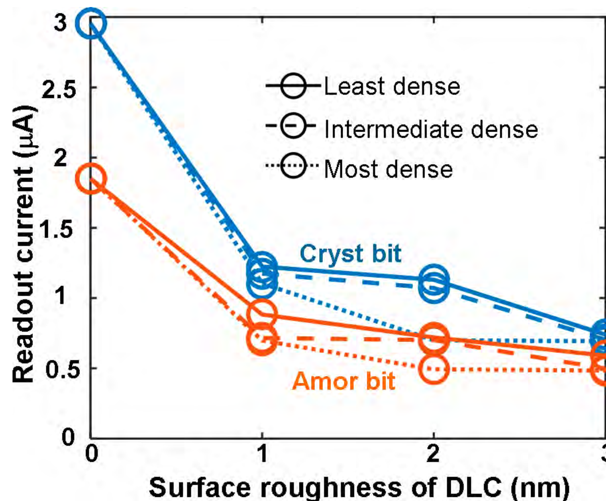

FIGURE 11. Readout current as a function of the DLC roughness rms and density for reading crystalline and amorphous bits from amorphous and crystalline background, respectively. Other layer surfaces (i.e., GST, TiN, and Si) are considered completely smooth.

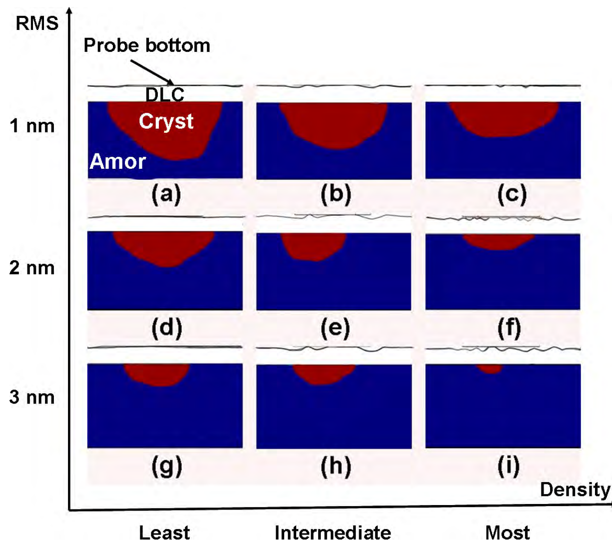

FIGURE 12. Resulting crystalline bits with respect to different roughness rms and densities. Other layer surfaces (i.e., GST, TiN, and Si) are considered completely smooth.

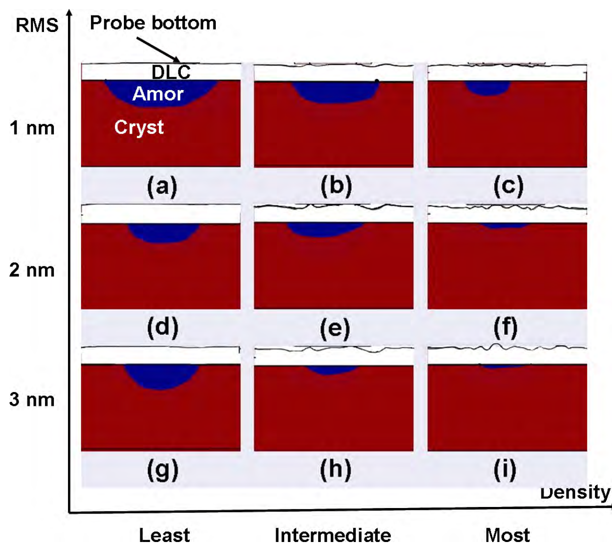

FIGURE 13. Resulting crystalline bits with respect to different roughness rms and densities. Other layer surfaces (i.e., GST, TiN, and Si) are considered completely smooth.

undergoes a sharp decline when increasing rms from 0 nm to 1 nm, subsequently followed by a diminishing variation for rms > 1 nm. Similar to the write operation, DLC surface roughness destroys the smoothness of the tip-DLC interface where large contact resistance is therefore introduced. This turns out to reduce the readout current from 2.95 μA and 1.85 μA to 0.73 μA and 0.59 μA for reading crystalline and amorphous bits, respectively (for the case of 1 nm rms with the most dense roughness). Continuous increase on rms further moves probe tip away from the readout bit and consequently diminishes the readout current. Moreover, using a DLC surface with larger dense roughness also causes a reduction on the resulting readout current due to the advent of more resistive tip-DLC interface. Nevertheless, no pronounced changes on readout currents with respect to rms and roughness density are observed particularly when DLC rms is > 1 nm. This may be attributed to the limited influence of DLC rms on entire device resistance.

IV. DISCUSSIONS

According to results presented so far, surface roughness of phase-change media stack confines the conductive region where write/readout current can flow at layer interfaces, and thus affects the resulting I_{max}, T_{max}, and readout current differently, depending on the layer position. Within these layers, DLC capping that bridges probe tip with GST layer dominates the device resistance and its surface roughness therefore has a stronger impact on aforementioned parameters than other layers. To demonstrate this, the influences of rms and roughness densities of DLC surface on resulting crystalline and amorphous bits are revealed in Figures 12 and 13, respectively.

It was indicated in Figure 12 that depth of the crystalline bits diminishes by increasing either the rms or roughness density, as it varies from 6 nm with 1 nm rms and the smallest density, to 0.1 nm with 3 nm rms and the largest density. It is evident that entire device resistance rises up because of the increase on either rms or roughness density. This undoubtedly reduces the temperature inside the GST media and the resulting write current, as also reported in section 3.3. In this case, the GST layer cannot be heated sufficiently especially for its bottom area, thus preventing the formed bit from extending through the entire thickness. The similar dependence on DLC surface roughness was also noticed during the write of amorphous bits, as the amorphous bit depth changes from 3 nm with 1 nm rms and the smallest density, to 0.5 nm with 3 nm rms and the largest density. Although surface roughness of DLC capping are significantly pertinent to write performances of probe device, surface

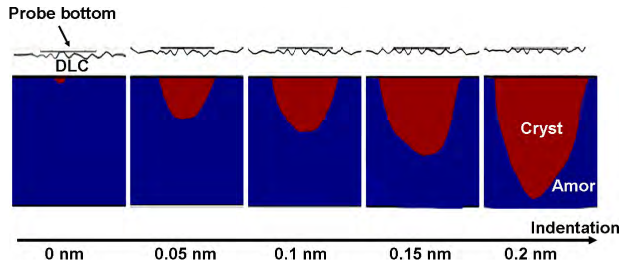

FIGURE 14. Resulting crystalline bits with respect to probe indentation distances. The DLC surface is assumed to have 3 nm rms with the densest roughness, while other layer surfaces (i.e., GST, TiN, and Si) are considered completely smooth.

properties of other layers (e.g., GST media, TiN electrode, and Si substrate) can barely affect the depth of the written bits. This is mainly because varying surface properties of these layers has a very weak effect on device resistance, which thus yields comparable temperature and write current to smooth surface cases.

As shown in Figures 12 and 13, presence of surface roughness makes the written bits either in crystalline or amorphous phases embedded inside the GST layer other than extending through the whole thickness. Due to the remarkable resistivity contrast between amorphous and crystalline phases, it is possible to distinguish embedded amorphous bits (low read current) from its surrounding crystalline matrix (high read current). However, the amorphous region under embedded crystalline bits significantly increases the device resistance and therefore makes embedded crystalline bits (low read current) unreadable from surrounding amorphous background (low read current) [33]. As a result, the written crystalline bit is required to extend through the whole GST thickness even if the layer surface is not completely smooth. A possible paradigm to realize this is to make probe tip partly penetrate through the DLC capping, which equivalently reduces the distance between probe and GST media and thus generates more joule heating for a given write pulse. However, probe penetration obviously requires strong external force applied to probe, likely deteriorating the tip wear [34]. To achieve successful readout operation while alleviating tip wear, the formed crystalline bit size is re-assessed according to indentations of probe tip into the DLC capping (indentations imply different probe force), giving rise to Figure 14. As clearly illustrated in Figure 14, increasing probe indentation into DLC capping from 0 nm to 0.2 nm extends the resulting bit depth from 0.1 nm to 10 nm (i.e., full GST thickness), respectively. In this case, only a slight indentation can ensure formation of a crystalline bit that extends through the whole GST layer, thus simultaneously providing for a good readout signal and a superb anti-wear characteristic.

V. CONCLUSIONS

Surface roughness of layered components of phase-change electrical probe memory was mimic here and their influence on write and readout performances of probe memory device were assessed. It was found that due to their weak impact on device resistance, surface roughness of Si substrate, TiN electrode and GST layer hardly affects the resulting temperature, write/read current and the formed bit depth. However, surface roughness of DLC capping layer that dominates the entire device resistance strongly pertains to electro-thermal properties and phase-transformation extent of the GST media. The temperature and write/read current diminish by using a DLC layer with larger rms and denser roughness, thus causing formed bits embedded inside the active layer for both crystallization and amorphization processes. To mitigate readout signals as well as tip wear, probe is required to slightly penetrate into DLC capping by $\sim$ 0.2 nm (for DLC roughness with 3 nm rms and the largest density).

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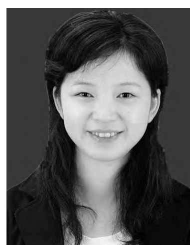

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