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A Fully-Integrated Optoelectronic Detector With High Gain Bandwidth Product

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ABSTRACT An optoelectronic circuit integrated with a photodiode is proposed, which simultaneously achieves 3.5-MΩ transimpedance gain and 18-MHz bandwidth. The design is intended to address the limits on bandwidth introduced by the large parasitic capacitance of the integrated photodiodes in optoelectronic applications. The proposed circuit consists of a transimpedance amplifier (TIA) and a voltage gain stage. The pre-stage TIA with low input impedance provides the main transimpedance gain of the circuit over a wide bandwidth. The post voltage gain stage provides the supplemental voltage gain for the circuit and increases its driving capability. The circuit is fabricated in a 0.5-μm CMOS process with an active area of 501.2 μm $\times$ 291.6 μm. When the light input is a 100-ns pulse with 905-nm wavelength and 1.5-μW optical power, the amplitude of output signal is 1.6 V with a rise time of 24.5 ns and a delay time of 21 ns.

INDEX TERMS Fully-integrated optoelectronic detector, high-bandwidth, high-gain, transimpedance amplifier.

I. INTRODUCTION

Optoelectronic integrated circuits (OEIC) consists of optoelectronic devices and microelectronic devices fabricated on a single chip to achieve specific functions. With the development of information technology and the continuing growth in the applications of fiber optic networks, an increasing demand for OEICs can be witnessed.

The conventional high-speed optoelectronic detector includes a photodiode (PD) and a micro-current sensing circuit. The PD receives an optical signal to output a proportional current signal, and the micro-current sensing circuit performs the current-to-voltage conversion subsequently [1]–[4]. The important specifications of the micro-current sensing circuit include gain-bandwidth, input current noise and power dissipation.

The parasitic capacitance of PD is the main limitation of system bandwidth. Several circuit techniques have been developed to relax the input parasitic effects [5]–[14]. Common-base input configuration and common-gate input configuration are simple and effective methods to lower input impedance [5]–[7]. However, the poor device characteristic such as small g_m cannot completely isolate the parasitic capacitance. Therefore, regulated cascode (RGC) input configuration is developed to further lower the input impedance [8]–[10]. The RGC configuration can alleviate bandwidth reduction better than common-base configuration, but the added components directly at the input deteriorate sensitivity and noise performance. Besides lowering input impedance, the negative capacitance technique [11], [12], under-Damped TIA [13], and area efficient inverter [14] are also used to extend the bandwidth.

The noise performance limits the input range of the micro-current sensing circuit. For multi-stage amplifiers, the gain of the first voltage amplifier stage needs to be made large to get a low integrated noise [15], [16]. In addition, several other circuit techniques are implemented for better noise performance. The Darlington input is used for high gain and a low input noise current [17]. The series inductor can lead to noise reduction at the cost of consumed die area [18]. Compared to resistive feedback, capacitive feedback can be used to minimize the noise, but it requires an input DC current removal block to prevent the TIA from saturating [19], [20].

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Since integrated PDs have advantages in miniaturization and convenience, fully-integrated OEIC is preferred in actual applications. Although integrated PDs have more simplified system interconnection than that of discrete ones, their larger parasitic capacitance and lower spectral responsivity cannot be handled by the existing current sensing circuit techniques designed for discrete PDs. In order to solve the problems, this paper presents an optoelectronic circuit customizing the integrated PDs. Low input impedance and high voltage gain allow the proposed circuit with an integrated PD to be applied in high gain-bandwidth product application.

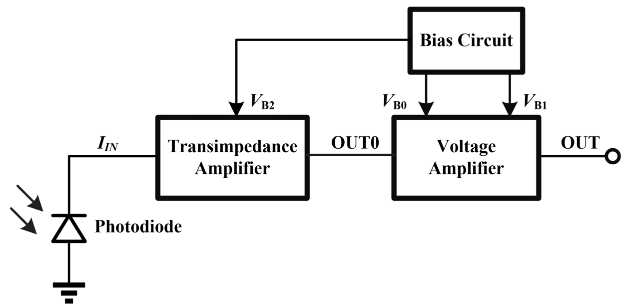


FIGURE 1. Block diagram of the proposed circuit.

Figure 1 displays the building blocks of proposed optoelectronic circuit, which includes a transimpedance amplifier (TIA), a voltage amplifier and a bias circuit. The PD generates the current signal IIN and the pre-stage TIA converts IIN into a voltage signal OUT0. The following voltage amplifier provides supplemental voltage gain and increases the drive capability. VB0, VB1 and VB2 are the bias voltages.

II. PROPOSED OPTOELECTRONIC CIRCUIT

A. STRUCTURE OF PROPOSED TIA

The detailed schematic of proposed TIA is shown in Figure 2, which is a multi-stage amplifier cascaded by common source and source follower. Considering the common source with a source follower as a unit, the amplifier can be divided into three units. The first unit includes M_1, M_2, R_1, R_2, the second unit contains M_3, M_4, R_3, R_4, and the third unit includes M_5, M_6, MP_0, R_6. The resistance R_{F1} constitutes an internal feedback network. R_{F2}, R_{F3} and C_{F1} form an external feedback network. In order to ensure the matching of these units, their parameters need to be the same, and the feedback ensures them to operate at the same quiescent point.

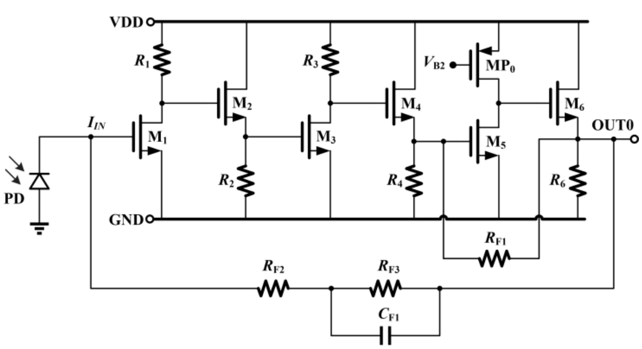


FIGURE 2. Schematic of the proposed TIA.

Since the gain and bandwidth are mutually restricted, the large transimpedance gain cannot be realized directly by crossing a large resistor at the input and output terminals. Therefore, the transimpedance gain in the circuit is divided into two parts: the first part is from the TIA, and the second part is from the post voltage amplifier.

According to the structure in Figure 2, the low frequency transimpedance gain of the first part is given by $A_1 = R_{F2} + R_{F3}$, which shows that the transimpedance gain of the TIA is proportional to (R_{F2}+ R_{F3}).

Since the parasitic capacitance of the PD is very large, the main pole of the feedback loop is located at the gate of M_1, and the frequency of the pole is determined by the parasitic capacitance of PD and the impedance across the input and output of TIA. The DC loop gain of the TIA can be written as:

$$LG = g_{m1}g_{m3}\,(R_1||r_{M1})\,(R_3||r_{M3})\,g_{m4}R_{\mathrm{F1}} \tag{1}$$

where g_{m1}, g_{m3}, and g_{m4} are the small-signal transconductance of M_1, M_3 and M_4, respectively. r_{M3} and r_{M4} are the output resistance of M_3 and M_4. The main pole locates at:

$$f_{p1} = 1/[2\pi(R_{F2} + R_{F3})C_{PD}] \tag{2}$$

where C_{PD} is the parasitic capacitance of integrated PD.

Assuming that there is only one pole at the input of TIA feedback loop, the closed-loop −3dB bandwidth of TIA depends on the parasitic capacitance of the PD and the equivalent input impedance at the input node, which can be expressed as:

$$Z_{IN} = (R_{F2} + R_{F3})/(1 + LG) \tag{3}$$

$$f_{-3dB} = 1/(2\pi Z_{IN} C_{PD}) \tag{4}$$

Equation (3) and (4) indicate that the bandwidth is inversely proportional to ($R_{F2} + R_{F3}$). Therefore, there is a constraint between the gain and the bandwidth of the TIA, which can be overcome by increasing loop gain. But the requirements of high gain often result in additional low frequency pole effects, which will worsen the stability of feedback loop, especially at high frequencies.

The poles exist at every stage of the TIA. Due to the low output impedance of M_2 and M_4 in common drain stages and the relatively low load resistance R_1 and R_3 in the common source stages, the corresponding pole frequency is high and their effect on the feedback loop can be ignored. For the high gain requirements of the common source, the poles of the common source stages have an impact on the loop, which prevents the amplifier from achieving a wider bandwidth.

For the purpose of broadening bandwidth, an additional feedback loop is built between the gate of M_5 and the source of M_6 through the resistor R_{F1} to get a proper pole frequency. At the same time, the impedance at the output node OUT0 is further reduced due to the introduction of the internal feedback resistor R_{F1}. This causes the pole at OUT0 to be pushed to a higher frequency, increases the drive capability of the TIA, and reduces the impact of the post-stage.

In conventional TIAs, the compensation capacitor is connected between the input and the output. Although the loop stability can be improved, rise time of the output signal cannot be reduced. When the output signal rises, it contains a large number of high-frequency components, which will reduce the equivalent transimpedance. In order to improve the transimpedance gain, the transimpedance is divided into R_{F2} and R_{F3} with compensation capacitor C_{F1}. The total transimpedance gain is:

$$A1 = RF2 + RF3/(1 + sRF3CF1) \tag{5}$$

By adjusting R_{F2}, R_{F3} and C_{F1}, there will be a high speed channel from the input terminal I_{IN} to the output terminal OUT0. It can also ensure enough transimpedance gain under the high-frequency components at the rise edge of the output signals, so it can speed up the rising of the output signal.

The complete TIA loop gain function can be expressed as:

$$LG(s) \approx \frac{1 + sC_{F1}R_{F3}}{(1 + sC_{PD}R_{F3})(1 + sC_{F1}R_{F2})} A(s) \tag{6}$$

where $A(s)$ is the transfer function of the amplifier in TIA, and the approximation is based on the assumption that $C_{PD} \gg C_{F1}$ and $R_{F2} \gg R_{F3}$. The poles of $A(s)$ are pushed to high frequency by R_{F1}. From (6), the poles and zero point can be written as:

$$\omega_{P1} = 1/C_{PD}R_{F3} \tag{7}$$

$$\omega_{P2} = 1/C_{F1}R_{F2} \tag{8}$$

$$\omega_{Z1} = 1/C_{F1}R_{F3} \tag{9}$$

The dominant pole ω_{P1} is located at a relatively low frequency, while ω_{P2} and ω_{Z1} are located at much higher frequencies. The pre-TIA can be recognized as a stable system.

B. ANALYSIS OF VOLTAGE AMPLIFIER

The post-stage voltage amplifier is attached after the TIA. The primary function of the voltage amplifier is to amplify the output signal of the TIA to appropriate amplitude and provide enough load capacity for the entire circuit.

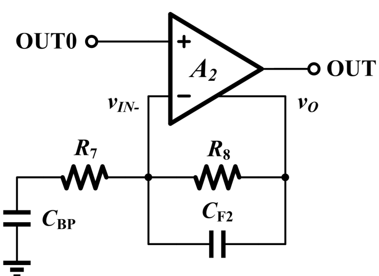


FIGURE 3. Topology of voltage amplifier.

Figure 3 shows the topology of the voltage amplifier. In order to ensure that the output voltage is positive, the voltage amplifier is a non-inverting amplifier. The architecture of operational amplifier is shown in Figure 4. As the input

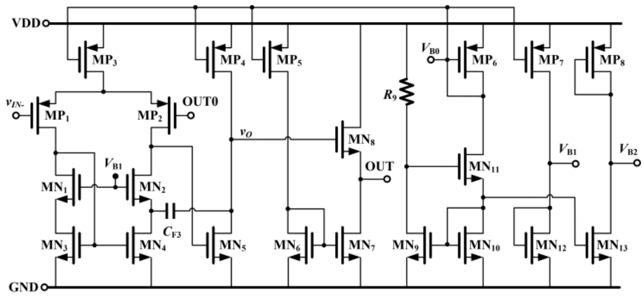


FIGURE 4. Schematic of the voltage amplifier and the bias circuit.

and output quiescent voltage of the whole circuit is very low, the input voltage of the voltage amplifier is about 1.2 V. In order to make all the transistors work in the saturation region, the PMOS transistor is selected as the differential input for the input stage.

MN_1, MN_2, MN_3 and MN_4 form a low-voltage cascode current mirror that accurately mirrors the current and converts the differential double-ended output into a single-ended output. At the same time, the low-voltage cascode current mirror provides a greater output resistance and output dynamic range. The second stage of the voltage amplifier uses the common source structure as the gain stage, and the third stage utilizes source follower to improve the driving capability. The voltage gain can be expressed as:

$$A_2(s) = 1 + \frac{sC_{BP}R_8}{(sC_{BP}R_7 + 1)(sC_{F2}R_8 + 1)} \tag{10}$$

Since the DC voltage of the voltage amplifier input in Figure 4 is determined by the TIA's output, a DC blocking capacitor C_{BP} is added between R_7 and ground to compromise quiescent operating point and AC gain. The capacitors C_{F2} and C_{F3} are frequency compensation capacitors, which can ensure loop stability.

C. ANALYSIS OF NOISE

The noise of proposed optoelectronic circuit comes mainly from the PD, feedback resistors of TIA, and internal amplifier of TIA.

The output noise is related to the amplifier gain. The multistage amplifier noise figure can be written as:

$$N_{F1\sim n} = N_{F1} + \frac{N_{F2} - 1}{G_1} + \frac{N_{F3} - 1}{G_1G_2} + \frac{N_{F4} - 1}{G_1G_2G_3} + \ldots + \frac{N_{Fn} - 1}{G_1G_2G_3 \ldots G_{(n-1)}} \tag{11}$$

where N_{Fx} is the noise figure for the x-th amplifier and G_x is the gain for the x-th amplifier.

It can be concluded that the total noise figure of a multistage amplifier depends mainly on the noise figure of the first stage and the subsequent stages have less effect on the overall noise figure. For the pre-TIA, the noise figure should be as small as possible and the gain should be as large as possible. Therefore, the pre-transimpedance gain assigned in the design is $A_1 = 280$ kΩ, and the post-amplifier voltage gain

$A_2 = 12.5$. This arrangement is to ensure the overall gain of the current sensing circuit, but also to meet the requirements of reducing noise.

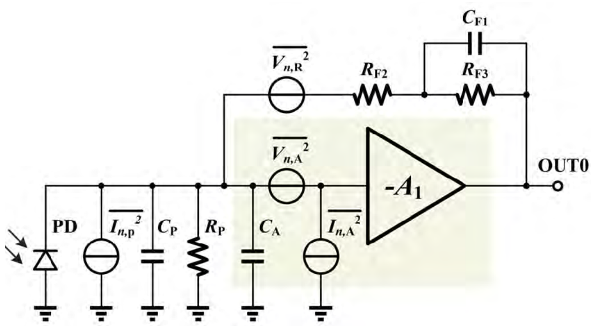


FIGURE 5. Noise model of PD and pre-TIA.

Figure 5 shows the noise model of PD and pre-TIA. C_p and R_p are the parasitic capacitance and resistance of the PD, respectively. C_A is the parasitic capacitance of the input node of the pre-TIA. The equivalent model of the TIA is in the green color box. The noise of PD can be represented as:

$$\overline{I_{n.p}^2} = 2qI_D + 2qI_L + 4kT/R_p \tag{12}$$

where I_D and I_L are dark current and photocurrent, respectively. Without light exposure, $I_L = 0$, $I_D \approx 2$ pA, and $R_p \approx 100$ MΩ. The shot noise power of dark current is about 6.408×10^{-31} A^2/Hz; the thermal noise power generated by the shunt resistor is about 1.38×10^{-29} A^2/Hz. The noise of the PD is determined by the process.

The feedback resistors R_{F2} and R_{F3} generate thermal noise. The equivalent output voltage noise power can be expressed as:

$$\overline{V_{n\cdot R}^2} = 4kT\left(R_{F2} + R_{F2}\right) \tag{13}$$

The primary noise of the TIA internal amplifier is from the first common-source stage. Thus, the equivalent input voltage noise power of the TIA internal amplifier can approximate to the first common-source stage equivalent input noise:

$$\overline{V_{n\cdot A}^2} = 4kT\left[2/(3g_{m1}) + 1/\left(g_{m1}^2 R_1\right)\right] + K/(C_{OX}WLf) \tag{14}$$

By increasing the transconductance g_{m1} of first common-source stage and the common-source load resistance R_1, the equivalent input noise will be reduced. However, since the load resistor R_1 affects the common-source output pole, R_1 needs to be increased with the limitation of loop stability. Increasing the transconductance g_{m1} is at the cost of power dissipation. As shown in (10), the capacitor C_{BP} of voltage amplifier can also reduce noise. The total output noise can be expressed as:

$$\begin{aligned}\overline{V_{n,OUT}} &= \frac{\sqrt{\overline{V_{n,\mathrm{A}}^2}\,[A(s)]^2 + \overline{V_{n,\mathrm{R}}^2}}}{1 + LG(s)} \cdot A_2(s) \\ &= \frac{\sqrt{\overline{V_{n,\mathrm{A}}^2}\,[A(s)]^2 + \overline{V_{n,\mathrm{R}}^2}}}{1 + \frac{(1+sC_{\mathrm{F1}}R_{\mathrm{F3}})A(s)}{(1+sC_{\mathrm{PD}}R_{\mathrm{F3}})(1+sC_{\mathrm{F1}}R_{\mathrm{F2}})}} \\ &\quad \times \left[1 + \frac{sC_{\mathrm{BP}}R_8}{(1+sC_{\mathrm{BP}}R_7)(1+sC_{\mathrm{F2}}R_8)}\right]\end{aligned} \tag{15}$$

At low frequency, $A_2(s) \approx 1$, and the low-frequency noise can be filtered out by C_{BP}. Furthermore, high frequency noise within the GBW of pre-TIA can be effectively reduced by the pole which is determined by C_{F1} and R_{F3}. Thus, the circuit shows low noise characteristics in a wide range of frequency.

III. SIMULATION AND EXPERIMENTAL RESULTS

The proposed fully-integrated optoelectronic detector is implemented in a 0.5 μm CMOS process. Figure 6 shows the loop characteristics of the TIA, where the loop gain is 56 dB, the unit gain bandwidth is 23 MHz, and the phase margin is 76ř with the proposed TIA structure and compensation method.

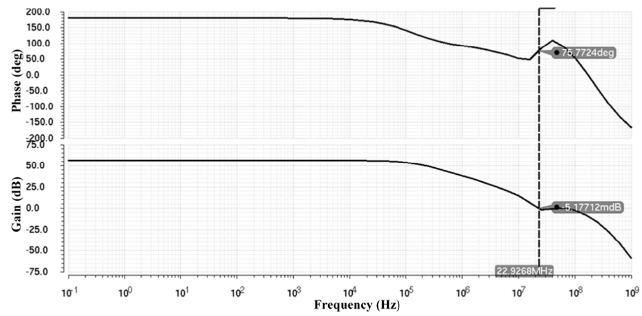


FIGURE 6. Loop simulation results of proposed pre-stage TIA.

Figure 7 shows the loop characteristics of voltage amplifier, where the main pole is located at a low frequency and there is a zero point locating at 200 Hz, and the zero point is negated with the main pole. It makes the loop gain and phase substantially constant at low frequencies.

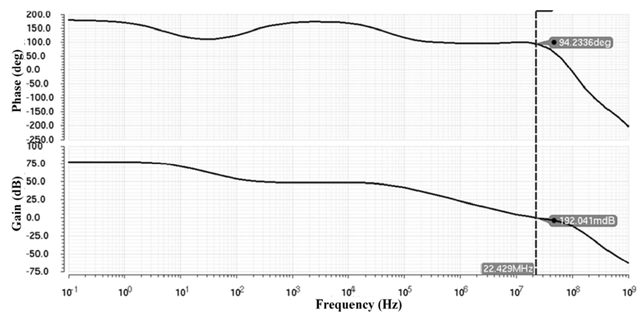


FIGURE 7. Loop simulation results of voltage amplifier.

In order to make the simulation results closer to the actual test situation, a 13 pF capacitor and a 1MΩ resistor are connected at output nodes to emulate the load effect of oscilloscope. As shown in Figure 8, the output voltage maintains a very linear relationship with the input optical power from 0 to 3.5 μW. When input optical power is 0, the output voltage is 106mV. The conversion rate between the input optical power and the output voltage is 65.6 mV/μW with 0.23 A/W low spectral-responsivity integrated PD.

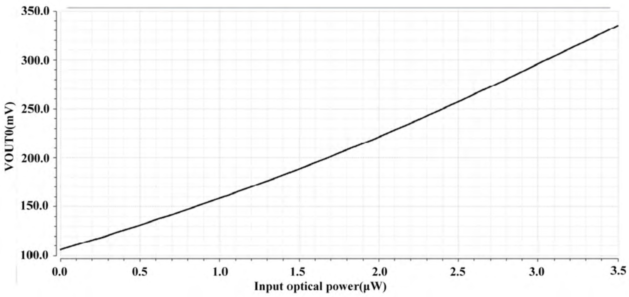


FIGURE 8. Simulation results of VOUT0 versus input optical power.

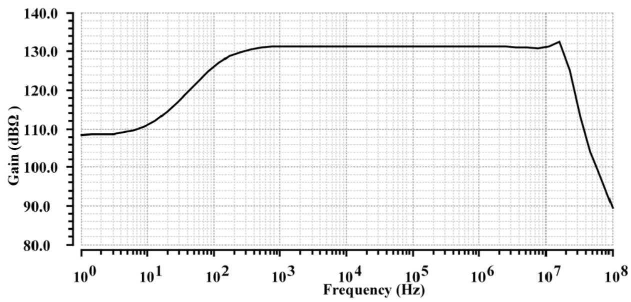


FIGURE 9. Simulated frequency response of whole amplifier.

The frequency response of the whole amplifier is shown in Figure 9. The middle frequency gain of the proposed structure is over 3.5 MΩ and 18 MHz bandwidth is achieved. The gain attenuation in low frequency range is mainly caused by gain damping of the voltage amplifier, which is determined by the capacitor CBP in Figure 3. The low frequency range can be shrunk by decreasing the capacitance of CBP with application requirements.

TABLE 1. Output voltage amplitude versus temperature and corner (V).

Temp (□) / Corner	-40	25	85
Typical	2.73	2.70	2.65
Fast	2.29	2.27	2.19
Slow	3.20	3.15	3.02

Table 1 displays total output voltage versus temperature variations and corner variations with the 2.5 μW input optical power. The pre-transimpedance gain is mainly generated by the feedback resistors. As the resistance has a negative temperature coefficient, the output amplitude is inversely proportional to the temperature. In slow corner, the resistance becomes larger making the output voltage amplitude larger; the resistance in fast corner becomes smaller leading the output voltage amplitude to become smaller.

In Figure 10, Plight and VOUT represent input optical power and output voltage, respectively. It can be seen from Figure 10 that the optical power, rise time and pulse width of input signal is 2.5 μW, 4 ns, and 400 ns. The measured rise time and delay time of output voltage is 15.61 ns and 18.87 ns.

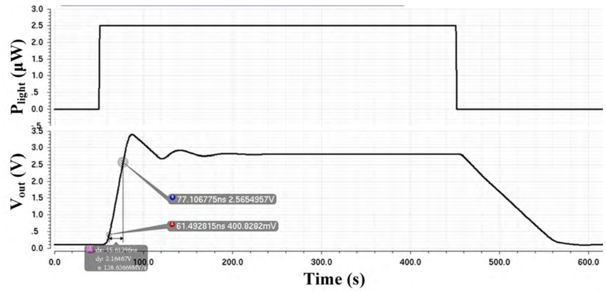


FIGURE 10. Transient simulation results.

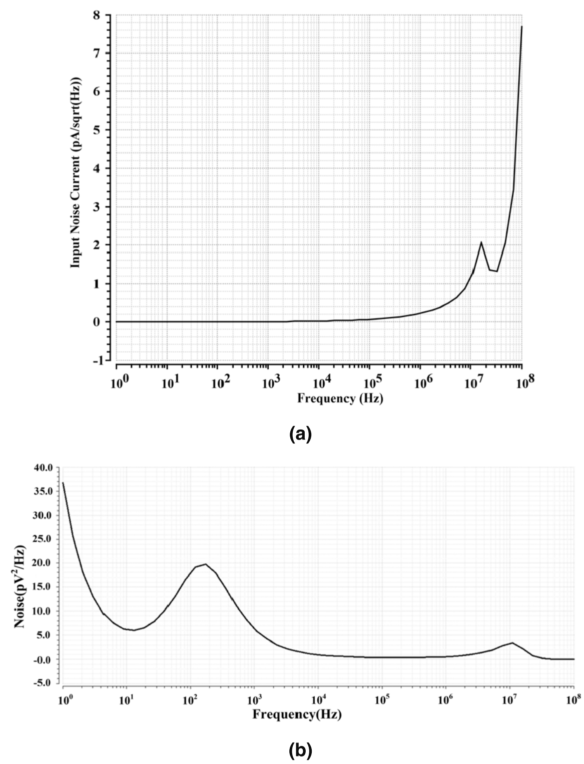


FIGURE 11. Noise characteristics of proposed circuit. (a) The input noise current waveform of proposed amplifier. (b) The output noise waveform of overall circuit.

The noise characterizes of proposed circuit is shown in Figure 11. As shown in Figure 11 (a), the average noise current spectral density is estimated to 1.069 pA/sqrt(Hz), which corresponds to the optical sensitivity of −28 dBm for 10-12 bit-error rate (BER) with 0.23 A/W responsivity [21]. Figure 11 (b) shows the noise output waveform. The flicker noise is reduced by the attenuation effect of voltage amplifier on the low frequency noise. At frequencies near 20 MHz, the amplifier loop has reached its unit gain bandwidth, so the noise increases rapidly. However, continuing to high frequencies, the noise is bound to decrease due to the characteristic frequency of the device, so the second peak in the waveform appears.

Table 2 and Table 3 show the rise time and the delay time of output voltage versus temperature variations and corner

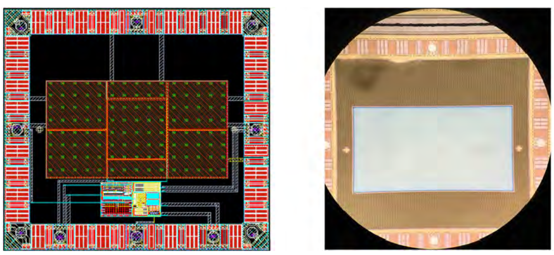
TABLE 2. Rise time versus temperature and corner (ns).

Corner \ Temp (□)	-40	25	85
Typical	10.98	15.61	16.73
Fast	11.19	12.10	13.69
Slow	11.75	22.95	22.26

TABLE 3. Delay time versus temperature and corner (ns).

Corner \ Temp (□)	-40	25	85
Typical	16.79	18.87	20.83
Fast	14.81	15.86	17.99
Slow	24.99	23.94	24.98

variations, respectively. Since the resistance across the TIA has a temperature coefficient, the position of the main pole changes with temperature. That makes the simulated rise time and delay time changed simultaneously. In slow corner, the main pole of the circuit moves to the low frequency with larger resistance and capacitance, and the transient response becomes slower. In similar way, the main pole moves to the high frequency and the transient response becomes faster with smaller resistance and capacitance in fast corner.



(a) (b)

FIGURE 12. Layout and chip micrograph of proposed integrated circuit. (a) Layout. (b) Chip Micrograph.

The layout and chip micrograph of proposed fully-integrated optoelectronic detector is shown in Figure 12. The total area of the layout is 2200 μm $\times$ 2000 μm with integrated PD, of which the proposed circuit part area is 501.2 μm $\times$ 291.6 μm.

Figure 13 shows the measured results of rise time. The input light power is the trigger signal of light pulse. The pulse width of input light is 100 ns, the wavelength is 905 nm, and the optical power is 1.5 μW. The output pulse amplitude is 1.6 V, the rise time is 24.5 ns, and the delay time is 21 ns. The difference between the simulated value and the measured value is mainly from the parasitic capacitance of the test board and the resistance deviation in the process.

Figure 14 shows the measured waveforms of output noise. When testing, the oscilloscope bandwidth is 500 MHz, AC coupled. The final measured noise is 13 mV.

Table 4 summarizes a comparison on the results of proposed detector and other structures reported in literature.

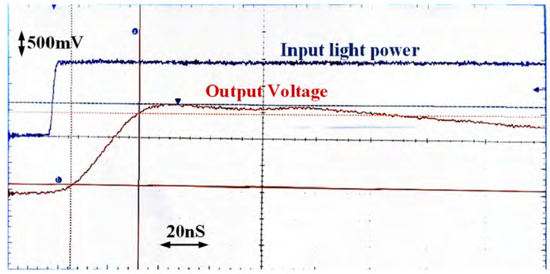


FIGURE 13. Measured waveforms of the proposed circuit.

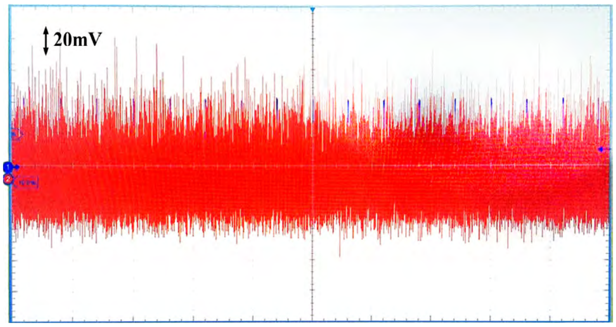


FIGURE 14. Measured waveforms of output noise.

TABLE 4. Comparison to reported works.

Ref.	[8]	[14]	[19]	[20]	This Work
Process(nm)	350	600	130	350	500
Supply voltage(V)	3	5	3.3	3.3	5
Power Dissipation (mW)	30	27	30	21	7.5
PD Area(mm^2)	N/A	0.25	N/A	N/A	1.2
Total Area(mm^2)	0.047	2.87	0.2	0.11	1.35
PD Cap (pF)	2	2.2	6	1	21.6
Gain (dBΩ)	90	79.5	170	140	130
BW (MHz)	255	220	1	2	18
Gain×BW (kΩ×GHz)	8.06	2.08	316	20	56.92
Average Input Noise (pA/sqrt (Hz))	6.8	7.08	52	0.004	1.069
FoM=Gain·BW·PD Cap/sqrt (Power·Noise) (kΩ×GHz×pF/ sqrt [mW×pA/sqrt (Hz)])	1.13	0.33	48	69	434

Only optoelectronic detectors in [14] and our work are with on-chip photo diodes. Since integrated photo diodes usually have worse characteristics than discrete PDs, it is usually more challenging to achieve good performance with fully integrated structures. Except [19], the gain bandwidth product of proposed structure is the highest one. However, circuit in [19], which is not fully integrated, consumes higher power consumption with capacitance TIA structure. Since the difficulties with larger parasitic PD capacitance and smaller power dissipation increase, it is necessary to adopt a figure of merit (FoM) for fair evaluation. The FoM $=$ Gain$\times$BW$\times$(PD

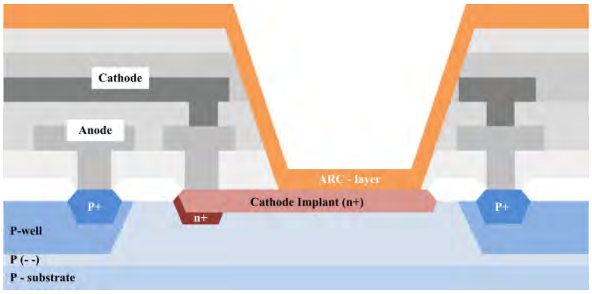


FIGURE 15. PIN Diode cross-section.

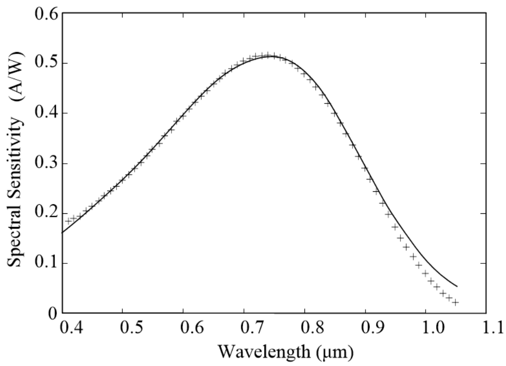


FIGURE 16. Spectral Sensitivity of PIN diode.

TABLE 5. Device parameter.

Device	Cut off freq. [MHz]	Sensitivity [A/W]	BreakdownVoltage [V]
PIN diode	85 (100 × 100μm2)	0.23@905nm	>50

Capacitance) / sqrt (Power×Noise) is used in Table 4, which shows the highest FoM value is realized by the proposed structure.

IV. CONCLUSION

In this paper, a fully-integrated optoelectronic detector, which simultaneously achieves 3.5 MΩ transimpedance gain and 18 MHz bandwidth, is proposed. The circuit is implemented in a 0.5μ m CMOS technology with integrated PD and the active area of the presented circuit is 501.2 μm × 291.6 μm. With the techniques of local negative feedback and compensation, the proposed structure has achieved competitive performance with conventional structures based on discrete PDs in optoelectronic detector applications.

APPENDIX

The PIN diode cross-section and Spectral Sensitivity are shown in Figure 15 and Figure 16, where the anti-reflective coating (ARC) is optimized for light. The area of PIN diode in proposed circuit is 1500 um × 800 um. The specifications are summarized in table 5.

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