IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 17, 2019, accepted April 14, 2019, date of publication April 23, 2019, date of current version June 4, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2912859

A Novel Low Voltage Ride-Through Technique of Three-Phase Grid-Connected Inverters Based on a Nonlinear Phase-Locked Loop

GUANGYU SUN, YONGLI LI, WEI JIN, SONG LI, AND YAN GAO
Department of Electrical Engineering and Automation, Tianjin University, Tianjin 300072, China

Corresponding author: Yongli Li (lyltju@163.com)

This work was supported in part by the National Key Research and Development Program under Grant 2016YFB0900603, in part by the Science and Technology Project from Headquarters of State Grid Corporation of China (Research on Key Protection Technologies for New-type Urban Distribution Network with Controllable Sources and Loads), in part by the National Natural Science Foundation of China under Grant 51577128, and in part by the Science and Technology Foundation of SGCC under Grant 52094017000W.

ABSTRACT In this paper, a novel low voltage ride-through (LVRT) technique for three-phase grid-connected inverters is proposed. The proposed technique consists of two parts: a nonlinear phase locked loop based on complex-coefficient filters (NLCCF-PLL) and an LVRT control scheme. Generally, the synchronization process of three-phase grid-connected inverters is performed via PLL with a relatively low bandwidth, which delays the detection of voltage sag and recovery during the LVRT process. To accelerate the synchronization process, the NLCCF-PLL with adaptive controller gains is proposed to improve both the filtering capability and dynamic performance of PLL at the same time. The stability of the NLCCF-PLL is validated by the second method of Lyapunov in the nonlinear model, and the superiority of its operating performance is verified. The proposed LVRT control scheme consists of a reference current calculation block to effectively suppress the power ripples and an inner loop controller with strong robustness as well as fast dynamic response. By comparing the proposed LVRT technique with the existing LVRT technique on the basis of experimental results, the superiority of the proposed LVRT technique is confirmed.

INDEX TERMS Low voltage ride-through (LVRT), phase-locked loops (PLL), nonlinear control, the second method of Lyapunov, three-phase grid-connected inverters, power ripples.

I. INTRODUCTION

Many renewable energy generation systems (REGSs) have been installed to address energy shortages and environmental challenges [1]. Given the remarkable proliferation of REGSs, the stability and safety of the power grid have encountered serious obstacles due to the uncertainty and intermittence of renewable energies, especially in the case of grid faults. To support grid stability during grid faults, continuous connection and fast response of grid-connected inverters are essential [2]. Until now, many countries defined their own low-voltage ride-through (LVRT) regulations to regulate the operations of grid-connected inverters during sags in grid voltage [3], [4]. Under these regulations, grid-connected inverters must be able to participate in dynamic network support during grid faults by injecting reactive currents continuously into the grid [5].

The associate editor coordinating the review of this manuscript and approving it for publication was Shravana Musunuri.

Synchronous reference frame PLL (SRF-PLL) is the most popular grid voltage detection technique for grid-connected inverters to provide uninterrupted output power due to its simplicity, effectiveness and robustness [6]. However, SRF-PLL is highly sensitive to distorted and unbalanced voltage [7]. Moreover, in the power grid, voltage sag during grid faults is accomplished by phase shifts, frequency variations, voltage imbalances and distortions [8]. Therefore, the bandwidth of common SRF-PLLs in industrial converters is limited to 15Hz–75Hz to mitigate the influences of unbalanced and distorted grid voltage, resulting in a longer dynamic detection process [9]. The prolonged dynamic detection process of grid voltage causes large transit fluctuations in the output current of the grid-connected inverter, and may even destroy the stability of the power grid system.

To accelerate the synchronous process under distorted and unbalanced voltage, by inserting additional filters into the control loop of SRF-PLL or before its input, advanced PLLs with enhanced filtering capabilities, (e.g., MAF-PLL,

DCCF-PLL, DSOGI-PLL, MSRF-PLL, and DSC-PLL) have been proposed [10]–[15]. However, inserted filters still constrain the dynamic response of PLLs, resulting in a relatively long detection process and degraded the LVRT performance of grid-connected inverters. Other efforts have been made to improve the dynamic performance of PLLs by adopting of specially-designed inserted filters [16], [17]. However, an unavoidable tradeoff exists between the steady-state filtering capability and dynamic performance of PLLs with linear controllers above, which strictly restricts the practical application of these PLLs [18]. To avoid this problem, a nonlinear PLL with adaptive controller gains (NLPI-PLL) was proposed [19]. By regulating the open-loop controller gains according to phase deviation, the steady-state filtering capability and dynamic performance is improved simultaneously. Even so, concerns remain regarding the stability of this NLPI-PLL, limiting its feasibility [20]. In summary, it is difficult for existing PLLs to obtain both fast dynamic responses and good disturbance rejections without compromising PLLs' stability; thus there is still room for improvement in the LVRT performance of grid-connected inverters associated with existing PLLs.

Despite PLL performance, advanced LVRT control schemes are also capable of improving the LVRT performance of grid-connected inverters. Regarding unbalanced grid faults, to provide uninterrupted active power and reactive power as regulated in [4], grid-connected inverters can generate positive-sequence currents during unbalanced voltage sag [21]. However, output power ripples remain obvious due to unbalanced grid voltage. To completely block these output power ripples, together with the positive-sequence component, negative-sequence component and harmonic component are also included in output currents during voltage sag as deduced in [22]. Yet these output harmonic currents further deteriorate voltage quality during the grid faults. In [23], without harmonic injections, positive-sequence and negative-sequence output currents were optimized to eliminate active power ripples without restraining the reactive power ripples. In [24], a consolidated control scheme that can readily adjust between eliminating real or reactive power ripples, or simply generating the positive-sequence currents without harmonic injections is proposed. However, according to the existing researches above, the strategies for restraining the total power ripples of both reactive power and active power of grid-connected inverters are still worth discussing. On the other hand, compared with the conventional inner loop controller of grid-connected inverters, the inner loop controller in the LVRT technique is expected to possess the following advantages: 1) good dynamic performance in response to sudden changes of grid voltage; 2) good robustness to remain stable when grid faults substantially deteriorate the performance of the pre-designed inner loop controller. Therefore, investigations of the specific inner loop controller in grid-connected inverters during the LVRT process are also necessary.

In this paper, to improve the LVRT performance of grid-connected inverters, a nonlinear PLL based on complex-coefficient filters (NLCCF-PLL) is proposed by introducing the adaptive controller gains into the PLL structure. The nonlinear control scheme of NLCCF-PLL guarantees a fast dynamic response and good disturbance rejection capability simultaneously. The stability of NLCCF-PLL is validated with the second method of Lyapunov, and the operating performance of NLCCF-PLL is analyzed in detail. An improved LVRT control scheme is also proposed in this paper. Among the LVRT control scheme, to ensure a proper response under unbalanced voltage and improvements in reliability, the reference currents with the fewest total power ripples are derived by matrix calculations. Based on the encouraging performance of NLCCF-PLL, an inner loop controller is proposed, which is characterized by good robustness and a fast dynamic response. Experiments are conducted to verify the superiority in dynamic response and power ripple restrictions of the proposed LVRT technique.

The rest of this paper is structured as follows. In Section II, the structure and control scheme of NLCCF-PLL are proposed, and the stability of NLCCF-PLL is verified. In Section III, the proposed LVRT control scheme consisting of a reference current calculation block and an inner loop controller is presented. Finally in Section IV, the superiority of the proposed NLCCF-PLL and LVRT technique is confirmed by experimental results.

II. DESCRIPTION OF NLCCF-PLL

As the synchronous unit that significantly influences the LVRT performance of grid-connected inverters, the proposed NLCCF-PLL is discussed in this section.

A. OVERVIEW OF CONVENTIONAL DCCF-PLL

Among existing PLL techniques, complex-coefficient filters (CCFs) are characterized by an asymmetrical frequency response around zero frequency, which implies that they can extract positive or negative sequence components in the same frequency [12]. By placing two paralleled bandpass CCFs before the input of SRF-PLL, a dual complex-coefficient filter-based PLL (DCCF-PLL) is established, as shown in Fig.1 [12]. V^+, $\hat{\omega}_g$, $\hat{\theta}_g$ respectively denote the amplitude, frequency, and phase angle of the fundamental positive sequence component of the grid voltage estimated by DCCF-PLL; $\hat{\omega}_{\text{ref}}$ represents the nominal frequency; *CCF* and *PI* are the bandpass CCF and proportional–integral (PI) controller, respectively. The transfer functions of the CCF block and PI controller, $G_{\text{CCF}}(s)$ and $G_{\text{PI}}(s)$, can be written as

$$G_{\text{CCF}}(s) = \frac{\hat{\omega}_b}{s - j\hat{\omega}_g + \hat{\omega}b} \tag{1}$$

$$G_{\text{PI}}(s) = K_p + \frac{K_i}{s} \tag{2}$$

where $\hat{\omega}_b$ is the bandwidth of CCF; K_p and K_i respectively denote the proportional gain and integral gain of the PI controller.

As shown in Fig.1, the CCF block acts as a pre-processing filter by extracting the fundamental positive sequence

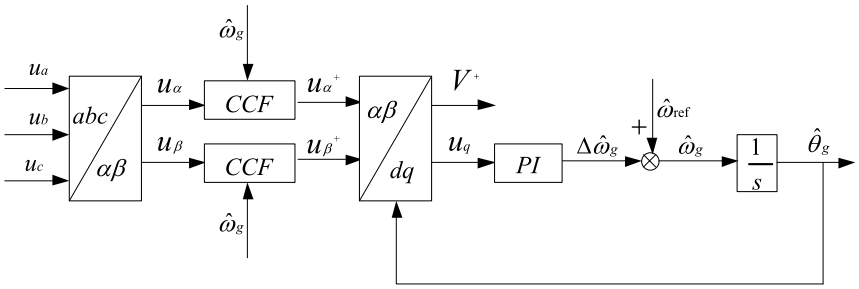

FIGURE 1. Block diagram of the conventional DCCF-PLL.

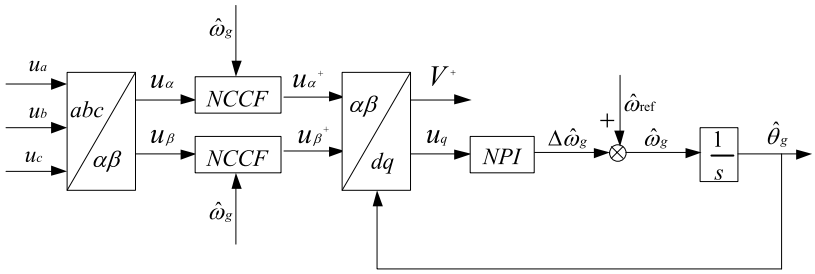

FIGURE 2. Block diagram of the proposed NLCCF-PLL.

component of the grid voltage, whereas the other control blocks of DCCF-PLL are identical to those of conventional SRF-PLLs [12]. In this way, the harmonic and unbalanced components of the grid voltage are simply and effectively blocked without substantially degrading PLL dynamic behaviors [20].

B. BASIC CONFIGURATION OF NLCCF-PLL

Although DCCF-PLL is characterized by its simplicity and effectiveness, the tradeoff between the dynamic response and filtering performance brought about by the linear controller strictly restricts its PLL performance.

To further improve the dynamic response and filtering capability, nonlinear controllers are introduced based on the structure of DCCF-PLL in this paper. The basic configuration of the proposed NLCCF-PLL is illustrated in Fig.2, in which *NCCF* and *NPI* represent the adaptive bandpass complex-coefficient filters (NCCF) and the nonlinear proportional–integral (NPI) controller respectively. The transfer functions of the NCCF and NPI controller can be expressed as

$$G_{\text{NCCF}}(s) = \frac{\hat{\omega}_b(\Delta\hat{\omega}_g)}{s - j\hat{\omega}_g + \hat{\omega}_b(\Delta\hat{\omega}_g)} \tag{3}$$

$$G_{\text{NPI}}(s) = G_{Kp}(\Delta\hat{\omega}_g) + \frac{G_{Ki}(\Delta\hat{\omega}_g)}{s} \tag{4}$$

where $G_{\text{NCCF}}(s)$ and $G_{\text{NPI}}(s)$ denote the transfer functions of the NCCF and NPI controller respectively; $\hat{\omega}_b(\Delta\hat{\omega}_g)$ is the adaptive bandwidth of NCCF; and $G_{Kp}(\Delta\hat{\omega}_g)$, $G_{Ki}(\Delta\hat{\omega}_g)$ are adaptive proportional gain and integral gain of NPI controller respectively. The specific transfer functions for $\hat{\omega}_b(\Delta\hat{\omega}_g)$, $G_{Kp}(\Delta\hat{\omega}_g)$, $G_{Ki}(\Delta\hat{\omega}_g)$ are

$$\begin{cases} \hat{\omega}_b(\Delta\hat{\omega}_g) = \hat{\omega}_{b\min} + \dfrac{\hat{\omega}_{b\max} - \hat{\omega}_{b\min}}{\Delta\hat{\omega}_g} f(\Delta\hat{\omega}_g) \\ G_{Kp}(\Delta\hat{\omega}_g) = K_{p\min} + \dfrac{K_{p\max} - K_{p\min}}{\Delta\hat{\omega}_g} f(\Delta\hat{\omega}_g) \\ G_{Ki}(\Delta\hat{\omega}_g) = \left(K_{i\min} + \dfrac{K_{i\max} - K_{i\min}}{\Delta\hat{\omega}_g} f(\Delta\hat{\omega}_g)\right)^2 \\ f(\Delta\hat{\omega}_g) = \begin{cases} \left|\Delta\hat{\omega}_g\right| - \varepsilon & \left(\left|\Delta\hat{\omega}_g\right| > \varepsilon\right) \\ 0 & \left(\left|\Delta\hat{\omega}_g\right| \le \varepsilon\right) \end{cases} \\ \dfrac{\hat{\omega}_{b\max}}{\hat{\omega}_{b\min}} = \dfrac{K_{p\max}}{K_{p\min}} = \dfrac{K_{i\max}}{K_{i\min}} \end{cases} \tag{5}$$

where $\hat{\omega}_{b\min}$, $K_{p\min}$, $K_{i\min}$ respectively denote the minimum value of $\hat{\omega}_b(\Delta\hat{\omega}_g)$, $G_{Kp}(\Delta\hat{\omega}_g)$, $G_{Ki}(\Delta\hat{\omega}_g)$; $\hat{\omega}_{b\max}$, $K_{P_{\max}}$ and $K_{i\max}$ are the maximum values of $\hat{\omega}_b(\Delta\hat{\omega}_g)$, $G_{Kp}(\Delta\hat{\omega}_g)$ and $G_{Ki}(\Delta\hat{\omega}_g)$ respectively; ε is the threshold value of $\Delta\hat{\omega}_g$. Based on (5), variations of the nonlinear parameters according to $\Delta\hat{\omega}_g$ are plotted in Fig.3.

As indicated in (5) and Fig.3, during the dynamic process when the tracking error $\Delta\hat{\omega}_g$ is large, the bandwidths of the NCCFs and nonlinear PI controllers enlarge simultaneously to increase the open-loop gain of NLCCF-PLL, resulting in an accelerated dynamic response; during the steady state when the tracking error $\Delta\hat{\omega}_g$ is small, the control parameters are decreased to inhibit the open-loop gain of NLCCF-PLL, resulting in better steady-state filtering performance.

Based on the control scheme depicted in (5), another state variable ΔV is introduced in to accelerate the dynamic

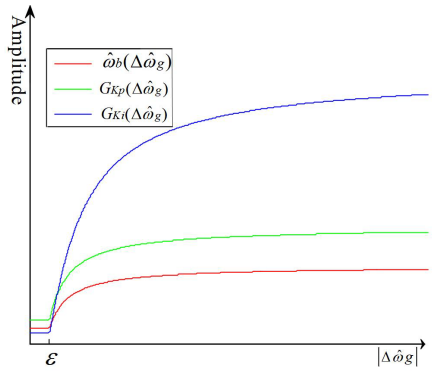

FIGURE 3. Variations of the nonlinear parameters according to $\Delta\hat{\omega}_g$.

response of NLCCF-PLL. The expression of ΔV is

$$\Delta V = \frac{2}{3}(U_a \cos\hat{\theta}_g + U_b \cos(\hat{\theta}_g - 120°) + U_c \cos(\hat{\theta}_g + 120°)) \quad (6)$$

As presented in (6), different from $\Delta\hat{\omega}_g$, the defined state variable ΔV is characterized by a fast dynamic response under the condition of a sudden change in grid voltage. By comparing ΔV with a threshold value T, the steady state and dynamic process can be distinguished. Therefore, when ΔV is larger than T, the NLCCF-PLL system is deemed to be in a dynamic process, and the open-loop gain of NLCCF-PLL is amplified to accelerate the dynamic response.

In this way, T should be larger than the largest amplitudes of ΔV in the steady state, which is caused by harmonics, DC offsets, and negative-sequence voltages. The relationships between ΔV and harmonics, DC offset and negative-sequence voltage in steady state is [25]

$$\Delta V = U_{\rm dc}\cos(\hat{\theta}_g + \varphi_{\rm dc}) + U^-\cos(2\hat{\theta}_g + \varphi^-) + \sum_{n=2} U_n \cos((n \pm 1)\hat{\theta}_g + \varphi_n) \quad (7)$$

where $U_{\rm dc}$, U^-, and U_n respectively denote the amplitude of DC offset, negative-sequence voltage and harmonic voltage. According to (7), the range of the amplitude of ΔV in a steady state is

$$|\Delta V| \le a_{\max} + b_{\max} + c_{\max} \quad (8)$$

where $a_{\max}$ is the maximum amplitude of harmonic voltage, $b_{\max}$ is the maximum amplitude of negative-sequence voltage, and $c_{\max}$ is the maximum amplitude of DC offset voltage. Considering certain margins for ΔV, T is selected as

$$T = 1.3(a_{\max} + b_{\max} + c_{\max}) \quad (9)$$

By introducing the state variable ΔV into the control scheme, the overall transfer functions of $\hat{\omega}_b(\Delta\hat{\omega}_g)$, $G_{Kp}(\Delta\hat{\omega}_g)$, and $G_{Ki}(\Delta\hat{\omega}_g)$ are modified as

$$\begin{cases} \text{if } \Delta V \ge T, & \begin{cases} \hat{\omega}_b(\Delta\hat{\omega}_g) = \hat{\omega}_{b\max} \\ G_{Kp}(\Delta\hat{\omega}_g) = K_{p\max} \\ G_{Ki}(\Delta\hat{\omega}_g) = K_{i\max}^2 \end{cases} \\ \text{else}, & \begin{cases} \hat{\omega}_b(\Delta\hat{\omega}_g) = \hat{\omega}_{b\min} + \dfrac{\hat{\omega}_{b\max} - \hat{\omega}_{b\min}}{\Delta\hat{\omega}_g} f(\Delta\hat{\omega}_g) \\ G_{Kp}(\Delta\hat{\omega}_g) = K_{p\min} + \dfrac{K_{p\max} - K_{p\min}}{\Delta\hat{\omega}_g} f(\Delta\hat{\omega}_g) \\ G_{Ki}(\Delta\hat{\omega}_g) = \left(K_{i\min} + \dfrac{K_{i\max} - K_{i\min}}{\Delta\hat{\omega}_g} f(\Delta\hat{\omega}_g)\right)^2 \\ f(\Delta\hat{\omega}_g) = \begin{cases} |\Delta\hat{\omega}_g| - \varepsilon & (|\Delta\hat{\omega}_g| > \varepsilon) \\ 0 & (|\Delta\hat{\omega}_g| \le \varepsilon) \end{cases} \\ \dfrac{\hat{\omega}_{b\max}}{\hat{\omega}_{b\min}} = \dfrac{K_{p\max}}{K_{p\min}} = \dfrac{K_{i\max}}{K_{i\min}} \end{cases} \end{cases} \quad (10)$$

According to the parameter settings in (10), the relationships between nonlinear expressions $\hat{\omega}_b(\Delta\hat{\omega}_g)$, $G_{Kp}(\Delta\hat{\omega}_g)$, $G_{Ki}(\Delta\hat{\omega}_g)$ can be simplified as

$$\hat{\omega}_b(\Delta\hat{\omega}_g) : G_{Kp}(\Delta\hat{\omega}g) : G_{Ki}(\Delta\hat{\omega}_g) = k_{\max} : K_{p\max} : K_{i\max}^2 \quad (11)$$

C. STABILITY ANALYSIS OF NLCCF-PLL

Based on the preceding analysis, a fast dynamic response and good filtering performance can be achieved using the proposed nonlinear control scheme. However, the stability of existing PLLs with nonlinear controllers is questionable [20]. To ensure the feasibility of the proposed NLCCF-PLL, its stability must be verified.

Clearly, the stability criteria for a conventional linear system (e.g., the Routh-Hurwitz criterion) are no longer suitable for NLCCF-PLL due to its highly nonlinearity. In this paper, the second method of Lyapunov is applied to confirm the stability of NLCCF-PLL. Compared with other stability criteria for nonlinear systems, the second method of Lyapunov is simpler to implement because it does not require specific solutions to the nonlinear differential equations.

According to [26], the mathematically equivalent nonlinear model of DCCF-PLL is as depicted in Fig.4 (a). Correspondingly, the nonlinear model of NLCCF-PLL is shown in Fig.4 (b).

On the basis of Fig. 4(b), the necessary state variables are determined as follows

$$\begin{cases} x_1 = \hat{\theta}_{\rm gref} - \hat{\theta}_g \\ x_2 = \dfrac{\hat{\omega}_b(\Delta\hat{\omega}_g)}{s + \hat{\omega}_b(\Delta\hat{\omega}_g)} V^+ \sin(x_1) \\ x_3 = \dfrac{\sqrt{G_{Ki}(\Delta\hat{\omega}_g)}}{s} x_2 \end{cases} \quad (12)$$

where x_1, x_2, and x_3 are the selected state variables in the nonlinear model of NLCCF-PLL. State equations corresponding to this model in Fig.4 (b) with no external

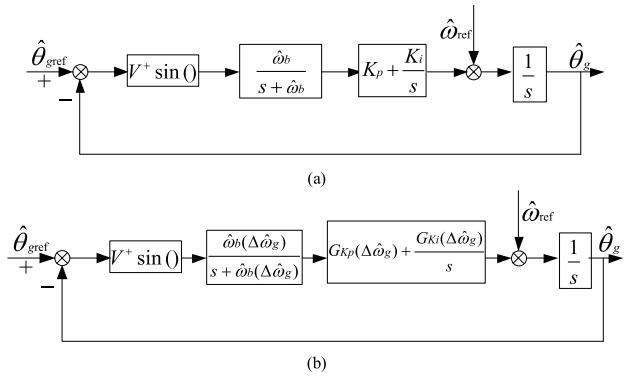

FIGURE 4. The equivalent nonlinear model of DCCF-PLL and NLCCF-PLL. (a) DCCF-PLL. (b) NLCCF-PLL.

inputs ($\theta^* = \omega_{\text{ref}} = 0$) are

$$\begin{cases} x_1' = -\sqrt{G_{Ki}(\Delta\hat{\omega}_g)}x_3 - G_{Kp}(\Delta\hat{\omega}_g)x_2 \\ x_2' = \hat{\omega}_b(\Delta\hat{\omega}_g)V^+\sin(x_1) - \hat{\omega}_b(\Delta\hat{\omega}_g)x_2 \\ x_3' = \sqrt{G_{Ki}(\Delta\hat{\omega}_g)}x_2 \end{cases} \tag{13}$$

To facilitate the stability analysis of NLCCF-PLL, by combining (12) and (13), the nonlinear model of NLCCF-PLL with state variables is redrawn in Fig.5.

The Lyapunov candidate function is constructed as

$$V(x_1, x_2, x_3) = \int_0^{x_1} \sin(\delta)d\delta + \frac{1}{2}[x_2 x_3]\boldsymbol{P}[x_2 x_3]^{\mathrm{T}} \tag{14}$$

where $\boldsymbol{P}$ is a symmetric, positive definite, 2×2 matrix. To invoke LaSalle's Theorem [27] to prove the globally asymptotically stability of the nonlinear system, we must have $\dot{V}(x_1, x_2, x_3) \leq 0, V(x_1, x_2, x_3) \geq 0$ with $V(0, 0, 0) = 0$.

Assuming that $\boldsymbol{P}_{2\times2} = \begin{bmatrix} P_1 & P_2 \\ P_2 & P_3 \end{bmatrix}$ ($P_1 > 0$ and $P_1P_3 - P_2^2 > 0$), then the expression of $\dot{V}(x_1, x_2, x_3)$ can be simplified as follows

$$\begin{aligned} \dot{V}(x_1, x_2, x_3) = \sin(x_1)x_1' + P_1x_2x_2' \\ + P_3x_3x_3' + P_2x_2x_3' + P_2x_3x_2' \end{aligned} \tag{15}$$

Substituting (13) into (15) yields

$$\begin{aligned} \dot{V}(x_1, x_2, x_3) = &(\hat{\omega}_b(\Delta\hat{\omega}_g)V^+P_2 - \sqrt{G_{Ki}(\Delta\hat{\omega}_g)})\sin(x_1)x_3 \\ &+ (\hat{\omega}_b(\Delta\hat{\omega}_g)V^+P_1 - G_{Kp}(\Delta\hat{\omega}_g))\sin(x_1)x_2 \\ &+ (\sqrt{G_{Ki}(\Delta\hat{\omega}_g)}P_2 - \hat{\omega}_b(\Delta\hat{\omega}_g)P_1)x_2^2 \\ &+ (\sqrt{G_{Ki}(\Delta\hat{\omega}_g)}P_3 - \hat{\omega}_b(\Delta\hat{\omega}_g)P_2)x_2x_3 \end{aligned} \tag{16}$$

For all state variables x_1, x_2, and x_3, to guarantee that $\dot{V}(x_1, x_2, x_3) = -kx_2^2 \leq 0 (k < 0)$, the following expressions are derived

$$\begin{cases} \hat{\omega}_b(\Delta\hat{\omega}_g)V^+P_2 - \sqrt{G_{Ki}(\Delta\hat{\omega}_g)} = 0 \\ \hat{\omega}_b(\Delta\hat{\omega}_g)V^+P_1 - G_{Kp}(\Delta\hat{\omega}_g) = 0 \\ \sqrt{G_{Ki}(\Delta\hat{\omega}_g)}P_2 - \hat{\omega}_b(\Delta\hat{\omega}_g)P_1 < 0 \\ \sqrt{G_{Ki}(\Delta\hat{\omega}_g)}P_3 - \hat{\omega}_b(\Delta\hat{\omega}_g)P_2 = 0 \\ P_1P_3 - P_2^2 > 0 \end{cases} \tag{17}$$

To satisfy the stability criterion of the second method of Lyapunov, the following equations can be derived by combining (11) and (17)

$$\begin{cases} P_1 = \dfrac{K_{p\max}}{V^+\hat{\omega}_{b\max}} \\ P_2 = \dfrac{K_{i\max}}{V^+\hat{\omega}_{b\max}} \\ P_3 = \dfrac{1}{V^+} \\ K_{p\max}\hat{\omega}_{b\max} - K_{i\max}^2 > 0 \end{cases} \tag{18}$$

According to (18), when $K_{p\max}\hat{\omega}_{b\max} - K_{i\max}^2 > 0$ and $\hat{\omega}_{b\max}, K_{p\max}, K_{i\max} > 0$, the nonlinear model of NLCCF-PLL is globally asymptotically stable, which means that the proposed PLL can stably track the reference phase at any initial value.

D. PERFORMANCE ANALYSIS OF NLCCF-PLL

To discuss the operating performance of NLCCF-PLL, the stability margins of NLCCF-PLL with different sets of control parameters are analyzed in this section.

We assume there are two sets of control parameters, $\hat{\omega}_b(\Delta\hat{\omega}_{g1})$, $G_{Kp}(\Delta\hat{\omega}_{g1})$, $G_{Ki}(\Delta\hat{\omega}_{g1})$, and $\hat{\omega}_b(\Delta\hat{\omega}_{g2})$, $G_{Kp}(\Delta\hat{\omega}_{g2})$, $G_{Ki}(\Delta\hat{\omega}_{g2})$, with the corresponding cutoff frequencies ω_1 and ω_2. According to Fig.4 (b), the small-signal open loop transfer function of $G_{\text{open}}(s)$ is

$$G_{\text{open}}(s) = V^+\frac{\hat{\omega}_b(\Delta\hat{\omega}_g)G_{Kp}(\Delta\hat{\omega}_g)s + \hat{\omega}_b(\Delta\hat{\omega}_g)G_{Ki}(\Delta\hat{\omega}_g)}{s^2(s + \hat{\omega}_b(\Delta\hat{\omega}_g))} \tag{19}$$

Assuming that $m = \hat{\omega}_b(\Delta\hat{\omega}_{g1})/\hat{\omega}_b(\Delta\hat{\omega}_{g2})$, we define

$$\begin{aligned} &\|G\text{open}(j\omega_1)\| \\ &= \left\| V^+\frac{\hat{\omega}_b(\Delta\hat{\omega}_{g1})G_{Kp}(\Delta\hat{\omega}_{g1})s + \hat{\omega}_b(\Delta\hat{\omega}_{g1})G_{Ki}(\Delta\hat{\omega}_{g1})}{(j\omega_1)^2(j\omega_1 + \hat{\omega}_b(\Delta\hat{\omega}_{g1}))} \right\| \\ &= 1 \end{aligned} \tag{20}$$

$$\begin{aligned} &\|G\text{open}(j\omega_2)\| \\ &= \left\| V^+\frac{\hat{\omega}_b(\Delta\hat{\omega}_{g2})G_{Kp}(\Delta\hat{\omega}_{g2})s + \hat{\omega}_b(\Delta\hat{\omega}_{g2})G_{Ki}(\Delta\hat{\omega}_{g2})}{(j\omega_2)^2(j\omega_2 + \hat{\omega}_b(\Delta\hat{\omega}_{g2}))} \right\| \\ &= \left\| V^+\frac{\frac{\hat{\omega}_b(\Delta\hat{\omega}_{g1})G_{Kp}(\Delta\hat{\omega}_{g1})}{m^2}(j\omega_2) + \frac{\hat{\omega}_b(\Delta\hat{\omega}_{g1})G_{Ki}(\Delta\hat{\omega}_{g1})}{m^3}}{(j\omega_2)^2(j\omega_2 + \frac{\hat{\omega}_b(\Delta\hat{\omega}_{g1})}{m})} \right\| = 1 \end{aligned} \tag{21}$$

where $||G_{\text{open}}(j\omega_1)||$ and $||G_{\text{open}}(j\omega_2)||$ are the magnitudes of $G_{\text{open}}(s)$ at the cutoff frequency with the control parameters as shown in (10).

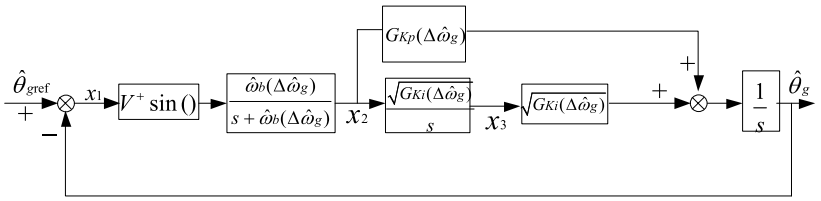

FIGURE 5. The nonlinear model of NLCCF-PLL with state variables.

Upon comparing (20) and (21), we can see that (21) is established when $\omega_1 = m\omega_2$. On the other hand, $||G_{\text{open}}(j\omega)||$ declines as ω increases, as can be confirmed in Fig.6. Therefore, only when $\omega_1 = m\omega_2$, $||G_{\text{open}}(j\omega_1)|| = ||G_{\text{open}}(j\omega_2)|| = 1$ holds, and the following equation can be derived

$$m = \frac{\omega_1}{\omega_2} = \frac{\hat{\omega}_b(\Delta\hat{\omega}_{g1})}{\hat{\omega}_b(\Delta\hat{\omega}_{g2})} \tag{22}$$

On the basis of (22), PM_1 and PM_2, representing the phase margin at ω_1 and ω_2, are deduced as follows:

$$\begin{aligned} PM1 &= \angle G_{\text{open}}(j\omega_1) \\ &= \arctan\frac{G_{Kp}(\Delta\hat{\omega}_{g1})\omega_1}{G_{Ki}(\Delta\hat{\omega}_{g1})} - \arctan\frac{\omega_1}{\hat{\omega}_b(\Delta\hat{\omega}_{g1})} - 180^\circ \end{aligned} \tag{23}$$

$$\begin{aligned} PM2 &= \angle G_{\text{open}}(j\omega_2) \\ &= \arctan\frac{G_{Kp}(\Delta\hat{\omega}_{g2})\omega_2}{G_{Ki}(\Delta\hat{\omega}_{g2})} - \arctan\frac{\omega_2}{\hat{\omega}_b(\Delta\hat{\omega}_{g2})} - 180^\circ \\ &= \arctan\frac{G_{Kp}(\Delta\hat{\omega}_{g1})\omega_1}{G_{Ki}(\Delta\hat{\omega}_{g1})} - \arctan\frac{\omega_1}{\hat{\omega}_b(\Delta\hat{\omega}_{g1})} - 180^\circ \end{aligned} \tag{24}$$

It can be inferred from (23) and (24) that $PM_1 = PM_2$. Therefore, when the control parameters of NLCCF-PLL vary, the phase margin of the small-signal model is constant. To intuitively highlight the advantage of NLCCF-PLL in the phase margin, open-loop bode plots of NLCCF-PLL with different sets of control parameters are presented in Fig.6.

As can be seen in Fig.6, the phase margin of NLCCF-PLL is always 67.9° when the cutoff frequency increases from 10.7Hz to 650Hz, furtherdemonstrating that the proposed NLCCF-PLL is stable with sufficient stability margins. Moreover, by setting the control scheme of NLCCF-PLL as discussed above, its operating performance can be estimated with good robustness.

During the grid faults, transit disturbance (e.g., voltage sags and sudden drift in the frequency and phase of voltages) and steady-state disturbance (e.g., unbalanced and distorted voltages) should be considered by the LVRT performance of grid-connected inverters [28]. As discussed above, with good filtering capability, fast dynamic response and good robustness, NLCCF-PLL could improve the LVRT performance of inverters by accelerating the dynamic process when transit disturbance occurs as well as decrease the tracking errors in the steady state.

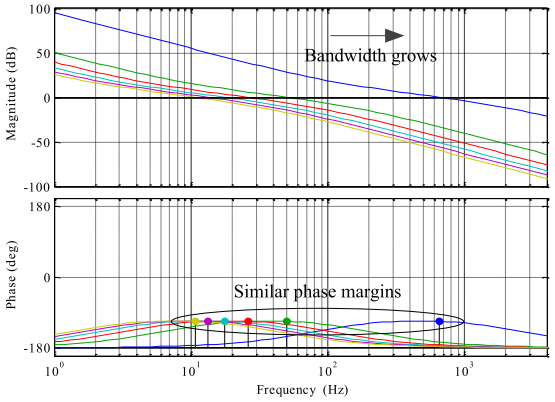

FIGURE 6. Open-loop bode plots of NLCCF-PLL with different sets of control parameters.

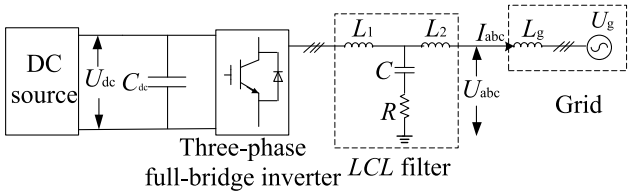

FIGURE 7. Three-phase voltage source inverter connected to the power grid.

III. THE PROPOSED LVRT CONTROL SCHEME

In addition to the proposed NLCCF-PLL, an advanced LVRT control scheme is also important for the LVRT performance of grid-connected inverters. The investigation of the proposed LVRT control scheme is based on a three-phase voltage source inverter connected to the power grid, as illustrated in Fig. 7. In this paper, an LCL filter is inserted between the grid and inverter to attenuate the high-frequency harmonics injected into the grid [29]. At the same time, the DC-link voltage is assumed to be constant under LVRT operation, and supported by a DC source with constant DC voltage.

The proposed LVRT control scheme is composed of a reference current calculation block and an inner loop control, depicted in Fig.8. According to the grid voltage estimated by the NLCCF-PLL, the reference current of the inner loop controller is generated by the reference current calculation block. Meanwhile, the proposed inner loop controller is also conducted under $\alpha\beta$ static coordinates. The specific design procedure for reference current calculations and the inner loop controller are discussed below.

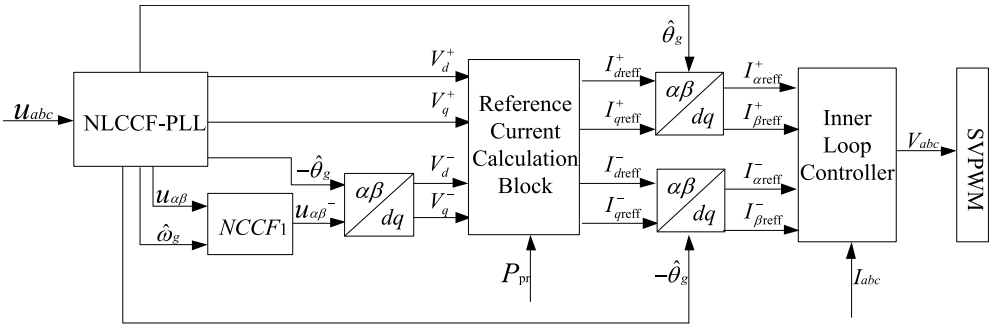

FIGURE 8. The specified control flow for LVRT operation.

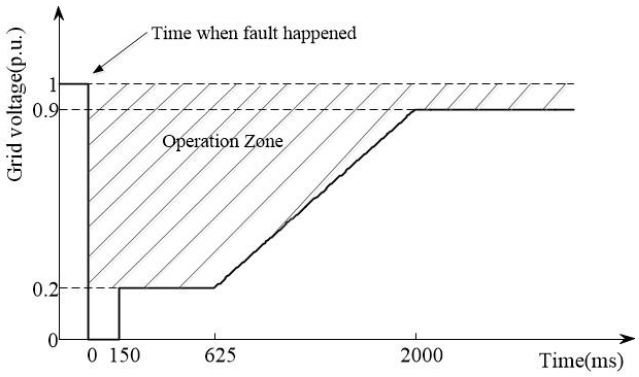

FIGURE 9. LVRT requirements of grid connection.

A. REFERENCE CURRENT CALCULATIONS

As required in [5], grid-connected inverters should be able to inject active and reactive currents into the grid during grid faults in order to facilitate grid voltage recovery. The specific operational requirements for grid connections in [5] during the LVRT process are illustrated in Fig.9. The reference active power P_{ref} and Q_{ref} are stated as

$$\begin{cases} V_{\text{p.u.}} = \dfrac{\sqrt{(V_\alpha^+)^2 + (V_\beta^+)^2 + (V_\alpha^-)^2 + (V_\beta^-)^2}}{V_{\text{n}}} \\ 0 \le V_{\text{p.u.}} < 0.5 \begin{cases} P_{\text{ref}} = 0 \\ Q_{\text{ref}} = P_{\text{pr}} \end{cases} \\ 0.5 \le V_{\text{p.u.}} < 0.9 \begin{cases} P_{\text{ref}} = \sqrt{P_{\max}^2 - Q_{\text{ref}}^2} \\ Q_{\text{ref}} = 2(1 - V_{\text{p.u.}})P_{\text{pr}} \end{cases} \\ 0.9 \le V_{\text{p.u.}} \le 1 \begin{cases} P_{\text{ref}} = P_{\text{pr}} \\ Q_{\text{ref}} = 0 \end{cases} \end{cases} \tag{25}$$

where V_{n} is the per unit value of the grid voltage, and P_{pr} is the output active power before a grid fault occurs.

As indicated in Fig.8 and (24), when unbalanced voltage sag occurs, the specific relationships between the output power and output currents are [23]

$$\begin{cases} P(t) = P_0 + P_c\cos(2\omega t) + P_s\sin(2\omega t) \\ Q(t) = Q_0 + Q_c\cos(2\omega t) + Q_s\sin(2\omega t) \end{cases}$$

$$\text{where} \begin{bmatrix} P_0 \\ Q_0 \\ P_c \\ P_s \\ Q_c \\ Q_s \end{bmatrix} = 1.5 \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_q^+ & -V_d^+ & V_q^- & -V_d^- \\ V_d^- & V_q^- & V_d^+ & V_q^+ \\ V_q^- & -V_d^- & -V_q^+ & V_d^+ \\ V_q^- & -V_d^- & V_q^+ & -V_d^+ \\ -V_d^- & -V_q^- & V_d^+ & V_q^+ \end{bmatrix} \times \begin{bmatrix} I_d^+ \\ I_q^+ \\ I_d^- \\ I_q^- \end{bmatrix} \tag{26}$$

where $V_d^+, V_q^+, V_d^-, V_q^-$ are the positive sequence and negative sequence components of the grid voltage in dq axis respectively; $I_d^+, I_q^+, I_d^-, I_q^-$ are the positive sequence and negative sequence components of output currents in dq axis respectively.

As shown in (26), inevitable power ripples occur during unbalanced voltage sag. To suppress the total power ripples of active power and reactive power, specific matrix calculations are conducted below.

According to (26), the total power ripples S_f are deduced as

$$S_f = \sqrt{P_c^2 + P_s^2} + \sqrt{Q_c^2 + Q_s^2} \tag{27}$$

To obtain the minimum value of S_f in (27), P_c and Q_c in (26) are assumed to be 0 in the first place, the corresponding output currents $I_{d1}^+, I_{q1}^+, I_{d1}^-, I_{q1}^-$ are

$$\begin{bmatrix} I_{d1}^+ \\ I_{q1}^+ \\ I_{d1}^- \\ I_{q1}^- \end{bmatrix} = \frac{2}{3} \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_q^+ & -V_d^+ & V_q^- & -V_d^- \\ V_d^- & V_q^- & V_d^+ & V_q^+ \\ V_q^- & -V_d^- & V_q^+ & -V_d^+ \end{bmatrix}^{-1} \begin{bmatrix} P_0 \\ Q_0 \\ 0 \\ 0 \end{bmatrix} \tag{28}$$

By substituting (28) into (26), the relationships between the output power and output currents can be

rewritten as

$$\begin{bmatrix} P_0 \\ Q_0 \\ 0 \\ P_{s1} \\ 0 \\ Q_{s1} \end{bmatrix} = 1.5 \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_q^+ & -V_d^+ & V_q^- & -V_d^- \\ V_d^- & V_q^- & V_d^+ & V_q^+ \\ V_q^- & -V_d^- & -V_q^+ & V_d^+ \\ V_q^- & -V_d^- & V_q^+ & -V_d^+ \\ -V_d^- & -V_q^- & V_d^+ & V_q^+ \end{bmatrix} \begin{bmatrix} I_{d1}^+ \\ I_{q1}^+ \\ I_{d1}^- \\ I_{q1}^- \end{bmatrix} \tag{29}$$

Similarly, assuming that $P_s = Q_s = 0$, the corresponding output currents $I_{d2}^+, I_{q2}^+, I_{d2}^-, I_{q2}^-$ are

$$\begin{bmatrix} I_{d2}^+ \\ I_{q2}^+ \\ I_{d2}^- \\ I_{q2}^- \end{bmatrix} = \frac{2}{3} \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_q^+ & -V_d^+ & V_q^- & -V_d^- \\ V_q^- & -V_d^- & -V_q^+ & V_d^+ \\ -V_d^- & -V_q^- & V_d^+ & V_q^+ \end{bmatrix}^{-1} \begin{bmatrix} P_0 \\ Q_0 \\ 0 \\ 0 \end{bmatrix} \tag{30}$$

Substituting (30) into (26) yields

$$\begin{bmatrix} P_0 \\ Q_0 \\ P_{c2} \\ 0 \\ Q_{c2} \\ 0 \end{bmatrix} = 1.5 \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_q^+ & -V_d^+ & V_q^- & -V_d^- \\ V_d^- & V_q^- & V_d^+ & V_q^+ \\ V_q^- & -V_d^- & -V_q^+ & V_d^+ \\ V_q^- & -V_d^- & V_q^+ & -V_d^+ \\ -V_d^- & -V_q^- & V_d^+ & V_q^+ \end{bmatrix} \begin{bmatrix} I_{d2}^+ \\ I_{q2}^+ \\ I_{d2}^- \\ I_{q2}^- \end{bmatrix} \tag{31}$$

In such cases, assuming that the reference output currents $I_{d\text{ref}}^+, I_{Q_{\text{ref}}}^+, I_{d\text{ref}}^-, I_{Q_{\text{ref}}}^-$ are

$$\begin{bmatrix} I_{d\text{ref}}^+ \\ I_{Q_{\text{ref}}}^+ \\ I_{d\text{ref}}^- \\ I_{Q_{\text{ref}}}^- \end{bmatrix} = \lambda \begin{bmatrix} I_{d1}^+ \\ I_{q1}^+ \\ I_{d1}^- \\ I_{q1}^- \end{bmatrix} + (1-\lambda) \begin{bmatrix} I_{d2}^+ \\ I_{q2}^+ \\ I_{d2}^- \\ I_{q2}^- \end{bmatrix} \quad (0 =\leq \lambda \leq 1) \tag{32}$$

By combining (28)-(32), the output power is

$$\begin{bmatrix} P_0 \\ Q_0 \\ (1-\lambda)P_{c2} \\ \lambda P_{s1} \\ (1-\lambda)Q_{c2} \\ \lambda Q_{s1} \end{bmatrix} = 1.5 \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_q^+ & -V_d^+ & V_q^- & -V_d^- \\ V_d^- & V_q^- & V_d^+ & V_q^+ \\ V_q^- & -V_d^- & -V_q^+ & V_d^+ \\ V_q^- & -V_d^- & V_q^+ & -V_d^+ \\ -V_d^- & -V_q^- & V_d^+ & V_q^+ \end{bmatrix} \begin{bmatrix} I_{d\text{ref}}^+ \\ I_{Q_{\text{ref}}}^+ \\ I_{d\text{ref}}^- \\ I_{Q_{\text{ref}}}^- \end{bmatrix} \tag{33}$$

Correspondingly, the total power ripples are

$$S_f(\lambda) = \sqrt{(1-\lambda)^2 Q_{c2}^2 + \lambda^2 Q_{s1}^2} + \sqrt{(1-\lambda)^2 P_{c2}^2 + \lambda^2 P_{s1}^2} \tag{34}$$

When $dS_f(\lambda_1)/d(\lambda_1) = 0$ $(0 < \lambda_1 < 1)$ holds, it can be derived that $S_f(\lambda_1)$ is the minimum value of $S_f(\lambda)$. According to (34), the reference output currents with the fewest total power ripples can be calculated under the condition where $\lambda = \lambda_1$.

In addition, considering the hard limit of the RMS value of output currents, there is still one more step before obtaining the final current references. To restrain current references within the allowable range, the final reference currents $I_{d\text{reff}}^+, I_{q\text{reff}}^+, I_{d\text{reff}}^-, I_{q\text{reff}}^-$ are scaled down as follows:

$$\begin{bmatrix} I_{d\text{reff}}^+ \\ I_{q\text{reff}}^+ \\ I_{d\text{reff}}^- \\ I_{q\text{reff}}^- \end{bmatrix} = f \begin{bmatrix} I_{d\text{ref}}^+ \\ I_{Q_{\text{ref}}}^+ \\ I_{d\text{ref}}^- \\ I_{Q_{\text{ref}}}^- \end{bmatrix} \left(f = \begin{cases} 1 & k < 1 \\ 1/k & k \geq 1 \end{cases}\right) \tag{35}$$

where $k = \dfrac{\sqrt{(I_{d\text{ref}}^+)^2 + (I_{Q_{\text{ref}}}^+)^2 + (I_{d\text{ref}}^-)^2 + (I_{Q_{\text{ref}}}^-)^2}}{I_{\text{lim}}}$

B. INNER LOOP CONTROLLER

When a grid fault occurs, the equivalent grid impedance and grid voltage change substantially, seriously threatening the stability of the pre-designed inner loop controller. Moreover, the dynamic process of the inner loop controller during grid faults can cause transit fluctuations in the output currents; thus, good robustness and a fast dynamic response of the inner loop controller is required during the LVRT process.

Based on the conventional proportional resonant (PR) controller and harmonic compensators (HC) [30] under $\alpha\beta$ static coordinates, the proposed inner controller is structured as

$$\begin{cases} if\ V_{p.u.} < 0.9 & G_{\text{IN}}(s) = G_{\text{PR1}}(s) \\ else & G_{\text{IN}}(s) = G_{\text{PR}}(s) + G_{\text{HC}(s)} \end{cases} \tag{36}$$

where $G_{\text{IN}}(s)$ is the transfer function of the inner loop controller in the s-domain; $G_{\text{PR1}}(s)$ is the PR controller during LVRT process in s-domain,$G_{\text{PR}}(s)$ and $G_{\text{HC}}(s)$ are the PR controller and HC controller under normal grid conditions in the s-domain, respectively. The expressions of $G_{\text{PR}}(s)$, $G_{\text{HC}}(s)$, and $G_{\text{PR1}}(s)$ are

$$\begin{cases} G_{\text{HC}}(s) = \sum\limits_{h=5,7} K_{rh} \dfrac{2\xi_h h\omega_0 s}{s^2 + 2\xi_h h\omega_0 s + \omega_0^2} \\ G_{\text{PR}}(s) = K_p + K_r \dfrac{2\xi\omega_0 s}{s^2 + 2\xi\omega_0 s + \omega_0^2} \\ G_{\text{PR1}}(s) = k_1 K_p + k_2 K_r \dfrac{2\xi\omega_0 s}{s^2 + 2\xi\omega_0 s + \omega_0^2} \end{cases} \tag{37}$$

where $k_1 > 1$ and $k_2 < 1$. $G_{\text{PR}}(s)$ and $G_{\text{PR1}}(s)$ in (37) provide high open-loop gain at the fundamental frequency to accurately track positive and negative sequence current references at fundamental frequency, whereas $G_{\text{HC}}(s)$ offers precise tuning at n-order ($n = 5, 7$) harmonics to improve the power quality of the output current.

According to (36) and (37), during the LVRT process, the HC controllers are blocked and parameters of the PR controller are modified. Bode diagrams of the open-loop inverter system with the proposed inner loop controller are shown in Fig. 10. Detailed modeling and parameter designs of the inner loop controller can be found in [31], [32].

As depicted in Fig.10, the proposed inner-loop controller has the following advantages during the LVRT process: 1) the

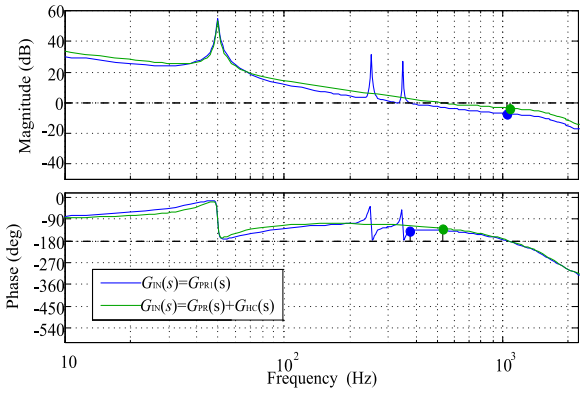

FIGURE 10. Bode diagrams of the open-loop inverter system with the proposed inner loop controller.

phase margin is increased by blocking the HC controllers; 2) the bandwidth is improved by modifying the control parameters of the PR controllers. Therefore, although the tracking accuracy is sacrificed to some extent, better robustness and a faster dynamic response can be expected during the LVRT process for the proposed inner loop controller.

To elucidate improvements in the robustness of the proposed inner loop controller, pole-zero maps of the closed loop system with the proposed inner loop controller when the equivalent grid impedance L_g declines are respectively illustrated in Fig. 11(a) and (b). The pole-zero maps intuitively display the variation tendency of the system stability when L_g declines.

When L_g is reduced in Fig.11 (a), two poles gradually move into the unit circle and then out of the unit circle. The tendency of poles moving into the unit circle in Fig.11 (a) implies sufficient stability margins for the inverter system when a grid fault occurs. By contrast, in Fig.11 (b), the corresponding two poles gradually move out of the unit circle as L_g declines. The poles far from the zero point will inevitably deteriorate the stability of the inverter system.

Therefore, during grid faults, the proposed LVRT inner loop controller enhances the dynamic performance and robustness of the inverter system simultaneously.

IV. EXPERIMENTAL VERIFICATIONS

In this section, the performance of the proposed NLCCF-PLL and the overall proposed LVRT technique are respectively evaluated on the basis of experimental results.

A. PERFORMANCE TEST OF NLCCF-PLL

The performance of the proposed NLCCF-PLL was tested by a comparison based on the prototype controlled by a TMS320F28335 digital signal processor (DSP). In this experiment, the nominal frequency was 50 Hz, and the sampling frequency was fixed at 10 kHz.

Throughout the experimental verifications, the DSP generated the three-phase input signals internally. They were then fed to the external digital-to-analog (D/A) converter AD7808 to generate analog signals. After performing the

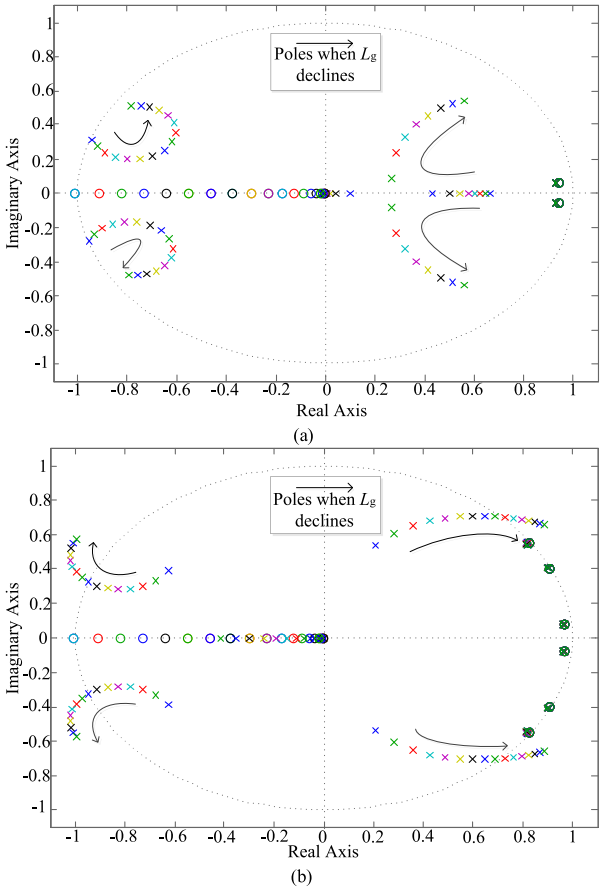

FIGURE 11. Pole-zero maps of the closed-loop system when the equivalent grid impedance L_g decreases. (a) When $G_{IN}(S) = G_{PR1}(S)$. (b) When $G_{IN}(S) = G_{PR}(S) + G_{HC}(S)$.

TABLE 1. Control parameters of PLLs in experiments.

DCCF-PLL	NLADRC-PLL
V_N=200V	V_N=200V
$\hat{\omega}_b$ =2π× 25$\sqrt{2}$ rad/s	$\hat{\omega}_{b\ max}$ =2π× 500$\sqrt{2}$ rad/s
K_p=1	K_{pmax}=20
K_i=100	K_{imax}=200
	K_{pmax}/ K_{pmin} =50
	$\triangle$=30
	ε =5

proposed PLL algorithms with the signals acquired by DSP, the signals were converted by another external D/A converter DAC7724 and finally measured by an oscilloscope.

In the experiments, the PLL performances of the conventional DCCF-PLL and the proposed NLCCF-PLL are compared. Brief introductions and parameter design guidelines for the conventional DCCF-PLL are provided in [12], and parameter design guidelines for the proposed NLCCF-PLL are mentioned in Section II. Control parameters of the PLLs are listed in Table 1, where V_N is the amplitude of nominal voltage of the compared PLLs.

To compare the dynamic and steady-state performances of the above PLLs, the test cases can be summarized as follows:

TABLE 2. Summary of PLL performance in experiments.

	Setting time when frequency error is less than 0.5Hz under test case I (ms)	Setting time when phase error is less than 5° under test case I (ms)	Peak phase error(°)/Peak frequency error (Hz) under test case II
DCCF-PLL	24	21	1.4/1.3
NLCCF-PLL	6	5	0.2/0.2

1) Test case I: The grid voltage undergoes a frequency jump from 45Hz to 55Hz and a phase-angle jump of +60° simultaneously, as illustrated in Fig. 12(a).

2) Test case II: The grid voltage is severely polluted by imbalance and harmonics, as illustrated in Fig. 13(a).

In test case I, the obtained transit frequency responses for compared PLLs are shown in Fig. 12(b). It takes approximately 6ms for the estimated frequency of NLCCF-PLL to reach the quasi-steady state (where the frequency tracking error is less than 0.5Hz). For DCCF-PLL, the time is about 24ms. As indicated in Fig. 12(c), the tracking phase-angle errors (i.e., difference between the real and estimated phase angles) of the NLCCF-PLL and DCCF-PLL converge to less than 5° in 5ms and 21ms, respectively.

As shown in Fig. 12(b) and (c), NLCCF-PLL achieves better dynamic performance when the grid voltage experiences a jump in the frequency and phase angle.

The experimental results of test case II are shown in Fig. 13(b) and (c). The peak frequency offsets in the steady state for DCCF-PLL and NLCCF-PLL in Fig. 13(b) are 1.3Hz and 0.2Hz, respectively. The peak phase-angle tracking errors in the steady state for DCCF-PLL and NLCCF-PLL are Fig. 13(c) is 1.4° and 0.2°, respectively.

As shown in Fig. 13(b) and (c), NLCCF-PLL demonstrates better harmonic and imbalance rejection in the steady state compared with DCCF-PLL.

To further reveal the fast dynamic response and excellent disturbance rejection capability, detailed PLL performances of the compared PLLs under the two test cases are shown in Table 2.

B. PERFORMANCE TEST OF PROPOSED LVRT TECHNIQUE

The proposed LVRT technique is evaluated using an 11kW three-phase grid-connected converter prototype in this section. The proposed converter prototype is controlled by a DSP TMS320F28335. To simulate grid faults, a shunt passive load that contains a nonlinear load, and an unbalanced three-phase passive load, is connected between the inverter and grid. When connected to the grid, the load can generate voltage sag, imbalance and distortion. The adopted nonlinear load is a three-phase diode rectifier with a resistance load at the DC side. The hardware configuration of the laboratory prototype is outlined in Table 3.

In the experiments, the performances of the proposed LVRT technique and the conventional LVRT technique are compared. The proposed LVRT technique is realized as shown in Fig.8. The conventional LVRT technique contains a conventional DCCF-PLL, a positive sequence reference current generator [21] and a PR+HC controller [30].

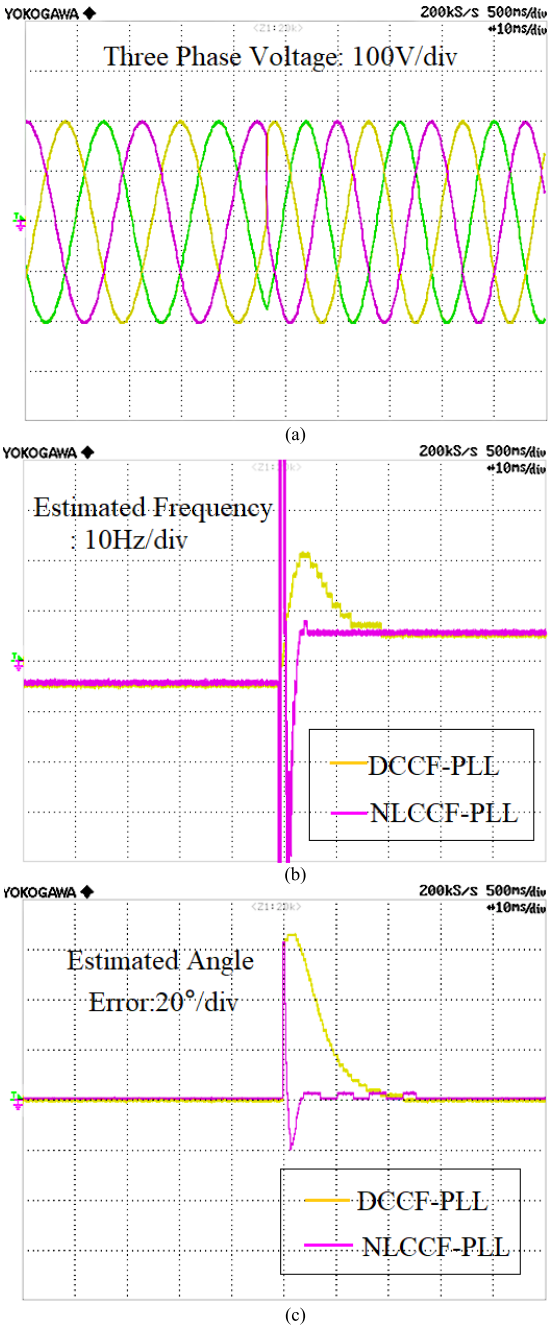

FIGURE 12. Experimental results under test case I. (a) Three phase grid voltage. (b) Transit frequency response. (c) Phase-angle tracking error. (X-axis:10ms/div).

Experimental results of the converter prototype with the above two LVRT techniques are shown in Fig. 14 and 15, respectively.

Fig.14(a) and Fig.15(a) show that the grid voltage circumstances are similar under the two test cases. By comparing the output currents in Fig.14 (b) and Fig.15 (b), it is clear that the

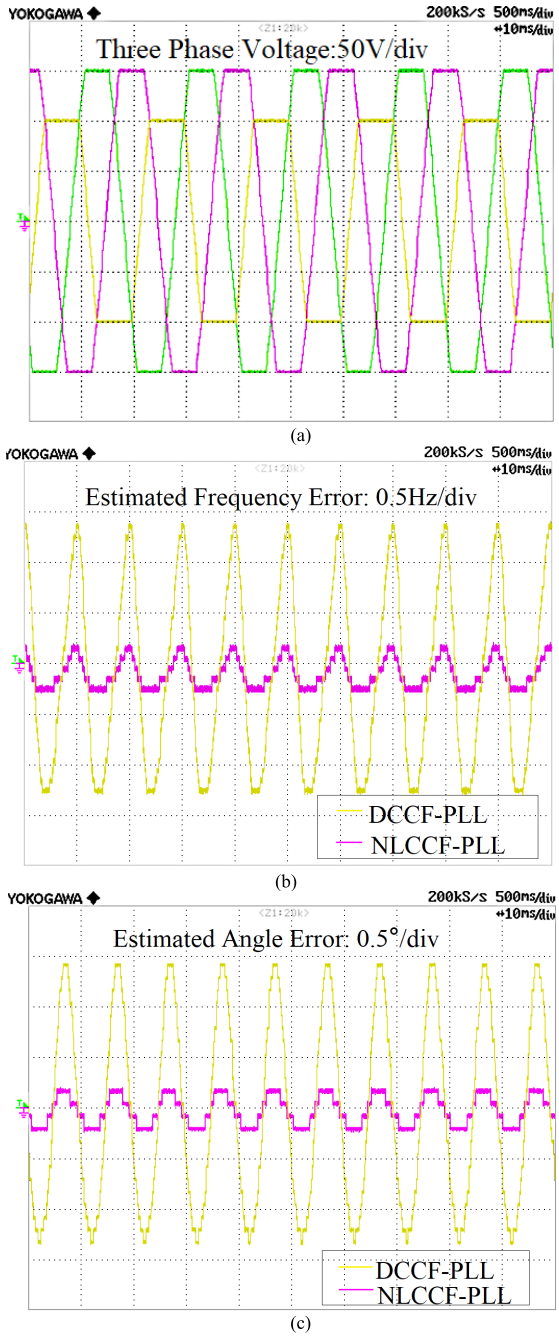

FIGURE 13. Experimental results under test case II. (a) Three phase grid voltage. (b) Estimated frequency error. (c) Estimated angle error. (X-axis: 10ms/div).

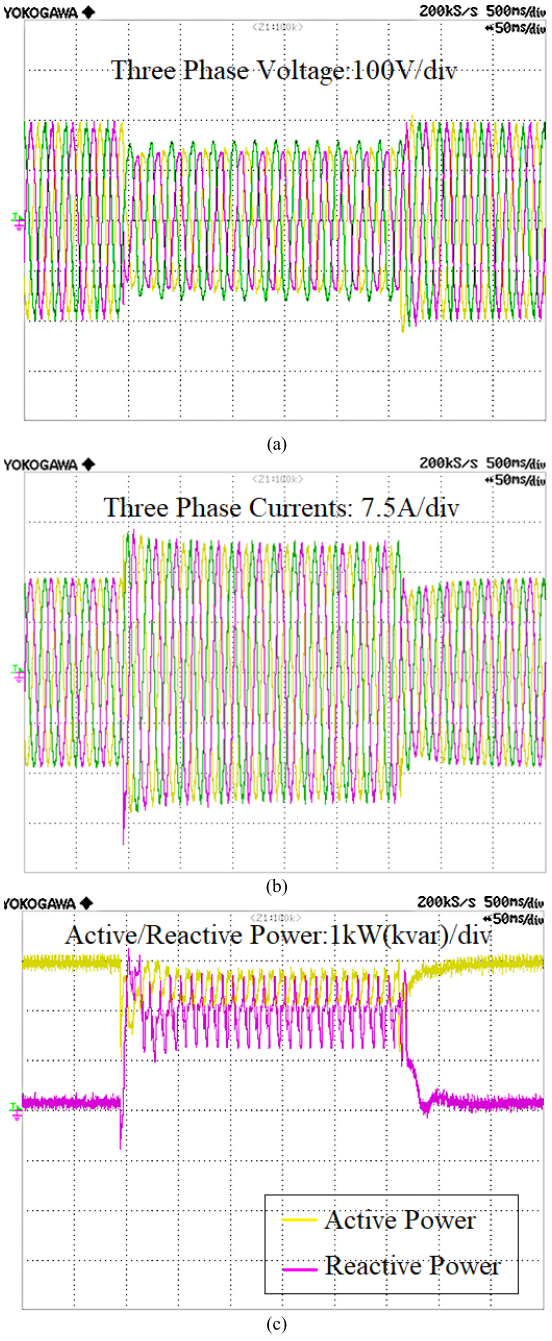

FIGURE 14. Experimental results with the conventional LVRT technique under voltage sag. (a) Grid voltages. (b) Grid currents. (c) Instantaneous active and reactive powers. (X-axis: 50ms/div).

transit fluctuations of the output currents with the proposed LVRT technique are much smaller than those with the conventional LVRT technique during the LVRT process. Thanks to the combination of the NLCCF-PLL and the LVRT inner loop controller in the proposed LVRT technique, the transit current fluctuations are effectively restrained. Moreover, different from the conventional LVRT technique, unbalanced currents are generated by the proposed LVRT technique under unbalanced voltage sag.

In Fig.14 (c), the peak active and reactive power ripples during voltage sag are respectively 1.1kvar and 1.7kvar using the conventional LVRT technique. As shown in Fig.15(c), the peak active and reactive power ripples during voltage sag are respectively 0.6kvar and 0.9kvar with the proposed LVRT technique. In addition, the transit power fluctuations of the proposed LVRT technique are much smaller than those of the conventional LVRT technique during the LVRT process. By adopting the proposed LVRT technique, the steady-state

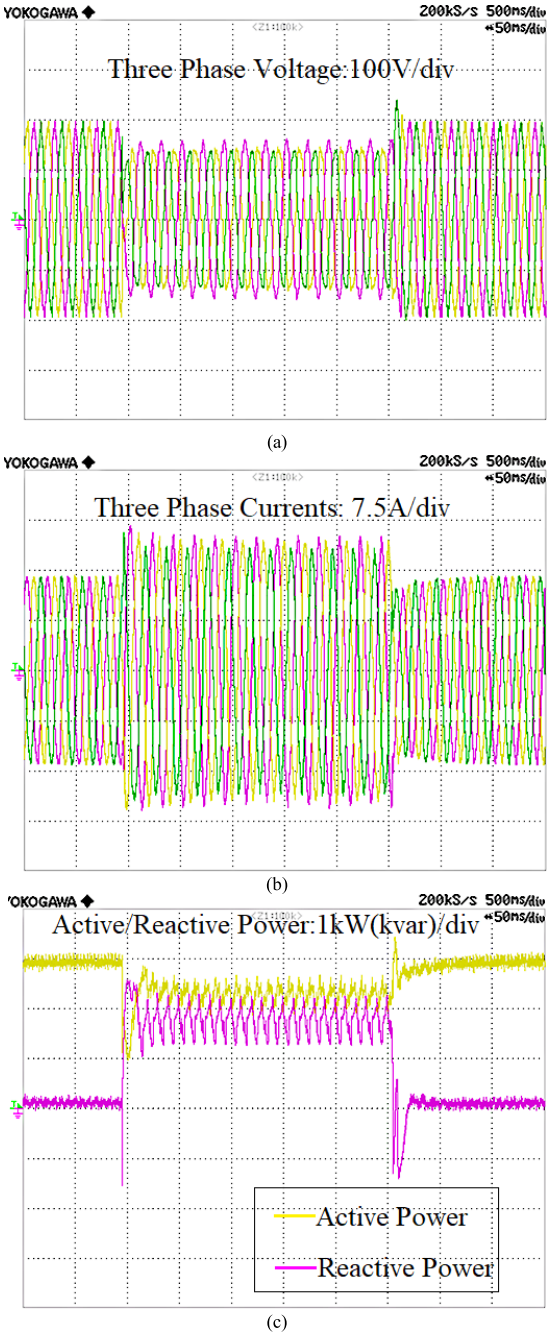

FIGURE 15. Experimental results with the proposed LVRT technique under voltage sag. (a) Grid voltages. (b) Grid currents. (c) Instantaneous active and reactive powers. (X-axis: 50ms/div).

active and reactive power ripples and transit power fluctuations are effectively restrained.

Detailed LVRT performances of the proposed LVRT technique compared with the conventional LVRT technique are shown in Table 4. Compared with the conventional LVRT technique, the proposed LVRT technique can afford grid-connected inverters better dynamic performance in terms of output currents. The ripples in active power and reactive power are also effectively restrained by the proposed LVRT technique as shown in Table 4.

TABLE 3. Experimental parameters of laboratory prototype.

Parameters	Value
System frequency f_0/Hz	50
Switching frequency f_s/kHz	10
DC link voltage U_{dc}/V	290
Rated grid line to line voltage U_g/V	136
Rated output power P_{rate}/kW	6
Output active power before grid fault occurs P_{pt}/kW	3
Converter side inductance of LCL filter L_1/mH	0.3
Grid side inductance of LCL filter L_2/mH	0.2
Capacitor of LCL filter C/μF	100
Damping resistance of LCL filter R/Ω	0.2
Resistance of shunt passive load in each phase R_L/Ω	1/1/2
Resistance at DC side of nonlinear load R_d/Ω	10
Grid inductance L_g/mH	1
Voltage sag duration/ms	250

TABLE 4. Summary of the LVRT performance in experiments.

	Setting time of output currents under grid voltage drop/recovery (ms)	Peak steady-state active power/ reactive power ripples (kVA)	Peak transit current fluctuation (A)
Proposed LVRT technique	31/44	0.6/0.9	3
Conventional LVRT technique	47/62	1.1/1.7	6

V. CONCLUSION

In this paper, a nonlinear three-phase PLL (NLCCF-PLL) with fast dynamic response, enhanced disturbance rejection capability and good robustness, is presented. An LVRT control scheme based on NLCCF-PLL is also proposed. The following conclusions can be drawn:

1) By adaptively adjusting the open-loop gain of the conventional DCCF-PLL according to the magnitude of disturbance, the dynamic performance and steady state filtering capability of the proposed NLCCF-PLL are substantially improved.

2) The proposed NLCCF-PLL is certified to be stable by the second method of Lyapunov, which guarantees a wide range of parameter variations and good robustness.

3) The proposed LVRT control scheme can effectively restrain the overall ripples in active power and reactive power by matrix calculations.

4) The proposed inner loop controller further improves the dynamic performance of the proposed LVRT technique and guarantees good robustness of the inverter system.

The experimental results indicate good performance of the proposed NLCCF-PLL together with the proposed LVRT control scheme, confirming the availability and practical value of the proposed LVRT technique.

REFERENCES

[1] Z. Chen, J. M. Guerrero, and F. Blaabjerg, "A review of the state of the art of power electronics for wind turbines," *IEEE Trans. Power Electron.*, vol. 24, no. 8, pp. 1859–1875, Aug. 2009.

[2] J. Miret, A. Camacho, M. Castilla, L. G. de Vicuña, and J. Matas, "Control scheme with voltage support capability for distributed generation inverters under voltage sags," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5252–5262, Nov. 2013.

[3] *Technical Requirements for Wind Generation Interconnection and Integration*, Gen. Electric (GE) Energy Appl. Syst. Eng.; EnerNex Corp.; AWS Truepower, Independ. Syst. Operator-New England (ISO-NE) Wind Integr. Study, Schenectady, NY, USA, pp. 1–128, Nov. 2009

[4] *Technical Rule for Connecting Wind Farm to Power System*, Standard GB/T 19963, Beijing General Administration of Quality Supervision Inspection and Quarantine and Standardization Administration of China, Beijing, China, 2011.

[5] M. Tsili and S. Papathanassiou, "A review of grid code technical requirements for wind farms," *IET Renew. Power Generat.*, vol. 3, no. 3, pp. 308–332, Sep. 2009.

[6] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg, "Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 127–138, Jan. 2010.

[7] N. Hui, D. Wang, and Y. Li, "A novel hybrid filter-based PLL to eliminate effect of input harmonics and DC offset," *IEEE Access*, vol. 6, pp. 19762–19773, 2018.

[8] R. Chiumeo, A. Porrino, L. Garbero, L. Tenti, and M. de Nigris, "The Italian power quality monitoring system of the MV network results of the measurements of voltage dips after 3 years campaign," in *Proc. 20th Int. Conf. Exhib. Electr. Distrib.*, 2009, pp. 1–4.

[9] S. Golestan and J. M. Guerrero, "Conventional synchronous reference frame phase-locked loop is an adaptive complex filter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1679–1682, Mar. 2015.

[10] H. A. Hamed, A. F. Abdou, E. H. E. Bayoumi, and E. E. El-Kholy, "Frequency adaptive CDSC-PLL using axis drift control under adverse grid condition," *IEEE Trans. Ind. Electron.*, vol. 64, no. 4, pp. 2671–2682, Apr. 2017.

[11] S. Golestan, M. Ramezani, J. M. Guerrero, F. D. Freijedo, and M. Monfared, "Moving average filter based phase-locked loops: Performance analysis and design guidelines," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2750–2763, Jun. 2014.

[12] X. Guo, W. Wu, and Z. Chen, "Multiple-complex coefficient-filter-based phase-locked loop and synchronization technique for three-phase grid-interfaced converters in distributed utility networks," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1194–1204, Apr. 2011.

[13] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg, "A new single-phase PLL structure based on second order generalized integrator," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–6.

[14] P. Xiao, K. A. Corzine, and G. K. Venayagamoorthy, "Multiple reference frame-based control of three-phase PWM boost rectifiers under unbalanced and distorted input conditions," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2006–2017, Jul. 2008.

[15] H. Awad, J. Svensson, and M. J. Bollen, "Tuning software phase-locked loop for series-connected converters," *IEEE Trans. Power Del.*, vol. 20, no. 1, pp. 300–308, Jan. 2005.

[16] F. D. Freijedo, A. G. Yepes, Ó. López, A. Vidal, and J. Doval-Gandoy, "Three-phase PLLs with fast postfault retracking and steady-state rejection of voltage unbalance and harmonics by means of lead compensation," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 85–97, Jan. 2011.

[17] B. I. Rani, C. K. Aravind, G. S. Ilango, and C. Nagamani, "A three phase PLL with a dynamic feed forward frequency estimator for synchronization of grid connected converters under wide frequency variations," *Int. J. Elect. Power Energy Syst.*, vol. 41, pp. 63–70, Oct. 2012.

[18] S. Golestan, E. Ebrahimzadeh, J. M. Guerrero, J. C. Vasquez, and F. Blaabjerg, "An adaptive least-error squares filter-based phase-locked loop for synchronization and signal decomposition purposes," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 336–346, Jan. 2017.

[19] T. Thacker, R. Wang, D. Dong, R. Burgos, F. Wang, and D. Boroyevich, "Phase-locked loops using state variable feedback for single-phase converter systems," in *Proc. IEEE 24th Annu. Appl. Power Electron. Conf. Expo.*, Feb. 2009, pp. 864–870.

[20] S. Golestan, J. M. Guerrero, and J. C. Vasquez, "Three-phase PLLs: A review of recent advances," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1894–1907, Mar. 2017.

[21] P. Rodriguez, A. V. Timbus, R. Teodorescu, M. Liserre, and F. Blaabjerg, "Flexible active power control of distributed power generation systems during grid faults," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2583–2592, Oct. 2007.

[22] X. Song, Y. Wang, W. Hu, and Z. Wang, "Three reference frame control scheme of 4 wire grid-connected inverter for micro grid under unbalanced grid voltage conditions," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Feb. 2009, pp. 1301–1305.

[23] D. Shin, K. J. Lee, J. P. Lee, D. W. Yoo, and H. J. Kim, "Implementation of fault ride-through techniques of grid-connected inverter for distributed energy resources with adaptive low-pass notch PLL," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2859–2871, May 2015.

[24] R. Kabiri, D. G. Holmes, and B. P. McGrath, "Control of active and reactive power ripple to mitigate unbalanced grid voltages," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1660–1668, Mar./Apr. 2016.

[25] V. Kaura and V. Blasko, "Operation of a phase locked loop system under distorted utility conditions," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 58–63, Jan./Feb. 1997.

[26] S. Golestan, M. Monfared, and F. D. Freijedo, "Design-oriented study of advanced synchronous reference frame phase-locked loops," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 765–778, Feb. 2013.

[27] R. Kalman and J. Bertram, "Control system analysis and design via the second method of Lyapunov: (I) continuous-time systems (II) discrete time systems," *IRE Trans. Autom. Control*, vol. 4, no. 3, p. 112, Dec. 1959.

[28] *IEEE Standard for Interconnecting Distributed Resources With Electric Power Systems*, IEEE Standard 1547-2003, Jul. 2003.

[29] T.-F. Wu, M. Misra, L.-C. Lin, and C.-W. Hsu, "An improved resonant frequency based systematic LCL filter design method for grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6412–6421, Aug. 2017.

[30] D. G. Holmes, T. A. Lipo, B. P. McGrath, and W. Y. Kong, "Optimized design of stationary frame three phase AC current regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2417–2425, Nov. 2009.

[31] J. Dannehl, C. Wessels, and F. W. Fuchs, "Limitations of voltage-oriented PI current control of grid-connected PWM rectifiers with *LCL* filters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 380–388, Feb. 2009.

[32] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan, and K. Weng, "Step-by-step controller design for LCL-type grid-connected inverter with capacitor–current-feedback active-damping," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1239–1253, Mar. 2014.

GUANGYU SUN was born in Liaoning, China, in 1990. He received the B.S. degree in electrical engineering from Tianjin University, Tianjin, China, in 2012, where he is currently pursuing the Ph.D. degree with the Department of Electrical Engineering and Automation.

His research interests include the design of grid interface filter for converters, phase-locked loop and control for power engineering applications, and power quality control of the microgrid, and distribution networks.

YONGLI LI was born in Hebei, China, in 1963. She received the B.S. and M.S. degrees in electrical engineering from Tianjin University, Tianjin, China, in 1984 and 1987, respectively, and the Ph.D. degree in electrical engineering from the Universite Libre de Bruxelles, Brussels, Belgium, in 1993.

She is currently a Professor with the Department of Electrical Engineering and Automation, Tianjin University. Her research interests include fault analysis of power systems and fault diagnosis of electrical equipment, protection and adaptive reclosing of EHV/UHV transmission systems, protection and control of the microgrid, and distribution networks.

WEI JIN was born in Shanxi, China, in 1990. He received the B.S. degree in electrical engineering from Tianjin University, Tianjin, China, in 2013, where he is currently pursuing the Ph.D. degree with the Department of Electrical Engineering and Automation.

His research interests include control technology of converters, and power quality control of the microgrid, and distribution networks.

SONG LI was born in Hebei, China, in 1991. He received the B.S. and M.S. degrees in electrical engineering from the Tianjin University of Technology, Tianjin, China, in 2015. He is currently pursuing the Ph.D. degree with the School of Electrical and Information Engineering, Tianjin University, Tianjin.

His research interests include control technology of converters, power quality control of micro-grids and distribution networks, and system stability analysis.

YAN GAO was born in Hebei, China, in 1995. He received the B.S. degree in electrical engineering from Tianjin University, Tianjin, China, in 2017, where he is currently pursuing the M.A.Sc. degree with the Department of Electrical Engineering and Automation.

His research interests include the relay of urban power grid adapted to flexible and controllable power and load.