IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received March 12, 2019, accepted April 8, 2019, date of publication April 17, 2019, date of current version April 30, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2911710

Structure Optimization of Fast Discharge Resistor System for Quench Protection System

KUN WANG[1,2], ZHIQUAN SONG[1], PENG FU[1], WEI TONG[1,2], HUA LI[1], AND XIUQING ZHANG[1]

[1]Institute of Plasma Physics, Chinese Academy of Sciences, Hefei 230031, China
[2]Science Island Branch, University of Science and Technology of China, Hefei 230026, China

Corresponding author: Zhiquan Song (zhquansong@ipp.ac.cn)

This work was supported in part by the Fundamental Research Funds for the Central Universities under Grant WK6030000130, and in part by the EAST Team at the Institute of Plasma Physics, Chinese Academy of Sciences (ASIPP).

ABSTRACT In the quench protection (QP) process of superconducting fusion devices, the operating reliability and efficiency of power components are affected by stray parameters of the fast discharge resistor (FDR) system, especially the system stray inductance. In this paper, the fundamental condition of the QP operating process and the large power FDR system structure layout for the Large-scale Superconductor Test Facility (LSTF) are presented. The negative affected VCB, CPC circuit action, and the energy discharging process are further analyzed. The stray inductance optimization method of the resistor module and structure connections are proposed to reduce the stray inductance value. Finally, the optimization results are presented by the Q3D module of the FEA software.

INDEX TERMS Quench protection, superconducting, fusion, fast discharge resistor, structure, stray inductance.

I. INTRODUCTION

With the rapid evolution of the technology of customized superconducting magnet in fusion area, it is crucial to conduct effective test for the superconducting magnet load. The main characteristics of testing object includes large electromagnetic force, complicated structure and especially huge energy [1]. Facing such testing condition, Institute of Plasma Physics, Chinese Academy of Sciences (ASIPP) is constructing the Large-scale Superconductor Test Facility (LSTF) to provide testing environment, especially directly works for the new generation of fusion device: the Comprehensive Research Facilities in Support of CFETR. This test facility is with the maximum magnetic field of 15 T, rated current of 90 kA, magnetic field rate of 1.5 T/s. And the testing range of the customized superconducting magnet load can be up to 2 H for the load inductance, 90 kA for the rated current and 9 GJ for the energy. As shown in the table 1, compared with the other fusion devices such as EAST, ITER, KSTAR and JT60, the LSTF asks for a higher current demand which requires a new power supply and protection system beyond current power capacity [2]–[5].

The associate editor coordinating the review of this manuscript and approving it for publication was Sing Kiong Nguang.

TABLE 1. Parameter of different quench protection system.

Item	EAST	ITER	KSTAR	JT60-SA	LSTF
Rated Voltage	2 kV	10 kV	8 kV	5 kV	20 kV
Rated Current	15 kA	70 kA	40 kA	25.7 kA	90 kA
Energy Load	0.4 GJ	41 GJ	0.5 GJ	1 GJ	9 GJ

As an important part of the power protection system, the QP system is responsible for energy transferring and consumption from the superconducting magnet. When the LSTF platform works in the normal operation, large current flows through the superconducting magnet and DC protection switch. However, once the quench phenomenon happens, huge electromagnetic energy stored inside will be converted to heat energy, or else the irreversible damage will be produced in the superconducting magnet load. Therefore, the energy is required to be transferred out quickly and consumed by the Fast Discharge Resistor (FDR) system within the specific time according to the QP requirement of superconducting magnet load [6], [7].

In the LSTF platform, the circuit structure of the QP system and the action sequence are shown in Fig. 1. When quench happens, the main circuit is opened and the transferring

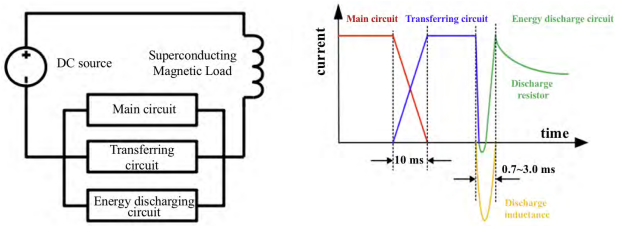


FIGURE 1. Circuit structure and current change diagrams of the QP system for LSTF platform. Each circuit currents change with the power breaker actions and finally the quench current was damping with FDR system's energy consumption.

circuit is closed with load current shifting, after the blocking performance of main circuit is recovered, the load current turns into energy discharging circuit along with load-energy consumption and transferring circuit switch off.

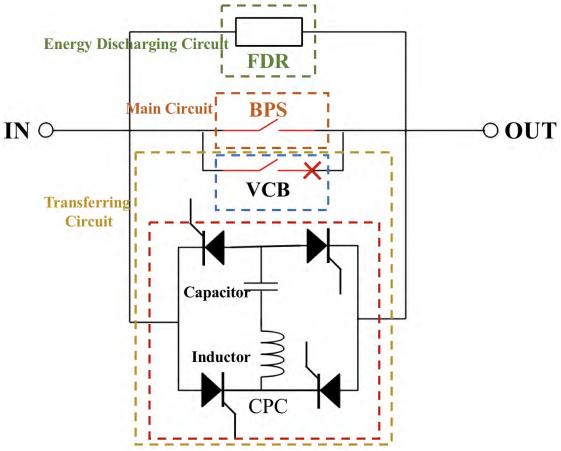


FIGURE 2. Detailed circuit topological scheme without back protection of QP system. Each power components are circled to show the belonging of the circuit.

The detailed circuit topological scheme without backup protection breaker of QP system is shown in Fig. 2. The operating principle is summarized as follows (BPS: Bypass Switch; VCB: Vacuum Circuit Breaker; CPC: Counter-pulse Capacitor Unit):

1. During the normal operation, BPS and VCB are all closed, the BPS carries large current flowing due to the equivalent internal resistance of BPS is far less than that of the VCB;

2. When quench happens, BPS firstly opens and produces sufficient voltage to enable the large current turn into VCB;

3. After BPS reaches zero current, the reversed current is produced by CPC to neutralize the large current in VCB and make the VCB open. The CPC is composed of capacitor and inductor to generate counter pulsed current;

4. After the VCB is reliably switched off, the energy discharging circuit comes into operating state and the magnet energy is transferred into the FDR system, consequently reducing the current to zero and protecting the magnet load.

From the steps above, it can be seen that the FDR system plays a key role in bearing and consuming the large energy in the last step of energy discharging in the QP process. According to the testing requirement of the LSTF platform in the full-load condition, the FDR system is required to provide the energy consumption capability of 8.1 GJ. With the system cooling and structure stability consideration for such large energy, the FDR system consists of 9 resistor stacks connected. Each resistor stack with 1 GJ energy consumption (to be safety, each stack has a safe margin of 10%, therefore, 9 GJ energy in total) is composed of 30 resistor module. To connect all the resistor module into a whole stack and all the stacks into the FDR system, the metal bus must be placed in a right position to keep a good current flowing as well as the structure stability. However, the bus connection for the resistor module also brings stray inductance, which has negative influence not only on the FDR system itself but also on the CPC and the VCB [8]. Therefore, the stray inductance produced in the system should be reduced to improve the operating satiability. The stray inductance optimization is requested by the specific design of structure, layout and connection mode in the FDR system.

In this paper, stray inductance optimization concerning about the structure of FDR system is proposed and simulated to provide improved operating condition in the QP system. Firstly, the operation sequence of the QP process in the LSTF, especially the fast discharge process is introduced, and the power parameters and space layout requirement of the FDR system are refined in the QP system as well. Then the increased variance of stray inductance, both of the resistor module and the bus connections are analyzed for the negative impact on CPC and VCB. The appropriate stray inductance value is discussed and proposed for the design requirement of the FDR system. Lastly, the full-scale structure simulations of system stray inductance are performed and compared, and the design solutions for the system inductance optimization are presented.

II. STRUCTURE DESIGN CONDITION

The FDR system, whose size is about 20 m × 4 m × 3 m (length × height × width) for the space layout requirement as shown in Fig. 3. This system is composed of 9 resistor stacks

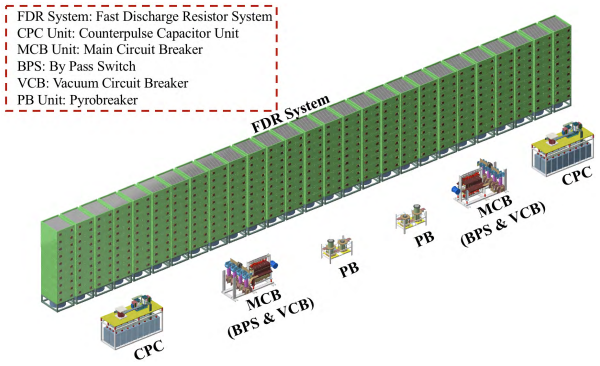


FIGURE 3. The QPsystem space layout and resistor stack structure. Two sets of the CPC, MCB and PCB are placed in the row arrangement, the FDR system shared for the two set is placed on the back.

with forced air ventilation for cooling down. For different superconducting magnet load, the FDR system with specific connection is required to provide the resistance and energy consumption values to control the transferring time duration and the temperature rise so as to meet the QP requirement.

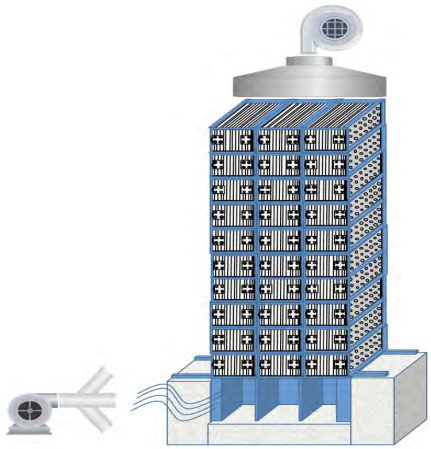


FIGURE 4. Single resistor stack scheme. Each single resistor stack is composed by 30 resistor module arranged with current joint connection. The inlet and outlet of air-flowing is to work for cooling down the temperature of the inner resistor material.

When the superconducting magnet is under full-load condition, the FDR system will be required to form 0.1 Ω resistance value with 9 resistor stack connecting in series and parallel arrangement. Each resistor stack consists of 10×3 resistor module matrices, which is shown in Fig. 4. In this structure, the stray inductance of the FDR system comes from three parts: the resistor itself made of metal material, the metal bus connection between each resistor module, and the metal bus connection between each resistor stack.

In the QP system, the magnetic shielding cable is used as the in-out connection between the FDR system and other components. And copper buses are used as connections between each module and stack. Due to the metal material resistor arranged inside case of each resistor module is out of the safety operation temperature under large current, so the forced-air ventilation method (air flowing from bottom to top) is used for internal metal cooling. Under the maximum current of 90 kA, the metal bus must be carefully designed to protect from overheat and deformation. The heat transferring ability of copper is much better than that of the stainless steel. Therefore, the metal connection between each module and stack are stuck to the joint of resistor module and has no need for cooling with right shape.

III. STRAY INDUCTANCE IMPACT ANALYSIS

During the fast discharge process, the stray inductance of the FDR system will produce negative impact on three parts: Energy consumption of FDR itself; VCB feasibility under overvoltage; CPC capacitor feasibility under overvoltage.

A. THE ENERGY CONSUMPTION OF FDR SYSTEM

In the LSTF platform, the designed power parameter range of the superconducting magnet load is approximately: $0 \sim 2$ H, $0 \sim 90$ kA. For the FDR system, the nominal maximum energy consumption of the superconducting magnet load is 9 GJ with safety margin in the full-load condition. To meet the requirement of QP, the energy stored inside magnet load must be transferred outside in specific time. However, when large inductance emerges in the FDR system, the decay time of the large current flowing from the magnet load to the FDR system. In such circumstance, over-heated will be happed in somewhere of the superconducting magnet load [9].

When the superconducting magnet has large inductance value, the stray inductance of FDR has slight influence on the energy transferring process. On the contrary, in the case of the testing superconducting magnet load with small inductance value, the stray inductance of the FDR system imposes significant negative impact on the magnet load.

The large stray inductance brings significant time delay for current decay in the case of the small inductance magnet load. It will lead to the over-heated damage inside magnet load. To address the issue of effective energy transferring, the inductance of the FRD system is expected to be as less as possible. To clear illustrate the issue, the dummy superconducting magnet load with 5 mH inductance and 10 kA rated current in the Experimental Advanced Superconducting Tokamak (EAST) is taken as example. The current decay time of the load is about 6 s as shown in Fig. 5. Without considering the inductance variance under current change, the current decay speed of the process with stray inductance of 50 μ H is slower than that of without stray inductance in the QP circuit. The sharpest current drop could reach 350 A during the process, which may produce damage on the superconducting magnet load. Therefore, the stray inductance in the system is expected as less as possible.

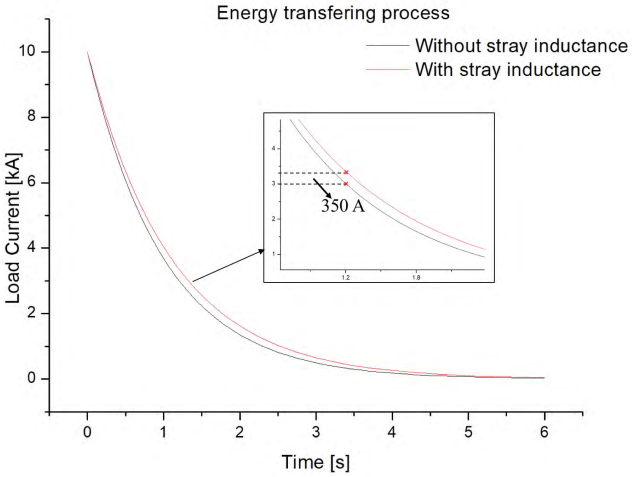


FIGURE 5. Current discharge process of dummy superconducting magnet load. Two waveforms are plotted to show the current quantitative difference of condition with/without stray inductance of the FDR system.

B. THE VCB FEASIBILITY WITH STRAY INDUCTANCE

In the transferring circuit, the VCB is in parallel connected with the FDR system. The voltage of VCB varies with the FDR system voltage change in the QP process, so the peak voltage caused by the stray inductance under fast-changing current must be decreased. A large amount of previous theoretical analysis and experimental work proved that the VCB is determined by the product of current and voltage rate of change at the moment of CPC zero current [10]. Therefore, in order to promote VCB feasibility at breaking moment, reducing the parameter value of di/dt_0 and du/dt_0 is of significant importance at the critical point of zero current.

At the moment of VCB turning-off, the voltage of VCB reaches the highest level, which may lead to the breakdown of the vacuum gap and the failure of breaking action [11]. Therefore, if there is a high value of the stray inductance in the fast discharging circuit, the reversing recovery voltage increases accordingly, which may reduce the reliability of the fast discharging process.

In the ideal operating process of VCB turning-off, the contact terminal of VCB is split into the certain distance and the CPC is forced to provide counter-pulsed current i_c to reduce the VCB current into zero gradually in short time.

Suppose that the CPC switch closes at t0 moment and VCB current i_V reaches zero at t1 moment. During this process, the fast discharging circuit equation is:

$$\begin{cases} i_V = I + U_{C0}\sqrt{\dfrac{C}{L}}\sin\left(\sqrt{\dfrac{1}{LC}}\,(t-t_0)\right) \\ i_C = -U_{C0}\sqrt{\dfrac{C}{L}}\sin\left(\sqrt{\dfrac{1}{LC}}\,(t-t_0)\right) \\ u_C = U_{C0}\cos\left(\sqrt{\dfrac{1}{LC}}\,(t-t_0)\right) \end{cases} \tag{1}$$

where, i_V and i_C are respectively currents of VCB and capacitor. U_{C0} is the initial voltage of capacitor, u_c is the voltage of capacitor. C is the capacitance of capacitor. L is the inductance of inductor.

Refer to (1), the voltage and current waves of each branch in the QP system with no stray inductance of FDR are shown in Fig. 6 and 7, respectively.

Suppose the arc extinguishes of the VCB without stray inductance in the circuit at t_1, two current flowing paths (transferring circuit and fast discharging circuit) are interacted for the reversing recovery-voltage characteristics. This process is described in (2).

$$L\frac{d^2i_c}{dt^2} + R_{dc}\frac{di_c}{dt} + \frac{1}{C}i_c = 0 \tag{2}$$

where, R_{dc} is the resistance of the FDR system.

When there has stray inductance L_{dc}, the fast discharging circuit equation is:

$$\begin{cases} I_{L0} = i_{RD} + i_C \\ \dfrac{1}{C}\int i_C dt + L\dfrac{di_C}{dt} = R_{dc}i_{RD} + L_{dc}\dfrac{di_{RD}}{dt} \end{cases} \tag{3}$$

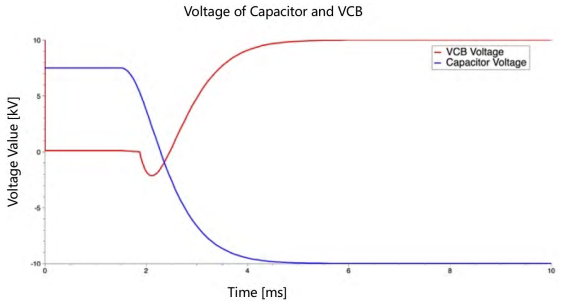


FIGURE 6. Voltage waveforms of capacitor and VCB in QP system. The ideal condition for the capacitor and VCB voltages are within the required voltage limitation so that the damage on the power units will be reduced.

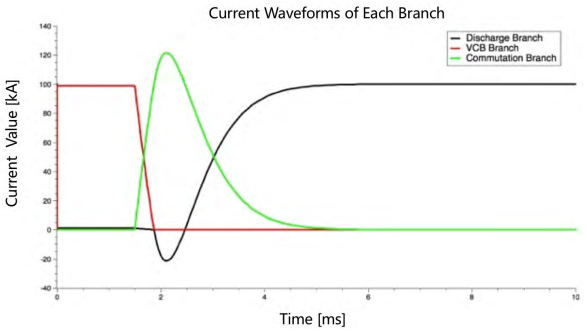


FIGURE 7. Current waveforms of each branch in QP system. The current flowing path and the current value are in correspondent with the voltage change. The commutation branch current is slightly larger than that of the VCB branch so as to effectively neutralize breaker current in VCB.

Equation (3) can be rewritten as:

$$\begin{cases} (L + L_{dc})\dfrac{d^2i_c}{dt^2} + R_{dc}\dfrac{di_c}{dt} + \dfrac{1}{C}i_c = 0 \\ u_{VCB} = R_{dc}i_{RD} + L_{dc}\dfrac{di_{RD}}{dt} \end{cases} \tag{4}$$

where u_{VCB} is the voltage of VCB. I_{L0} is the initial inductor current.

To make the study one step further, the qualitative analysis of current and voltage is performed, which is outlined as follows:

1. As current is unable to vary sharply under the condition of stray inductance constraints, the voltage of fast discharging circuit increases dramatically at the moment of current transferring into the FDR system. Consequently, the voltage rate of current du/dt is enlarged and the peak voltage of fast discharging circuit increased as well.

2. Provided that there is no stray inductance in the FDR system, the VCB and BPS recovery voltages in parallel with the FDR system are consecutive. However, when the stray inductance emerges, the voltage of VCB is enlarged along with the increment of the voltage variation rate and the peak voltage of VCB also increased.

In the Fig. 8, the variation curves of the VCB voltage is plotted with respect to time when different stray inductance values of the FDR system are chosen.

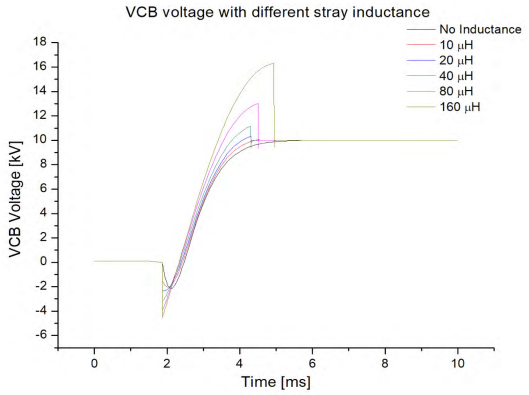


FIGURE 8. VCB voltage with different stray inductancs. The VCB voltages with different stray inductance values will be influenced which may result in th irreversible damage when surpasses the safety voltage.

C. THE CPC CAPACITOR FEASIBILITY

When the current flows through the fast discharge circuit, the capacitor is charged in the corresponding branch inversely. Therefore, the energy stored inside the stray inductance of the FDR system is transferred into the capacitor in the form of electricity and eventually the reverse charging voltage is increased. If the reverse charging voltage surpasses the rated voltage for a long time, the life-time and decay speed of charging voltage of the capacitor will be degraded to a large extent [12].

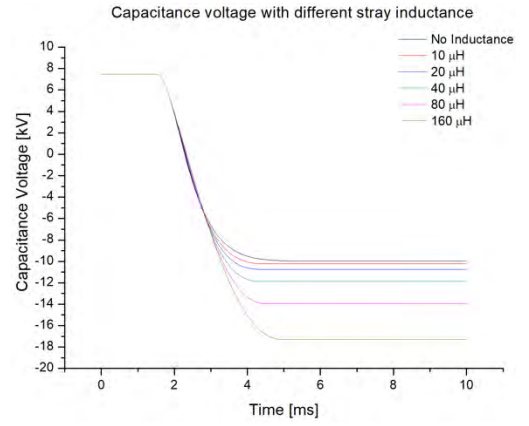


FIGURE 9. Capacitor voltages with different stray inductances. The capacitor in the CPC unit will be damaged when the revised voltage goes higher and be larger than the protection voltage. In the figure, the more the stray inductance in the system, the larger of the revised voltage on the capacitor will get.

The variation curves of the capacitor voltage in the CPC circuit is plotted in the Fig.9 with respect to time when different stray inductance values of the FDR system are chosen.

From Fig. 9, it can be concluded that the reverse recovered voltage of the capacitor in the CPC circuit reaches higher with the increment of the FDR stray inductance and could get damaged once the value exceeds the safety value of reversed voltage.

TABLE 2. Comparison of each branch voltage under different stray inductance.

Stray Inductance	VCB Peak Forward Recovered Voltage	VCB Peak Reversed Recovered Voltage	Capacitor Peak Reversed Recovered Voltage
10 μH	10.03 kV	-0.95 kV	-10.00 kV
20 μH	10.09 kV	-1.31 kV	-10.20 kV
40 μH	10.62 kV	-1.79 kV	-11.01 kV
80 μH	12.17 kV	-2.21 kV	-12.85 kV
160 μH	15.24 kV	-2.50 kV	-16.06 kV

From Fig. 8, it can be seen that the final stable voltages under different stray inductances are around 10 kV. The recovered voltages of each branch with respect to different values of stray inductance are summarized in Table 2. The voltage values monotonically increase with the larger value of stray inductance. According to the numerical calculation results on capacitor, the voltage variation is controllable and acceptable if the stray inductance of FDR is less than 40 μ H, which is in accordance with the requirement.

IV. STRAY INDUCTANCE OPTIMIZATION

The stray inductance is generated by the connecting lead, resistor structure, bus, bolts, insulating casing and other components in the FDR system. When current flows through the system, the magnetic sense is formed to resist the current. The stray inductance of FDR system is depend on the different structure [13].

However, the stray inductance analysis of the FDR system is a difficult task due to the complicated structure. Each resistor module and stack have intricate influence on each other, so that the design of FDR system concerning the stray inductance should be carried out level by level. According to the analysis described above, the stray inductance is expected to be as low as possible. The effective way to reduce the stray inductance is to optimize the module structure, overall layout and the connection mode.

The stray inductance optimization process of the FDR system is conducted from resistor module, stack to the overall system. Each level of stray inductance of the FDR system is comprehensively analyzed within the process of model construction and inductance simulation using the FEA software.

A. RESISTOR MODULE STRAY INDUCTANCE

The metal resistor surrounded by the epoxy case comprises 138 pieces of 304 stainless steel (SUS304) slice in the series arrangement. The stray inductance of the module mainly includes two parts: the metal resistor slice and the module joint.

For the metal resistor slice, the inductance of single resistor slice is determined by its self-inductance and mutual-inductance with all the rest resistor slice. And the whole inductance of the metal resistor is composed of all the self and mutual inductance by the slices. The inductance

optimization process focuses on the resistor material shape and welding method of the module structure.

The resistor slices in single module are connected by edge welding into series connection and the opposite-direction current flowing through each neighboring resistor slice can neutralize mutual inductance. According to the calculation theory of inductance on self and mutual inductance of linear conductors [14], the self-inductance of single resistor slice is calculated by:

$$\begin{cases} L_{self} = 2l[\log \dfrac{2l}{R_1} - 1] \\ \log R_1 = \log b - \dfrac{3}{2} \end{cases} \tag{5}$$

where R_1 is the mean geometrical distance, l and b are respectively the length and width of single resistor slice.

The mutual inductance of two neighboring resistor slice with distance d is:

$$\begin{cases} \log R_2 = \dfrac{d^2}{b^2} \log b + \dfrac{1}{2}(1 - \dfrac{d^2}{b^2}) \log(b^2 + d^2) \\ \qquad\qquad +2\dfrac{d}{b} \tan^{-1} \dfrac{b}{d} - \dfrac{3}{2} \\ L_{mutual} = 2l[\log \dfrac{2l}{R_2} - 1] \end{cases} \tag{6}$$

where R_2 is the mean geometrical distance of two neighboring resistor slice.

As the self and mutual inductance of every resistor slice cannot be eliminated due to the designed structure, the feasible way to reduce stray inductance of the resistor module is to change edge-welding pattern. According to the experience theory on current flowing arrangement inside the body and surface [15], the stray inductance of the resistor slice is relatively small when the connection part smoothly welded. Therefore, similar-zigzag is applied to welding in consideration of manufacturing process. The overall inductance of resistor slice is simulated by the ANSYS Q3D Extractor. In the simulation process, the inductances of resistor slice with real scale are 1.0664 μ H and 1.1851 μ H, respectively, with discrepancy in similar-zigzag and perpendicular welding method as shown in Fig.10. Besides, there are still other welding methods. However, it is uneconomical to adopt other welding methods even less stray inductance value due to economical and timing cost of complicated process.

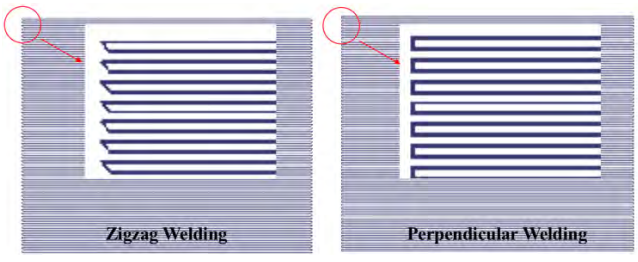


FIGURE 10. The resistormodule inductance under different welding methods. Two frequently-used shapes for the edge welding are expressed to compare the stray inductance value. And the zigzag welding in the left image has less stray inductance.

For the module joint, it is stuck on the case with connecting the two outermost resistor slice. The copper metal is adopted as the material for the joint due to its low contact resistivity. On the basis of joint immobilization and inductance optimization, three selected joint configurations are selected for the structure. The design with omitting the bolt and hole on the copper joint are: copper joint welding onto the outermost resistor slice directly, copper joint welding onto the short-extended arc-like resistor slice, and copper joint welding onto the long-extended arc-like resistor slice. The three resistor joint shape are plotted in the Fig. 11, respectively. And the current flowing scheme are illustrated as well.

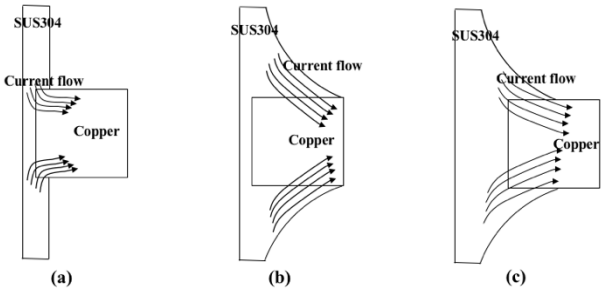


FIGURE 11. The current flowing in the different configuration of joint. With the right shape and connection mode, the configuration which makes the current flow fluent can make smaller stray inductance as figure (c).

The current flowing from the SUS304 resistor slice to the copper joint can be regarded as countless tiny conductor current overlaid in two directions [16]. Therefore, the stray inductance value of joint should be smaller when the current flowing path broaden as the number of tiny current line connected in parallel increases.

By different types of connection mode between the resistor slice and the current joint, the comparative stream structure could provide better current flowing fluency thus to reduce the stray inductance value. Therefore, the type (c) in the Fig. 11 has the relative smaller stray inductance value.

To verify the theory analysis result, the structures with different joint configuration are simulated. As shown in Fig. 12, provided that the ideal welding contact, the stray inductances of the whole resistor module are 1.0886 μ H, 1.0844 μ H and 1.0831 μ H, respectively. According to the theoretical analysis and simulation results above on the stray inductance, design of copper joint welding onto the long-extended arc-like resistor slice is adopted to obtain less stray influence, and the applied approach is demonstrated in Fig. 12(c).

B. RESISTOR STACK STRAY INDUCTANCE

Each resistor stack of FDR system is composed of 30 resistor modules arranged in series and parallel connections. Each stack is connected by a copper bus fixed on the joint of the resistor module. In terms of the full-scale design requirement of the FDR system, three resistor modules (one group) are

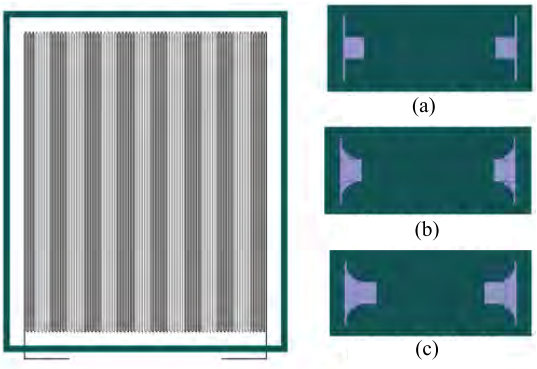


FIGURE 12. The inductance of different configuration of joint: The left is top view of full-sized structure and the right three are the inductance value under different joint configuration. The simulated stray inductance value is listed on the figure as well.

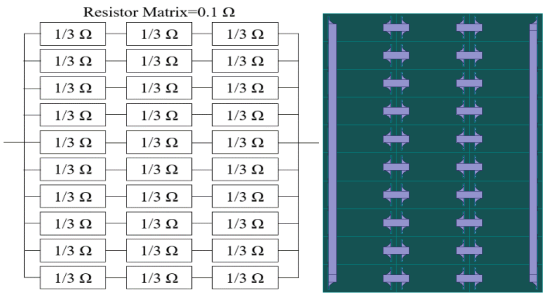


FIGURE 13. Resistor stack connection diagra. (a) Logic scheme diagram (b) structure scheme diagram. The basic connection for the full-load condition is make 30 resistor module into three-in series and 10 in parallel connecting mode.

set up with series connection, and then 10 identical groups are connected into one stack. The diagram is shown in Fig. 10(a). As demonstrated in Fig. 10(b), each three-resistor module in the same horizontal location are arranged-in-series by the neighboring joint connection and then each ten-resistor module joint in the same vertical position are connected by a perpendicular bus.

The inductance of resistor stack comes from two parts, the inductance produced by the resistor slice between intra and inter-module, and the bus connected each resistor module. For the first part, the value is fixed as the structure and location of each resistor module is unchangeable. For the second stray inductance, the value varies with the in-out current location variation of the bus structure which changes the current flowing path. Due to the relationship between magnetic field and inductance above, the connection mode connecting in the middle part from the two sides is the best choice as they can centralize the magnetic intensity under symmetry current flowing.

The simulation of inductance calculation is carried out by using the Q3D tools. The whole stray inductance calculation includes resistor slice self and mutual inductance, joint inductance, bus inductance and other inductance. Four different styles of buses and current joint point settings are proposed and simulated. The simulation results are shown in Fig. 14.

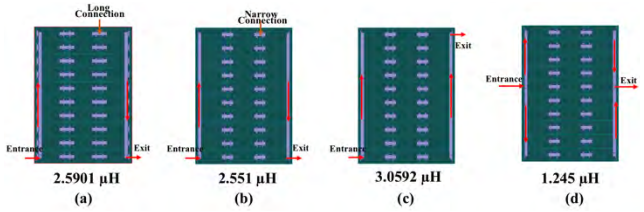


FIGURE 14. Inductance simulation of resistor stack. Figure (a) and (b) are shown the difference in the length of connection bus, respectively. Figure (c) and (d) are shown the different current connection position change for the resistor stack to analyze the stray inductance value change. The simulated values are also listed to the each figures.

According to the simulation results demonstrated in Fig. 14(a) and (b), the stack with long-connection(the length between two neighboring resistor joints) bus between the subsequent two resistor modules has slightly larger inductance than that of the narrow connection. It is certified by the relevance that the inductance value grows larger with more area of metal, as the self and mutual inductance of the metal increased. In addition, the inductance value during the operating process is also relevant to the current flowing direction, which is determined by the current inlet and outlet. From Fig. 14(b), 14(c) and 14(d), it can be seen that the current flowing path determined by the metal joint of entrance and exit is able to increase or counteract the magnetic distribution, so as to increase or decrease the stray inductance value.

As shown in Fig. 14(c), the superimposed magnetic field made by the current flowing through the vertical bus produces a larger inductance value, while the neutralized magnetic field yielded by the opposite current can make an overall relatively small inductance. And the magnetic field is dispersed and reduced when the current enters and exits from the central part of the vertical bus, so that the stray inductance is eliminated to a large extent due to the current diffusion illustrated as shown in Fig. 14(d). Therefore, the structure shown in Fig. 14(d) can well meet the requirement in consideration of both the stray inductance and the design solution.

C. FDR SYSTEM STRAY INDUCTANCE

Under the full load condition, the FDR system, constituted of 9 resistor stacks, is required to form a resistance of 0.1 Ω. The connection mode between each resistor stack is three stack arranged-in-series followed by parallel connecting or three stack arranged-in-parallel followed by series connecting as shown in the Fig. 15.

According to the series and parallel connection law of inductance, the overall inductance of the FDR system are identical without considering the system stray inductance. Therefore, in terms of the system inductance optimization, the key factor lies in the connection mode determining the overall inductance by bus layout. Based on the space arrangement of the FDR system, the layout of 9 resistor stack is placed in one row so that the resistor stack connected by metal bus can be arranged as close as possible, which is illustrated in Fig. 16.

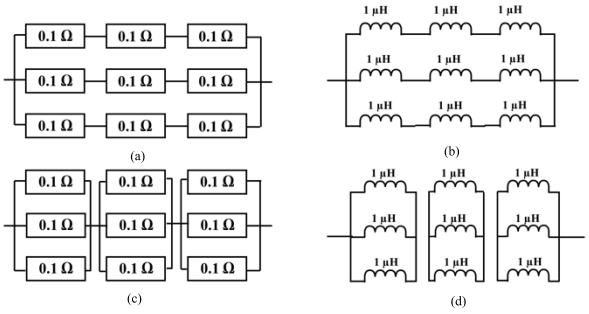


FIGURE 15. Topological scheme of FDR system connection mode. Figure (a) and (b) are corresponding group which shows the series-then-parallel connection mode. Figure (c) and (d) are another corresponding group which shows the parallel-then-series connection mode.

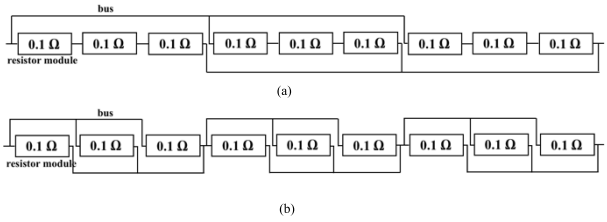


FIGURE 16. Schematic diagram of different connection modes. As the resistor stack in the FDR system are placed in the row layout on the ground, the different connection mode would have the dissimilar layout of the connecting bus. The two different connection modes as illustrated followed the figure 15 are presented in the figure (a) and (b), respectively.

As illustrated in Fig. 16, if all the resistor stack are placed in row arrangement, the parallel connection mode needs more metal bus connection. Every three resistors are grouped into a block via series or parallel connection, and then the FDR system is finally made up by these constructed blocks.

In Fig. 16(a) and 16(b), the series-parallel connection mode requires a long-connection between each stack which brings more metal path for stray inductance. Therefore, the parallel-series connection mode are selected and the certification of simulation process will be shown in the following.

By the mode in the FDR system, three resistor stacks are firstly connected in parallel arrangement. The adjustable part in three resistor stack is to change the bus connection location due to the stationarity of each resistor stack. The stray inductance of the bus connection arises from the magnetic field produces by current flowing. So, the layout counteracting the mutual magnetic effect is the key to reduce the overall stray inductance value. Similar to the analysis on the single stack, the bus connected to the module joint in the central position of the stack can form the spitted current flowing up and down. The magnetic field is neutralized by the symmetric layout bringing opposite current direction. The stray inductance can be reduced when compared to the structure of bus connections on the top and base as shown in Fig. 17(a) and (b).

In Fig. 17 four different parallel connection arrangements is plotted: (a) the top and bottom module joint are respectively connected for the inlet and outlet of the current flowing;

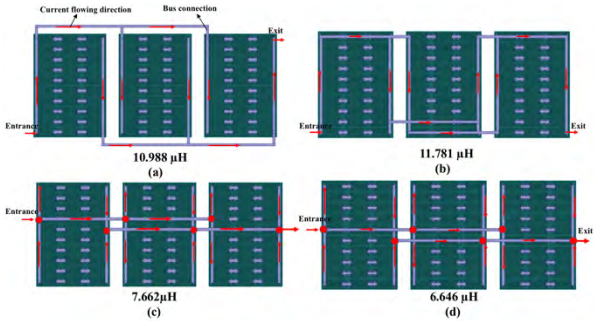


FIGURE 17. Inductance of parallel connection arrangement. Figure (a) and (b) show the uppermost and lowermost connection but with different current outlet position. Figure (c) and (d) shows the different connecting position in the middle of the bus. The connecting position of figure (d) is in the exact middle of the inlet and outlet bus bar.

(b) the top and bottom module joint are alternatively connected for the entrance and exit of the current flowing; (c) the inlet and outlet current are connected on the fourth and fifth module joint from top to bottom; (d) the inlet and outlet current are connected on the fifth and sixth module joint from top to bottom.

It can be seen that the structure illustrated in Fig. 17(d) is able to provide the least overall stray inductance when compared with those structures in Fig.16 (a), 16(b) and 16(c). Compared with the connection mode on the top and bottom with the inductance value exceeding 10 μ H, the mode on the central module can provide more than 20% reduction on the stray inductance and the smallest value reaches 6.646 μ H. As noted above, the bus connection bus stuck on the central joint can make the stray magnetic field to be eliminated so that the stray inductance can be optimized automatically.

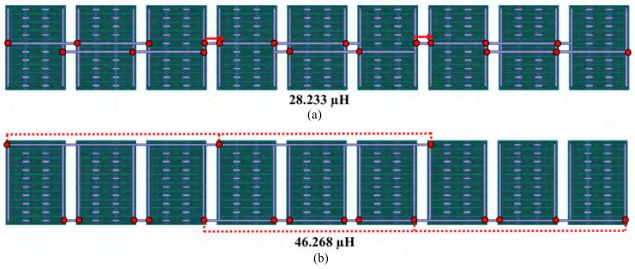


FIGURE 18. Inductance of FDR system in different connection modes. The figure (a) is three resistor stack in the parallel connection then the identical three groups in the series connection mode. Figure (b) is the three resistor stack in the series connection then the identical three groups in the parallel connection mode. The imaginary line in the figure (b) is to show the connecting points on the bus and the overall layout clearly.

Applying the rule of parallel-series connection mode for the FDR system, the bus connections between each resistor group of three stacks are directly connected by the neighboring resistor module joint on different resistor, which is shown in Fig.18. Therefore, the bus connections are short enough to restrain the stray inductance existence. With the simulation process, as shown in Fig.18, the overall

system can be restrained below 30 μ H. By contrast, the result of series-parallel connection mode under simulation is 46.268 μ H, which is much larger.

With the simulation process and according to the power and space parameter requirements, the stay inductance can obtain the least inductance value for the FDR system. Therefore, the impact on the fast discharge process and power components in the CPC can be reduced to the lowest extent.

V. CONCLUSION

In this paper, a comprehensive stray inductance analysis and structure design of the FDR system aiming at reducing stray inductance are presented:

1. The operation process of power components of the QP system is affected by the stray inductance of FDR system. Especially the VCB and CPC voltage will suffer negative influence and may even get damaged with the high voltage, which is generated by the FDR system stray inductance. Therefore, the system stray inductance is required to reduce as much as low.

2. The stray inductance optimization process of the FDR system is carried out by the detailed design of resistor module, the stack and the system. Especially, by changing the connection mode, the current direction can be altered which can modify the magnetic field distribution. Thus, the stray inductance of the FDR system can be optimized, accordingly. The optimization process is performed by theory analysis and FEA simulation whose results have proved that the stray inductance can be reduced by the proposed method.

3. The analysis results has proved an optimized solution in the QP system of LSTF when regarding the FDR system. Besides, it can be also served for the stray inductance optimization of similar resistor systems and even for the metal instruments or devices with analogous structure.

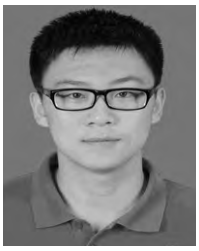
REFERENCES

[1] A. Portone, G. D'Amico, and L. Reccia, "Superconducting magnet systems in tokamak engineering and optimization," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 4, Jun. 2016, Art. no. 4204205.
[2] L. Xu, X. Liu, J. Jiang, and Y. Liao, "The design of quench protection of EAST toroidal field power supply system," *Fusion Eng. Des.*, vol. 81, nos. 20–22, pp. 2549–2554, Nov. 2006.
[3] I. Song, C. Choi, and M. Cho, "Quench protection system for the superconducting coil of the KSTAR tokamak," *IEEE Trans. Appl. Supercond.*, vol. 17, no. 1, pp. 1–6, Mar. 2007.
[4] E. Gaio *et al.*, "Final design of the quench protection circuits for the JT-60SA superconducting magnets," *IEEE Trans. Plasma Sci.*, vol. 40, no. 3, pp. 557–563, Mar. 2012.
[5] M. Coatanéa, J.-L. Duchateau, B. Lacroix, S. Nicollet, F. Rodriguez-Mateos, and F. Topin, "Selection of a quench detection system for the ITER CS magnet," *Fusion Eng. Des.*, vol. 86, nos. 6–8, pp. 1418–1421, Oct. 2011.
[6] L. Bottura and O. C. Zienkiewicz, "Quench analysis of large superconducting magnets. Part I: Model description," *Cryogenics*, vol. 32, no. 7, pp. 659–667, 1992.
[7] L. Bottura and O. C. Zienkiewicz, "Quench analysis of large superconducting magnets. Part II: Model validation and application," *Cryogenics*, vol. 32, no. 8, pp. 719–728, 1992.
[8] G. Zou, Z. Zhao, and L. Yuan, "Study on DC busbar structure considering stray inductance for the back-to-back IGBT-based converter," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2013, pp. 1213–1218.
[9] V. Marinozzi *et al.*, "Effect of coupling currents on the dynamic inductance during fast transient in superconducting magnets," *Phys. Rev. Special Topics -Accel. Beams*, vol. 18, no. 3, Mar. 2015, Art. no. 032401.
[10] J. Jiang, X. Liu, L. Xu, and Y. Liao, "Analysis of discharge based on toroidal field coils of EAST," *High Voltage Eng.*, vol. 35, no. 1, pp. 186–191, Jan. 2009.
[11] F. Bellina *et al.*, "Design, construction and operation of the 66 kA life test facility for the ITER magnet protection vacuum circuit breakers," in *Proc. 17th IEEE/NPSS Symp. Fusion Eng.*, Oct. 1997, pp. 1137–1140.
[12] I. Song, A. Roshal, V. Tanchuk, J. Thomsen, F. Milani, and I. Benfatto, "The fast discharge system of ITER superconducting magnets," in *Proc. Int. Conf. Elect. Mach. Syst.*, Beijing, China, Aug. 2011, pp. 1–6.
[13] L. Müller and J. W. Kimball, "Effects of Stray Inductance on Hard-Switched Switched Capacitor Converters," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6276–6280, Dec. 2014.
[14] E. B. Rosa, "The self and mutual inductances of linear conductors," in *Bulletin Bureau Standards*, vol. 4. Washington, DC, USA, 1907, no. 2, pp. 321–326.
[15] G. A. Barbashova, "Electric circuit inductance dependence of a hydrodynamic load on a thrown plate during high-speed impact welding of two plates," *Surf. Eng. Appl. Electrochem.*, vol. 48, no. 3, pp. 260–263, May 2012.
[16] Y. Takada, T. Kimura, and T. Nakagawa, "Influence of inductance properties on a magnetic levitation for thin-steel plates," *IEEE Trans. Magn.*, vol. 53, no. 11, Nov. 2017, Art. no. 2500705.

KUN WANG was born in Anhui, China, in 1989. He received the M.S. degree in electrical engineering from the Stevens Institute of Technology, Hoboken, NJ, USA, in 2015. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Science and Technology of China, Hefei. His research interests include power supply system and fast discharge resistor system for quench protection breaker.

ZHIQUAN SONG was born in Anhui, China, in 1975. He received the B.S. degree in power supply system and automation from the Hefei University of Technology, in 1999, and the Ph.D. degree in nuclear energy science and engineering from the Graduate University of Chinese Academy of Sciences, in 2007, where he is currently a Senior Engineer of the International Thermonuclear Experimental Reactor project with the Institute of Plasma Physics. His current research interests include coil power supply systems and quench protection breaker of fusion devices.

PENG FU was born in Hubei, China, in 1962. He received the B.S. degree in electrical engineering from the Huazhong University of Science and Technology, Wuhan, China, in 1985, and the M.S. and Ph.D. degrees in electrical engineering from the Chinese Academy of Sciences, Hefei, China, in 1990 and 1997, respectively, where he is currently a Professor and a Manager of the International Thermonuclear Experimental Reactor project with the Institute of Plasma Physics. His current research interest includes power supplies and their control systems of fusion devices.



WEI TONG was born in Anhui, China, in 1993. He received the B.S. degree in electrical engineering and automatization from the Huazhong University of Science and Technology (HUST), China. He is currently pursuing the Ph.D. degree in nuclear energy science and engineering with the University of Science and Technology of China (USTC), Hefei. His current research interests include high-power electronic switches and quench protection.

HUA LI was born in Hubei, China, in 1984. He received the B.S. degree in electrical engineering from the Huazhong University of Science and Technology (HUST), China, in 2005, the M.S. degree in power electronic from Shanghai Marine University (SMU), China, in 2010, and the Ph.D. degree in nuclear energy science and engineering from the University of Chinese Academy of Sciences, in 2015. He is currently with the Institute of Plasma Physics, Chinese Academy of Sciences (ASIPP), Hefei, China. His current research interests include electric machine drive, high-voltage high-frequency converter and high power dc breaker.

XIUQING ZHANG was born in Anhui, China, in 1980. She received the B.S. degree in electrical engineer and automation from the Hefei University of Technology, Hefei, China, in 2005, and the Ph.D. degree in nuclear energy science and engineering from the Institute of Plasma Physics, Chinese Academy of Science, Beijing, China, in 2015. Her current research interest includes integration and test of coil power supply systems.