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Elimination of High Frequency Oscillation in Dual Active Bridge Converters by dv/dt Optimization

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ABSTRACT With the increased switching speed, the high-frequency oscillation (HFO) problem caused by the stray capacitances of the transformer and the high *dv/dt* of the dual active bridge (DAB) converter becomes more serious. In this paper, a frequency-domain model considering the circuit parasitic parameters is derived to figure out the mechanism of HFO. It shows that HFO could be mitigated by reducing the *dv/dt* of the H-bridge output voltage. However, HFO will become apparent again, as the *dv/dt* continues to decrease. Based on the mathematical model, the HFO problem could be eliminated theoretically by placing the zero crossing points (ZCP) of the DAB *dv/dt* excitation at the oscillation frequency. The DAB *dv/dt* is adjusted by adding parallel capacitors to the power devices. A calculation method for the required capacitance is given to obtain an optimal *dv/dt*. Not only the HFO problem is eliminated, but also the efficiency could be improved due to the better soft-switching condition and less oscillation loss in the transformer. The simulations and experiments on a 6.6-kW DAB prototype are carried out to validate the proposed method. The HFO voltage spike amplitude is reduced by about 95% with the proposed method, which accords well with the theoretical analysis.

INDEX TERMS Dual active bridge, energy storage systems, high frequency oscillation, stray capacitance.

I. INTRODUCTION

Due to the depletion of fossil energy and the change of climate, technologies related to renewable energies have been greatly developed. Large scale energy storage systems (ESS) are required to smooth the power fluctuations when intermittent renewable energies such as the solar energy and the wind power are deployed. The energy flows among the ESS, the power source and the power grid are controlled through the efficient and reliable power electronics converters [1], [2]. With the bidirectional power flow control capability, high power density, inherent soft switching, galvanic isolation and flexible control features [3]–[5], the dual active bridge (DAB) based dc-dc converters are considered as the competitive power flow control topologies for the energy storage systems.

Despite the advantages, a high frequency oscillation (HFO) problem exists in the DAB converter. The parasitic capacitances of the DAB transformer together with the leakage inductances and the phase shift inductance make up unwanted high frequency resonant tanks, which can be easily excited by the high frequency square-wave voltage waveform from the H-bridge, causing undesired ringing and oscillations [6], [7]. The HFO problem could severely affect the converters' performance. For one thing, the voltage spikes on the transformer ports require thicker insulation materials [8], which would further limit the heat dissipation capability and decrease the power density of the transformer. The HFO could also increase high frequency losses [9], induce electro-magnetic interference (EMI) and common mode (CM) noise, distort the voltage and current waveforms and reduce the overall efficiency and reliability of the converters [6]–[8], [10].

When new materials and devices are applied to improve the power density and efficiency of the DAB converters [11], the HFO problem may become more serious. The Fe-based nanocrystalline alloy is considered as the most promising material for the high frequency transformer cores because of its higher saturation, lower losses and higher Curie temperature characteristics [12]. Compared with the ferrite cores, the nanocrystalline cores are more like conductors because of its high electrical conductivity [13], which could increase the stray capacitances of the transformers apparently [14], [15]. The silicon carbide (SiC) power devices have lower switching

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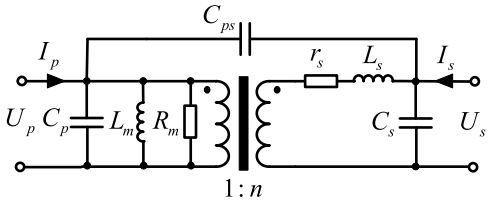


FIGURE 1. Transformer lumped model with three lumped capacitors.

losses and higher switching frequencies, but a higher dv/dt (usually around 50-100kV/μ s [16]) of the H-bridge output voltage would be produced, exciting larger HFO.

As the parasitic capacitances of the transformer are the main reason for the HFO, many efforts have been made to evaluate the capacitive effects of the transformer [13], [15], [17], [18]. For a two windings high frequency transformer, one-capacitor [19], three-capacitor [20]–[22], six-capacitor [8] and ten-capacitor [13] lumped models are proposed [23]. Among which, the three-capacitor model with a π-shaped network shown in Fig. 1 is widely used for the purpose of dynamic circuit modeling taking the transformer as a two-port system [10], [24], [25]. The transformer leakage inductance L_s, magnetizing inductance L_m, core loss equivalent resistance R_m and winding resistances R_s could be determined directly by the open-circuit and short-circuit measurements of the transformer [24]. C_p and C_s are the equivalent self-capacitances of the primary and the secondary windings respectively, and C_{ps} is the equivalent mutual-capacitance between the two windings. To extract C_p, C_s and C_{ps}, various methods have been proposed, such as analytical formula [15], [18], numerical methods [8], [13], [16], or experimental measurements [19], [24]. The experimental measurement method based on the self-resonant frequencies of the transformer is widely used owing to its practicality and accuracy [22], [24].

HFO could be significantly alleviated with lower parasitic capacitances. In [7], [8], [10], different constructions and winding arrangements of the transformer are proposed to mitigate HFO by reducing the capacitances with the aid of analytical formula or finite element analysis (FEA). However, there is always a contradiction between the leakage inductance and the stray capacitance [17]. The smaller the capacitance is, the larger the leakage inductance is. Moreover, to reduce the capacitances of the transformer needs a complicated design of the transformer, which may increase the difficulties of winding and the cost of manufacturing.

This paper analyzes the HFO mechanism mathematically from the perspectives of the self-resonant frequencies of the DAB and the frequency spectrum of the square-wave excitation from the H-bridge. It comes out that HFO could be mitigated to a great extent by reducing the dv/dt of the H-bridge output voltage, and it could even be theoretically eliminated with an optimal dv/dt. Accordingly, a method of reducing the dv/dt to a calculated optimal value by adding paralleled capacitors with specified capacitances to the power switches in the DAB is proposed. The transfer functions of the transformer voltage are derived to obtain the voltage oscillation amplitudes under different dv/dt. Simulations and experiments are carried out on a 6.6 kW prototype to validate the proposed method. It shows that the proposed method could not only solve the HFO problem with a 95% reduction of the voltage spikes, but also improve the overall efficiency simultaneously.

II. MODELING FOR HIGH FREQUENCY OSCILLATION PROBLEM

A. PROBLEM DESCRIPTION

The circuit schematic of a 6.6-kW DAB prototype is shown in Fig. 2. Two phase shift inductors are symmetrically placed on both sides of the transformer to alleviate the current spikes caused by the parasitic capacitances of the transformer and the high dv/dt of the H-bridge [6], [19]. A three-capacitor model of the transformer is employed to characterize the electrical coupling effect of the transformer [24]. The distributed parameters of the transformer are experimentally extracted with the impedance characteristics (ICs) method [22], [24], [26]. The specifications and parameters of the DAB circuit and the parameters of the transformer are listed in Table 1 and Table 2 respectively.

The picture of the DAB prototype is shown in Fig. 3. The typical measured voltage and current waveforms with HFO of the transformer are shown in Fig. 4. It can be seen that the waveforms are severely distorted due to the HFO problem. The oscillation frequencies of the current and the voltage are the same. They have a fixed phase difference of 90 degrees.

The input impedance of the DAB AC network of Z_{in} shown in Fig. 2 is applied for analyzing the HFO problem.

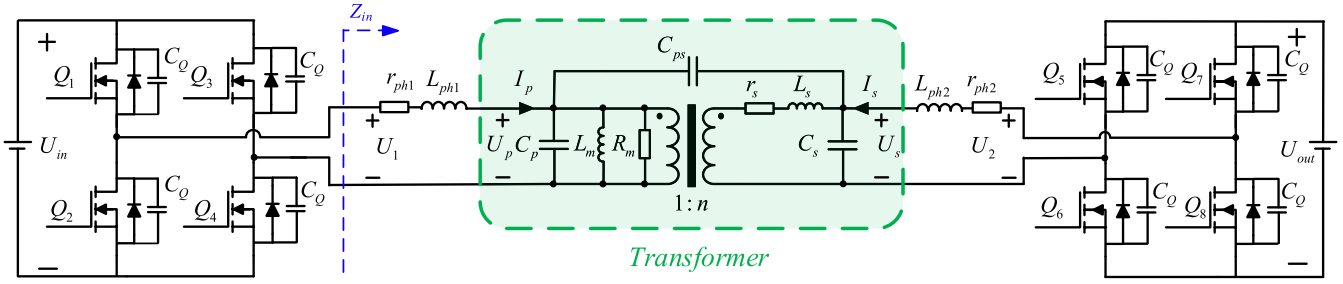


FIGURE 2. Schematic circuit of 6.6-kW DAB converter prototype.

TABLE 1. Specifications and parameters of DAB prototype circuit.

Symbol	Parameters	Values
U_{in}	Rated input voltage	600 VDC
U_{out}	Rated output voltage	600 VDC
P	Rated power	6.6 kW
f	Switching frequency	40 kHz
L_{ph1} ,L_{ph2}	Phase-shift inductor	60.51μH
r_{ph1} ,r_{ph2}	Resistance of Phase-shift inductor	0.016 Ω
D	Phase-shift angle at rated power	0.245

TABLE 2. Parameters of transformer.

Symbol	Parameters	Values
C_p	Self-capacitance of the primary winding	39.1 pF
C_s	Self-capacitance of the secondary winding	39.1 pF
C_{ps}	Mutual capacitance between two windings	129 pF
L_m	Magnetizing inductance	63 mH
r_s	Winding resistance	0.04 Ω
L_s	Leakage inductance	5.1 μH
R_m	Core loss equivalent resistance	10850 Ω
n	Transformer ratio	1:1

The frequencies of the zeros and poles of Z_{in} are defined as the self-resonant frequencies (SRF) of the DAB converter. As the resonant frequencies are usually above the level of MHz, the fundamental frequency of the AC network input voltage U_1 has little contribution to the oscillation. However, the fast changing of U_1 during a switching transient process, referred as dv/dt, has plentiful harmonic components in the frequency range of MHz, which will be the main excitation source for the HFO problem [24]. The most serious HFO occurs when the output power is the highest, which means the phase shift between U_1 and the AC network output voltage U_2 is the largest. In this case, U_1 and U_2 do not contribute to HFO at the same time. In the following analysis, only the HFO caused by U_1 is taken into account. HFO caused by U_2 occurs at a delayed time of the phase shift, which can be analyzed using the same method.

B. INPUT IMPEDANCE OF DAB AC NETWORK

The model in Fig.2 can be redraw as a parallel connection of a magnetic field coupling circuit and an electric field coupling circuit as shown in Fig.5.

The currents in the model can be expressed as (1) and (2)

$$\begin{cases} I_{p1} = (n^2 y_l + y_m)U_p + (-n^2 y_l)\dfrac{U_s}{n} \\ nI_{s1} = (-n^2 y_l)U_p + (n^2 y_l)\dfrac{U_s}{n} \end{cases} \tag{1}$$

$$\begin{cases} I_{p2} = j\omega(C_p + C_{ps})U_p - j\omega C_{ps}U_s \\ I_{s2} = -j\omega C_{ps}U_p + j\omega(C_s + C_{ps})U_s \end{cases} \tag{2}$$

where the admittances of the leakage branch y_l and the magnetizing branch y_m are represented by

$$\begin{cases} y_l = \dfrac{1}{r_s + j\omega L_s} \\ y_m = \dfrac{1}{r_m} + \dfrac{1}{j\omega L_m} \end{cases} \tag{3}$$

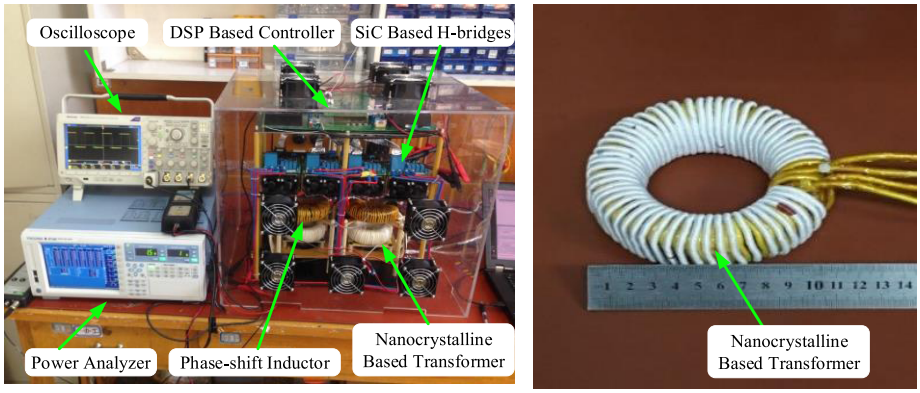
From (1) and (2), the admittance matrix Y_m for the magnetic field coupling circuit and the admittance matrix Y_c for the electric field coupling circuit are defined as

$$Y_m = \begin{bmatrix} n^2 y_l + y_m & -n y_l \\ -n y_l & y_l \end{bmatrix} \tag{4}$$

$$Y_c = j\omega \begin{bmatrix} C_p + C_{ps} & -C_{ps} \\ -C_{ps} & C_s + C_{ps} \end{bmatrix} \tag{5}$$

The total admittance matrix of the transformer Y is given by

$$\begin{aligned} Y &= Y_m + Y_c = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \\ &= \begin{bmatrix} n^2 y_l + y_m + j\omega(C_p + C_{ps}) & -n y_l - j\omega C_{ps} \\ -n y_l - j\omega C_{ps} & y_l + j\omega(C_s + C_{ps}) \end{bmatrix} \end{aligned} \tag{6}$$



(a) (b)

FIGURE 3. Photos of a DAB prototype (a) DAB prototype built by SiC devices (CREE-C2M0040120D). (b) Transformer of Fe-based nanocrystalline alloy cores (VAC-500F W342).

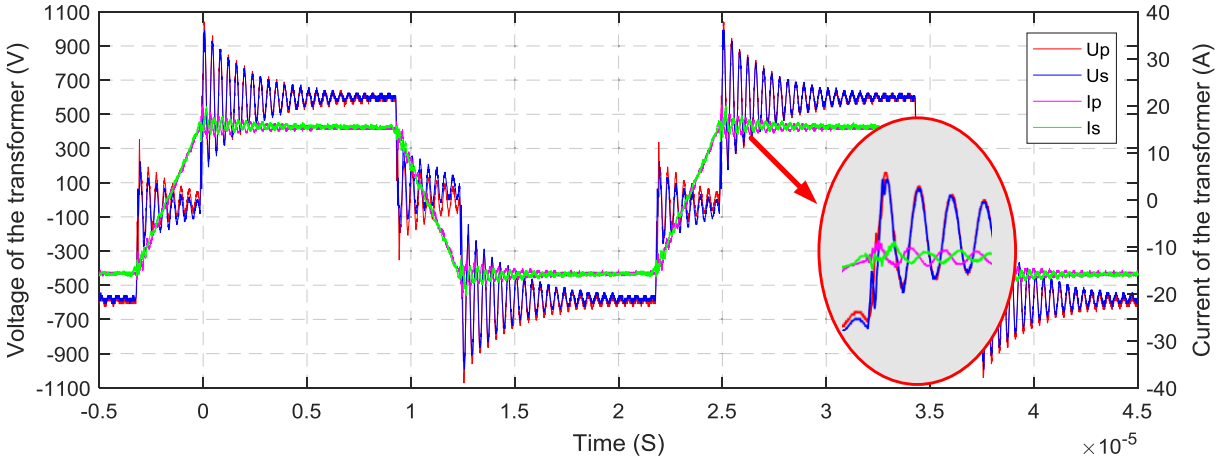


FIGURE 4. Measured waveforms with HFO of DAB prototype under rated power of 6.6-kW with switching frequency of 40kHz.

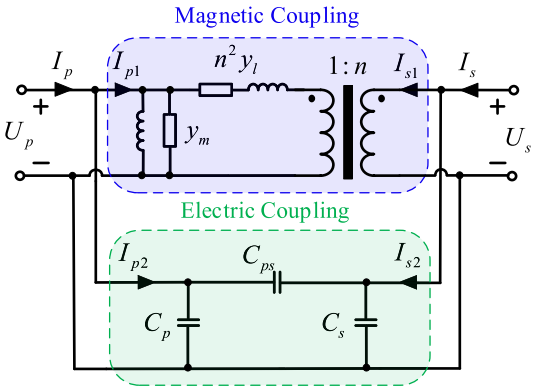


FIGURE 5. Transformer model by magnetic field coupling circuit paralleled with electric field coupling circuit.

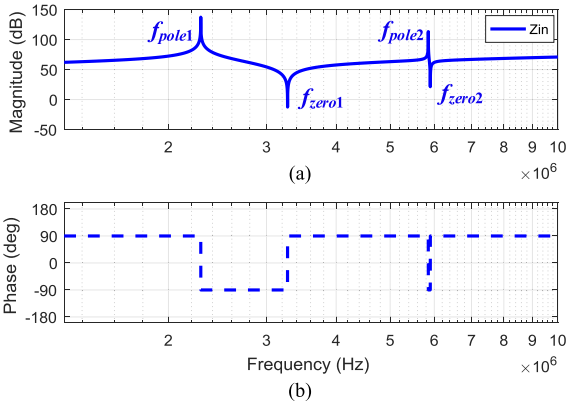


FIGURE 6. Bode diagram of input impedance for DAB AC network. (a) Magnitude. (b) Phase.

The currents in the DAB AC network can be expressed as

$$\begin{cases} I_p = y_{11}U_p + y_{12}U_s \\ I_s = y_{21}U_p + y_{22}U_s \\ I_p = y_{ph1}(U_1 - U_p) \\ I_s = y_{ph2}U_s \end{cases} \tag{7}$$

where the admittances of the phase-shift inductances are given by

$$\begin{cases} y_{ph1} = \dfrac{1}{r_{ph1} + j\omega L_{ph1}} \\ y_{ph2} = \dfrac{1}{r_{ph2} + j\omega L_{ph2}} \end{cases} \tag{8}$$

From (7), the input impedance of the DAB AC network Z_{in} can be derived as (9), as shown at the bottom of this page.

C. ZEROS AND POLES OF INPUT IMPEDANCE Z_{in}

If the transformer turns ratio is n, the following equation should be met to realize a symmetrical structure,

$$L_{ph1} = \frac{L_{ph2}}{n^2} \tag{10}$$

Ignoring the resistances, the zeros of the input impedance Z_{in} in (9) can be solved as in (11) and (12), as shown at the bottom of the next page, the poles of Z_{in} as in (13) and (14), as shown at the bottom of the next page, where L_{ph} equals to L_{ph1}.

The Bode diagram of the input impedance Z_{in} for the DAB prototype are shown in the Fig. 6, where the frequencies of the zeros and poles are all marked. Each frequency of the zeros

$$Z_{in} = \frac{U_1}{I_p} = \frac{y_l + y_{ph2} + j\omega(C_s + C_{ps})}{[n^2 y_l + y_m + j\omega(C_p + C_{ps})][y_l + y_{ph2} + j\omega(C_s + C_{ps})] - (ny_l + j\omega C_{ps})^2} + \frac{1}{y_{ph1}} \tag{9}$$

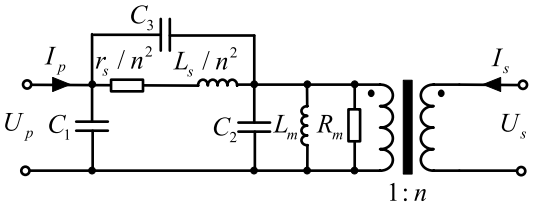


FIGURE 7. Lumped model of transformer referred to primary side.

and poles represents a self-resonance frequency of the DAB converter.

Generally, as the leakage inductance of the transformer is smaller than the phase shift inductance, it can be deduced from (11)-(14) so that,

$$\begin{cases} \dfrac{f_{zero1}}{f_{zero2}} \approx \sqrt{\dfrac{2L_s(C_pC_s + C_pC_{ps} + C_sC_{ps})}{L_{ph}[C_p + n^2C_s + (n-1)^2C_{ps}]^2}} < 1 \\ \dfrac{f_{pole1}}{f_{pole2}} \approx \sqrt{\dfrac{L_s(C_pC_s + C_pC_{ps} + C_sC_{ps})}{L_{ph}[C_p + n^2C_s + (n-1)^2C_{ps}]^2}} < 1 \end{cases} \tag{15}$$

Therefore, f_{zero1} is smaller than f_{zero2}, and f_{pole1} is smaller than f_{pole2}. f_{zero1} and f_{pole1} are defined as the first zero and the first pole respectively.

As a matter of fact, the first zero of the input impedance (i.e. f_{zero1}) would make the major contributions to the HFO. Because not only the input impedance is the smallest, but also the harmonic component of the excitation source is usually the largest under the lowest frequency among all the zeros.

The distributed capacitances of the transformer can be referred to the primary side as shown in Fig. 7 when the leakage inductance L_s is much smaller than the magnetizing inductance L_m. The node voltage equations, and the admittance matrix Y_c^* can be rewritten as (16) and (17) correspondingly.

$$\begin{cases} j\omega(C_1 + C_3)U_p - j\omega C_3(\frac{1}{n}U_s) = I_p \\ -j\omega C_3 U_p + j\omega(C_2 + C_3)(\frac{1}{n}U_s) = nI_s \end{cases} \tag{16}$$

$$Y_c^* = j\omega \begin{bmatrix} C_1 + C_3 & -\frac{1}{n}C_3 \\ -\frac{1}{n}C_3 & \frac{1}{n^2}(C_2 + C_3) \end{bmatrix} \tag{17}$$

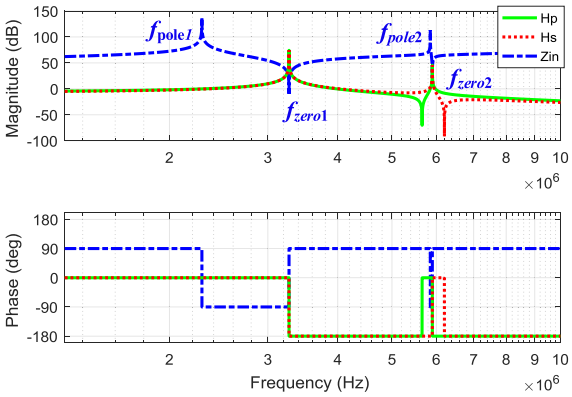


FIGURE 8. Bode diagram of transformer voltages and input impedance of Z_{in}.

The relationships of the capacitances C_1, C_2 and C_3 with C_p, C_s and C_{ps} are given by

$$\begin{cases} C_1 = C_p - (n-1)C_{ps} \\ C_2 = n^2C_s + n(n-1)C_{ps} \\ C_3 = nC_{ps} \end{cases} \tag{18}$$

Therefore, the first self-resonance frequency f_{zero1} can be simplified as (19).

$$f_{zero1} \approx \frac{1}{2\pi\sqrt{\frac{L_{ph}}{2}(C_1 + C_2)}} \tag{19}$$

From (19), it can be seen that f_{zero1} mainly depends on the parasitic capacitances C_1, C_2 and the phase shifting inductance L_{ph}.

D. TRANSFER FUNCTION OF TRANSFORMER VOLTAGES

In order to evaluate the voltage stresses of the transformer, the transfer functions of the primary and secondary voltages U_p and U_s to the source voltages U_1 and U_2 can be derived from Equation (7) as (20) and (21), as shown at the bottom of the next page.

In the Bode diagram of Fig. 8, the transfer functions of the transformer voltages and the input impedance of the DAB

$$f_{zero1} \approx \frac{1}{2\pi\sqrt{\frac{L_sL_{ph}[C_p+n^2C_s+(n^2+1)C_{ps}]+n^2L_{ph}^2[C_p+n^2C_s+(n-1)^2C_{ps}]}{L_s+2n^2L_{ph}}}} \tag{11}$$

$$f_{zero2} \approx \frac{1}{2\pi\sqrt{\frac{n^2L_sL_{ph}(C_pC_s+C_pC_{ps}+C_sC_{ps})}{L_s[C_p+n^2C_s+(n^2+1)C_{ps}]+n^2L_{ph}[C_p+n^2C_s+(n-1)^2C_{ps}]}}} \tag{12}$$

$$f_{pole1} \approx \frac{1}{2\pi\sqrt{L_{ph}[C_p + n^2C_s + (n-1)^2C_{ps}] + \frac{L_s}{n^2}(C_p + C_{ps})}} \tag{13}$$

$$f_{pole2} \approx \frac{1}{2\pi\sqrt{\frac{n^2L_{ph}L_s[C_pC_s+C_pC_{ps}+C_sC_{ps}]}{n^2L_{ph}[C_p+n^2C_s+(n-1)^2C_{ps}]+L_s(C_p+C_{ps})}}} \tag{14}$$

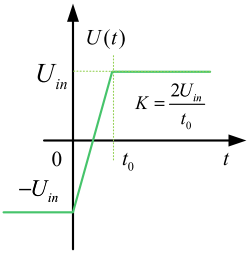


FIGURE 9. Waveform of excitation voltage.

AC network are shown simultaneously. It can be calculated from (20), (21) that the transfer functions of the primary and secondary voltages H_p and H_s have the same poles under the frequencies of both f_{zero1} and f_{zero2}, which are the zeros of the input impedance. It means that the maximum input current and maximum transformer voltages will occur under the same frequency, that is the first zero of the input impedance f_{zero1}. This is proved by the measured results shown in Fig.4 where the input current and voltage of the transformer oscillates under the same frequency.

Looking back on Fig. 4, it can be seen that the input current and voltage of the transformer have the same oscillation frequency. Therefore, f_{zero1} is the exactly the oscillation frequency, which contributes to the voltage stresses of the transformer and the input current of the DAB converter.

E. FREQUENCY SPECTRUM OF dv/dt EXCITATION

Fig. 9 shows the waveform of the input voltage of the AC network U_1 produced by the H-bridge of DAB, which can be expressed mathematically by

$$U_1(t) = K[tu(t) - (t - t_0)u(t - t_0)] - U_{in} \tag{22}$$

where $u(t)$ is a unit step function, t_0 is the rising time and K is the dv/dt of the converter.

The Fourier transformation of (22) is given by

$$U_1(j\omega) = \frac{K}{\omega^2}[\cos(wt_0) - 1 - j\sin(wt_0)], (\omega > 0) \tag{23}$$

The corresponding magnitude is

$$|U_1(j\omega)| = \frac{K}{\omega^2}\sqrt{2 - 2\cos(wt_0)}, (\omega > 0) \tag{24}$$

From (24), the zero crossing points (ZCP) is derived as

$$wt_0 = n \cdot 2\pi, (n \in N^*) \tag{25}$$

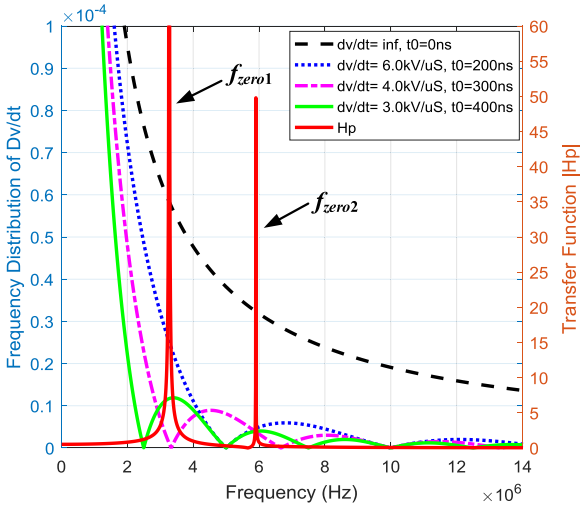


FIGURE 10. Frequency spectrum of different dv/dt and transfer function of $|H_p|$.

which means that there is no excitation under the frequencies of ZCPs.

On the other hand, the piecewise linear function in Fig. 9 will become to a step function when t_0 tends to zero. The corresponding voltage can be expressed as

$$\lim_{t_0 \to 0} |U_1(j\omega)| = \lim_{t_0 \to 0} \frac{K}{\omega^2}\sqrt{2 - 2\cos(wt_0)} = \frac{2U}{\omega} \tag{26}$$

It means that there is no ZCP in the frequency spectrum of a step function.

III. METHOD TO SOLVE HIGH FREQUENCY OSCILLATION PROBLEM

Fig. 10 shows the frequency spectrum of the excitation voltage magnitude under different dv/dt together with the transfer function magnitude H_p. It can be seen that the magnitude of the excitation voltage at f_{zero1} decreases at first by reducing dv/dt, which means that HFO could be mitigated theoretically. The HFO could be eliminated completely when the self-resonant frequency of f_{zero1} equals to ZCPs of dv/dt. However, with dv/dt being further reduced, the excitation magnitude at f_{zero1} will increase. There is an optimal dv/dt at which HFO could be eliminated to a great extent.

To adjust dv/dt of the DAB converter, an effective approach is to connect parallel capacitors to the power devices. By doing so, the switching losses may also decrease due to the improved soft-switching condition.

$$H_p = \frac{U_p}{U_1} = \frac{\frac{L_s+n^2L_{ph}}{n^2\omega^2L_sL_{ph}} - (C_s + C_{ps})}{\frac{L_s+n^2L_{ph}}{n^2\omega^2L_sL_{ph}} + \omega^2L_{ph}(C_pC_s + C_pC_{ps} + C_sC_{ps}) - \frac{C_p+n^2C_s+(n^2+1)C_{ps}}{n^2} - L_{ph}\frac{C_p+n^2C_s+(n-1)^2C_{ps}}{L_s}} \tag{20}$$

$$H_s = \frac{U_s}{U_1} = \frac{n\frac{1}{\omega^2L_s} - C_{ps}}{\frac{L_s+n^2L_{ph}}{n^2\omega^2L_sL_{ph}} + \omega^2L_{ph}(C_pC_s + C_pC_{ps} + C_sC_{ps}) - \frac{C_p+n^2C_s+(n^2+1)C_{ps}}{n^2} - L_{ph}\frac{C_p+n^2C_s+(n-1)^2C_{ps}}{L_s}} \tag{21}$$

Three steps could be implemented as follows to determine the optimal dv/dt and then the parallel capacitance.

A. FIRST STEP: CALCULATING THE SELF-RESONANT FREQUENCY OF THE DAB CONVERTER

As analyzed above, the frequency f_{zero1} would make the major contributions to the HFO problem of the DAB converter. f_{zero1} could be calculated from (19) as

$$f_{zero1} \approx \frac{1}{2\pi\sqrt{\frac{L_{ph}}{2}(C_1+C_2)}} = 3.2\text{MHz} \tag{27}$$

where the result is for the 6.6-kW DAB prototype.

Another way to obtain the self-resonant frequency f_{zero1} is by directly measuring the oscillation frequency of the voltage or current of the transformer.

B. SECOND STEP: CALCULATING THE OPTIMAL dv/dt TO SOLVE THE HFO PROBLEM

The optimal rising time of the excitation voltage could be derived from (25) as follows when the frequency of the first ZCP of the excitation equals to f_{zero1}.

$$t_0 = \frac{1}{f_{zero1}} = 313\text{ns} \tag{28}$$

So the optimal dv/dt of the converter can be derived as (29) when the excitation voltage $U(t)$ changes from -U_{in} to U_{in} during the rising time of t_0. The result is also for the 6.6-kW DAB prototype.

$$K = \frac{dv}{dt} = \frac{2U_{in}}{t_0} = 3.83\text{kV}/\mu\text{s} \tag{29}$$

C. THIRD STEP: CALCULATING THE OPTIMAL CAPACITANCE TO BE CONNECTED PARALLELLY TO THE POWER SWITCHES

The instant current of $i_p(t_n)$ can be determined as (30) through the voltage and current waveforms of DAB shown in Fig. 11

$$\begin{cases} i_p(t_1) = -\dfrac{U_{in}+(2D-1)U_{out}/n}{8f_sL_{ph}} \\ i_p(t_3) = \dfrac{U_{in}+(2D-1)U_{out}/n}{8f_sL_{ph}} \\ i_p(t_2) = \dfrac{U_{out}/n+(2D-1)U_{in}}{8f_sL_{ph}} \\ i_p(t_4) = -\dfrac{U_{out}/n+(2D-1)U_{in}}{8f_sL_{ph}} \end{cases} \tag{30}$$

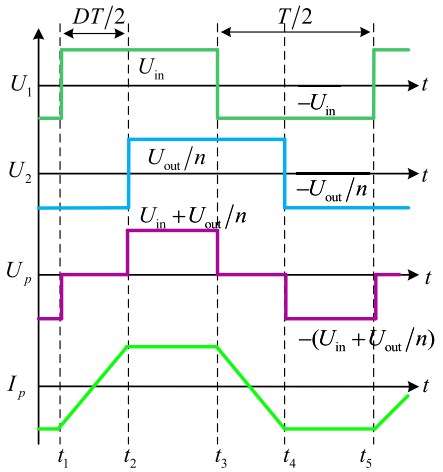


FIGURE 11. Ideal voltage and current waveforms of DAB.

where U_{in} is the input DC voltage, U_{out} is the output DC voltage, D is the phase shift ratio of DAB, f_s is the switching frequency.

As the paralleled capacitors are charged or discharged during the transient states, the relationship of the transient voltage Uc and current i_c through the capacitors is given by

$$\frac{dU_C}{dt} = \frac{1}{C_{parall}}i_C = \frac{1}{C_{parall}}\cdot\frac{i_p(t_n)}{2} = \frac{1}{2}\cdot\frac{dv}{dt}(t_n) \tag{31}$$

Therefore, the optimal paralleled capacitance C_{parall} can be derived as

$$C_{parall} = \frac{1}{\frac{dv}{dt}(t_n)}i_p(t_n) \tag{32}$$

The optimal paralleled capacitance C_{parall} for the DAB prototype under the rated power condition can be calculated as 3.8nF. As the value is much bigger than the junction capacitances of the switching devices, the influence of the junction capacitances could be eliminated.

It could be seen from (30), (32) that the required optimal paralleled capacitances under light load conditions are smaller than the rated condition due to reduced power and phase shift ratios. Therefore, the capacitance should be determined by the rated power condition as the relative larger paralleled capacitance would not generate a much higher excitation under light load conditions seen from Fig. 10.

$$\left|U_p\right| = H_p\left|U_1\right| = \frac{[\frac{L_s+n^2L_{ph}}{n^2\omega^2L_sL_{ph}} - (C_s+C_{ps})][\frac{2U}{\omega^2t_0}\sqrt{2-2\cos(wt_0)}]}{\frac{L_s+n^2L_{ph}}{n^2\omega^2L_sL_{ph}} + \omega^2L_{ph}(C_pC_s+C_pC_{ps}+C_sC_{ps}) - \frac{C_p+n^2C_s+(n^2+1)C_{ps}}{n^2} - L_{ph}\frac{C_p+n^2C_s+(n-1)^2C_{ps}}{L_s}} \tag{33}$$

$$|U_s| = H_s|U_1| = \frac{[n\frac{1}{\omega^2L_s} - C_{ps}][\frac{2U}{\omega^2t_0}\sqrt{2-2\cos(wt_0)}]}{\frac{L_s+n^2L_{ph}}{n^2\omega^2L_sL_{ph}} + \omega^2L_{ph}(C_pC_s+C_pC_{ps}+C_sC_{ps}) - \frac{C_p+n^2C_s+(n^2+1)C_{ps}}{n^2} - L_{ph}\frac{C_p+n^2C_s+(n-1)^2C_{ps}}{L_s}} \tag{34}$$

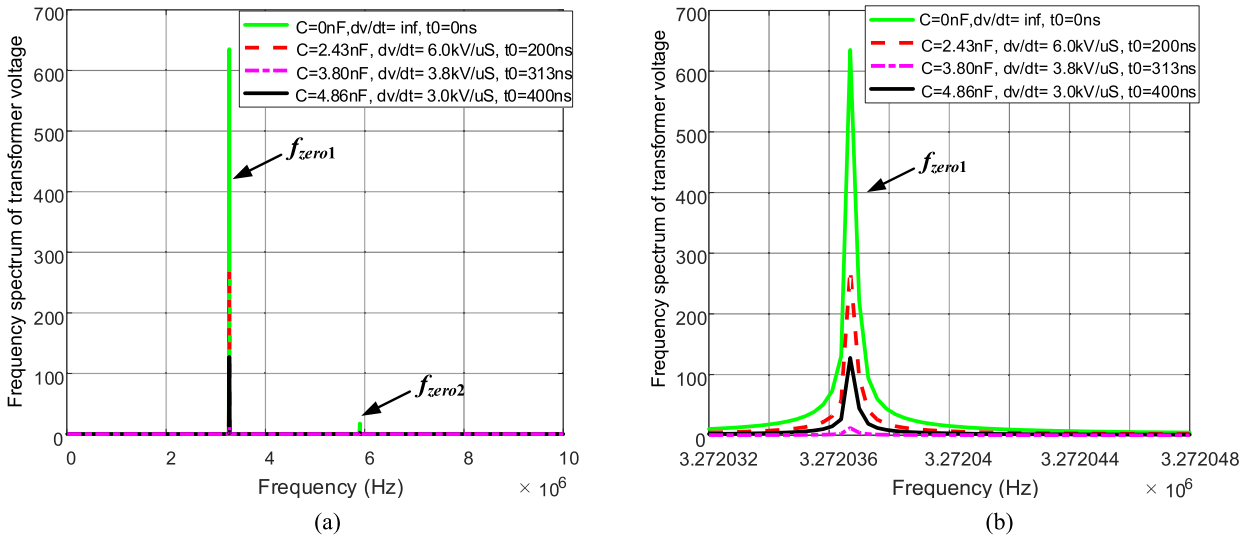


FIGURE 12. Frequency spectrum of transformer voltage of U_p. (a) 0 to 10 MHz; (b) zoom in around f_{zero1}.

In order to evaluate the method of decreasing dv/dt to an optimal value to solve the HFO problem, the primary and secondary transformer voltages excited by dv/dt of the primary H-bridge can be derived as (33) and (34), as shown at the bottom of the previous page, from (20), (21) and (24).

The primary voltage amplitude of the transformer under different frequencies can be drawn from (33) as shown in Fig. 12.

1) It can be seen that the first resonant frequency of the transformer voltage f_{zero1} dominates the oscillation.

2) HFO is almost eliminated when the paralleled capacitance goes up to 3.80 nF. However, as the paralleled capacitance continues to increase, the primary voltage of the transformer will increase conversely. Therefore, the paralleled capacitance is not the higher the better.

IV. SIMULATION VERIFICATION

In order to evaluate the proposed method, a circuit model of the DAB converter is built in LTspice with the circuit parameters listed in Table 1 and Table 2. The model of SiC power devices (CREE-C2M0040120D) is downloaded from CREE, INC, the model of the transformer are built based on the three lumped capacitor model as shown in Fig. 1.

The voltage waveform of the transformer under different dv/dt are shown in Fig. 13 (a). It can be seen that the oscillation frequency is equal to the first self-resonance frequency f_{zero1}, which is 3.2 MHz calculated from (25). The oscillation is almost eliminated when dv/dt is close to the optimal dv/dt of 3.83 kV/μs calculated from (27). When dv/dt is further reduced to 2.7 kV/μs by increasing the paralleled capacitance to 5.4 nF, the oscillation voltage of the transformer will increase on the contrary.

Fig. 13 (b) shows the voltage and current waveforms of the transformer with the optimal dv/dt. There is almost no oscillation in the waveforms.

Fig. 13 (c) shows the voltage spike of the transformer under different paralleled capacitances to the power devices. The voltage spike is reduced significantly with the optimal capacitance, which agrees with the analysis in Section III.

V. EXPERIMENTAL VERIFICATION

The experiments are carried out on a DAB prototype to verify the above theoretical analysis and simulations. The specifications and parameters of the prototype is introduced in Section II. The waveform of the transformer terminal voltage U_p and the H-bridge output voltage U_2 are shown in Fig.14 (a). The HFO voltage spike difference is less than 10% compared with the simulation and analysis results. At the optimal point, the voltage spike was reduced from 470 V to about 25 V. Fig. 14(b) gives the waveform of the transformer voltage U_p, U_s and current I_p and I_s at the optimal dv/dt point. Fig. 14(c) gives the voltage spike under different paralleled capacitances.

Further experiments under the rated power are carried out with different MOSFET gate resistances and different paralleled capacitances. As shown in Fig.15 (a), the maximum dv/dt can be as high as 46kV/μs due to the fast switching features of the SiC devices. The dv/dt can be reduced by increasing the gate resistances or paralleled capacitances to the power devices. When the paralleled capacitances are larger than 1 nF, dv/dt is mainly determined by the capacitance, and the gate resistance has little influence.

In Fig.15 (c), the efficiency of the DAB converter under the rated power with different gate resistances and paralleled capacitances are shown. It can be seen that the efficiency of the converter increases as the paralleled capacitance

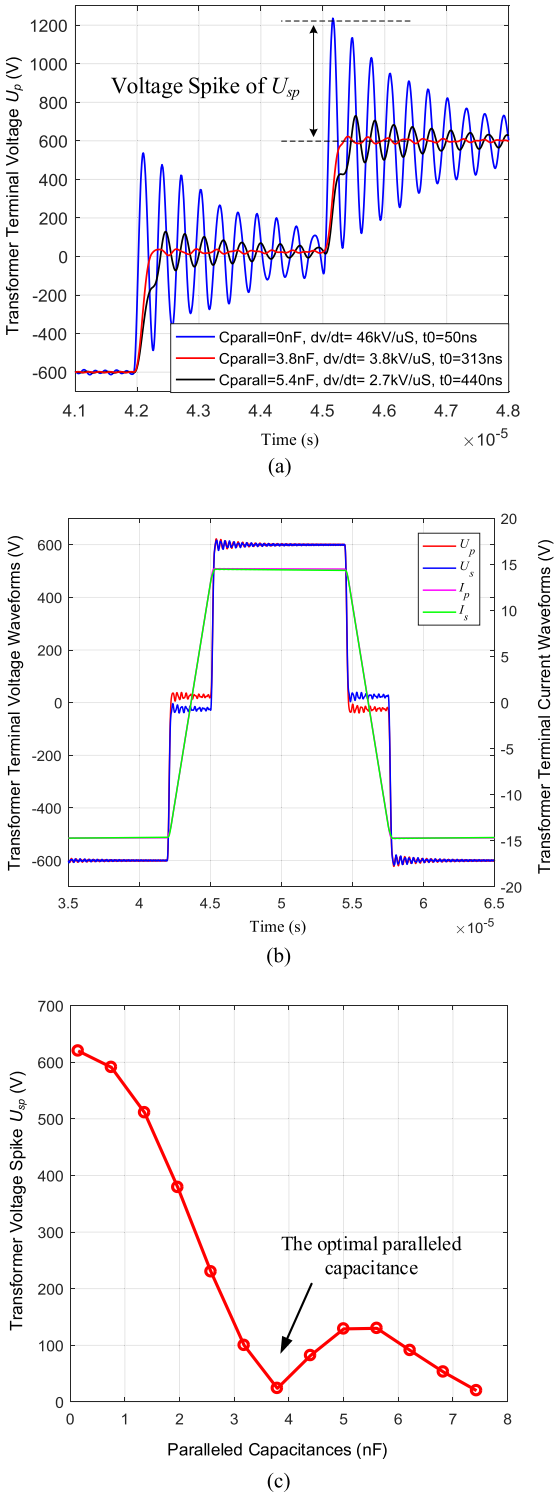


FIGURE 13. Simulation results by LTspice. (a) Primary voltage waveforms of the transformer under different dv/dt. (b) Voltage and current waveforms of transformer with optimal paralleled capacitance. (c) Voltage spike of transformer with different paralleled capacitances to the power devices.

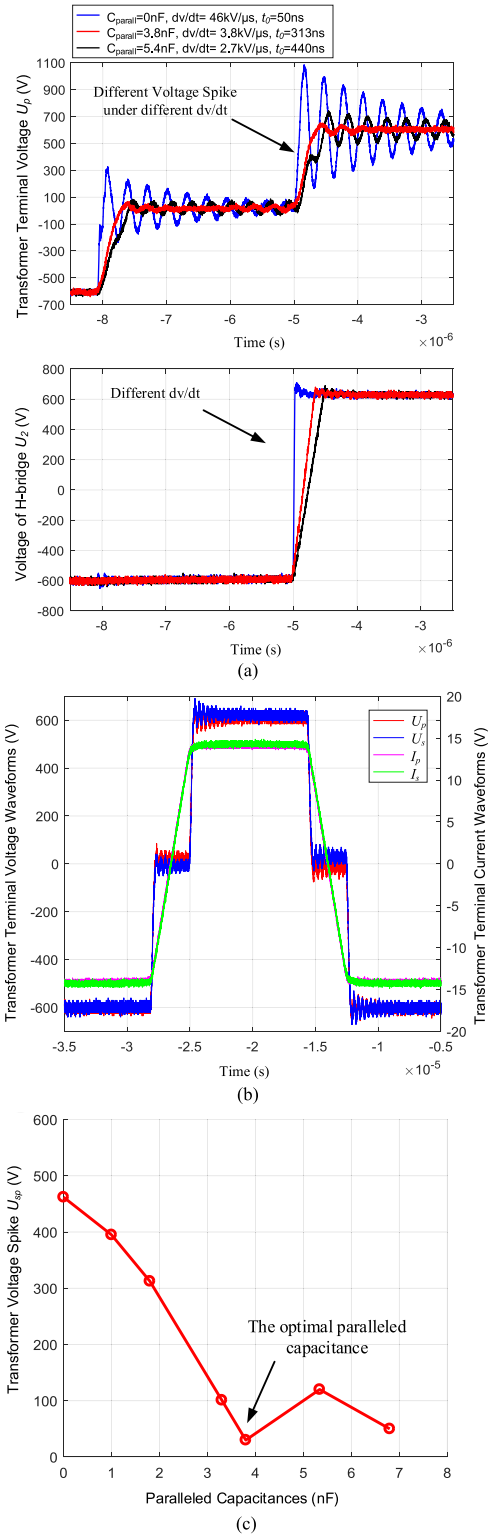


FIGURE 14. Experiment results of the DAB prototype. (a) Primary voltage waveforms of transformer under different dv/dt. (b) Voltage and current waveforms of transformer with optimal paralleled capacitances. (c) The experimental voltage spike of the transformer with different paralleled capacitances.

increases, but decreases as the gate resistance increases. The efficiency of the converter is mainly determined by the paralleled capacitance and has less relationship with the gate resistance when the paralleled capacitance is large enough. The highest efficiency of the converter goes up to over 98.2% with the paralleled capacitances larger than 3 nF.

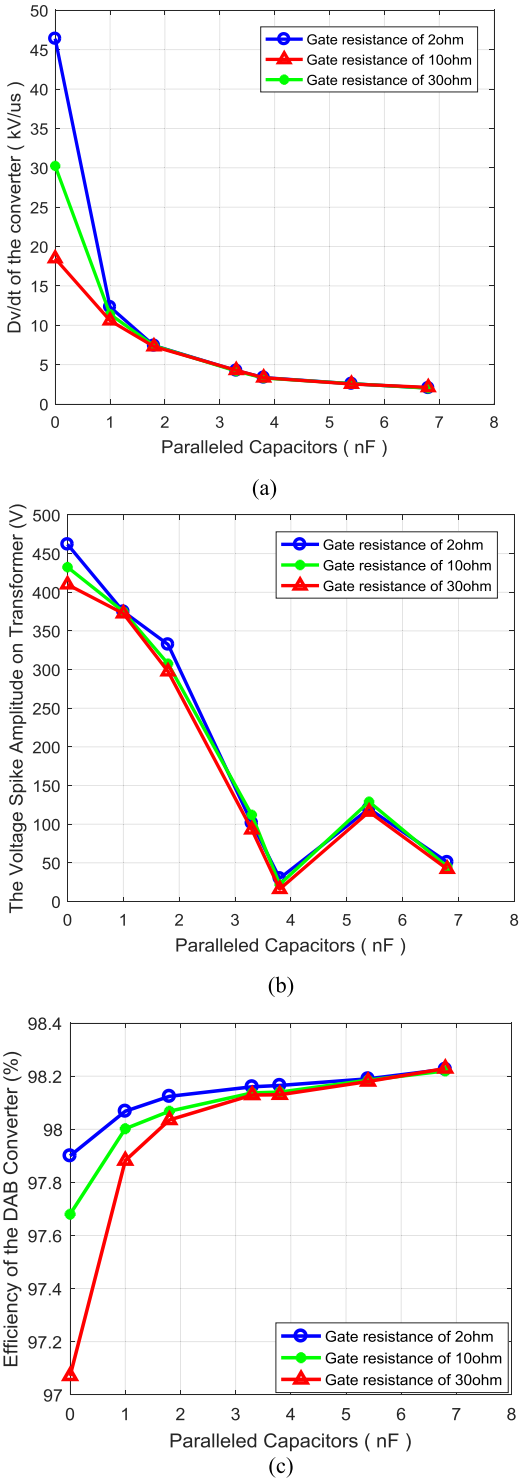


FIGURE 15. Experiment results under the rated power with different gate resistances and different paralleled capacitances to power devices. (a) dv/dt of the converter. (b) Voltage spike of the transformer. (c) Efficiency of the DAB converter.

In Fig.16, the efficiency of the DAB converter under light load conditions with various paralleled capacitances are shown. It can be seen that the efficiency varies little under different operating power and the efficiency of the converter increases as the paralleled capacitance increases.

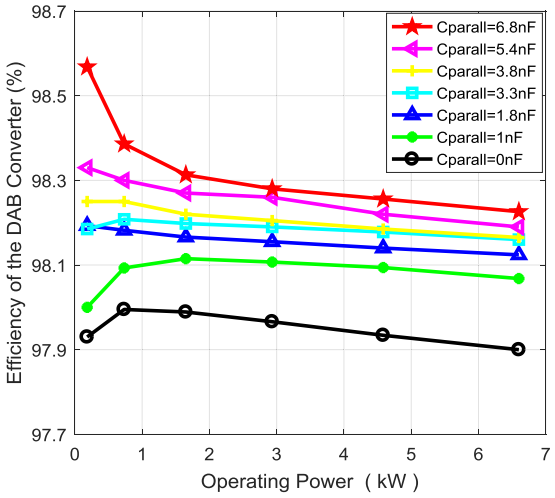


FIGURE 16. Efficiency of the DAB converter under light load conditions with different paralleled capacitances to the power devices.

VI. CONCLUSIONS

Mathematical derivations of the self-resonant frequency of a DAB converter and the frequency distribution of the dv/dt excitation are deduced in this paper, with the conclusions that there is an optimal value of dv/dt of the converter to solve the HFO problem in DAB converters. The analytical formula of the optimal dv/dt is derived to eliminate the HFO problem in the DAB converter theoretically. Accordingly, a method of reducing dv/dt to an optimal value by connecting paralleled capacitors to the power switches is proposed to solve the HFO problem. Simulations and experiments are carried out to validate the proposed method, which corresponds to the theoretical analysis well.

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