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An Energy Metering Chip With a Flexible Computing Engine

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ABSTRACT This paper presents an energy metering chip with a flexible computing engine. The flexible computing engine includes the metering program and a dedicated DSP. Besides providing the generally required energy metering data, the chip can also provide different energy metering and measurement data through the control registers accessible by a host MCU via the UART or SPI interface. The flexible computing engine adjusts the computing tasks of the DSP according to applications, reducing the amount of redundant computing and, therefore, reducing the power consumption. The chip can be used in general energy metering, fundamental energy metering, direct current (DC) energy metering, and various measurement and monitoring of the electricity signals. The energy metering chip is fabricated in a 0.11-μm CMOS process. The chip meets the metering accuracy requirements by the international standard IEC-62053-21/22/23/24. The grid monitoring of the chip meets the international standard IEC-61000-4-30 Class S. The total power consumption when performing the energy metering is only 6.6 mW. The chip is currently in production.

INDEX TERMS Energy metering and measurement, dedicated DSP, grid monitoring.

I. INTRODUCTION

The energy Internet of Things (EIoT) develops rapidly to meet the growing energy demand in a robust, flexible, environmental-friendly, and cost-effective way [1]. As the grid evolves into the EIoT, smart energy meters are not just energy metering devices but also sensor nodes that sense and process the signals on the network and transmit the information to the host [2].

For the energy metering, the traditional methods are total energy metering and fundamental energy metering for Alternating Current (AC) signal. Most renewable energy is DC signal where the DC energy metering is required. Moreover, a smart meter consists of an MCU and a metering chip. The traditional grid monitoring is realized by software in the MCU or DSP units inside the MCU. Flexibility comes with the software implementation. However relative to a hardware implementation, the software implementation is inferior in terms of response time, reliability, etc. There is a trend to realize some of the grid monitoring in hardware. In addition, as the sensor nodes of EIoT, smart meters need to be deployed in large numbers. It is estimated that during the ''Thirteenth Five-Year Plan'' period, China will add 460 million smart meters. According to the BERG Insight [3], in Europe, it is estimated that 80% of all the meters will be smart meters in 2020 for a goal of 20% renewable energy [4].

Thus, it is valuable to design an energy metering chip that can meter both AC signal and DC signal as well as monitor the grid by hardware according to the international standard IEC-61000-4-30. It is also very meaningful to study how to reduce the power consumption of the chip.

There are many researches on the design of smart meter and smart monitoring system. A real-time monitoring system of electrical quantities is proposed, which can monitor the energy consumption on a building [5]. The electrical energy is measured by voltage and current sensors and calculated in a single on-board ARM processor. A smart meter integrating a measurement unit and a computing unit is also proposed in [6]. The computing unit is an MCU which processes the waveform sampled by the measurement unit. The computing tasks of the two systems are implemented by the software. This type of implementation consumes more power than

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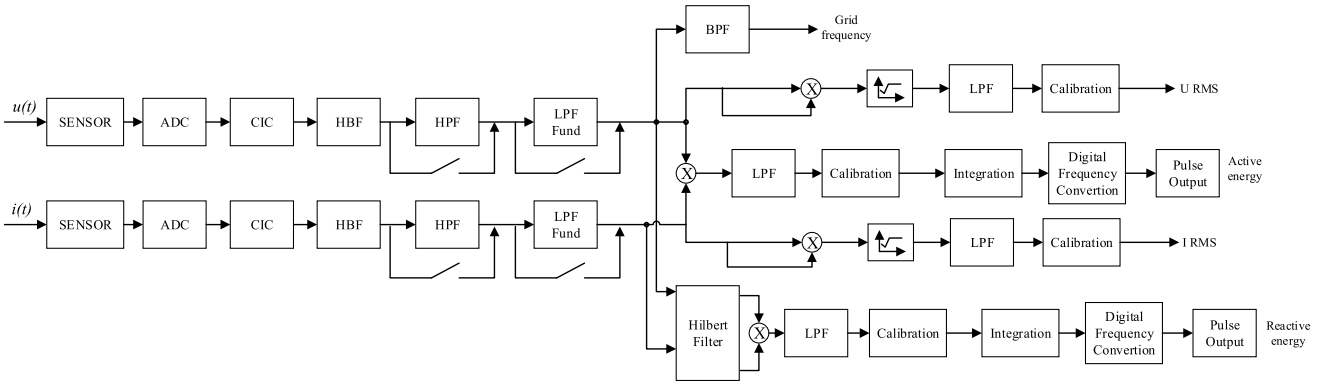

FIGURE 1. Metering algorithm.

the application specific integrated circuit (ASIC). There are several reported ASIC chips for energy metering. An SoC integrating a high precision metering sensing and processing unit and a power line communication (PLC) modem is proposed in [7]. The metrology sub-system provides active and reactive energy measurement with less than 0.1% error over a 5000:1 dynamic range. A low-cost smart energy monitoring and control system for smart buildings based on the ADE7753 is provided in [8]. Reference [9] proposed a smart anti-tampering algorithm design for single phase smart meter equipped with an energy metering chip ADE7953. Two measurement and monitoring systems are based on ADE7758[10]–[11]. ADE7753 and ADE7758 achieve less than 0.1% active energy error over a dynamic range of 1000:1 while ADE7953 achieves 0.1% error of active and reactive energy over a dynamic range of 3000:1. They can also measure the dip and swell event [12]–[14]. There are also newest commercially available energy metering chips of famous incorporation. The ADE9153A of ADI. Inc. provides total active, reactive and apparent power/energy, RMS and fundamental reactive power/energy [15]. This chip can achieve less than 0.1% total active energy and total reactive energy error over a dynamic range of 3000:1. It provides dip and swell measurements and over-current detection. The STPM32 of ST. Inc. only provides total energy data [16]. This chip can achieve less than 0.1% metering error of total active energy over a dynamic range of 5000:1 and total reactive energy error over a dynamic range of 2000:1. It provides over- and under- current and voltage detection. The CS5490 of Cirrus Logic Inc. provides the total energy data as well as dip and swell measurements and over-current detection [17]. Its power consumption is 13mW when performing the energy metering. This chip can achieve less than 0.1% error of total active and reactive energy over a dynamic range of 4000:1. These chips do not support the fundamental energy metering, even though they support the DC energy metering.

In this paper, an energy metering chip with a flexible computing engine is presented. The flexible computing engine consists of the metering program and a dedicated DSP. The metering algorithm is stored as the program of the dedicated DSP in the ROM of the chip. The flexible computing engine provides the total energy data and optional types of the fundamental energy data. The type of fundamental data can be altered by configuring the control registers through the UART or SPI interface without modifying the program in the ROM. This approach reduces the cost of re-tape-out while adapting to different applications and reduces the power consumption of the chip. The chip also supports DC energy metering. In addition, the 1/2-cycle real mean square (RMS) and the 10-cycle RMS/12-cycle RMS (for different grid fundamental frequencies) according to the IEC-61000-4-30 Class S can provide instantaneous RMS measurements for real-time monitoring. The fast detection of over- or under- voltage and current is also provided based on the waveform. Meanwhile, the waveform can not only be uploaded to the host MCU in real time for in-depth analysis but also be stored in the waveform memory of the chip. The presented energy metering chip has been fabricated in a 0.11μm CMOS process. Through testing the actual chip, both total and fundamental energy and RMS have been accurately calculated at a minimum operating frequency of 3.2MHz. The test chip meets the metering accuracy requirements by the international standard IEC-62053-21/22/23/24.

The remaining paper is organized as follows. Section II introduces the metering algorithm briefly. Section III details the chip design. Section IV illustrates the measurements of the chip. Finally, the conclusions are drawn in Section V.

II. METERING ALGORITHM

The metering algorithm is shown in Fig. 1. It enables accurate calculation of the total and the fundamental active power, reactive power, RMS of the voltage and the current, apparent power and the grid fundamental frequency. The computational process of the fundamental power/energy and the total power/energy is the same. They differ in the raw waveform, where one is the total wave which is the waveform of the signal within the metering bandwidth and the other is only the fundamental waveform low-pass filtered (LPF_Fund) from the total wave. The metered active/reactive energy is obtained by integrating the active/reactive power over time. When

the integrated energy is larger than the energy threshold, an energy pulse is generated. The process of the integration and the generation of energy pulses is implemented in hardware.

Assume that the voltage and current signals sampled by the analog-to-digital converter (ADC) are

$$u(t) = \sum_{k=1}^{n} (U_k \cdot \cos(\omega_k t + \varphi_{u_k}) + U_0 \tag{1}$$

$$i(t) = \sum_{k=1}^{n} (I_k \cdot \cos(\omega_k t + \varphi_{i_k}) + I_0 \tag{2}$$

where U_k and I_k are the amplitude of voltage and current of the k^{th} harmonic respectively, ω_k is the angular frequency of the k^{th} harmonic, t is the time value, φ_{uk} is the phase of the voltage and φ_{ik} is the phase of the current of the k^{th} harmonic. U_0 is the DC of the voltage while I_0 is the DC of the current. The cascaded integrator comb (CIC) filter [18]–[19] and half-band filter (HBF) filter out the high frequency noise and determine the metering bandwidth. The DC component is filtered out by high-pass filter (HPF) in the AC energy metering. The HPF can be bypassed to meter the DC energy.

According to the IEEE standard 1459-2010 [20], the instantaneous power is the multiplication of the voltage and the current. It is given by

$$\begin{aligned}
p(t) &= u(t) \cdot i(t) \\
&= \sum_{k=1}^{n} (U_k \cdot I_k \cdot cos(\omega_k t + \varphi_{u_k}) \cdot cos(\omega_k t + \varphi_{i_k})) \\
&\quad + \sum_{j=1, j\neq k}^{n} \sum_{k=1}^{n} (U_k \cdot I_j \cdot cos(\omega_k t + \varphi_{u_k}) \cdot \\
&\qquad \times cos(\omega_j t + \varphi_{j_k})) \\
&\quad + I_0 \cdot \sum_{k=1}^{n} (U_k \cdot \cos(\omega_k t + \varphi_{u_k}) \\
&\quad + U_0 \cdot \sum_{k=1}^{n} (I_k \cdot \cos(\omega_k t + \varphi_{i_k}) + U_0 \cdot I_0 \\
&= \sum_{k=1}^{n} (\frac{1}{2} U_k \cdot I_k \cdot cos(\varphi_{u_k} - \varphi_{i_k})) \\
&\quad + \sum_{k=1}^{n} (\frac{1}{2} U_k \cdot I_k \cdot cos(2\omega_k t + \varphi_{u_k} + \varphi_{i_k})) \\
&\quad + \sum_{j=1, j\neq k}^{n} \sum_{k=1}^{n} [\frac{1}{2} m U_k \cdot I_j \cdot cos((\omega_k + \omega_j)t \\
&\qquad + \varphi_{u_k} + \varphi_{j_k})] \\
&\quad + \sum_{j=1, j\neq k}^{n} \sum_{k=1}^{n} [\frac{1}{2} U_k \cdot I_j \cdot cos((\omega_k - \omega_j)t \\
&\qquad + \varphi_{u_k} - \varphi_{j_k})] \\
&\quad + I_0 \cdot \sum_{k=1}^{n} (U_k \cdot \cos(\omega_k t + \varphi_{u_k}) \\
&\quad + U_0 \cdot \sum_{k=1}^{n} (I_k \cdot \cos(\omega_k t + \varphi_{i_k}) + U_0 \cdot I_0
\end{aligned} \tag{3}$$

Due to the periodicity of the cosine signal, the active power is defined as [13], which is

$$\begin{aligned}
P &= \frac{1}{hT} \int_{\tau}^{\tau+hT} p(t)dt \\
&= U_0 \cdot I_0 + \sum_{k=1}^{n} (\frac{1}{2} \cdot U_k \cdot I_k \cdot cos(\varphi_{u_k} - \varphi_{i_k}))
\end{aligned} \tag{4}$$

The metering of the active energy is the integration of the active power over time after calibration for the gain and phase error, where h is usually set to 1. The active energy is compared with the energy threshold. When the active energy is larger than the threshold, an energy pulse is generated.

The definition of the reactive power is the same except the phase between the voltage and current is shifted by 90 degrees. The Hilbert filter is utilized to realize the 90-degree phase shift [21].

The RMS can be usually averaged within the integer of half fundamental period. Based on [20], the RMS of the voltage and current is given by (5) and (6) respectively.

$$\begin{aligned}
U_{RMS} &= \sqrt{\frac{1}{hT} \int_{\tau}^{\tau+hT} (u(t) \cdot u(t))dt} \\
&= \sqrt{U_0^2 + \frac{1}{2} \cdot \sum_{k=1}^{n} U_k^2}
\end{aligned} \tag{5}$$

$$\begin{aligned}
I_{RMS} &= \sqrt{\frac{1}{hT} \int_{\tau}^{\tau+hT} (i(t) \cdot i(t))dt} \\
&= \sqrt{I_0^2 + \frac{1}{2} \cdot \sum_{k=1}^{n} I_k^2}
\end{aligned} \tag{6}$$

As for the grid fundamental frequency, it is measured by counting the number of the high frequency clock cycles between two successive zero crossing points. The zero-crossing point is acquired by the signal through the band pass filter (BPF). The BPF is a second order elliptical filter with the transfer function

$$H(z) = \frac{1-a}{2} \cdot \frac{1 - z^{-2}}{1 + bz^{-1} + az^{-2}} \tag{7}$$

where a and b are the coefficients of the filter. The amplitude-frequency response in the 50Hz grid is shown as Fig. 2.

By configuring the coefficients of BPF, the center frequency can be set at the grid fundamental frequency.

III. CHIP DESIGN

A. CHIP ARCHITECTURE

The architecture of the presented energy metering chip is shown in Fig. 3.

For the analog module, there are three analog programmable gain amplifiers (APGAs) and high-performance analog to digital converters (ADCs) that dictate the accuracy

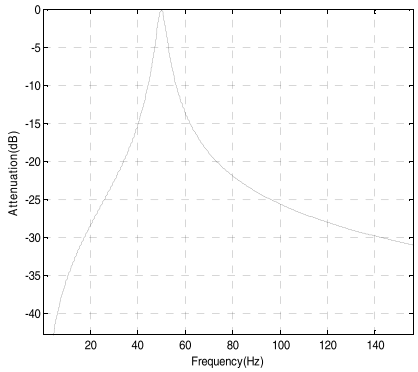

FIGURE 2. The amplitude-frequency response of the BPF.

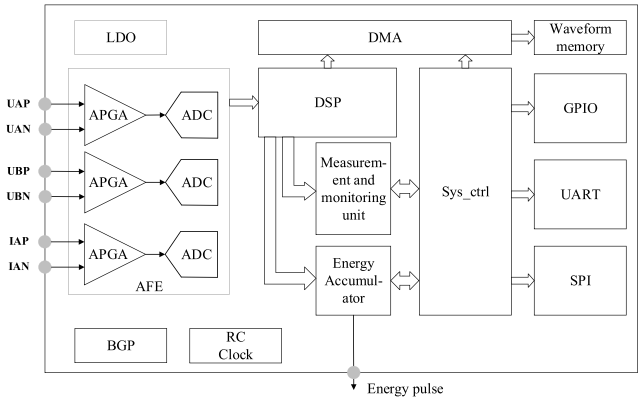

FIGURE 3. Chip architecture.

of the metering. Both APGAs and ADCs use the chopper stabilization technique to reduce the flicker noise that can limit the metering accuracy. The ADCs are the second order sigma-delta modulators. It is widely used in high precision narrow band applications. There is also a low-power low dropout linear regulator (LDO), a bandgap circuit (BGP) and a resistor-capacitor (RC) clock generator circuit. The low-power LDO supplies the power to the chip. The BGP generates a 1.2V reference voltage with a typical performance of 10ppm/°C. Normally, the system clock is provided by an external crystal. When using in the application without external crystal, the RC clock generator provides the system clock for the digital circuits.

For the digital module, there are a dedicated DSP, an energy accumulator, a measurement and monitoring unit and a direct memory access (DMA) unit which are detailed in the following parts. There are also UART and SPI interface which can access the registers or SRAMs by the host MCU. The UART and SPI interface share the IO ports. The chip automatically detects the current communication interface. Besides, the general-purpose input/output (GPIO) determines the functions of IO ports and the system control unit (Sys_ctrl) controls the operation of each unit.

B. ANALOG MODULE: APGA AND ADC

The signal coming from current sensors are usually small. To utilize the dynamic range of an ADC, we use a low-noise

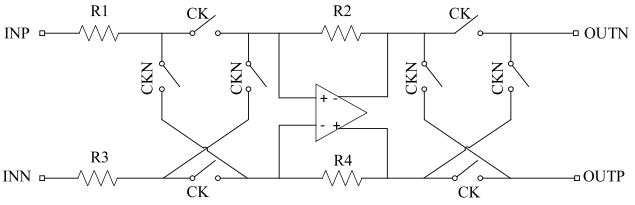

FIGURE 4. Block diagram of APGA.

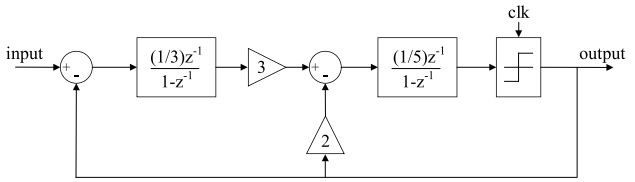

FIGURE 5. Architecture of the sigma-delta modulator.

APGA with chopper stabilization [22]. The block diagram of APGA is shown in Fig. 4.

It is composed of eight switches, four resistors and one operational amplifier. These switches are controlled by the chopping clock. CK and CKN are anti phases. Resistors together with the operation amplifier amplify the input signal by a factor of R2/R1 (R1 = R3; R2 = R4).

The ADCs are 2nd sigma-delta modulators. The clock frequency is 819.2kHz with an oversampling ratio of 64, 128 or 256. The architecture of this sigma-delta modulator is shown in Fig. 5 [23].

In this modulator, there are two integrators and one quantizer. The coefficients of these integrators are not ideal but 1/3 and 1/5, or else the output of these two integrators will saturate and drive the transistors in the integrators into deep linear status. This would severely decrease the performance of the integrators.

C. FLEXIBLE COMPUTING ENGINE: DEDICATED DSP

The flexible computing engine consists of the metering program and a dedicated DSP. The metering algorithm is stored in the ROM as the metering program for the dedicated DSP.

The dedicated DSP is equipped with an ultra-reduced instruction set (URIS). TABLE 1 shows the instruction set.

There are five types of instructions in the URIS. The first type is the NOP instruction realizing the function of waiting. The second type is the memory management (MMU) instruction. By them, the memory is accessed by the DSP cores. Also the registers of the DSP cores can be swapped among them. The third type is the ALU instruction realizing add (ADD), subtraction (SUB), shift (SHF), multiplication (MUL) and radication (RAD) instruction. For the adding and subtracting, data A can be added/subtracted by several times or half or one quarter or one eighth of data B. The expansion of data B is protected by anti-overflow. In this way, most FIR filters can be realized in a fewer clock cycles. For the multiplication, there is a single-cycle multiplier. For the radication, the operating period are 25 clock cycles. The square root extractor is

TABLE 1. Ultra reduced instruction set.

Instruction		Function
NOP	NOP	Blank instruction
MMU	MRD	Read data from SRAM
	MWR	Write data to SRAM
	MSP	Swap data between A and B register
ALU	ADD	Addition
	SUB	Subtraction
	SHF	Shifting
	MUL	Multiplication
	RAD	Radication
CND	CND	Condition of jump
JMP	JMPA	Absolute jump
	JMPC	Conditional jump

not used in most filters and is optimized for area. The fourth type is the CND instruction. It can be used in the jump and comparison. The fifth type is the JMP function. It controls the program counter. By them, the program counter jumps to an absolute address or a relative address.

The architecture of the dedicated DSP is shown in Fig. 6.

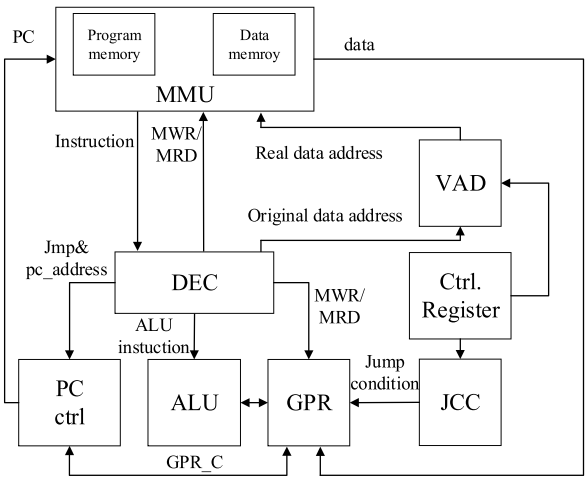

FIGURE 6. DSP architecture.

In order to achieve optional types of the fundamental data without changing the ROM, the dedicated DSP equips with a virtual address decoder (VAD) and a jump condition controller (JCC). The VAD can re-map the virtual address in the metering program to the corresponding real address according to the control register. The JCC determines whether the jump condition is satisfied and assigns a value to the jump condition register.

For the process of program operation, according to the address provided by the program counter (PC), the corresponding instruction is sent to the instruction decoder (DEC) from the ROM which is the program memory.

For the ALU instruction, data from the GPR module is calculated in the ALU. There are two 64-bits registers and 1-bit register in the general purpose register (GPR) module. The two 64-bits registers are used for storing temporary data for calculating. The 1-bit register is the condition in the conditional jump instruction.

For the MMU instruction, the MMU module is used to write the data from the GPR to the SRAM or the data registers, and read the data from the SRAM or the data registers to the GPR. In this instruction, the data address is divided into the real address and the virtual address. The real address is the memory address of arithmetic results and the temporary data while the virtual address does not take up any memory space. The virtual address is re-mapped to the real data address determined by the control registers in the VAD module.

For the JMP instruction, PC will jump to the generated PC address when performing the JMPA instruction. In the conditional jump, the JCC operates and sends the information whether the jump condition is satisfied to the GPR. Then the GPR generates GPR_C signal to the PC ctrl module to adjust the PC. With the satisfaction of the jump condition, the PC generates the executing address to the program memory.

In this chip, the program operation is implemented in a two-stage pipeline. Without the pipeline design, each program will take at least two clock cycles to be executed, which reduces the operating efficiency. Meanwhile, in order to reduce the chip size and power consumption, there is a trade-off that more than two-stage pipeline is not applied [24]. In order to speed up the operation, while the sequential logic of digital circuits is triggered by the rising edge, only the execution unit utilizes the falling edge of the clock to perform arithmetic and memory access. The operation process is divided into the sequential execution and the non-sequential execution.

Fig. 7 shows the sequential execution. The PC increments one to the original program address every clock cycle. The longest decoding path of the digital circuit is the virtual address decoding. However, the transition time of these combinational logics is much less than half a clock cycle in the 0.11μm CMOS process. Therefore, there is a little issue to utilize the both clock edges in this design.

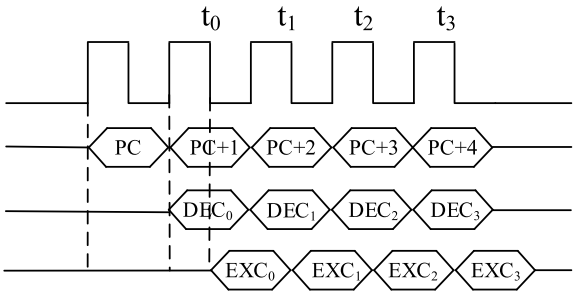

FIGURE 7. Sequential execution.

Fig. 8 shows the non-sequential execution. Due to the pipeline design, the execution unit steps into the idle state when the instruction decoder generates the JMP command. The execution unit will not respond and perform any execution, while only the PC and the instruction decoder work.

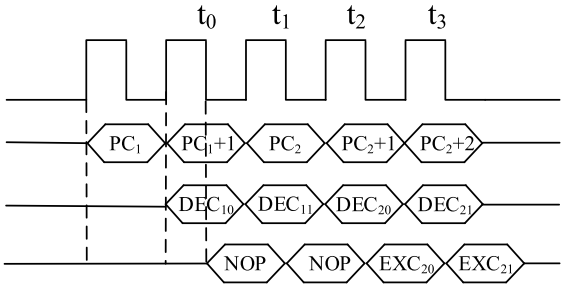

FIGURE 8. Non-sequential execution.

When the PC has jumped to the corresponding program address, the execution unit resumes working.

D. FLEXIBLE COMPUTING ENGINE: IMPLEMENTATION OF METERING PROGRAM

The metering bandwidth and the operating frequency of the DSP determine the computing period for each sampling point which is 1024 clock cycles. All the tasks to be executed by the dedicated DSP are divided into two categories. One is the arithmetic task related to the metering algorithm while the other is the control task related to the operation sequence of the metering program. The both tasks are stored in the ROM as the operating program of the DSP.

The flow diagram of the program implementation is shown in Fig. 9.

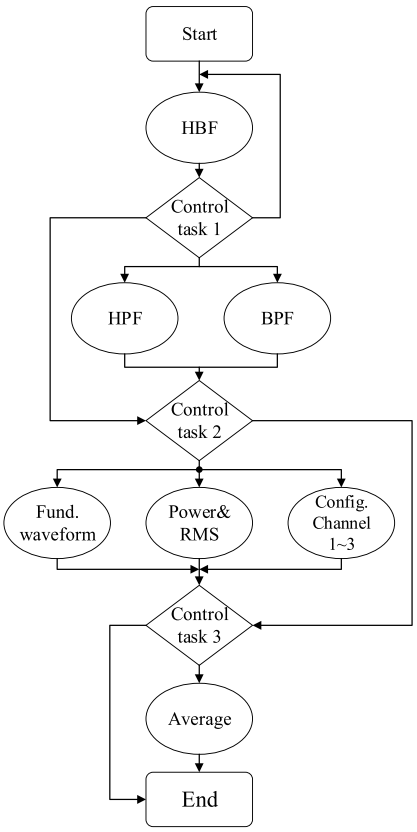

FIGURE 9. Flow diagram of the program implementation.

The control tasks determine the operation sequence of arithmetic task within each computing period. In any control task, up to 16 jump conditions are automatically generated according to the configured metering mode. In different metering modes, the metering bandwidth, the type of the fundamental data, the refreshing time of the data and the initial delay of filters can all be configured. The control tasks are executed in order. With the first condition satisfied, the PC jumps to the corresponding arithmetic task or any control task immediately. However, if it is not satisfied, the operation sequence is determined by the next jump condition. If none of the jump conditions are met, the PC jumps to the end of the metering program and waits for resetting. The arithmetic tasks can be executed at the minimum operating frequency of 3.2MHz.

For the arithmetic task, it is divided into four categories. The first type is the HBF operation. Each time the signal passes through the HBF, the metering bandwidth is reduced by half. The number of HBF can be configured by the control register. When performing two or more HBF operation, the control task 1 automatically jump to the program start or the next arithmetic task according to the number of HBF.

The second type is the HPF and BPF operation. When the signal passes through the HPF, the AC energy metering is enabled. When bypassing the HPF, the DC energy metering can be realized. The output of the BPF is used to measure the gird fundamental frequency through counting the clock cycles between two continuous zero-crossings When performing the DC energy metering, the control task 1 jumps to the control task 2 immediately.

The third type includes threes subclasses, which are the calculation of fundamental waveform, the calculation of fundamental power/RMS in three configurable channels and the calculation of total power/RMS. For each arithmetic task in the subclass of this type, the operation frequency can be configured by the control registers and controlled by the control task 2 independently. In this type, besides providing the total power and RMS, three configurable computing channels for fundamental data are designed. By configuration, the type of the fundamental data can be optionally calculated. Three data from the fundamental active/reactive/apparent power and voltage/current RMS can be selected for calculation in these channels. It is not implemented by storing all the fundamental calculation programs, but by means of program multiplexing. This does not increase the size of program memory and data memory while it decreases the power consumption of DSP operation. However, this multiplexing method requires hardware cooperation where the VAD and JCC in the DSP architecture work. The implementation of the configurable channel is shown in Fig. 10.

The similarity among active power, reactive power and RMS calculation is that the input signals multiply and the multiplication passes through a low-pass filter (LPF) presented in the Fig. 1. The difference is that the signals before calculating the reactive power need to pass through the Hilbert filter and in the RMS calculation the multiplication

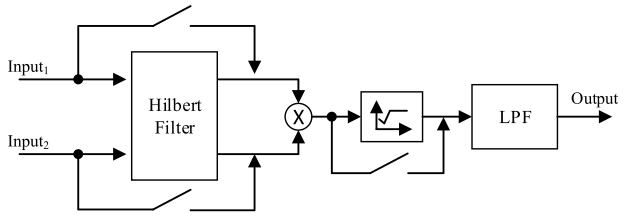

FIGURE 10. Implementation of the configurable channel.

needs to perform square root operation. In these channels, the real address of the input and output data is controlled by the VAD according to the computing type of fundamental data. Through the execution of the JCC and control task 2, it is selected whether the input signals pass through the Hilbert filter and whether the square root operation performs. The three configurable channels share the same program of the Hilbert filter as its program size is far larger than that of the square root and the LPF.

The fourth type is the averaging calculation of the total and the fundamental data. The averaging period for each data can be configured by the control registers independently. The operation frequency of this type is considerably low and, therefore, the control task 3 will jump to the end of the program if none of arithmetic tasks need to be executed.

E. ENERGY ACCUMULATOR

There are two energy accumulators in the chip. Each energy accumulator can selectively accumulate the total active power, reactive power, apparent power, RMS or three types of the fundamental data. Fig. 11 shows the architecture of the energy accumulator.

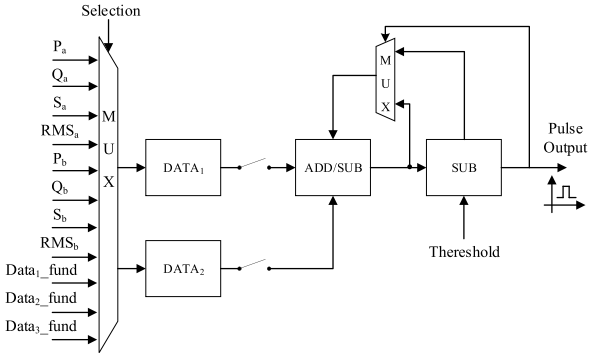

FIGURE 11. Architecture of energy accumulator.

The energy accumulator can add or sub two metering data and can also achieve the accumulation of single data. Afterwards the accumulation subtracts the energy threshold. Once the difference is positive, the energy accumulator will generate a pulse with a fixed width of 80ms. Energy accumulator operates in the normal mode or the low-power mode. In the low-power mode, the accumulation frequency is 32768kHz. As in the normal mode, the accumulation frequency is 204.8kHz. However, fast accumulating frequency yield better metering accuracy yet at higher power dissipation.

As there is the gain and phase error in the voltage and the current sensor outside the chip, each energy metering chip in the smart meter needs to be calibrated before getting into the application. Through comparing the difference between the interval of the generated pulses and the interval of the standard pulses, the calibration can be achieved. In addition, through counting the number of the energy pulses, the consuming energy can be acquired.

F. MEASUREMENT AND MONITORING UNIT

The chip measures the grid fundamental frequency, the magnitude of the supply voltage, the supply voltage dips and swells, the voltage interruptions and the transient voltages according to the IEC standard 61000-4-30 Class S.

The grid fundamental frequency is measured by passing signal through the BPF. Its center frequency can be programmed by coefficients for the 50Hz or 60Hz grid. The measured frequency can also be averaged to provide better accuracy. Besides, the 1/2-cycle RMS and 10-cycle RMS/12-cycle RMS are provided by the DSP. The magnitude of the supply voltage and transient voltage is based on the 10 cycle RMS/12 cycle RMS. The supply voltage dips and swells and voltage interruptions depend on the 1/2 cycle RMS of voltage. In order to ensure that the measurement results do not change frequently when the signal is near the threshold, the hysteresis is provided for every measurement. For instance, when the 1/2 cycle RMS is below the lower threshold, the dip event happens. The dip event disappears with the 1/2 cycle RMS larger than the upper threshold. There are the upper threshold and the lower threshold for every measurement, which can be configured through the registers.

In addition, there is a fast detection unit which is used to detect over- or under- voltage or current based on the waveform. There are upper and lower threshold for one channel detection. For example, to detect the over voltage, the monitoring unit records the number of points which are over the configurable threshold and generates an interrupt signal or flags the status bit when the criteria are met. In the same way, the over- or under- voltage and current can be detected simultaneously.

G. DMA AND WAVEFORM MEMORY

There is a direct memory access (DMA) which can automatically transmit the captured waveform to the host MCU. The DMA operates every sampling point of the signal. With the captured waveform accessible by the MCU, the MCU can perform grid analysis. In traditional commercial applications, MCU reads the waveform based on the interrupt of timer. When utilizing the presented DMA, it reduces the work-load of external MCU and increases the reliability of the system. The speed of the DMA automatically adjusts by the number of transmitting channels and sampling points.

In applications that require electrical isolation, the time of waveform transmission is not enough for every

sampling point. Furthermore, a waveform memory is built into the chip. This waveform memory can store one or two channels of waveform according to the configuration. It can record the waveform before or after a measurement event occurs or record waveform manually determined by the control register. Fig. 12 shows the structure of the waveform memory.

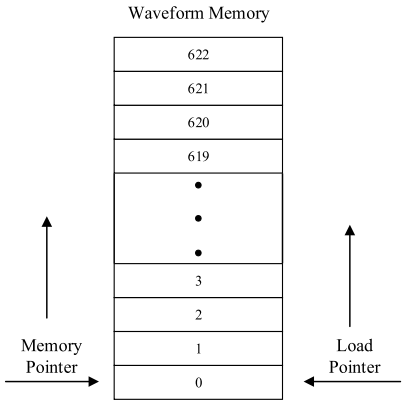

FIGURE 12. Waveform memory.

The waveform memory can store up to 622 16-bits waveform for tolerating the offset of the grid fundamental frequency. The memory pointer and the load pointer are controlled separately. Due to the limited memory space, when the memory pointer or the read pointer reaches the maximum, they automatically jump to the zero address.

IV. MEASUREMENT RESULTS

A. CHIP INFORMATION

The presented chip is fabricated in the 0.11μm CMOS process and the die photo of the chip before packaging is shown as Fig. 13. The chip information is shown as Table 2.

TABLE 2. Chip information.

Area including pads	1.2*1.4mm^2
Power supply voltage (Digital circuit)	1.5V
Power supply voltage (Analog circuit)	3.3V
Power consumption (3.2MHz, three ADCs and energy metering on)	6.6mW
ROM size	3072x17bits
SRAM size	880x32bits

B. MEASUREMENTS

The chip is used in an energy meter and tested in the environment of HS-3303 [25] which is shown in Fig. 14. HS-3303 is a single phase/three phase electricity meter test equipment. It integrates a standard power source, a standard reference meter (HS-5300) [26] and a high accuracy error processor. The testing accuracy of HS-3303 can reach 0.05%. The standard power source generates the voltage and current to the standard reference meter and the device under test (DUT). HS-3303 can sample the energy pulses of the test chip and the standard meter for the measurement of the metering error. By comparing the difference between the interval of DUT and the standard interval, the high accuracy error processor can measure the metering error of the energy. The metering error of the energy is defined as

$$E_m = \frac{T_{DUT} - T_{sta}}{T_{sta}} \times 100\% \tag{8}$$

T_{DUT} is the interval between two continuous energy pulses for the tested chip. T_{sta} is the standard interval for the standard meter. E_m is the metering error. As for the RMS, the tested value is compared with the value that the standard power source displays

There are four experiments for the energy metering and the grid monitoring. At first, the following experiment is to measure the accuracy of the total and the fundamental active energy, the reactive energy and the RMS of voltage

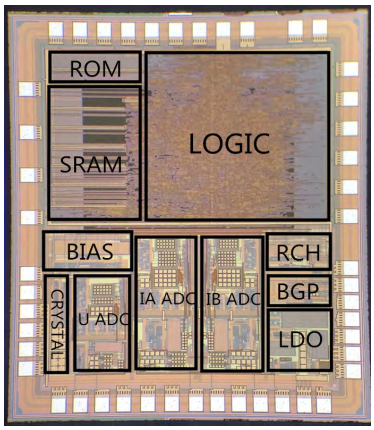

FIGURE 13. Die photo.

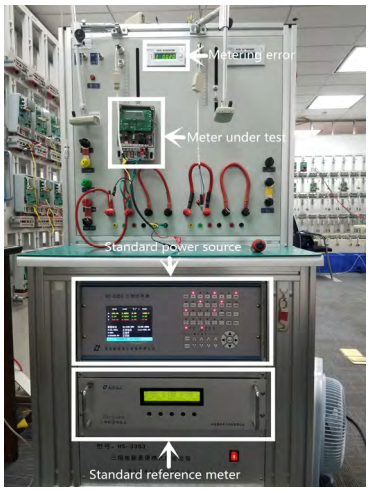

FIGURE 14. HS-3303 Instrument.

TABLE 3. Metering error of total active and reactive energy over the dynamic range in sinusoidal environment.

Current supply	power factor 1.0 (units: %)		power factor 0.5 Inductive load (units: %)		power factor 0.8 Capacitive load (units: %)	
	Total Active energy	Total Reactive energy	Active energy	Reactive energy	Active energy	Reactive energy
I_{max}	-0.013	-0.014	-0.011	-0.010	0.009	-0.010
$0.5I_{max}$	-0.007	-0.031	-0.002	-0.024	0.014	-0.015
I_b	0.008	-0.037	-0.007	-0.048	0.012	0.050
$0.1I_b$	0.025	-0.030	0.025	-0.034	0.023	0.026
$0.05I_b$	0.019	-0.020	0.011	0.025	0.014	0.032
$0.02I_b$	0.021	-0.028	-0.019	-0.031	0.031	0.041
$0.01I_b$	0.033	-0.029	-0.037	-0.037	-0.026	0.030
$0.004I_b$	-0.025	-0.043	0.028	-0.040	-0.034	-0.048

TABLE 4. Metering error of other energy and rms in sinusoidal environment.

	Power factor:1.0 (unit: %)	Power factor:0.5 Inductive load (unit: %)	Power factor:0.8 Capacitive load (unit: %)
Fundamental active energy	-0.029	0.008	0.013
Fundamental reactive energy	-0.057	-0.048	-0.058
Total Voltage RMS	0.030	0.032	0.034
Total current RMS	-0.061	-0.043	-0.054
Fundamental Voltage RMS	0.029	0.021	0.028
Fundamental current RMS	-0.063	-0.063	-0.048
1/2-cycle Total voltage RMS	0.201	0.232	0.216

and current in the sinusoidal system. The input voltage is 220V. The dynamic range is defined as the ratio between the maximum input current and the minimum input current. In this testing environment, I_{max} is the maximum input current of electricity meter, and I_b is the rated current. I_{max} is equal to 100A while I_b is 5A. Then the tested dynamic range (DR) of the chip is

$$DR = \frac{I_{max}}{0.004I_b} = \frac{5000}{1} \tag{9}$$

These electricity data are tested for different power factors. The metering error of active/reactive energy is averaged 20 times and the total and the fundamental RMS of voltage and current is averaged 10 fundamental cycles. The metering error of the 1/2-cycle total voltage RMS is the maximum error among 10 fundamental cycles.

At first, we tested the metering errors in different current amplitudes and different power factors in the sinusoidal environment. In TABLE 3, the first column represents the amplitude of the input current signal. As can be seen from TABLE 3, the metering errors are no more than 0.1%. The total active/reactive metering accuracy of 0.1% is achieved in the dynamic range of 5000:1. The metering error of fundamental active/reactive energy, 10-cycle total and fundamental voltage and current RMS and 1/2 cycle voltage RMS is measured with the rated input current. From TABLE 3 and TABLE 4, the metering error of total and fundamental active energy is less than 0.2% which is the limit in the IEC-62053-21/22. The metering error of total and fundamental reactive energy is less than 0.5% which is the limit in the IEC-62053-23/24. According to the IEC-61000-4-30 Class S standard, the measurement uncertainty of the events of grid monitoring depends on the accuracy of the RMS. The metering error of 1/2-cycle RMS of voltage is less than 1% and the metering error of 10-cycle RMS is less than 0.5%, which are the limits in the IEC-61000-4-30 Class S standard. Thus, the monitoring events specified in the IEC-61000-4-30 Class S standard can be accurately and timely detected.

Secondly, the chip is tested in the non-sinusoidal system for measuring the accuracy of energy metering. According to IEC62053-21/22/23/24 standard, the test conditions are to add 5^{th} harmonic of voltage and current or only add 5^{th} harmonic of current. The fundamental current amplitude is $0.5I_{max}$ and $0.5I_b$ respectively. The harmonic voltage amplitude is 10% of the fundamental voltage amplitude and the harmonic current amplitude is 40% of the fundamental current amplitude. The power factor is 1.0. This performance is defined by the maximum variation error.

$$max(E_v) = max(E_m - E_a) \tag{10}$$

where E_v is the variation error. E_m is the metering error after adding the harmonic. E_a is the average of 20 metering errors before adding the harmonic. After adding harmonic, the metering error of active/reactive energy is also tested 20 times.

As is shown in TABLE 5, the $max(E_v)$ of the active energy under two conditions is much less than 0.4% and 0.6% which are the limits in the IEC-62053-21/22. The $max(E_v)$ of the reactive energy under two conditions is much less than 2.5% which is the limit in the IEC-62053-23/24.

Thirdly, for the grid fundamental frequency measurement, the grid fundamental frequency can be obtained directly by accessing the registers. According to the IEC-61000-4-30 Class S standard, the fundamental frequency is obtained

TABLE 5. Metering error in non-sinusoidal environment.

		Total active energy	Total reactive energy	Fund. active energy	Fund. active energy
Basic averaged metering error: $0.5I_{max}$ (unit: %)		0.007	-0.031	-0.022	-0.049
Basic averaged metering error: $0.5I_b$ (unit: %)		-0.039	-0.005	-0.018	-0.046
5th harmonic of voltage and current	Maximum variation error: $max(E_v)$ (unit: %)	-0.018	-0.037	-0.019	-0.049
5th harmonic of current		-0.015	-0.031	-0.021	-0.045

every 10 second and the uncertainty shall not exceed 10mHz over the measuring ranges 42.5Hz to 57.5Hz/51Hz to 69Hz. Through experiments, the uncertainty of measured grid fundamental frequency is less than 10mHz with the averaging of 40 fundamental periods which is less than 10 second.

Finally, the timeliness and the flexibility of the grid monitoring is measured by waveform detection. In this experiment, we take the over-current event for example. The measurement period can be configured. We select the fastest and the slowest detection time which is 10ms and 80ms respectively for the 50Hz grid signal. When the over-current event happens, the interrupt signal can be pulled high and trigger the interrupt function in the host MCU for deeper management.

When the amplitude of the input current varies from 40mV to 80mV, we take the variation as the over-current event. The threshold is set to be 50mV and the number of sampling points over the threshold is set to be ten. From Fig. 15 and Fig. 16, the over-current event is detected within the limited time. As the threshold, the number of points over or under the threshold and the detection period can be configured, the flexibility of the grid monitoring by waveform can be achieved. Thus, the presented chip provides the grid monitoring by not only RMS but also waveform.

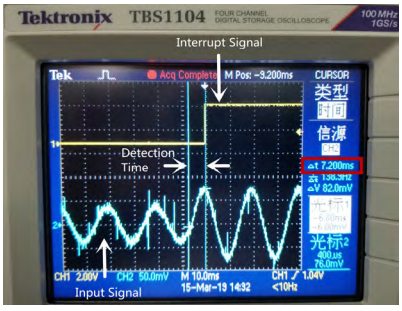

FIGURE 15. Detection within 10ms.

Therefore, the metering accuracy can meet the international standard IEC-62053-21/22/23/24 and the grid monitoring can meet the international standard IEC-61000-4-30 Class S.

C. COMPARISON WITH OTHER METERING CHIPS

The recent researches related to smart meters and smart monitoring systems make use of commercial energy metering chip. Thus, we chose the newest commercial metering chips

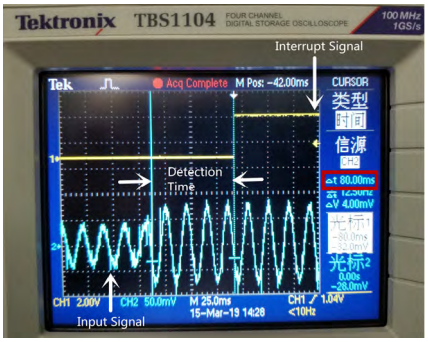

FIGURE 16. Detection within 80ms.

to compare with the presented metering chip in this paper. Besides, the comparison also includes an SoC integrating a metrology sub-system in [7]. The comparison results are shown in TABLE 6.

In terms of the power consumption, it is compared with three ADCs and the energy metering on. For the CS5490, the power consumption is 13mW but there are only two integrated ADCs. With three ADCs and the energy metering on, its power consumption will be over 13mW. As for the ADE9153A, the typical operating current is 9.3mA. Its analog power supply is 1.9V and its digital power supply is 1.7V. The power consumption is larger than the product of 1.7V and 9.3mA which is 15.81mW. Besides, our chip also provides three types of fundamental data and, therefore, the operand of our chip is larger than the CS5490 and the ADE9153A. Nevertheless, the power consumption of our chip is still lower. For the STPM32 and [7], the power consumption is not clear under the same circumstances and hard to be compared.

For the metering accuracy, the metering error in the presented chip achieves 0.1% of total active energy and reactive energy in the dynamic range of 5000:1. Among these chips and scientific work, it is better than or equal to others. In terms of the fundamental metering, only the ADE9153A provides fundamental reactive energy metering and our chip provides all the fundamental metering. And in terms of the grid monitoring, our chip and the ADE9153A can provide the original measurements data and implement the grid monitoring by hardware, which can measure the grid fundamental frequency, the magnitude of the supply voltage, the supply voltage dips and swells, the voltage interruptions

TABLE 6. Comparison with other metering chips.

Chip Number	Power consumption (three ADCs and the energy metering on)	Accuracy/Total Active power dynamic range	Accuracy/Total Reactive power dynamic range	Fundamental energy metering	Grid Monitoring	DMA and waveform memory
The design	6.6mW	0.1% / 5000:1	0.1% / 5000:1	Yes	Yes	Yes
CS5490	>13mW	0.1% / 4000:1	0.1% / 4000:1	No	No (without 10-cycle/12-cycle RMS)	No
ADE9153A	>15.81mW	0.1% / 3000:1	0.1% / 3000:1	No (only fundamental reactive energy)	Yes	No
STPM32	--	0.1% / 5000:1	0.1% / 2000:1	No	No (without 10-cycle/12-cycle RMS)	No
[7]	--	0.1% / 5000:1	0.1% / 5000:1	No (only fundamental active energy)	--	--

and the transient voltages according to the IEC standard 61000-4-30 Class S. Since the CS5490 and STPM32 does not provide 10-cycle/12-cycle RMS, it cannot meet the IEC standard 61000-4-30 Class S. In addition, all chips can perform the DC energy metering. Therefore, our chip not only provides the total energy metering, the fundamental energy metering, the DC energy metering and the grid monitoring, while achieving a 0.1% metering accuracy of total active energy and total reactive energy in the dynamic range of 5000:1, but also achieves low power consumption. Besides, only our chip is equipped with the DMA and the waveform memory which can reduce the work-load of external MCU and increases the reliability of the system when MCU performs grid analysis.

V. CONCLUSION

This paper presents an energy metering chip with a flexible computing engine. The flexible computing engine includes the metering program and a dedicated DSP. Besides providing the generally required energy metering data, the chip can also provide different energy metering and measurement data through the control registers accessible by a host MCU via the UART or SPI interface. The flexible computing engine adjusts the computing tasks of the DSP according to applications, reducing the amount of redundant computing and, therefore, reducing the power consumption. The chip can be used in total energy metering, fundamental energy metering, DC energy metering and various measurement and monitoring of the electricity signals. When the external MCU performs grid analysis, the chip can upload the waveform by DMA or store it in the local waveform memory. The energy metering chip is fabricated in a 0.11μm CMOS process. The test chip meets the metering accuracy requirements by the international standard IEC62053-21/22/23/24. The grid monitoring of the test chip meets the international standard IEC-61000-4-30 Class S. Compared with other commercial metering chips, the chip achieves lower power consumption when three ADCs and energy metering on. The chip is currently in production.

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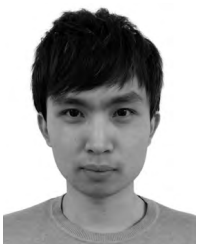

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