

Received February 12, 2019, accepted March 7, 2019, date of publication April 9, 2019, date of current version April 19, 2019. *Digital Object Identifier 10.1109/ACCESS.2019.2909928*

# Condition Monitoring of IGBT Modules Based on Changes of Thermal Characteristics

KEXIN WEI $^{1,2}$ , WENBAI WANG $^{1}$ , ZHEN HU $^{\textcolor{red}{\textbf{\textbf{0}}}}$ , (Member, IEEE), AND MINGXING DU $^{2}$ 

<sup>1</sup> School of Electrical and Information Engineering, Tianjin University, Tianjin 300072, China <sup>2</sup>School of Electrical and Electronic Engineering, Tianjin University of Technology, Tianjin 300384, China <sup>3</sup>College of Automation Nanjing University of Posts and Telecommunications, Nanjing 210003, China <sup>4</sup>College of Artificial Intelligence, Nanjing University of Posts and Telecommunications, Nanjing 210003, China

Corresponding author: Zhen Hu (huzhen0111@126.com)

This work was supported in part by the Tianjin Natural Science Foundation of China under Grant 17JCYBJC21300, and in part by the New Energy Vehicle Key Special Project of the National Key Research and Development Plan under Grant 2017YFB0102504.

**ABSTRACT** Condition monitoring (CM) of insulated-gate bipolar transistor (IGBT) modules is significant for improving power converter reliability and reducing the loss caused by IGBT failure. In this paper, we present an advanced method to evaluate the aging condition of an IGBT based on the changes of thermal characteristics in the module, which can be described by the junction and case temperatures. The variation of the case temperature distribution is used to monitor the solder fatigue. The estimated level of solder fatigue is used to update the parameters in the electrical-thermal model. Then, the junction temperature can be accurately estimated by the updated electrical-thermal model. The difference between junction temperatures estimated from the updated model and temperature-sensitive electrical parameter (TSEP) is utilized to monitor the aging of bond wires. The proposed CM method permits both of health level evaluation and accurate junction temperature estimation of IGBT in real time to prevent catastrophic failure caused by defective modules. The experimental results on a commercialized IGBT product have validated the feasibility of the proposed method.

**INDEX TERMS** IGBT, condition monitor, bond wires, solder fatigue.

### **I. INTRODUCTION**

With the superior performance of high switching frequency, low conduction loss, and high over-current capacity, insulated gate bipolar transistor (IGBT) modules are widely employed in safety-critical power drive systems like electric vehicles (EVs) [1]–[3], aircraft [4], wind turbines [5] and industrial power drives [6]. However, owing to the variable power load and control input, IGBT modules are subjected to additional stresses, which may lead to different extent of thermo-mechanical fatigue/failure and further deterioration in the electric properties, increasing leakage currents and decreasing safe operation areas. According to some studies, 31% of power electronic conversion system breakdowns can be attributed to power devices failure. Consequently, health management of IGBT modules has become an important issue in power electronic applications from the point of view of reliability.

The associate editor coordinating the review of this manuscript and approving it for publication was Luca Cassano.

The two main failure types in IGBT modules are bond wire aging and solder fatigue through power cycling. To address these two major degradation mechanisms, many studies have developed different strategies, such as material and semiconductor technologies [7], [8], package architectures [9] and interconnections [10], advanced control strategy [11] and cooling technologies [12]. However, failures of power devices are still observed in different reliability improvements, which can indicate that redundancy may not be a perfect solution in safety critical and mission critical applications. Then a stronger demand for higher reliability on IGBT modules exists. Analytical methods like X-ray and scanning acoustics microscopy analysis are proposed to observe the degradation level of IGBTs. But these methods are costly, destructive, offline and not able to reveal dynamic condition changes in the system.

To address the aforementioned issues, condition monitoring (CM) was developed to identify incipient faults in the IGBT modules and then take corrective actions before catastrophic failures occur. This easily implemented method

is cost effective, nondestructive, and requires little knowledge on the internal IGBT structure [13]. Furthermore, this method can adapt the degradation model under varying operating conditions. Existing CM techniques or approaches may be divided into the following two categories: electrical-based approaches and the thermal-based approaches.

Electrical-based approaches to performing CM rely on the characteristics of electrical parameters, which change with the aging process of an IGBT module. These approaches are promising for CM because they employ the device itself as a monitoring sensor with high accuracy and a fast response time. The common electrical parameters that can be identified as fault precursors for bond wire-related or solder-related faults consist of the on-state collector-emitter voltage (*VCE*−*ON* ), collector current (*IC*), gate-emitter voltage  $(V_{GE})$ , gate-emitter threshold voltage  $(V_{TH})$ , inverter harmonic current, electrical resistance and switch turn-ON (*Ton*) and turn-OFF  $(T_{off})$  times [14]–[20]. These parameters show significant sensitivity to the bond wire aging or the solder fatigue and are thereby appropriate fault precursors for the aging conditions of IGBT modules. Nevertheless, many challenges exist in electrical-based online implementation, like complexity of measurement circuitry, alteration to the converter structure and compensation of operating conditions.

Thermal-based approaches have been developed to monitor the aging process of IGBT modules in terms of the thermal behavior characteristics inside the modules. The major aging mechanisms in IGBT modules have two thermal consequences: the bond wire aging increases *VCE*−*ON* and, therefore, increase the power loss and heat generation in the IGBT module; the solder fatigue prevents the heat propagation inside the IGBT module, leading to a change in the temperature distribution. For monitoring the bond wire aging, the degradation method through the case temperature  $(T_C)$ of IGBT modules has been proposed in [21]: the aging of bond wires was monitored by the rise of *VCE*−*ON* that was calculated through the power loss estimated by the case temperatures. Unfortunately, the estimation of the increased *VCE*−*ON* has to be performed under steady state conditions to exclude the offsets due to various operating conditions, making this method conservative. For monitoring the solder fatigue, a method of detecting the change of case-to-ambient temperatures has been proposed in [22]: a lookup table providing the power loss information in a healthy IGBT module was incorporated for comparison with the actual power loss calculated from the case and ambient temperatures, which enabled the estimation of solder fatigue under various operating conditions. In these studies, the thermal transient within IGBT modules was assumed to be much faster than the working point varying. This assumption may limit the use of the method in applications, like wind power and electric traction systems, where the environmental and operating conditions may change faster than the duration required for IGBT chips to reach their steady-state temperatures.

According to the discussions above, an online mechanism to monitor the aging of IGBT module under normal working conditions remains challenging and important to improve the reliability of power electronic systems. This paper proposes a novel method that attempts to make use of two types of CM approaches by combining the knowledge of the behavioral characteristics of the electrical parameters and the information observed from the thermal dynamics to improve the monitoring performance. The following three aspects of the work are demonstrated: (a) the aging of bond wires can be indicated by the difference between the junction temperatures estimated through the electrical-thermal model and temperature-sensitive electrical parameter (TSEP); (b) the solder fatigue can be monitored in real time by detecting the change of the case temperature distribution, i.e., the nonuniformity of the temperature distribution at the IGBT's baseplate; and (c) the solder fatigue can lead to biases in the junction temperature estimated from the electrical-thermal model and this influence can be removed to guarantee both the accuracy of the junction temperature and the bond wire aging monitoring. Compared with traditional CM methods, this method accurately monitors the bond wire aging and the solder fatigue in IGBT modules simultaneously under normal working conditions and has the advantage of easy online implementation.

The remainder of this paper is organized as follows. Section II and III are about the bond wire aging and solder fatigue respectively, including the mechanisms and the corresponding parameters for monitoring. In Section IV, the interaction between these two monitoring process and the method for identifying each one in mixed aging in IGBT modules is proposed. In Section V, the feasibility of this series of methods is verified through experimental results.



<span id="page-1-0"></span>**FIGURE 1.** A commercial power module used in the test.

## **II. BOND WIRE AGING AND MONITORING PARAMETERS** A. MECHANISM OF BOND WIRE AGING

The structure of a typical IGBT module, as depicted in Fig. [1,](#page-1-0) is composed of several layers made of different materials. Each layer has its own coefficient of thermal expansion (CTE). In the module, by thick parallel aluminum bond wires, semiconductor chips are bridged to direct bond copper (DBC) substrate, which means metal conductors soldered to an insulating dielectric layer.

Temperature swings and the difference between CTEs of Si and Al could induce thermomechanical shear stress on the bond wire/chip interface, which is the main cause of bond wire aging. When the range of temperature swing is  $\Delta T_s$ ,

the total strain  $\varepsilon_{tot}$  on the interface between the silicon chip and its bonded aluminum wires can be described as follows:

<span id="page-2-0"></span>
$$
\varepsilon = L(\alpha_{Al} - \alpha_{Si}) \triangle T_s, \tag{1}
$$

where  $\alpha_{Al}$  and  $\alpha_{Si}$  are the CTEs of aluminum and silicon, respectively, and *L* is the wire contact length.

According to  $((1))$  $((1))$  $((1))$ , considering the large difference between CTEs of the silicon chips and their bonded aluminum wires, and the high temperature swing  $\Delta T$  due to power cycling, the total strain  $\varepsilon_{tot}$  at the interface can be large enough to result in a plastic region. Unlike elastic strain, plastic strain does not disappear even if the mechanical stress is withdrawn. The temperature swings can continually impact the IGBT module, leading to an accumulated plastic strain. Eventually, cracks appear at the edge of the interface and then propagate from both ends to the center along the small grain boundaries of the bond wires. A bond wire can lift off or demonstrate heel cracking when the cracks reach the center.

## B. MONITORING OF BOND WIRE AGING

The aging process of an IGBT module occurs slowly. During the aging process of bond wires, the resistance of the electrical connection rises, resulting in an increase of *VCE*−*ON* . Hence, *VCE*−*ON* can be utilized to characterize the aging level of bond wires. However, *VCE*−*ON* also changes with collector current and junction temperature, limiting the uses under different operating conditions of IGBT modules. An advanced condition monitoring strategy that removes the biases of *VCE*−*ON* caused by the currents and temperatures is reported in [23]. This proposed monitoring strategy is feasible in both static and dynamic conditions. In static conditions, the current is constant, and the temperature variation of heatsink is considered equal to that of junction and used to compensate the offsets of *VCE*−*ON* . However, in most situations, those two temperature variations are not equal, thus an inaccurate compensation can cause a misestimate of the bond wire aging level. In dynamic conditions, *VCE*−*ON* is measured at the intersection point between negative thermal coefficient (NTC) and positive thermal coefficient (PTC) regions, where the value of *VCE*−*ON* is independent of the temperature variations. This indicates that a reference voltage has to be first measured under a fixed working current, making this method conservative.

According to the analysis described above, using *VCE*−*ON* as a indicator of bond wire aging has many challenges in accuracy and implementation. However, *VCE*−*ON* is indeed a temperature-sensitive electrical parameter (TSEP), which can be used to estimate junction temperature *T<sup>j</sup>* . As described above, the aging of bond wires leads to an increase of electrical resistance and, thereby, a rise of *VCE*−*ON* , which ultimately leads to an overestimate of  $T_j$ . That means the  $T_j$ overestimated through *VCE*−*ON* can be a indicator of bond wire aging. Consequently, there is a temperature difference 4*T* between *T<sup>j</sup>* estimated from *VCE*−*ON* and the actual *T<sup>j</sup>* . It has been suggested that  $\Delta T$  depends on bond wire aging and can therefore indicate the aging level of bond wires.



<span id="page-2-1"></span>**FIGURE 2.** Heat flow in a healthy IGBT module [27].

Since bond wire fatigue happens upon the power chip and has no influence on the downward heat transfer paths in the IGBT module, as shown in Fig. [2,](#page-2-1) the actual  $T_i$  can be estimated through the electrical equivalent Foster model [24], [25]. The values of  $\Delta T$  can be calculated as follows:

<span id="page-2-2"></span>
$$
\Delta T = T_{j(V_{CE})} - T_{j (model)},\tag{2}
$$

where  $T_{j(V_{CE})}$  denotes the junction temperature determined from *VCE*−*ON* , and *Tj*(*model*) denotes the actual junction temperature obtained from the Foster model.

During IGBT module operation, varying collector currents *I*<sup>*C*</sup> have the same influence on  $T_j(\gamma_{CE})$  and  $T_j(\text{model})$ ; therefore, the variations of  $T_j(\gamma_{CE})$  due to current changes can be canceled out by the variations of *Tj*(*model*) . Thus, the value of 4*T* only depends on the aging of bond wires. *VCE*−*ON* monotonically increases in the aging process of bond wires, leading to a more serious overestimation of  $T_i$  using  $V_{CE-ON}$ ; this indicates that  $\Delta T$  also rises in step with the aging process of bond wires. Therefore, the  $\Delta T$  in [\(2\)](#page-2-2) can be used to evaluate the bond wire aging in progress. Compared with the method in [23], the proposed method has advantages in accuracy and can be applied to various operating conditions.

## **III. SOLDER FATIGUE AND MONITORING PARAMETERS** A. SOLDER FATIGUE MECHANISM

Solder fatigue is another dominant failure mechanism in

IGBT modules. There are two solder layers, the chip solder layer and the substrate solder layer, as shown in Fig. [2.](#page-2-1) Compared to the chip solder layer, the substrate solder layer is more critically subject to fatigue. Due to the CTEs mismatch under temperature variation, thermo-mechanical stresses are applied upon the solder layers and cause degradation on the interface, such as cracks and/or voids. These cracks or voids decrease the effective heat transfer routes from the chip, increasing the thermal impedance  $Z_{jc}$ . Consequently, the junction temperature of power semiconductor device would increase and could accelerate other failure types, such as bond wire fatigue. Furthermore, the rise of junction temperature could further induce hot spots and thermal runaway in the affected regions of the module. These coupling mechanisms intensify the IGBT module degradation.

## B. MONITORING OF SOLDER FATIGUE

The cracks or voids inside the solder layer can increase *Zjc* and inhibit the heat outflow, then increase the junction temperature and finally change the case temperature. The case temperature can be directly measured, unlike the junction temperature inside the IGBT module. Therefore, the variation

in case temperature is an appropriate thermal parameter for monitoring the solder layer aging of IGBT in practical applications. The rise of case-above-ambient-temperature and the relationship between two case-to-ambient thermal resistances have been applied for real-time solder fatigue monitoring in [21], [22]. However, the ambient temperature can be easily affected by other heat sources so the accuracy of that method may not be guaranteed. Considering this, a new parameter for monitoring the solder fatigue which is unaffected by the ambient heat sources, is proposed and will be described in detail.

As depicted in Fig. [2,](#page-2-1) in an IGBT module, the heat is generated on the top surface of a chip, and transfers down through several layers to the bottom surface of the baseplate. Compared with the chip, the baseplate is much larger and features a wider temperature distribution. Since most heat transfers along the optimal path, i.e., in the vertical direction, the temperature detected in the central area of the baseplate is much higher than that in the edge area. Consequently, the case temperature distribution on the bottom surface of the baseplate is nonuniform.



<span id="page-3-0"></span>**FIGURE 3.** Altered heat flow in a fatigued IGBT module [27].

Due to the effect of thermo-mechanical stress, cracks always start from the edge of the solder layer and then propagate from both ends to the center. These cracks can cut some routes for heat conduction. And the heat can only transfer through the undamaged regions to the baseplate, making a concentrated heat flux, as depicted in Fig. [3.](#page-3-0) As a result, in the central area of the baseplate the temperature rises steadily and in the edge area the temperature drops, intensifying the nonuniformity of the case temperature distribution on the baseplate. This indicates that the variation in the nonuniformity of temperature distribution on the baseplate is sensitive to the solder aging level. Therefore, the solder fatigue can be detected by monitoring this variation.

The nonuniformity of the temperature distribution can be characterized by the temperature gradient. The temperatures in two positions that are sensitive to the solder fatigue are selected to calculate the gradient as shown in Fig. [3.](#page-3-0) The first is *TC*−*chip* and it is sensitive to the concentrated heat flow. The second is *TC*−*side* and it is sensitive to the cracks in the edge of the solder layer. Thus, the value of temperature gradient  $\nabla T$  can be defined as follows:

$$
\nabla T = \frac{T_{C-chip} - T_{C-side}}{d},\tag{3}
$$

where *d* denotes the distance between the two points.

The value of  $\nabla T$  can characterize the impact of solder fatigue on the nonuniformity of the case temperature distribution. With the aging of solder layer, *TC*−*chip* rises due to the concentration of the heat flow and *TC*−*side* drops for its position beyond the main heat transfer paths. Considering other heat sources, not very close to the baseplate, their influences on  $T_{C-chip}$  and  $T_{C-side}$  cancel out in  $\nabla T$ . Thus,  $\nabla T$  increases monotonically through solder aging and it is a good sign of the aging levels. Additionally, the parameter should be normalized under the scale of power loss in corresponding operating condition. And the expression of  $\nabla T$  can be modified into  $\nabla T_{(P)}$  that can be expressed as follows:

<span id="page-3-1"></span>
$$
\nabla T_{(P)} = \frac{T_{C-chip} - T_{C-side}}{P \cdot d},\tag{4}
$$

where *P* denotes the power loss of the IGBT module.

Compared with the methods presented in [21], [22], the parameter  $\nabla T_{(P)}$  in ([\(4\)](#page-3-1)) only depends on the case temperature of IGBT. And the influences from other heat sources are naturally eliminated. This parameter can be used under different operating conditions with other heat sources, and easily measured by a pair of thermal sensors between the baseplate and heatsink. So this method is accurate, economic and easy to implement.

### **IV. MONITORING OF MIXED AGING**

When an IGBT module undergoes multiple aging processes, both the values of  $\Delta T$  and  $\nabla T_{(P)}$  may change over time. The aging level of bond wires has no effect on the heat conduction inside the IGBT module and therefore has no effect on the temperature distribution of the baseplate; thus, the solder fatigue can still be monitored by  $\nabla T_{(P)}$ . However, the solder fatigue can affect the estimation of bond wire aging. The thermal impedance  $Z_{jc}$  in the Foster model rises because of the cracks in solder fatigue, which further causes an underestimate of  $T_{j (model)}$ . Thus, the value of  $\Delta T$  in ([\(2\)](#page-2-2)) is increased because of the solder fatigue, not the bond wire aging. Thus, the effect of solder fatigue on  $\Delta T$  needs to be removed to accurately evaluate the aging level of bond wires.



<span id="page-3-2"></span>**FIGURE 4.** Foster thermal model.

The parameters of the Foster model consist of the thermal resistance  $R_i$  and thermal capacitance  $C_i$ , as shown in Fig. [4.](#page-3-2) To improve the accuracy of  $T_i$  estimate, the parameters should be updated and corrected. The correction method of the Foster model, based on the linear thermal behavior in IGBTs, has been described in detail in [26], [27]. Compared with  $R_i$ , the impact of solder fatigue on  $C_i$  is negligible and can be ignored. The thermal resistance  $R_i$  can be

corrected as follows:

<span id="page-4-0"></span>
$$
R_{i(aged)} = R_i(1 + \frac{Z_{jc(aged)} - Z_{jc}}{\sum_{i=1}^{n} R_i}),
$$
\n(5)

where  $R_{i(aged)}$  denotes the aged thermal resistance due to solder fatigue, and *Zjc*(*aged*) denotes the aged thermal impedance.

In equation [\(5\)](#page-4-0), all the variables except  $Z_{ic(aged)}$  are known. Thus, the correction of the parameter  $R_{i(aged)}$  only depends on the value of  $Z_{jc(aged)}$ . Since  $\nabla T_{(P)}$  in [\(4\)](#page-3-1) only changes with the solder aging process and is independent of the operating conditions of the IGBT module, the relationships between  $\nabla T_{(P)}$ and *Zjc*(*aged*) can be easily characterized. For example, such relationships can be obtained by recording the evolutions of  $\nabla T_{(P)}$  and  $Z_{jc(aged)}$  in a look-up table under offline solder aging tests in certain operating conditions. Then, according to  $\nabla T_{(P)}$ , the values of  $Z_{jc(aged)}$  can be obtained immediately in various operating conditions of the IGBT module, even if a mixed aging occurs.

By using [\(5\)](#page-4-0), the parameters of the Foster model are adapted to the solder fatigue, and the real value of  $T_i$  can be obtained from the corrected Foster model as *Tj*(*model*) . Thus, the influence of solder fatigue on  $\Delta T$  is removed. The remaining temperature difference  $\Delta T$  is attributed to the bond wire fatigue. Then the aging condition of bond wires can be evaluated by the method presented in Section II-B.

#### **V. IMPLEMENTATION OF THE PROPOSED METHOD**

The implementation of the proposed CM method consists of the following three blocks: a bond wire aging block, a solder aging block and a mixed aging block. The bond wire aging block is used to monitor the aging condition of bond wires using the parameter  $\Delta T$ . During the normal operation of the IGBT module, by measuring  $V_{CE-ON}$  and  $I_C$ ,  $T_{i(V_{CF})}$  can be easily obtained from the look-up table of  $T_j(\gamma_{CE})$ - $V_{CE-ON}$ - $I_C$ , which describes the relationship between  $T_{j(V_{CF})}$  and  $V_{CE-ON}$ under various collector currents. Meanwhile, the updating *Tj*(*model*) is obtained from the mixed aging block. By substituting the results of  $T_j(V_{CE})$  and  $T_j \neq (2)$  $T_j \neq (2)$ , the value of  $\Delta T$  is acquired and used to evaluate the aging condition of bond wires.

The solder aging block is used to detect the aging condition of solder. It can be easily implemented through continuous measurement the case temperature distribution by placing two thermal sensors on the bottom surface of the baseplate, as shown in Fig. [5.](#page-4-1) The original state of IGBT solder is characterized by the initial value of  $\nabla T_{(P)}$ . Through the solder aging process,  $\nabla T_{(P)}$  is updated by [\(4\)](#page-3-1) and compared with its initial value continuously. Then the aging level of IGBT solder can be quantified by he changes in  $\nabla T_{(P)}$ . Furthermore,  $\nabla T_{(P)}$  is provided to the mixed aging block to update the Foster model.

Considering the multiple aging processes in IGBT, the mixed aging block is used to prevent the effect on bond wire aging estimation caused by solder fatigue, correct the parameters in the Foster model, estimate  $T_{j (model)}$  as the accurate  $T_j$ , and guarantee the monitoring accuracy of bond



<span id="page-4-1"></span>**FIGURE 5.** Thermal sensors on the bottom surface of the baseplate.



<span id="page-4-2"></span>**FIGURE 6.** Flowchart of the proposed method.

wire aging. With  $\nabla T_{(P)}$  obtained from the solder aging block,  $Z_{jc(aged)}$  can be obtained and the parameter  $R_{i(aged)}$  in the Foster model can be corrected using [\(5\)](#page-4-0). The correction may be conducted several times to minimize the measurement uncertainty. Then, *Tj*(*model*) is calculated using the updated Foster model with the measured case temperature and estimated power loss. Thus, the accuracy of  $T_{j (model)}$  estimated by the Foster model is improved. Therefore, the influence of solder fatigue on  $\Delta T$  has been removed, and the bond wire aging can be accurately evaluated using  $\Delta T$ . The entire flowchart of the proposed CM method is presented in Fig. [6.](#page-4-2)

## **VI. EXPERIMENTAL VALIDATION**

The effectiveness of the condition monitoring method was comfirmed through an experimental study. The schematic of the experimental setup is illustrated in Fig. [7.](#page-5-0) The actual instruments, displayed as Fig. [8,](#page-5-1) include a commercial IGBT module (SKM300GB128D) made by SEMIKRON (the silica gel on the upper surface was intentionally removed), an infrared (IR) camera to obtain the upper surface temperature of the module, a recorder with an sampling circuit to obtain *VCE*−*ON* , a signal generator with its peripheral circuits



<span id="page-5-0"></span>**FIGURE 7.** Schematic of the experimental setup.



**FIGURE 8.** Actual experimental setup.

<span id="page-5-1"></span>to drive the IGBT module, a DC power supplier, an aluminum heatsink to cool the module down, and a National Instruments (NI) data acquisition instrument to obtain the case temperatures using precise fine wire thermocouples.

The experimental design was implemented as follows to remove the effects of disturbances in various operating conditions: (1) the IGBT module was cooled by a forced-air system; (2) an independent gate driver maintained the IGBT in the operation state; and (3) the test time was 20 min to ensure that the temperature inside the module can reach a steady state. The feasibility of the CM method proposed previously for bond wire aging and solder fatigue was confirmed.

## A. CONDITION MONITORING OF BOND WIRE AGING

In this section, the effectiveness of the CM method for bond wire aging is validated. The proposed method is based on the temperature difference  $\triangle T$ , which comes from the temperatures estimated through the Foster model and *V<sub>CE</sub>*−*ON*. The Foster model is an equivalent circuit model, and its parameters are fitted based on the transient thermal impedance  $Z_{jc}(t)$ , which can be easily acquired by finite element analysis (FEA). According to the work in [24], [25], the parameters of the Foster model were obtained, as listed in TABLE [1.](#page-5-2)

For the junction temperature estimated from *VCE*−*ON* , a preliminary calibration is necessary and the goal is to obtain the dependence of the temperature on *VCE*−*ON* for an IGBT

#### **TABLE 1.** Parameters of the Foster Model.

<span id="page-5-2"></span>



<span id="page-5-3"></span>**FIGURE 9.** Look-up table used to obtain  $T_i$  based on the measured V<sub>CE−ON</sub> and I<sub>C</sub>.



<span id="page-5-4"></span>**FIGURE 10.** Comparison of  $T_i$  obtained from the Foster model and  $V_{CE-ON}$ .

under given operating current conditions. The calibration process was introduced in [28] so the specific procedure is not presented in this paper. After the calibration, the relationship between  $T_j(V_{CE})$  and  $V_{CE-ON}$  under various currents can be found in a look-up table based on the work in [28], as presented in Fig. [9.](#page-5-3)

The performance of  $\Delta T$  in a healthy IGBT module under various operating conditions is displayed. A DC current that varied between 5A and 30A with an interval of 5 min flowed through the IGBT module, and the junction temperature  $T_j$ estimated from the Foster model and *VCE*−*ON* was obtained, as shown in Fig. [10.](#page-5-4) It can be seen that the estimate of  $T_i$ from the Foster model accurately tracks that from *VCE*−*ON* in both the heating and cooling regimes. This suggests that the values of  $T_j(V_{CE})$  and  $T_j_{model}$  are consistent. So when the IGBT module is healthy without bond wire aging, the values of  $\Delta T$  are independent of various operating conditions and always zero.

The effectiveness of  $\Delta T$  in monitoring the aging process of bond wires is validated. In order to compare and verify the experimental results conveniently, shearing off bond wires was adopted to simulate the bond wire fatigue. One intact IGBT module and three degraded ones were under test with different value of bond wire defects. One to three bond wires were sheared off in the three degraded IGBT modules. As analyzed in Section II-B, the parameter  $\triangle T$  depends only on the aging condition of bond wires and is not influenced by the operating conditions; therefore, the four IGBT modules were tested under different collector currents to prove the previous theoretical analysis.



<span id="page-6-0"></span>**FIGURE 11.** Evolution of  $\Delta T$  with the aging process of bond wires.

An intact IGBT module and three degraded IGBT modules were tested under various operating conditions by setting the working current to 20, 30, 40, and 50 A. The values of *VCE*−*ON* under different currents were measured, and the corresponding  $T_{j(V_{CE})}$  values were obtained from the look-up table. Additionally, the junction temperatures  $T_{j (model)}$  were also obtained by using the Foster model. By substituting the test results into [\(2\)](#page-2-2), the values of the four IGBT modules'  $\triangle T$ were acquired, as presented in Fig. [11.](#page-6-0) Then two facts can be found. Firstly,  $\Delta T$  rises with increasing number of lifted bond wires *n*. The values of  $\Delta T$  increased from 0 °C to 40 °C when the lifted bond wire number increased from 0 to 3. Secondly,  $\Delta T$  of one given IGBT module remains constant under different test currents. For example, in the IGBT module with two bond wires lifted off,  $\Delta T$  remained approximately 10 °C. This demonstrates that  $\Delta T$  only depends on the bond wire aging, while it is independent of the operating current condition. Therefore,  $\Delta T$  can be used to evaluate the aging state of bond wires under the normal operation of the IGBT module.

## B. CONDITION MONITORING OF SOLDER FATIGUE

The availability of  $\nabla T_{(P)}$  as an indicator of solder fatigue is validated in this section. The accelerated power cycling test for IGBT modules is complex and time consuming [28], [29], the state of cracks in the IGBT module solder was simulated by a hollow thermal pad between the baseplate and the heatsink [22], as shown in Fig. [12.](#page-6-1)



**FIGURE 12.** IGBT module test.

<span id="page-6-1"></span>

<span id="page-6-2"></span>**FIGURE 13.** Performance of  $\nabla T_{(P)}$  under various operating conditions.

The solid part of the pad represented the cracks in solder and the hollow part was full of thermal grease to represent the uncracked area in solder. The size of the void was set according to the studied extent of solder aging. Thus, the conditions of solder aging can be represented by the following four aging scenarios: 1) healthy condition without solder fatigue; 2) low level aging substrate solder with 20% area cracked; 3) medium level aging substrate solder with 40% area cracked; and 4) high level aging substrate solder with 60% area cracked. An intact IGBT module can be set to any scenario with a configurable thermal pad aforementioned.

Firstly, the experimental values of  $\nabla T_{(P)}$  under various operating conditions is shown. Four working currents from 20 A to 50 A with a step of 10 A were generated to flow through a healthy IGBT module. The two case temperatures *TC*−*chip* and *TC*−*side*, the reference of junction temperature *T<sup>j</sup>* from the IR camera and the value of *VCE*−*ON* were recorded under these operation conditions. The corresponding power losses of the IGBT module under these can be calculated according to the work in [22], [23]. With the case temperatures and the power losses,  $\nabla T_{(P)}$  were calculated using [\(2\)](#page-2-2). As presented in Fig. [13,](#page-6-2) it can be seen that  $\nabla T_{(P)}$ is almost constant versus the collector current, demonstrating that  $\nabla T_{(P)}$  is independent of the working conditions.

Secondly, to show the variation of  $\nabla T_{(P)}$  during the development of IGBT solder aging, a DC current of 30 A flowed through the IGBT modules in the four scenarios mentioned above, respectively. And the parameter of *TC*−*chip*, *TC*−*side* and  $T_i$  were measured and is listed in TABLE [2.](#page-7-0)

**TABLE 2.** Temperatures measured under various solder aging conditions.

<span id="page-7-0"></span>

<span id="page-7-1"></span>**FIGURE 14.** Evolution of  $\nabla T_{(P)}$  with the solder aging process.

From scenario 1 to 4, *TC*−*chip* increases while *TC*−*side* decreases. The difference that *TC*−*chip* minus *TC*−*side* increases from 11.3  $\degree$ C in scenario 1 to 16  $\degree$ C in scenario 4, more than 41%. Considering the constant operating condition, the 30A DC current, the only cause must be the heat flow confined and concentrated by the solder aging cracks inside the module. Substituting these values of *TC*−*chip*, *TC*−*side* and the power losses into [\(2\)](#page-2-2), the values of  $\nabla T_{(P)}$  versus the four scenarios were obtained, as shown in Fig. [14.](#page-7-1)

It is evident that with the expansion of cracks (solid area of the thermal pad) from none to 60% area of the solder,  $\nabla T_{(P)}$  increases monotonically from 8.7 to 12.3, nearly 41%. The value of  $\nabla T_{(P)}$  is sensitive to the area of solder cracks but insensitive to the variation of operating currents. Thus,  $\nabla T_{(P)}$  can be used to estimate the extent of solder layer aging by characterizing the change in the nonuniformity of the case temperature distribution.

### C. CONDITION MONITORING OF MIXED AGING

In this section, the feasibility of the proposed method in monitoring the mixed aging in the IGBT module is illustrated. Understandably, the bond wire aging makes no difference to the heat transfer routes, i.e., to the temperature distribution on the baseplate. The solder fatigue can be monitored by  $\nabla T_{(P)}$ without considering the bond wire aging. However, the cracks caused by the solder fatigue are equivalent to an increase of  $Z_{jc}$  in [\(5\)](#page-4-0). It causes a misestimate of  $T_j$  through the use of the Foster model with the parameter  $Z_{ic}$ . As a result, in the mixed aging conditions,  $\Delta T$  calculated from [\(2\)](#page-2-2) is susceptible to both the aging of bond wires, which affects  $T_{j(V_{CE})}$ , and the solder fatigue, which affects  $T_{j (model)}$ . Before  $\Delta T$  is merely used to monitor the bond wires aging, the influence of solder fatigue must be removed. Therefore, the parameters in Foster



<span id="page-7-2"></span>**FIGURE 15.** Comparison of  $T_j$  obtained from the Foster model and IR camera.

TABLE 3. Relationships between  $\triangledown T_{(P)}$  and  $Z_{jc (aged)}$ .

<span id="page-7-3"></span>

Scenarios			$\overline{\phantom{a}}$	
$\mathrm{C/m}$ W ٠		9.0J		
$\circ$ . $\langle aged \rangle$	0.085		9.115	

**TABLE 4.** Parameters of the improved Foster model.

<span id="page-7-4"></span>

model should be updated, and through which the accuracy of estimated  $T_i$  can be improved.

The main work in this section is to correct the parameters of the Foster model to adapt them to the solder aging condition. First, the values of the junction temperature  $T_i$  estimated from the original Foster model and measured by the IR camera are compared to display how the solder aging affect the estimation by the Foster model. A DC current flowed through a continuously switching IGBT module in scenario 4 described in Section VI-B. The current rose to 30 A. After the temperature  $T_i$  was stable the current dropped to 0 A. When  $T_i$  was stable again, a cycle was completed. The swings of the temperature  $T_i$  during 4 cycles, obtained by the Foster model and the IR camera, are shown in Fig. [15.](#page-7-2)

The differences between the two curves are greater than 4 ◦C most of the time, and the maximum reaches 11 ◦C. Obviously, these differences can make  $T_{j (model)}$  in [\(2\)](#page-2-2) much lower than the real *T<sup>j</sup>* . If these lower *Tj*(*model*) are substituted into [\(2\)](#page-2-2),  $\nabla T_{(P)}$  must be overestimated and the errors of  $T_i$ estimate, meaning solder fatigue, will go into the estimation of the bond wires aging. Therefore, the original parameters in the Foster model should be updated with the solder aging process to improve the accuracy of estimated *T<sup>j</sup>* .

As described in Section IV, the correction of the parameters in the Foster model depends on the value of *Zjc*(*aged*) , which was obtained from the look-up table of  $\nabla T_{(P)}$  versus  $Z_{jc(aged)}$ . According to the experimental results in Section VI-B, four couples of corresponding  $\nabla T_{(P)}$  and  $Z_{jc(aged)}$  are listed in TABLE [3.](#page-7-3) By substituting  $Z_{jc(aged)}$  into [\(5\)](#page-4-0), the parameter  $R_{i(aged)}$  was corrected, and the updated Foster model was obtained, as shown in TABLE [4.](#page-7-4)



<span id="page-8-0"></span>**FIGURE 16.** Comparison of  $T_i$  obtained from the improved Foster model and IR camera.

Under the aforementioned experimental conditions, the junction temperatures  $T_i$  estimated from the updated Foster model and measured from the IR camera are compared in Fig. [16.](#page-8-0) It can be seen that  $T_{j (model)}$  tracks the measured  $T_j$ accurately, with a maximum error of 1.8 %. The error between the  $T_i$  estimate and the IR camera measurement is approximately 1.2 ◦C throughout the process. The error can be attributed to several factors. Firstly, the IR camera measurement represents the upper surface temperature of the IGBT, whereas  $T_i$  obtained from the thermal model represents the temperature of the intrinsic body region inside the IGBT. Secondly, the bond wires on the top of the chip hinder the IR camera in measuring the maximum temperature through the shading effect. Therefore, the estimated temperature is lower than the measured temperature. As a result,  $T_{j (model)}$  can be treated as the real junction temperature *T<sup>j</sup>* .

These analyses demonstrate that the updated Foster model is competent in estimating  $T_i$  accurately. Thus, the influence of solder fatigue on  $\triangle T$  can be removed. So the temperature difference  $\Delta T$  in [\(2\)](#page-2-2) is only attributed to the bond wires aging and can be used to evaluate that. The accuracy of bond wire aging monitoring is guaranteed by the solder fatigue monitoring and the mixed aging monitoring.

#### **VII. CONCLUSION**

A new CM strategy was proposed in this paper to evaluate the IGBT module aging state. The two types of aging, bond wires aging and solder fatigue, and their effects on two kinds of junction temperature estimation under different operating conditions are entirely considered. In this method, the solder fatigue, which has negative effect on the accuracy of the temperature estimate from the electrical-thermal model, can be monitored by detecting the change in the temperature gradient on the IGBT baseplate. The effect can be directly removed. Then the junction temperature can be estimated accurately through updated electrical-thermal model. The bond wire aging can be indicated by the difference between junction temperatures estimated from the continuously updated electrical-thermal model and temperaturesensitive electrical parameter (TSEP). The effectiveness of this method is validated by the experimental results. Using this method, the more comprehensive state of health of the

IGBT module can be evaluated, and the module can be replaced in time before catastrophic failures occur. This study will aid in the development of CM methods and improve the reliability of the power converters in the future.

#### **REFERENCES**

- [1] B. Ji, V. Pickert, W. Cao, and B. Zahawi, ''*In situ* diagnostics and prognostics of wire bonding faults in IGBT modules for electric vehicle drives,'' *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5568–5577, Dec. 2013.
- [2] Z. Xu, M. Li, F. Wang, and Z. Liang, ''Investigation of Si IGBT operation at 200 ◦C for traction applications,'' *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2604–2615, May 2013.
- [3] X. M. Xu, R. Z. Li, J. Q. Fu, and H. B. Jiang, ''Research on the heat flow field synergy of electric vehicle power cabin at different charge and discharge rates,'' *Appl. Therm. Eng.*, vol. 117, pp. 397–408, May 2017.
- [4] W. Cao, B. C. Mecrow, G. J. Atkinson, J. W. Bennett, and D. J. Atkinson, ''Overview of electric motor technologies used for more electric aircraft (MEA),'' *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3523–3531, Sep. 2012.
- [5] O. S. Senturk, L. Helle, S. Munk-Nielsen, P. Rodriguez, and R. Teodorescu, ''Power capability investigation based on electrothermal models of presspack IGBT three-level NPC and ANPC VSCS for multimegawatt wind turbines,'' *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3195–3206, Jul. 2012.
- [6] X. Gong and J. A. Ferreira, ''Comparison and reduction of conducted EMI in SiC JFET and Si IGBT-based motor drives,'' *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1757–1767, Apr. 2014.
- [7] L. Ngwendson, M. R. Sweet, and E. M. S. Narayanan, ''An overview of the recent developments in high-voltage power semiconductor MOS-controlled bipolar devices,'' in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting*, Oct. 2009, pp. 198–205.
- [8] A. Morozumi, K. Yamada, T. Miyasaka, S. Sumi, and Y. Seki, ''Reliability of power cycling for IGBT power semiconductor modules,'' *IEEE Trans. Ind. Appl.*, vol. 39, no. 3, pp. 665–671, May/Jun. 2003.
- [9] S. Igarashi, H. Kakiki, Y. Nishimura, and T. Goto, ''Design of high reliability packaging for Fuji high power module,'' in *Proc. Int. Conf. Elect. Mach. Syst.*, Aug. 2011, pp. 1–6.
- [10] U. Scheuermann, "Reliability challenges of automotive power electronics,'' *Microelectron. Rel.*, vol. 49, nos. 9–11, pp. 1319–1325, Sep./Nov. 2009.
- [11] D. A. Murdock, J. E. R. Torres, J. J. Connors, and R. D. Lorenz, "Active thermal control of power electronic modules,'' *IEEE Trans. Ind. Appl.*, vol. 42, no. 2, pp. 552–558, Mar./Apr. 2006.
- [12] X. Wang, A. Castellazzi, and P. Zanchetta, "Observer based temperature control for reduced thermal cycling in power electronic cooling,'' *Appl. Therm. Eng.*, vol. 64, nos. 1–2, pp. 10–18, Mar. 2014.
- [13] M. S. Haque, S. Choi, and J. Baek, "Auxiliary particle filtering-based estimation of remaining useful life of IGBT,'' *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2693–2703, Mar. 2018.
- [14] A. Singh, A. Anurag, and S. Anand, ''Evaluation of VCE at inflection point for monitoring bond wire degradation in discrete packaged IGBTS,'' *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2481–2484, Apr. 2017.
- [15] M. A. Eleffendi and C. M. Johnson, "In-service diagnostics for wire-bond lift-off and solder fatigue of power semiconductor packages,'' *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 7187–7198, Sep. 2017.
- [16] D. W. Brown, M. Abbas, A. Ginart, I. N. Ali, P. W. Kalgren, and G. Vachtsevanos, ''Turn-off time as an early indicator of insulated gate bipolar transistor latch-up,'' *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 479–489, Feb. 2012.
- [17] D. Brown, M. Abbas, A. Ginart, I. Ali, P. Kalgren, and G. Vachtsevanos, ''Turn-off time as a precursor for gate bipolar transistor latch-up faults in electric motor drives,'' in *Proc. Annu. Conf. Prognostics Health Manage. Soc.*, 2010, pp. 10–16.
- [18] L. Dupont and Y. Avenas, ''Preliminary evaluation of thermo-sensitive electrical parameters based on the forward voltage for online chip temperature measurements of IGBT devices,'' *IEEE Trans. Ind. Appl.*, vol. 51, no. 6, pp. 4688–4698, Nov./Dec. 2015.
- [19] N. Patil, J. Celaya, D. Das, K. Goebel, and M. Pecht, "Precursor parameter identification for insulated gate bipolar transistor (IGBT) prognostics,'' *IEEE Trans. Rel.*, vol. 58, no. 2, pp. 271–276, Jun. 2009.
- [20] V. Smet, F. Forest, J.-J. Huselstein, A. Rashed, and F. Richardeau, "Evaluation of V*ce* monitoring as a real-time method to estimate aging of bond wire-IGBT modules stressed by power cycling.,'' *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2760–2770, Jul. 2013.
- [21] Z. Wang, B. Tian, W. Qiao, and L. Qu, "Real-time aging monitoring for IGBT modules using case temperature,'' *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 1168–1178, Feb. 2016.
- [22] D. Xiang, L. Ran, P. Tavner, A. Bryant, S. Yang, and P. Mawby, "Monitoring solder fatigue in a power module using case-above-ambient temperature rise,'' *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2578–2591, Nov./Dec. 2011.
- [23] U.-M. Choi, F. Blaabjerg, S. Jørgensen, S. Munk-Nielsen, and B. Rannestad, ''Reliability improvement of power converters by means of condition monitoring of IGBT modules,'' *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7990–7997, Oct. 2017.
- [24] A. S. Bahman, K. Ma, and F. Blaabjerg, ''A lumped thermal model including thermal coupling and thermal boundary conditions for highpower IGBT modules,'' *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2518–2530, Mar. 2018.
- [25] J. Reichl, J. M. Ortiz-Rodríguez, A. Hefner, and J.-S. Lai, ''3-D thermal component model for electrothermal analysis of multichip power modules with experimental validation,'' *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3300–3308, Jun. 2015.
- [26] H. Chen, B. Ji, V. Pickert, and W. Cao, "Real-time temperature estimation for power MOSFETs considering thermal aging effects,'' *IEEE Trans. Device Mater. Rel.*, vol. 14, no. 1, pp. 220–228, Mar. 2014.
- [27] Z. Hu, M. Du, K. Wei, and W. G. Hurley, "An adaptive thermal equivalent circuit model for estimating the junction temperature of IGBTS,'' *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 392–403, Mar. 2019.
- [28] U.-M. Choi, S. Jørgensen, and F. Blaabjerg, "Advanced accelerated power cycling test forreliability investigation of power device modules,'' *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8371–8386, Dec. 2016.
- [29] D. Astigarraga et al., "Analysis of the results of accelerated aging tests in insulated gate bipolar transistors,'' *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7953–7962, Nov. 2016.



KEXIN WEI received the M.S. degree in automation engineering from Tianjin University, Tianjin, China, in 1988.

He was a Visiting Scholar with the Delft University of Technology, Delft, The Netherlands, and Texas A&M University, College Station, USA, in 1994 and 2000, respectively. He was the Head of the Tianjin Key Laboratory of Control Theory and Applications in Complicated Systems. He is currently a Professor with the School of Electrical

and Electronic Engineering, Tianjin University of Technology, Tianjin, and a part-time Professor with the School of Electrical and Information Engineering, Tianjin University. His research interests include power electronics and control, high power converters, and electromagnetic compatibility in power electronics systems.



WENBAI WANG received the M.S. degree in electrical engineering from the North China University of Technology, Beijing, China, in 2013. He is currently pursuing the Ph.D. degree in automation engineering with the School of Electrical and Information Engineering, Tianjin University.

His research interests include advanced control strategy for inverter-fed electric motors such as PMSM and IM, optimized PWM methods for power semiconductors, and condition monitoring in power drive systems.



ZHEN HU received the M.S. degree in electrical engineering from the Tianjin University of Technology, Tianjin, China, in 2014. He is currently pursuing the Ph.D. degree in automation engineering with the School of Electrical and Information Engineering, Tianjin University.

He is currently a Lecturer with the College of Automation and College of Artificial Intelligence, Nanjing University of Posts and Telecommunications, Nanjing, China. His main research interests

include condition monitoring for power electronics, power semiconductor module thermal modeling, and electromagnetic compatibility in power electronics systems.



MINGXING DU received the Ph.D. degree in automation engineering from Tianjin University, Tianjin, China, in 2012.

He is currently an Associate Professor with the School of Electrical and Electronic Engineering, Tianjin University of Technology, Tianjin. His current research interests include condition monitoring for power electronics, power semiconductor module thermal modeling, and electromagnetic compatibility in power electronics systems.

 $\sim$   $\sim$   $\sim$