IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received January 11, 2019, accepted January 27, 2019, date of publication April 4, 2019, date of current version April 13, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2902979

A Simple, Efficient, and Novel Standalone Photovoltaic Inverter Configuration With Reduced Harmonic Distortion

MURALIDHAR NAYAK BHUKYA[1], (Member, IEEE), VENKATA REDDY KOTA[2], (Senior Member, IEEE), AND SHOBHA RANI DEPURU[1], (Member, IEEE)

[1]Department of Electrical and Electronics Engineering, Institute of Aeronautical Engineering, Hyderabad 500 043, India
[2]Department of Electrical and Electronics Engineering, University College of Engineering, Kakinada 533 001, India

Corresponding author: Muralidhar Nayak Bhukya (rathode.muralidhar@gmail.com)

ABSTRACT This paper is put forward a novel photovoltaic (PV) inverter topology for maximum solar power utilization, which incorporates a new maximum power point tracking (MPPT) scheme based on shading pattern identification using the artificial neural network, single-input and multi-output (SIMO) converter, and multilevel inverter (MLI). The performance of the proposed MPPT scheme is benchmarked under partially shaded conditions. In continuation, the PV voltage is fed to the SIMO converter, where the converter produces four independent (V_1, V_2, V_3 and V_4) voltages with different magnitudes. The MLI converts the dc output voltage of the SIMO converter into ac to feed the utility, with reduced harmonic distortion. This MLI consists of eight switching devices and produces thirty one level ac output voltage with very less harmonic distortion. The salient feature associated with the proposed topology is that the proposed MPPT scheme extracts utmost power in any weather conditions and MLI feeds the utility. An experimental prototype is designed and developed to verify the performance of the proposed PV inverter topology. FPGA Spartan trainer kit is used to program pulses required for the MLI and converter of the proposed topology.

INDEX TERMS Maximum power point tracking, photovoltaic inverter, single input and multi output converter, Spartan trainer kit.

I. INTRODUCTION

Nowadays, electric power generation through PV systems has emerged as an alternative to conventional power generating systems due to simple maintenance, eco-friendly nature, low noise and abundant availability. Extracting maximum power and inverting the output power of the PV system into useful ac to feed the utility are the tedious task associated with solar power generation. In order to extract maximum solar power, Maximum Power Point (MPP) of the PV system has to be tracked continuously using a Maximum Power Point Tracking (MPPT) controller [1]. In recent times, miniature range installation of solar power generating units on building rooftops is trending and also offers as an alternative primary source of energy for household purposes during emergence [2], [3].

The associate editor coordinating the review of this manuscript and approving it for publication was Shravana Musunuri.

In [4], presented the two Perturb and Observe (P&O) implementation technique based on the parameters like voltage and duty ratio and both the algorithm are applied to the solar pumping system. During dynamic weather conditions, voltage based algorithm performance is affected due to low pass filter noise at the same time duty ratio based P&O algorithm fails to track power path perfectly. A hybrid P&O scheme is presented in [5], still the response time of the scheme affects the performance. In [6], the performance of the traditional P&O is enhanced by improving a free running loop using Particle Swarm Optimization (PSO). Due to the involvement of metaheuristic algorithms, the proposed scheme is not suggested for low cost applications. During the change in irradiance there exists drift in the power curve, in order to eliminate the drift a new resolution is introduced into the system based on the panel current [7]. Due to excess feedback, the controller takes much time to decide MPP during regular conditions [8].

To feed the utility grid DC power generated from the PV array has to be inverted into AC power. Generally, the conversion circuit includes a dc-dc power converter and Multi-Level Inverter (MLI) [9]. To avoid voltage mismatch between PV source and DC voltage bus a dc-dc converter is incorporated such that low-level PV voltage is boosted up to the voltage level of DC bus. In continuation the boosted DC solar power is converted into AC power using inverters [10]. To reduce wastage of power, PV array and power conversion circuit efficiency should be high. From the past few years, many researchers have designed MLI with increased voltage levels having better conversion efficiency with reduced harmonic content and minimum interface to electromagnetic interface [11], [12]. Traditional MLI configurations such as diode-clamped and flying capacitors topologies generate several voltage levels using capacitor circuits. The major problems associated with these two configurations are it is not possible to regulate the voltage across the capacitors. Moreover, conversion efficiency decreases as the voltage level is increased. Cascade H-bridge is much suitable to develop several voltage levels by employing asymmetric voltage technology, but these converters require more switching devices.

In [13], experimentally implemented a novel topology to minimize DC offset voltage during unbalance and fault tolerant conditions. As the rating of the topology increases, it is difficult to control voltage across the capacitor. Hence, this topology is limited for off-grid applications. During low irradiance level, PV system produces the low voltage. To improve the efficiency of inverter during low voltage He and Cheng [14] developed a new multilevel inverter based on bridge modular switched capacitor. The configuration involves the number of switching devices and practical implementation of the control circuit is complex [15], [16]. Agrawal and Jain [17] presented a new MLI from the existing cross-connected source based inverter with a reduced number of switches by developing a simple control circuit to integrate low/medium/high voltages extracted from renewable energy sources to the grid. Under dynamic weather conditions, the proposed topology has poor performance.

The above limitations associated with the existing scheme gives scope for the development of a novel PV inverter topology.

II. PROPOSED PV INVERTRE TOPOLOGY

In order to generate thirty-one levels in the output voltage of the conventional cascaded H-bridge [18] MLI, it requires fifteen independent voltage sources and sixty power electronic switches. Lee *et al.* [19] presented modified H-bridge MLI with same thirty-one levels in the output voltage. Still the modified configuration requires four dc voltage sources and sixteen electronic switches. In view of the above limitations this paper presents a novel PV inverter topology for maximum solar power utilization, which consists of PV system, dc-dc Single Input and Multi Output power converter and a simple thirty-one level inverter with the reduced number of switches as shown in Fig. 1. The PV system is employed with a

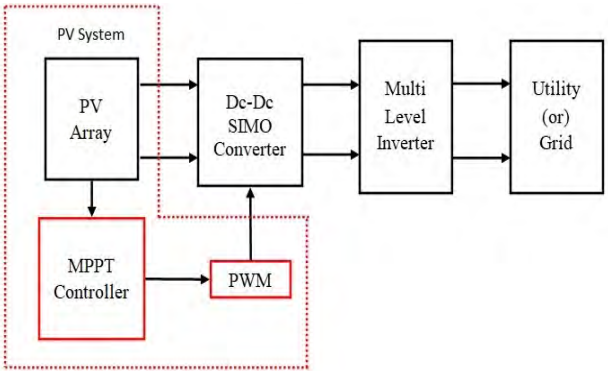


FIGURE 1. Schematic diagram of the proposed topology.

novel MPPT controller based on shading pattern identification using artificial neural network to harvest maximum available solar power from RNG 200D 200Watt PV panel in any weather condition. The dc-dc Single Input and Multi Output (SIMO) power converter incorporate a step-up converter with a transformer. The SIMO converter provides four independent output voltages V_1, V_2, V_3 and V_4 with different magnitudes. Finally, it is worth to mention that the thirty-one level inverter generates a sinusoidal waveform that is in phase with the utility grid using the four independent output voltages of the SIMO converter with unity power factor [20].

III. PROPOSED MPPT SCHEME

Conventional MPPT schemes fail to accomplish Global Maximum Power Point (GMPP) of the PV system during Partial Shaded Conditions (PSC) at the same time metaheuristic algorithms developed to track GMPP are complex, costly and require much time to track GMPP. Therefore, it is significant to develop a new optimizing algorithm for GMPP tracking under PSC, which has better accuracy, improved convergence time, simple to implement and moreover economical [21].

A. MATHEMATICAL MODELLING OF PV SYSTEM

Due to obstacles such as passing clouds, shadows of buildings, dust deposit on panels and bird's waste it is not possible to receive uniform irradiance all over the system. Hence, effective irradiance (G_E) on each PV module varies and it can be given as

$$G_E = (1 - S)G \tag{1}$$

where G is irradiance on un-shaded areas, S is the shading ratio of the panel. Shading ratio is defined as the ratio of shaded area on the module to total area of the module. Output current of the PV module is given as

$$I = I_{Ph} - I_D \left[\exp\left(\frac{q\,(V_{PV} + I_{PV} R_S)}{N_S A B_K T} \right) - 1 \right] - \frac{V_{PV} + I_{PV} R_S N_S}{N_S R_{Sh}} \tag{2}$$

where I_{Ph} is photo generated current (A), I_D is diode saturation current (A), V_{PV} is panel voltage (V), I_{PV} is panel

current (A), R_S is series resistance (Ω), N_S is number of PV cell connected in series, A is diode ideality factor, B_K is Boltzmann constant, T is temperature on the panel (°C) and R_{Sh} is parallel resistance (Ω).

Photo generated current with shaded and un-shaded cells can be written individually as

$$\left.\begin{aligned} I_{Ph(G_1)} &= \left(I_{SC,Ref} + K_{ISC}\left(T - T_{Ref}\right)\right)\frac{G_1}{G_{Ref}} \\ I_{Ph(G_2)} &= \left(I_{SC,Ref} + K_{ISC}\left(T - T_{Ref}\right)\right)\frac{G_2}{G_{Ref}} \\ I_{Ph(G_3)} &= \left(I_{SC,Ref} + K_{ISC}\left(T - T_{Ref}\right)\right)\frac{G_3}{G_{Ref}} \\ I_{Ph(G_4)} &= \left(I_{SC,Ref} + K_{ISC}\left(T - T_{Ref}\right)\right)\frac{G_4}{G_{Ref}} \end{aligned}\right\} \quad (3)$$

where $I_{Ph(G1)}$, $I_{Ph(G2)}$, $I_{Ph(G3)}$ and $I_{Ph(G4)}$ is photo generated current with respect to the irradiance on the panel surface (A), K_{ISC} is current coefficient, $I_{SC,Ref}$ is short circuit current at Standard Test Conditions (STC) (A), T_{Ref} is temperature at STC (°C), G_{Ref} is irradiance at STC (W/m^2), G_1, G_2, G_3 and G_4 is irradiance on individual panels (W/m2),

For a 2S2P configuration under PSC, PV system output current and voltage are expressed as

$$\left.\begin{aligned} I_{PV} &= Min(I_1, I_2, I_3, I_4) \\ V_{PV} &= V_1 + V_2 + V_3 + V_4 \end{aligned}\right\} \quad (4)$$

where I_1 I_2, I_3 and I_4 are panel currents that are calculated by substituting $I_{Ph(G1)}$, $I_{Ph(G2)}$, $I_{Ph(G3)}$ and $I_{Ph(G4)}$ in Eq. (3). In general, if the PV system has 'n' number of modules connected in series, the output current and voltage under PSC can be expressed as

$$\begin{aligned} &If \quad I_{PV} > I_{Ph(n-1)} \\ &I_{PV} = I_{Ph}\left(G_n\right) - I_D\left[\exp\left(\frac{q\left(V_n + I_{PV}R_S\right)}{N_S A B_K T}\right) - 1\right] \\ &\qquad - \frac{V_n + I_{PV}R_S N_S}{N_S R_{Sh}} \quad (5a) \\ &V_{PV} = V_n \quad (5b) \\ &If \quad I_{Ph(n-2)} < I_{PV} < I_{Ph(n-1)} \\ &I_{PV} = I_{Ph}\left(G_{(n-1)}\right) - I_D\left[\exp\left(\frac{q\left(V_{n-1} + I_{PV}R_S\right)}{N_S A B_K T}\right) - 1\right] \\ &\qquad - \frac{V_{n-1} + I_{PV}R_S N_S}{N_S R_{Sh}} \quad (6a) \\ &V_{PV} = V_n + V_{n-1} \quad (6b) \end{aligned}$$

Similarly if, $I_{PV} < I_{Ph1}$

$$\begin{aligned} I_{PV} &= I_{Ph}\left(G_1\right) - I_D\left[\exp\left(\frac{q\left(V_1 + I_{PV}R_S\right)}{N_S A B_K T}\right) - 1\right] \\ &\quad - \frac{V_1 + I_{PV}R_S N_S}{N_S R_{Sh}} \quad (7a) \\ V_{PV} &= V_1 + V_2 + \ldots\ldots + V_n \quad (7b) \end{aligned}$$

During partial shaded condition, total power (P_T) of PV system is

$$P_T = P_1(G_{E1}) + P_2(G_{E2}) + \ldots\ldots + P_n(G_{En}) \quad (8)$$

where E_1, E_2,……, E_n are the effective irradiances of the PV modules.

B. PROPOSED GLOBAL MPP TRACKING SCHEME

Fig. 2 shows P-V characteristics of 2S2P configuration. The critical observation that was made from P-V characteristics can be stated as, from Fig. 2 it is clearly observed that at a voltage of 18 V and 36 V no two patterns are having the same power. Therefore, by observing power at these two voltage points we can decide the shading pattern on the PV panel surface [22]. This is the main motivation behind the proposal to implement a new MPPT scheme irrespective of uniform irradiance or partial shaded condition. Making this statement into simple, power at two voltage points are calculated and given to artificial neural network along with temperature on the PV panel surface such that corresponding patterns is obtained. Furthermore, the pattern obtained from ANN and temperature on the panel surface is fed to the 2-Dimensional Lookup table to get exact MPP of PV system.

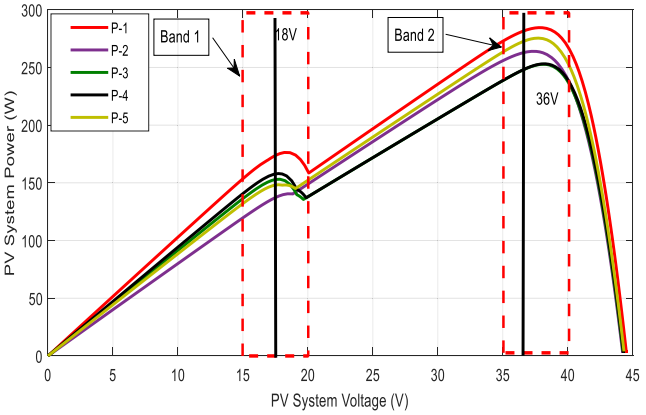


FIGURE 2. P-V characteristics of 2S2P configurations.

The lookup table is also provided with interpolation and extrapolation techniques and it provides the maximum power voltage corresponding to the shading pattern identified by the ANN. The dc-dc converter is operated at this voltage and maximum power is extracted from the PV system. The proposed scheme is very simple to implement, does not require any complex calculations and it can be applied on both uniform irradiance and partial shading conditions. Initially, the proposed scheme is developed with 2S2P configuration and simulated in Matlab/Simulink environment and their performance is verified using different shading patterns.

C. SHADING PATTERN IDENTIFICATION USING ANN

The basic idea behind Artificial Intelligence is to facilitate the system to make its own decision based on training and experience. Simulating biological neurons and implementing into a compound of an organization is named as Artificial Neural Networks (ANN). The ANN fitting tool maps between a set of input and target data hence, neural network doesn't require any complex calculations at the same time it can

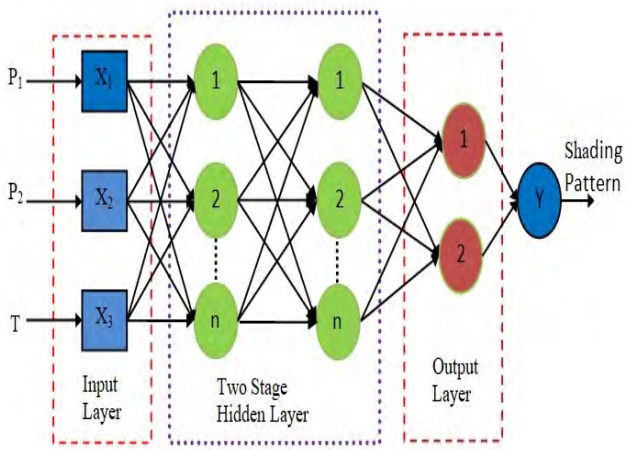


FIGURE 3. Architecture of the ANN.

be implemented in a low cost microcontroller. Due to the absences of computations, ANN generates target output faster compared to regular tools. The basic structure of the ANN has three layers, termed as inner, hidden and outer layers as shown in Fig. 3 [23]. Numeric data given to the input layer is stored and further processed to the hidden layer. The size and number of hidden layers depend on the task assigned to the ANN. By varying the number of neurons in the hidden layer, the optimum mapping is structured based on performance error and training period. The function of each neuron in the hidden and output layer is to take the sum of weighted inputs and transfer the result via a non-linear activation function. Generally, mean square error and regression analysis are used to evaluate the performance of the ANN.

A two layer feed forward error back propagation network with sigmoid hidden neurons and linear output neurons (newfit) are more suitable for power electronic applications. If suppose the target obtained from ANN is not the desired one, again the error is evaluated and weights of the links are changed from back to the front until target output is obtained. Scaled Conjugate Gradient back propagation (trainscg) and Levenberg-Marquardt back propagation (trainlm) algorithms are used to train the neural network. Among these two algorithms 'trainlm' is preferred because of faster convergence. Levenberg-Marquardt Back Propagation (LMBP) algorithm is a combination of Gradient Descent Method (GDM) and Gauss Newton Method (GNM). Hence, LMBP combines the advantages of global properties in GDM and local conveyance properties in GNM.

ANN is trained to identify shading pattern on the solar panel. At first, for a 2S2P configuration power at two different voltage points are predetermined for different irradiance pattern and temperatures as shown in Table 1. The obtained dataset of numeric input and target data is given to train ANN. The count of neurons in the hidden layer is 20 and Levenberg-Marquardt back propagation (LMBP) algorithm is used to train ANN. The performance validation curve during

TABLE 1. Data used to train ANN for A 2S2P configuration.

S.No	Input Data						Target
	T=20°C		T= 25°C		T= 30°C		Pattern
	P(19V)	P(38V)	P(19V)	P(38V)	P(19V)	P(38V)	
1	148	245.2	152.2	244.8	146.4	243.1	P#1
2	110.4	163.4	110.2	162.9	106.3	161.5	P#2
3	140.5	122.9	140.8	121.1	137.8	120.4	P#3
4	128.3	204.56	125.7	203.5	124	201.2	P#4
5	178.1	161.8	172.3	161.8	163.6	162.7	P#5

pattern identification is shown in Fig. 4 (a) and it is observed that error decreases and converges after 6 epochs to obtain the target. Training state and regression analysis are shown in Fig. 4 (b) and (c).

D. TWO-DIMENSIONAL LOOKUP TABLE

A 2-Dimensional Lookup table (2DLT) is found as the best alternative tool for the computational process with indexing operation. Instead of undergoing numerous calculations, 2DLT tool fetches directly the required value among pre-calculated data stored in the static memory. Similar to ANN, direct mapping the required values saves computational time. In addition, the promising feature of the 2DLT tool is, with the help of interpolation and extrapolation the required values which are not present in static memory can be calculated by itself.

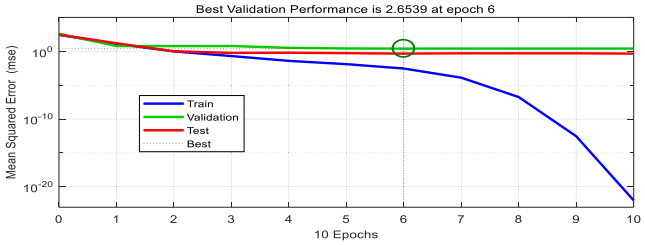
TABLE 2. MPP voltages obtained from 2DLT for a 2S2P configuration.

Pattern (P)	Temperature (°C)					
	20°C	25°C	30°C	35°C	40°C	45°C
P-1	38.3	37.8	35.9	34.9	33.9	32.65
P-2	39.25	38.5	36.9	35.9	34.9	33.33
P-3	39.25	38.3	37.5	36.9	34.9	33.9
P-4	18.62	17.62	17.61	16.62	15.62	15.64
P-5	18.69	17.66	16.67	16.64	15.69	15.62

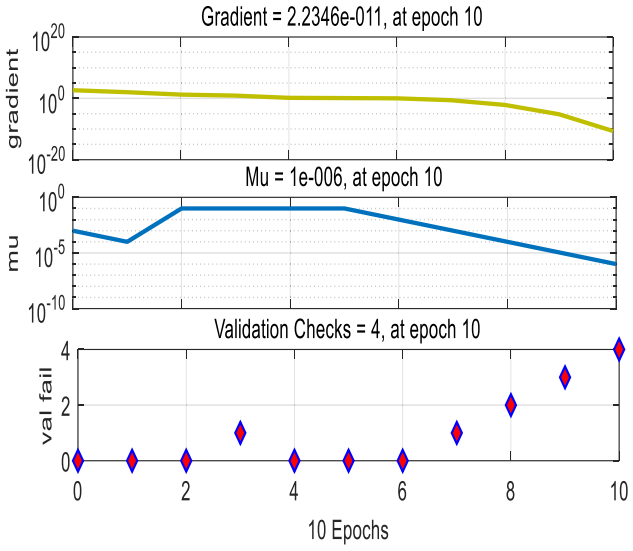
A 3-Dimensional view of MPP obtained for respective temperature and shading patterns are shown in Fig. 5. In the proposed GMPPT scheme, shading pattern and temperature on the panel surface are given as input to the 2DLT tool. The static memory data of 2S2P configuration is shown in Table 2, depending on numeric pattern and temperature 2DLT gives MPP of PV system. Interpolation and extrapolation technique guarantees the exact MPP of PV system.

IV. DC-DC SIMO CONVERTER

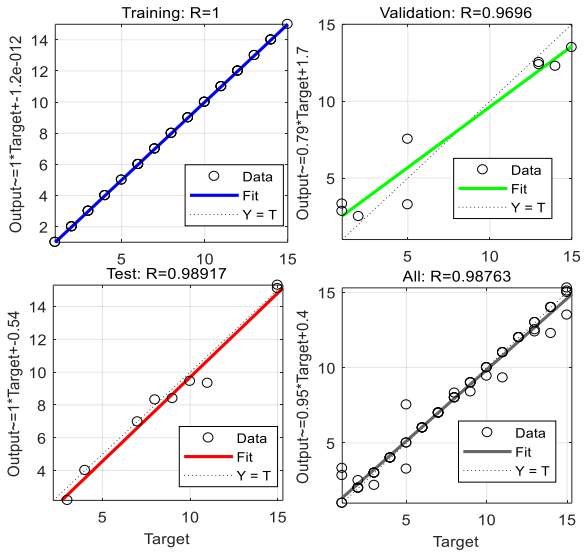
The Single Input and Multi Output (SIMO) converter configuration is shown in Fig. 6, [24] consists of filter capacitor (C_f), inductor (L_f), two power electronic switches (S_A and S_B) and two diodes (D_a and D_b). The dc-dc converter



(a)



(b)



(c)

FIGURE 4. (a) Performance validation curve, (b) training state, and (c) regression analysis.

develops four output voltages (V_1, V_2, V_3 and V_4) from a single input having different magnitudes which are fed to MLI [25].

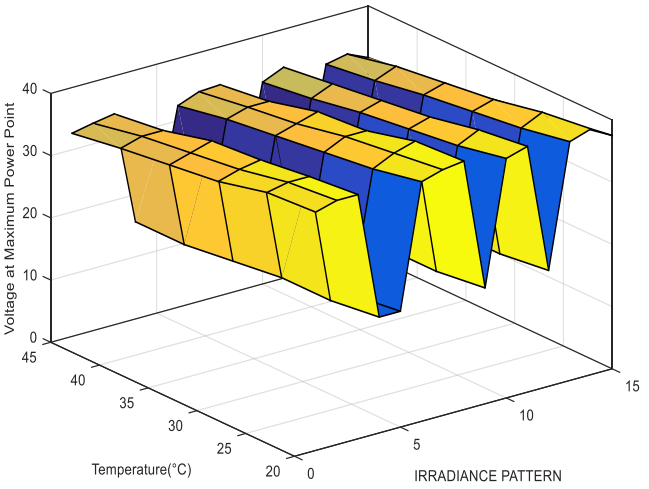


FIGURE 5. 3-dimensional view of MPP voltages stored in 2DLT.

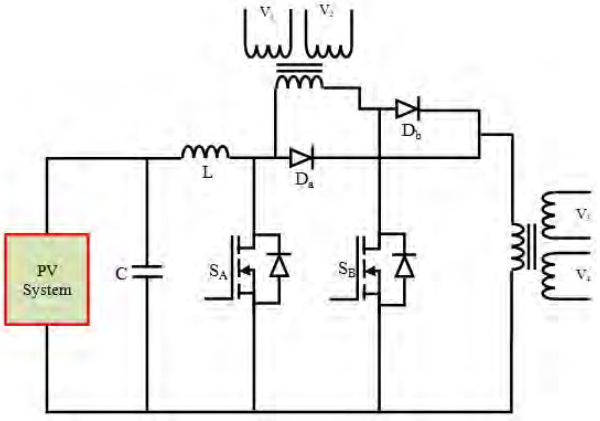


FIGURE 6. DC-DC single input and multi output converter.

As the SIMO converter power electronic switches, S_A is in on-state and S_B is in off-state, inductor (L_f) stores energy from PV array. When the switching states are inter changed, both the energy stored in inductor and energy from PV array are transferred to MLI through D_a. Hence, the output voltage of the converter is represented by the turns ratio of the transformer as

$$\left.\begin{aligned} V_1 &= \frac{1}{1-\delta} V_{PV} \\ V_2 &= \frac{1}{2\,(1-\delta)} V_{PV} \\ V_3 &= \frac{1}{4\,(1-\delta)} V_{PV} \\ V_4 &= \frac{1}{8\,(1-\delta)} V_{PV} \end{aligned}\right\} \tag{9}$$

V. MLI WITH REDUCED SWITCH COUNT

In this topology, full bridge converter is connected in cascade to the diode as shown in Fig. 7. Inverter operation is explained in two parts, (a) positive cycle and (b) negative cycle. V_1, V_2, V_3 and V_4 voltages of the converter are constant and made equal to 6V, 12V, 24V and 48V.

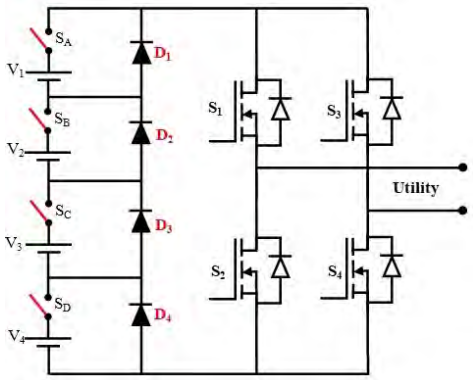


FIGURE 7. Thirty one level inverter configuration.

A. INVERTER OPERATION IN THE POSITIVE CYCLE

For ease of analysis, positive cycle operation is further divided into sixteen modes. During the entire positive cycle mode of operation, full bridge converter switches S_1 and S_2 are in on-state.

Mode 1: In this mode of operation, the switch S_A is in on-state and the rest of the switches are in off-state as shown in Fig. 8(a). At this point, inverter output voltage is equal to V_1 i.e., 6V.

Mode 2: In this mode of operation the switch S_B is in on-state, therefore D_1 is forward bias and the remaining diodes are reverse biased, hence the voltage path is through D_1 as shown in Fig. 8(b). At this point, inverter output voltage is 12V.

*Mode 3:*Fig. 8(c) shows the operation of the inverter. During this mode of operation S_A and S_B switches are turned on. At this particular mode, V_1 and V_2 voltages are added, the output voltage across the inverter will be 18V.

Mode 4: During this mode of operation the switch S_C is closed and the voltage path is through forward biased D_1 and D_2 diodes as shown in Fig. 8(d). The output voltage of the inverter will be 24V.

Mode 5: The switches S_A and S_C are closed, in this situation the diode D_2 is forward biased and the rest of the diodes are reverse biased. The voltage path is clearly shown in Fig. 8(e). The output voltage across the inverter will be 30V.

Mode 6: In this mode of operation, the switches S_B and S_C are in on-state as shown in Fig. 8(f). Both the voltages V_2 and V_3 are added to obtain an output voltage of 36V across the inverter.

Mode 7: During this mode of operation, switches S_A, S_B and S_C are closed such that the voltage V_1, V_2 and V_3 are added to give a total voltage of 42V as the output of the inverter. The switching states and voltage path is clearly shown in the Fig. 8(g).

Mode 8: The switch S_D is in on-state, in this situation D_1, D_2 and D_3 diodes are forward biased. Respective voltage path in this mode of operation is shown in Fig. 8(h). Therefore output voltage across the inverter will be 48V.

TABLE 3. Switching states of the power electronic devices (L- voltage levels, V-voltage).

L	V	S_A	S_B	S_C	S_D	S_1	S_2	S_3	S_4
1	90V	on	on	on	on	on	off	off	on
2	84V	off	on	on	on	on	off	off	on
3	78V	on	off	on	on	on	off	off	on
4	72V	off	off	on	on	on	off	off	on
5	66V	on	on	off	on	on	off	off	on
6	60V	off	on	off	on	on	off	off	on
7	54V	on	off	off	on	on	off	off	on
8	48V	off	off	off	on	on	off	off	on
9	42V	on	on	on	off	on	off	off	on
10	36V	off	on	on	off	on	off	off	on
11	30V	on	off	on	off	on	off	off	on
12	24V	off	off	on	off	on	off	off	on
13	18V	on	on	off	off	on	off	off	on
14	12V	off	on	off	off	on	off	off	on
15	6V	on	off	off	off	on	off	off	on
16	0V	off	off	off	off	on	off	off	on
17	-6V	on	off	off	off	off	on	on	off
18	-12V	off	on	off	off	off	on	on	off
19	-18V	on	on	off	off	off	on	on	off
20	-24V	off	off	on	off	off	on	on	off
21	-30V	on	off	on	off	off	on	on	off
22	-36V	off	on	on	off	off	on	on	off
23	-42V	on	on	on	off	off	on	on	off
24	-48V	off	off	off	on	off	on	on	off
25	-54V	on	off	off	on	off	on	on	off
26	-60V	off	on	off	on	off	on	on	off
27	-66V	on	on	off	on	off	on	on	off
28	-72V	off	off	on	on	off	on	on	off
29	-78V	on	off	on	on	off	on	on	off
30	-84V	off	on	on	on	off	on	on	off
31	-90V	on	on	on	on	off	on	on	off

Mode 9: During this mode of operation, the switch S_A and S_D are in on-state as shown in Fig. 8(i). The diodes

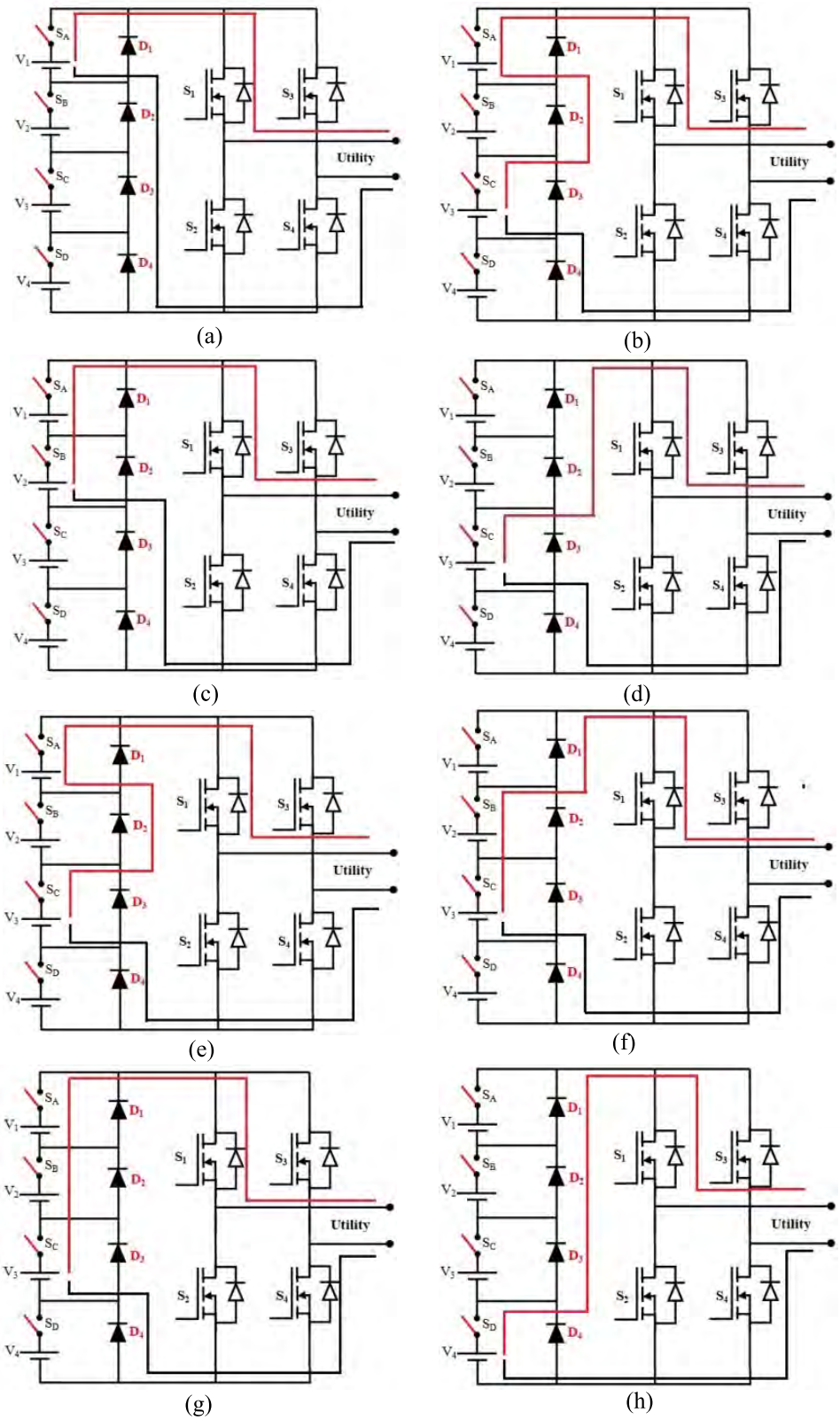


FIGURE 8. Operating Modes of Inverter during Positive Half Cycle (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5, (f) Mode 6, (g) Mode 7 and (h) Mode 8.

D_2 and D_3 are forward biased, therefore the voltages V_1 and V_4 are accumulated to obtain a voltage of 54V across the inverter.

Mode 10: In this mode of operation, switches S_B and S_D are closed as shown in Fig. 8(j). As the diode D_3 is forward biased both the voltage V_2 and V_4

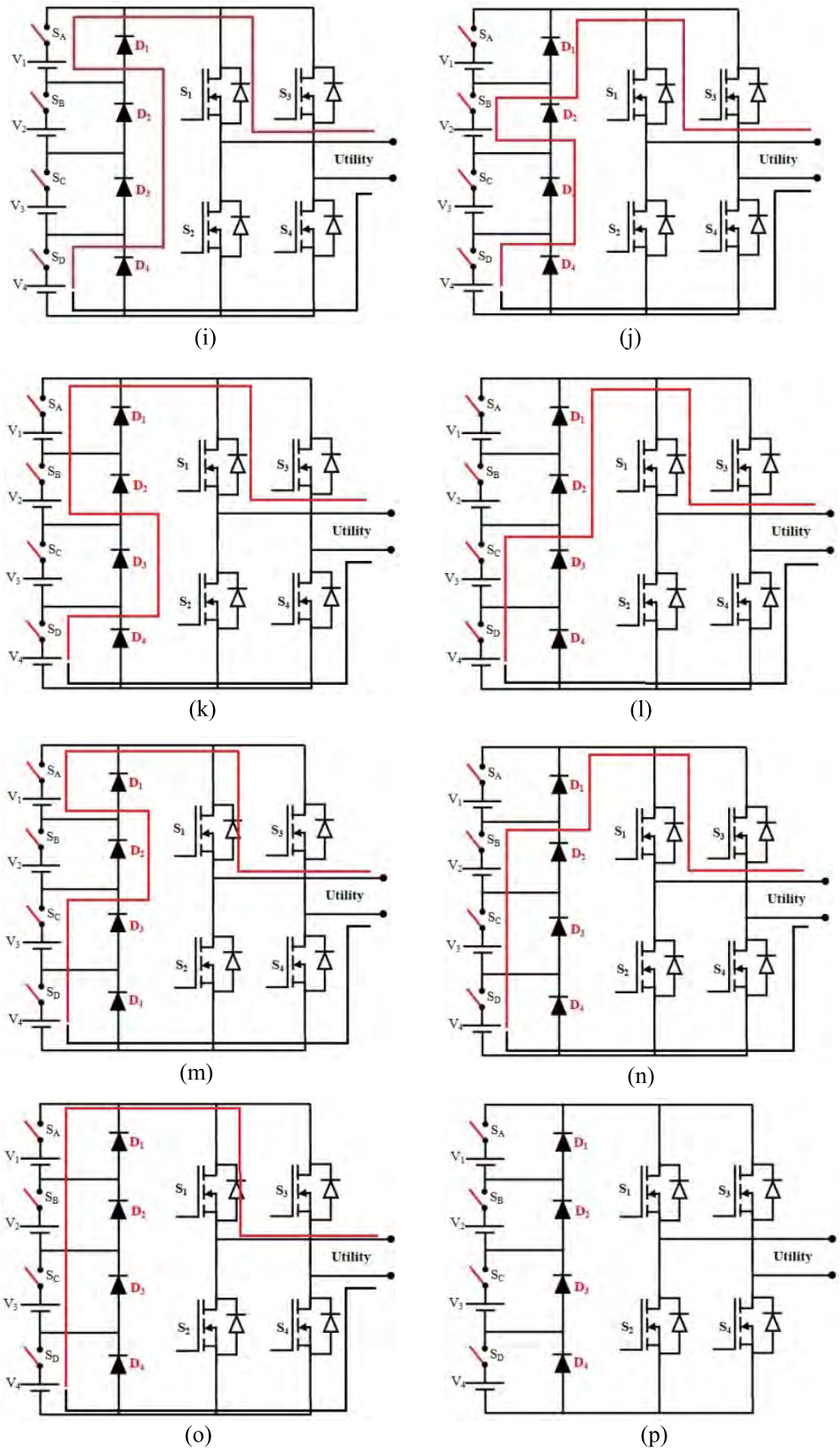
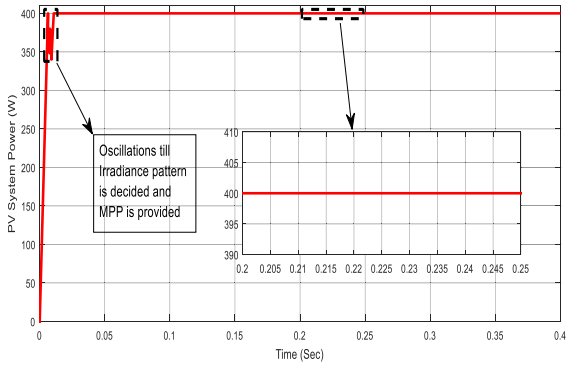


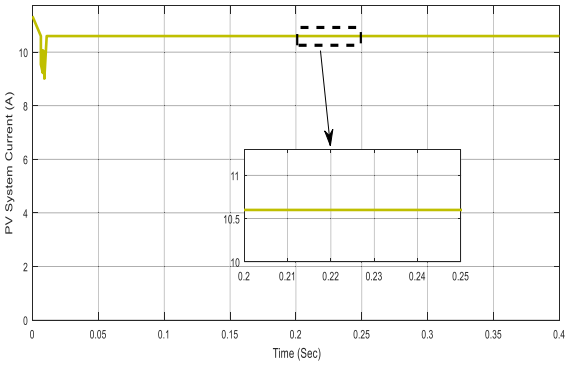
FIGURE 8. *(Continued) Operating Modes of Inverter during Positive Half Cycle (i) Mode 9, (j) Mode 10, (k) Mode 11, (l) Mode 12, (m) Mode 13, (n) Mode 12, (o) Mode 15 and (p) Mode 16.*

are added and hence the output voltage of the inverter is 60V.

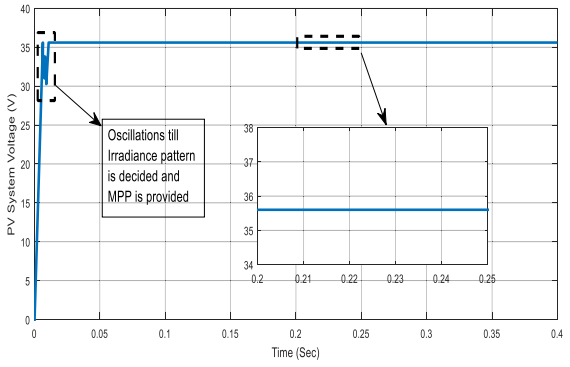
Mode 11: The switches S_A, S_B and S_D are closed as shown in Fig. 8(k). Due to this switching sequence, D_3 diode gets



(a)

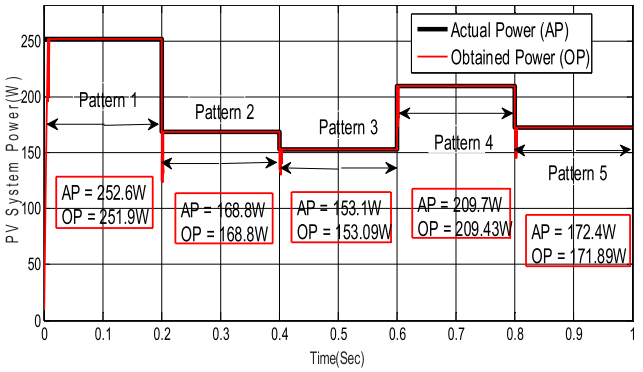


(b)

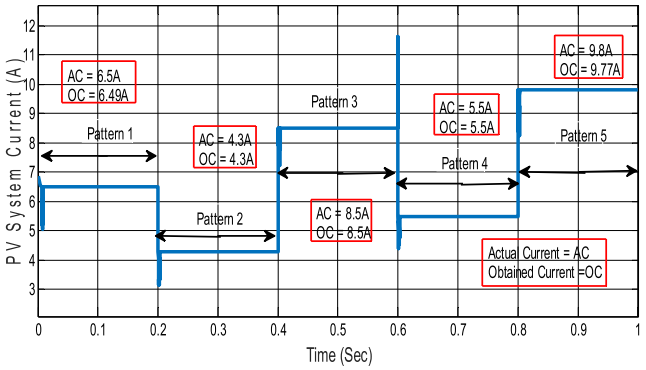


(c)

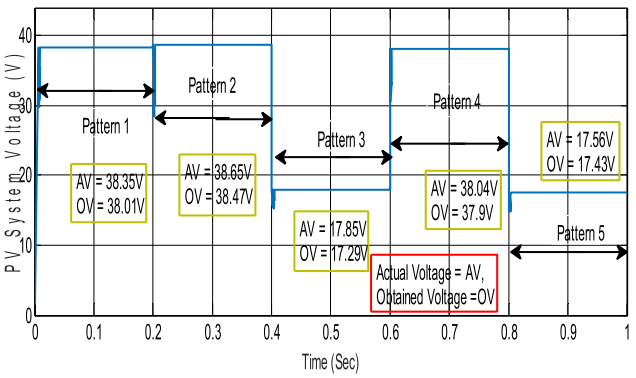
FIGURE 9. PV System Output Parameters of 2S2P configuration using proposed GMPPT scheme (a) Power, (b) Current and (c) Voltage.



(a)



(b)



(c)

FIGURE 10. PV System Output Parameters of 2S2P configuration using proposed GMPPT scheme under PSC (a) Power, (b) Current and (c) Voltage.

forward bias and hence all the three voltages V_1, V_2 and V_4 are added to get a 66V output voltage across the inverter.

Mode 12: In this mode of operation, the switch S_C and S_D are in on-state as shown in Fig. 8(l). Therefore this switching phenomenon results in inverter output voltage as 72V. The voltage path is through D_1 and D_2 diodes, which are forward biased.

Mode 13: During this mode of operation, the switches S_A, S_C and S_D are closed as shown in Fig. 8(m). As the D_2 diode gets forward bias all the three voltages are added. In this situation output voltage of the inverter will be 78V.

Mode 14: In the Fig. 8(n) operation of the inverter is depicted. From Fig, it is clear that the switches S_B, S_C and S_D are closed these results forward bias of the diode D_1. As the switches S_B, S_C and S_D are in on-state, the output voltage of the inverter will be 84V.

Mode 15: In this mode of operation all the four switches are closed as shown in Fig. 8(o). The final output voltage of the inverter will be 90V.

Mode 16: During this mode of operation, all the four switches are opened as shown in Fig. 8(p). The output voltage of the inverter is equal to 0V.

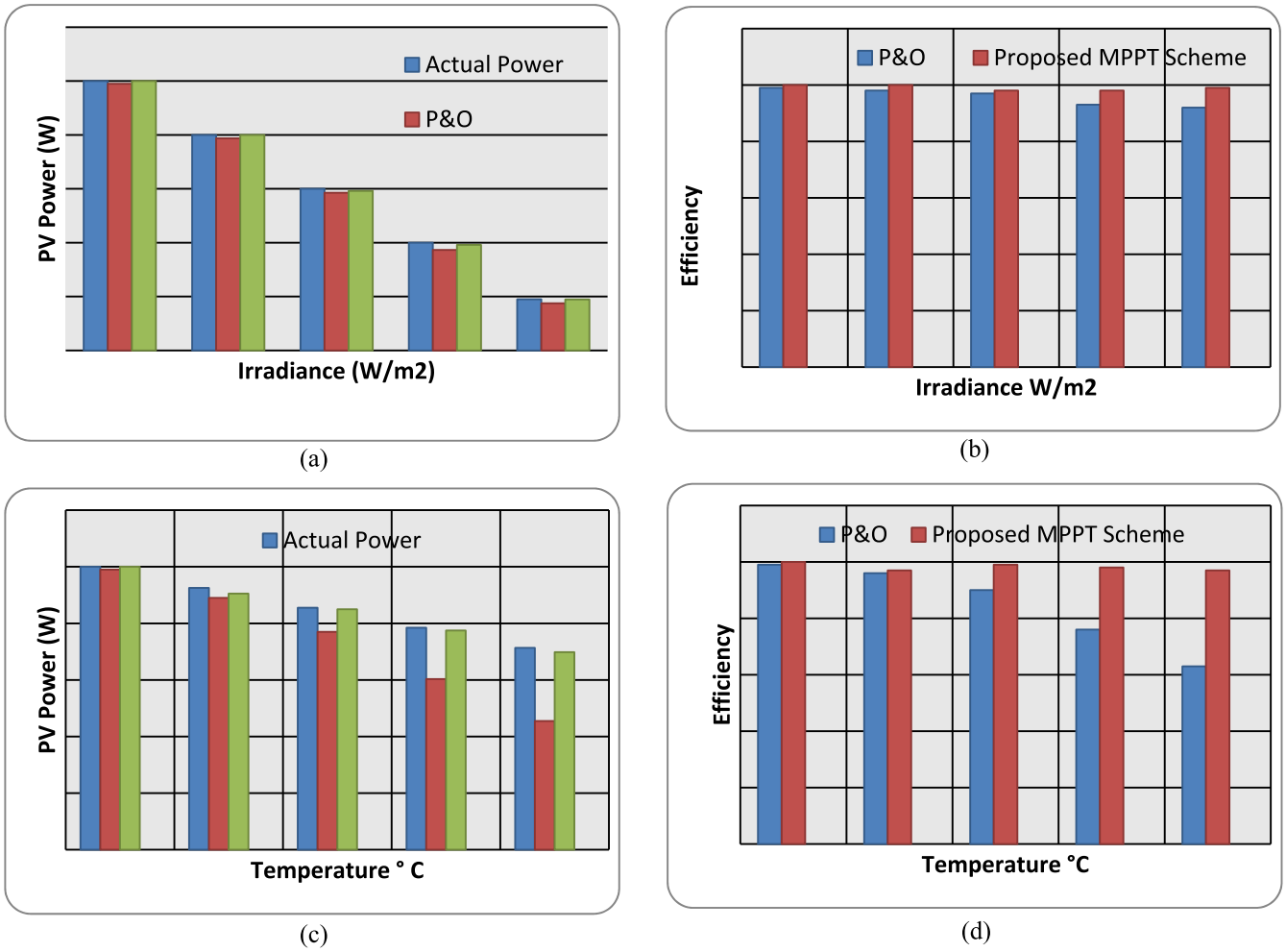


FIGURE 11. PV system output power and efficiency at (a) – (b) Variable irradiance with constant temperature of 25 °C and (c) – (d) Variable temperature with constant irradiance of 1000W/m^2.

Finally, inverter output voltages for the positive cycle in the sixteen modes of operation are 6V, 12V, 18V, 24V, 30V, 36V, 42V, 48V, 54V, 60V, 66V, 72V, 78V, 84V, 90V and 0V respectively.

B. INVERTER OPERATION IN THE NEGATIVE CYCLE

Similar, to the positive cycle the operation of the negative cycle is illustrated in sixteen modes. In the negative cycle, the output voltage of the inverter is same as that of the positive cycle. Furthermore, only switches S_2 and S_3 of the full bridge converter are operated. Output voltage of the inverter during negative cycle are −6V, −12V, −18V, −24V, −30V, −36V, −42V, −48V, −54V, −60V, −66V, −72V, −78V, −84V, −90V and 0V. The final summary of both the cycles can be given as 90V, 84V, 78V, 72V, 66V, 60V, 54V, 48V, 42V, 36V, 30V, 24V, 18V, 12V, 6V, 0V, −6V, −12V, −18V, −24V, −30V, −36V, −42V, −48V, −54V, −60V, −66V, −72V, −78V, −84V and −90V. Current Mode Controller (CMC) is used to control thirty-one level inverter. Pulse Width Modulation (PWM) technique is employed to generate control signals to the power electronic switches. As there is a change in the utility voltage, inverter output voltage has to be changed with respect to utility voltage. The proposed thirty-one level inverter topology has only eight power electronic switches. Hence, compared with the traditional multilevel inverters the proposed topology is simple to implement. Switching states of the power electronic devices are tabulated in Table 3.

VI. SIMULATION RESULTS

Initially, the proposed GMPPT scheme is tested at Standard Test Conditions. Fig. 9 shows the performance of 2S2P configuration (a) output power, (b) output current and (c) output voltage. From figure, it is clear that till irradiance pattern is decided and MPP voltage is provided transients are observed. Once duty cycle of the converter is obtained, maximum solar power is extracted with reduced oscillations. As of the tools employed in the MPPT scheme are direct mapping tools in between input and target data, very little percentage of oscillations are observed. Under standard test conditions, the proposed MPPT scheme has extracted maximum power from the PV system with reduced oscillations.

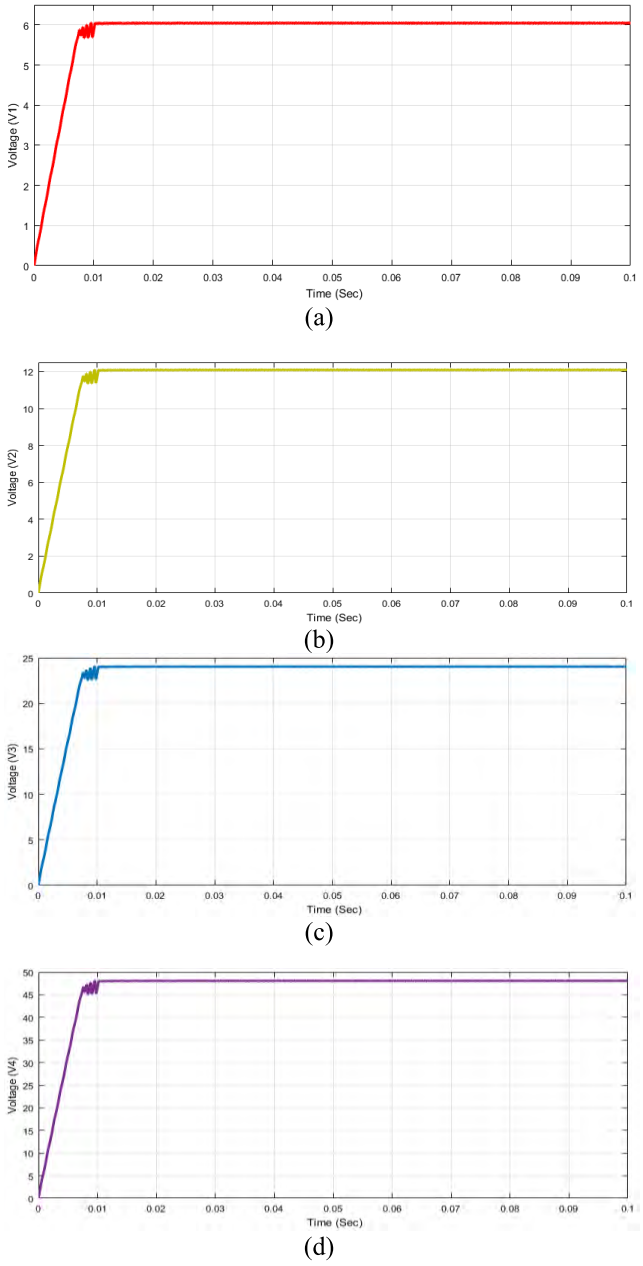


FIGURE 12. Output voltages of the converter (a) V_1, (b) V_2, (c) V_3, and (d) V_4.

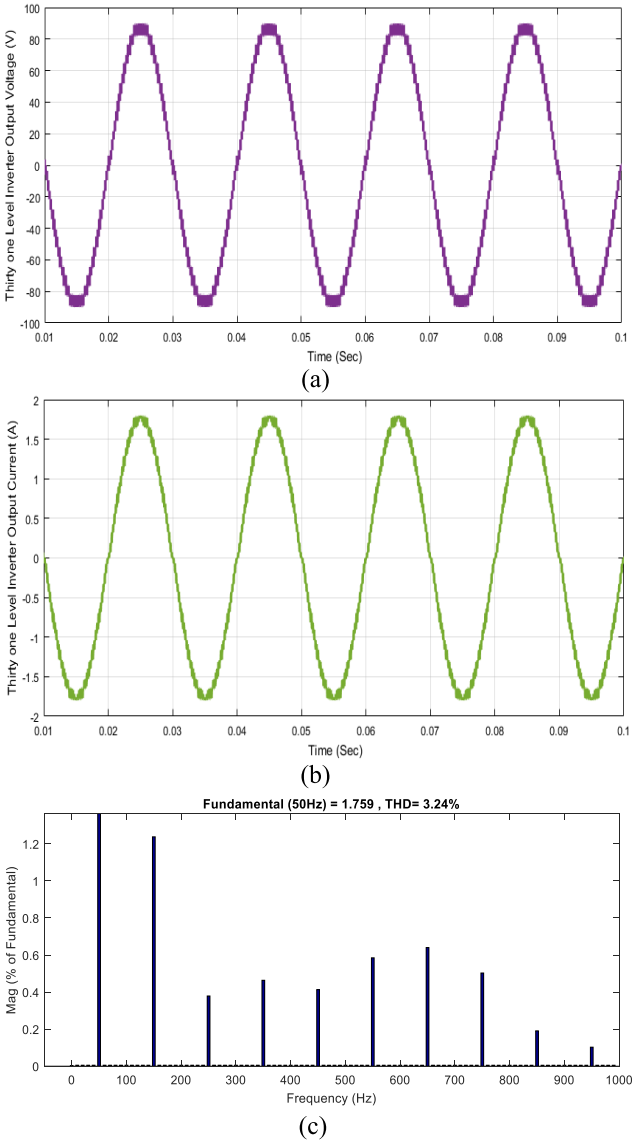


FIGURE 13. Output (a) voltage, (b) current, and (c) voltage THD of thirty-one level inverter.

During solar power generation partial shading phenomenon is unavoidable. Hence, testing at STC can't justify the effectiveness of the MPPT scheme. Therefore the performance of the proposed MPPT scheme is examined under PSC. GMPP tracking ability of the proposed MPPT scheme is examined under different shading patterns using 2S2P configurations. Using MATLAB/Simulink different shading patterns are developed and named in number. At a time duration of 0.2sec, shading patterns are changed from one to other respectively.

Fig. 10(a)-(c) depicts PV system output parameters of 2S2P configuration. For pattern 1, actual power from the PV system is 252.6W and the proposed GMPP tracking scheme succeeded in extracting a maximum power of 251.9W. As discussed earlier, till irradiance pattern and required MPP voltage is decided by the MPPT scheme transient oscillations are observed. But the transient oscillations are very little as of the direct mapping tools are involved to obtain target input. Similarly, for the rest of patterns the proposed GMPPT scheme has tracked the exact power path during partial shading conditions. The actual power for the respective patterns is indicated by the black graph. Similarly, red color represents obtained power using the proposed MPPT scheme. From Fig. 10, it is observed that there is no difference between the two graphs. Therefore the proposed GMPPT scheme has tracked the power path during partial shading condition.

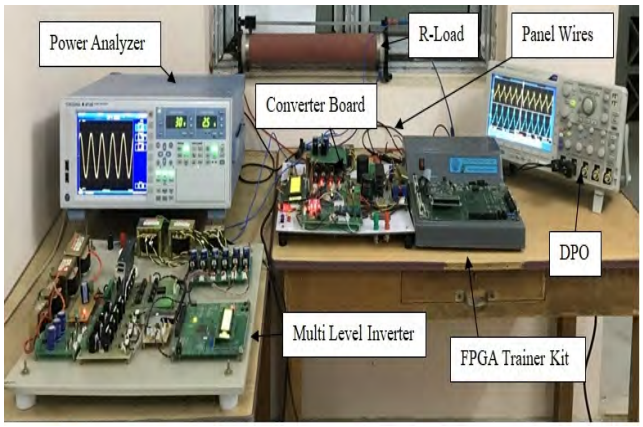


FIGURE 14. Experimental prototype of the PV inverter.

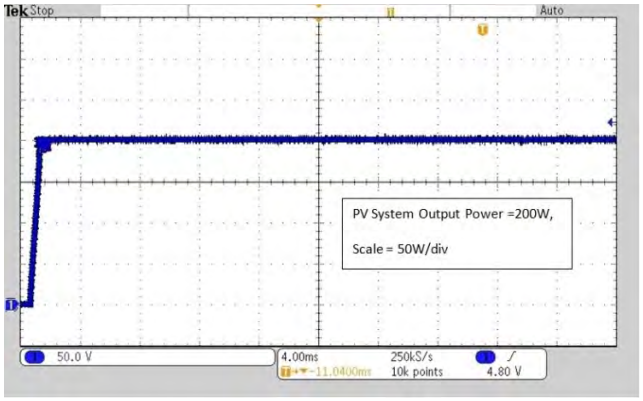


FIGURE 15. Experimental results of the PV system output power using proposed MPPT scheme.

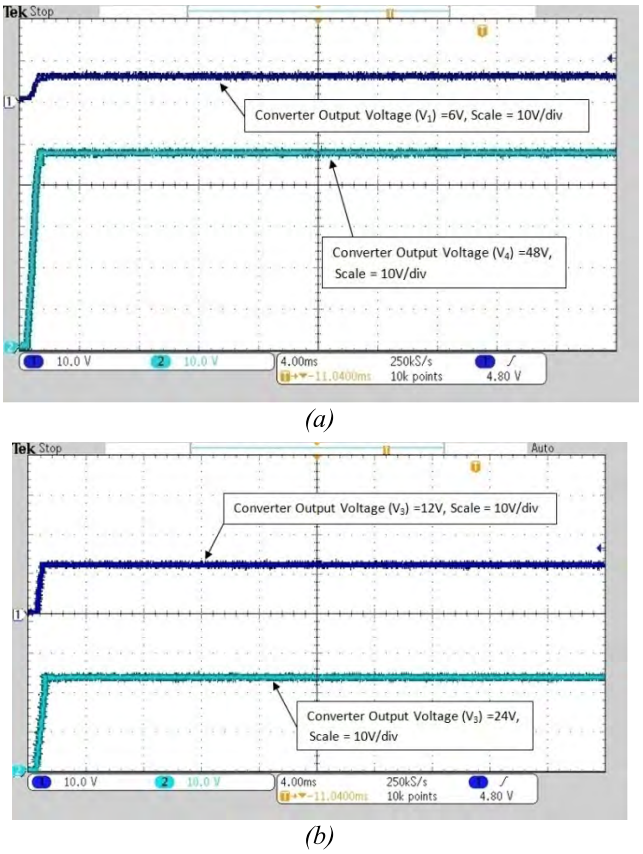


FIGURE 16. Output voltage of the SIMO converter (a) voltage V_1 and V_4, (b) Voltage V_3 and V_2.

Fig. 11(a), depicts total power harvested by the proposed GMPPT scheme under varying irradiance with constant temperature, in comparison with actual available power and conventional P&O controller. In continuation their efficiency are shown in Fig. 11(b). Similarly, PV system output power under varying temperature at a constant irradiance of 1000W/m^2 with concern efficiencies are depicted in Fig. 11(c)-(d).

A dc-dc intermediate boost converter is employed to maintain constant output voltage across the PV system. The PV system output voltage is fed to the SIMO converter, which divides the input voltage into four independent voltages. The magnitude of SIMO converter output voltages depends on the turns ratio incorporated in the converter. In this case SIMO converter output voltages are 6V, 12V, 24V and 48V as shown in Fig. 12(a)-(d). In continuation SIMO converter output voltages are given to the MLI. The MLI consists of diode configuration and full bridge converter. The individual DC voltages obtained are inverted into AC voltage. The results plotted in Fig. 13(a) and (b) shows that the inverter output voltage and current are having thirty-one levels, hence resemble a sinusoidal waveform and their respective THD results are depicted in Fig. 13(c). The ripples in the voltage given to the inverter are eliminated by SIMO converter.

VII. EXPERIMENTAL VALIDATION

A prototype is designed and developed to examine the performance of the proposed PV inverter topology as shown in Fig. 14. FPGA Spartan Trainer Kit is used to generate essential control signals to the multi level inverter and gate pulse to the dc-dc SIMO converter. The rating of the designed prototype is 200W fed to a single phase 50Hz utility. Prototype specifications are mentioned in Table 4.

TABLE 4. Prototype specifications.

S.No	Module	Parameter	Value
1	Dc-dc SIMO Converter	Filter Inductor	1mH
2		Filter Capacitor	10μF
3	Multi Level Inverter	Capacitor	1000μF
4		Filter Inductor	1.8mH
5		PWM Frequency	1550Hz
6		Maximum Power	200W
7	PV System	Maximum Voltage	37.8V
8		Maximum Current	5.3A

The proposed scheme is initially developed in Matlab platform and dumped into Xilinx Spartan 3A FPGA trainer kit

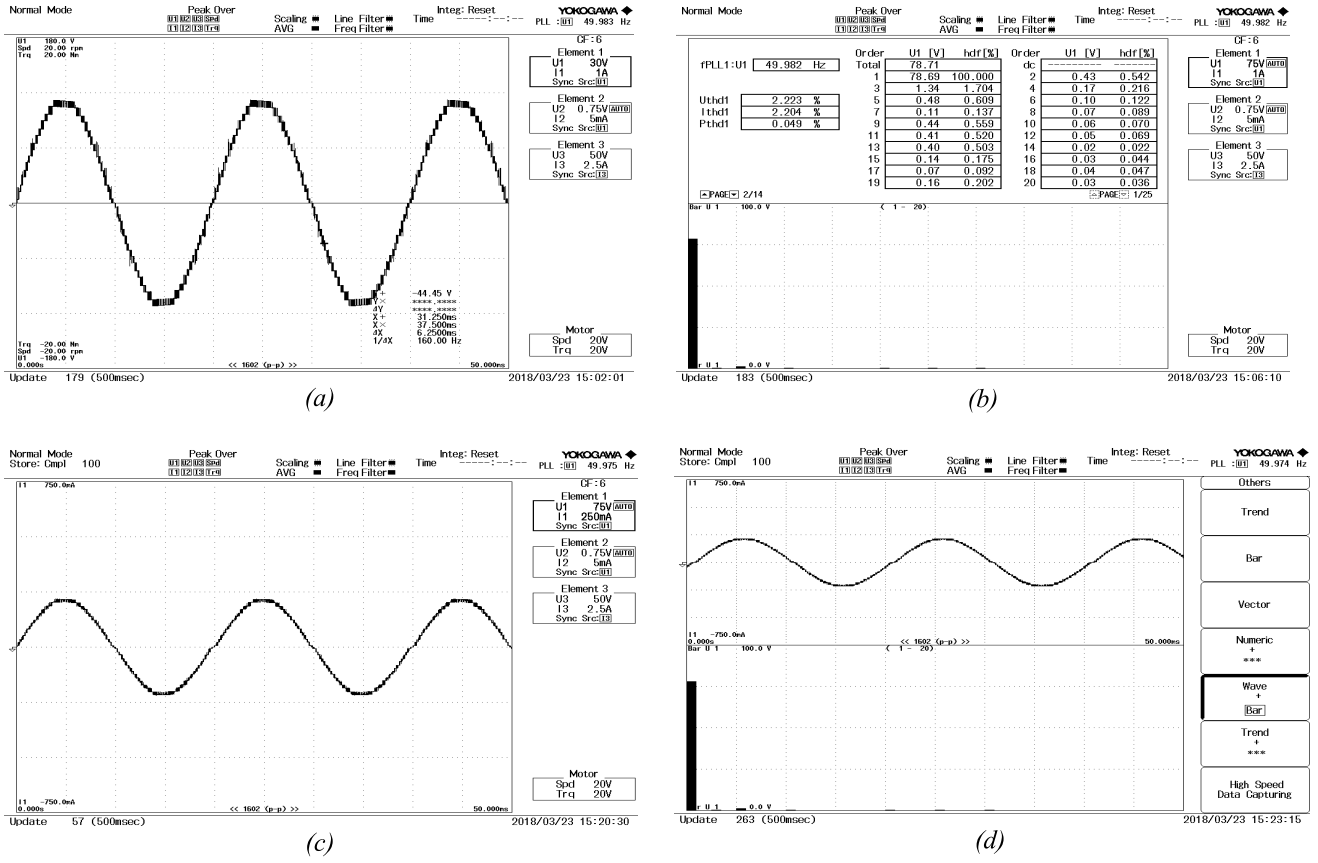


FIGURE 17. Experimental results of the MLI (a) output voltage, (b) voltage THD, (c) output current, and (d) current THD.

using HDL coder and obtained pulses are given to 4081IC based PWM generator. The HDL coder also provides integration with Xilinx ISE to synthesize the generated code into bit stream that can be downloaded on to the FPGA on Xilinx development boards for rapid prototyping. Based on powers at two different voltage points and temperature, shading patterns are identified and fed to 2DLT. From the static memory data saved on off-chip SDRAM memory, exact MPP is measured and develops the pulse width modulation (PWM) required for the dc-dc converter is generated using integrated circuit.

PV system produces P-V and I-V characteristics, which are similar to RNG 200D 200W mono-crystalline solar panel. PV current is sensed by Hall Effect LA25-P current sensor. Similarly, voltage is sensed by 7840 IC based voltage sensing circuit. These parameters are prearranged to FPGA trainer kit through the TL084 integrated circuit board, which scales down the voltage level between 0-5V. In order to reduce losses between sensing elements and control circuit TL082 buffer IC is incorporated. Gate pulses obtained from the controller is given to 4081 IC based PWM signals generator circuit, which is further connected to TLP250 opto-isolator. The output signal obtained from the controller is directly given to switching device. Overall voltage and current protection are supervised by 4027 and 4098 flip-flop IC. Fig. 15 depicts experimental results of PV system output power. From the Fig, it is clear that the proposed MPPT scheme had extracted the maximum solar power of 200W.

PV panel voltage and current are fed to the dc-dc SIMO converter, Fig. 16 depicts output voltage of the converter. From the graph, it is evident that the converter provides four output voltages with different magnitudes. The final output voltages obtained from the converter are connected to the filter capacitor. Across the capacitor, the D.C voltages are 6V, 12V, 24V and 48V which are given as input to the full bridge converter.

The FPGA Spartan kit operated by supplying an external voltage of 5V. The pulses obtained from the trainer board are connected to TLP250 opto-isolator which also acts as a PWM driver. The similar TLP250IC are used to provide pulses to the diode configuration and the IGBT switches of the full bridge need an external supply of 15V. The experimental results plotted in Fig. 17(a) and (c) shows the output voltage and current of the thirty-one level inverter.

From Fig. 17(a), it is clear that the output voltage of the MLI has thirty-one levels and current in Fig. 17(b) is sinusoidal, such that MLI feeds utility in phase. Similarly, voltage and current THD are depicted in Fig. 17(b) and (d), from the figure THD values are voltage is 2.223% and current is 2.204%.

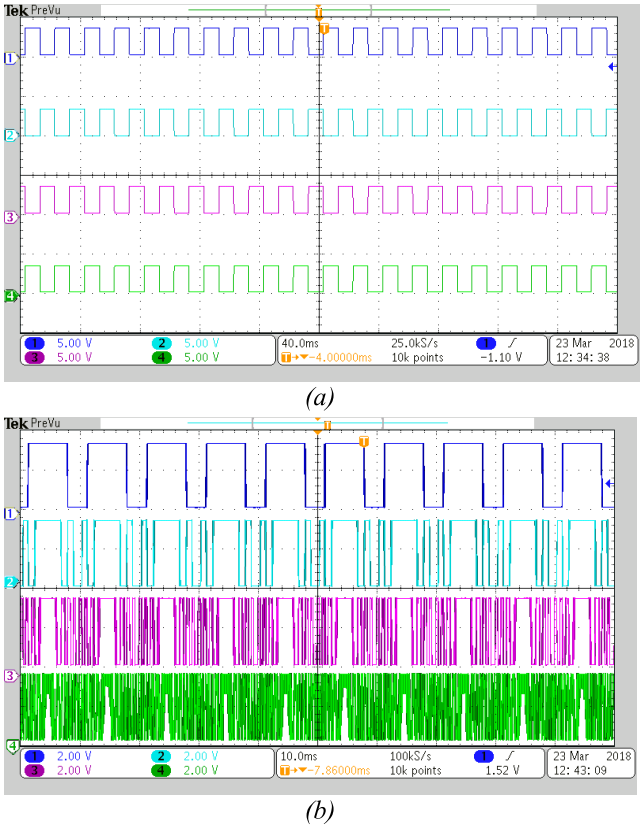


FIGURE 18. PWM pulses (a) full bridge converter and (b) diode connected switches.

The PWM pulses given to the switches of MLI are shown in Fig. 18(a) and (b). From the experimental results, it is evident that the proposed novel topology is succeeded in extracting maximum solar power from the PV panel using novel MPPT scheme based on shading pattern identification using artificial neural network. At the same time, multi level inverter produced thirty one levels in the output voltage and current, which resembles sinusoidal waveform and feeds the utility with low harmonic distortion.

VIII. CONCLUSION

This paper proposes a novel PV inverter topology for solar power generation. The proposed topology consists of a new MPPT scheme based on shading pattern identification using artificial neural network, dc-dc single input and multiple output power converter and a simple multi level inverter with the reduced number of switches. The proposed MPPT scheme is succeeded in harvesting maximum solar power in any weather conditions. The PV voltage is fed to SIMO converter, where PV voltage is segregated into four individual voltages with different magnitudes. Multilevel inverter accepts the four DC voltages as input and thereafter converts it into AC voltage with a minimum voltage and current harmonic distortion of 2.223% and 2.204%. From experimental results, it is clear that the proposed novel topology generates sinusoidal shaped voltage and current with thirty one levels and feeds the utility with unity power factor. It is worth to mention that the proposed topology extracts maximum power from PV array in any weather conditions and feed the utility at low cost.

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MURALIDHAR NAYAK BHUKYA (M'17) was born in India, in 1987. He received the B.Tech. degree in electrical and electronics engineering and the M.Tech. degree in power electronics from Jawaharlal Nehru Technological University, Hyderabad, India, in 2008 and 2013, respectively, and the Ph.D. degree in electrical and electronics engineering from Jawaharlal Nehru Technological University, Kakinada. His research interests include control systems, special machines, and application of power electronics in renewable energy systems.

VENKATA REDDY KOTA (M'12–SM'16) was born in India, in 1980. He received the bachelor's degree in electrical and electronics engineering and the master's degree in power and industrial drives from the JNTU College of Anantapur, India, in 2002 and 2004, respectively, and the Ph.D. degree in electrical engineering from Jawaharlal Nehru Technological University, Kakinada, India, in 2012.

He has more than 13 years of experience in teaching and research. He is currently an Assistant Professor with the Department of Electrical and Electronics Engineering, Jawaharlal Nehru Technological University, Kakinada, India. He is working on the control of special machines, FACTS, and power quality. His major field of study includes special electrical machines, electric drives, and power quality.

Dr. Kota is a Senior Member of the Institution of Engineers, India, and the Indian Society for Technical Education. He was a recipient of the Young Engineers Award, in 2013, and the Tata Rao Prize from the Institution of Engineers, India, in 2012.

SHOBHA RANI DEPURU (M'15) received the B.E. degree in electrical and electronics engineering from Jawaharlal Nehru Technology University, Hyderabad, and the M.Tech. degree in power system and the Ph.D. degree from Sri Venkateswara University, Tirupathi, India. She is currently a Professor with the Department of Electrical and Electronics Engineering, Institute of Aeronautical Engineering, Hyderabad, India. Her research interests include control systems and application of power systems, and power electronics.