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A Novel Transformerless Current Source Inverter for Leakage Current Reduction

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ABSTRACT High-frequency common mode voltage elimination is one of the most important issues for transformerless PV grid-connected inverters. Many interesting single-phase inverter topologies have been reported to reduce the common mode voltage. However, most of them are voltage-source inverters, which suffer from a limited lifetime and reliability. In order to solve the problem, a new single-phase six-switch current source inverter is proposed. A one-dimensional space vector modulation strategy is also presented so as to eliminate the high-frequency common mode voltage. The proposed topology yields lower total harmonic distortion (THD). The experimental results reveal that the maximum value of leakage current can be significantly reduced from 1.3A to 0.14 A with the proposed solution. And, the RMS value of leakage current for the proposed solution is 28.1 mA, which complies with VDE-0126-1-1 standard. In this paper, the theoretical analysis and experimental evaluation tests are carried out to verify the effectiveness of the proposed solution.

INDEX TERMS Grid-connected inverter, transformerless PV system, common mode voltage, leakage current.

I. INTRODUCTION

Power converters are the mandatory interface between PV and grid [1]–[4]. Typically, solar energy can be harvested by a grid-connected PV inverter with or without the transformer. Basically, the transformer is heavy, bulky, costly, and suffers from the power loss. In recent years, the transformerless PV inverters have been increasing attractive due to its low cost and high efficiency, compared with the transformer ones [5]–[7]. However, there are technical challenges to deal with before connecting them into grid. One of the technical issues is to eliminate the high-frequency common mode voltage and reduce the leakage current, which is mainly due to the lack of galvanic isolation [8]–[10]. The leakage current has the adverse impact on the grid current, potential human safety and the EMI problems. Therefore, the VDE 0126-1-1 specifies that the PV systems must be disconnected from the grid on the condition that the leakage current is beyond 300 mA. In order to cope with this problem, many interesting single-phase topologies, such as H5, oH5, H6 and Heric, have been presented in literature [11]–[14]. The basic objective is to achieve both the unipolar voltage pulse and effective leakage current reduction [5]. However, most of them are designed from the viewpoint of voltage source inverters. In these cases, an electrolytic capacitor is typically used, but it is more prone to failure and degrades the whole system's lifetime [15]. Critical stressors of the dc link capacitor that may compromise its reliability include temperature, vibration, and humidity. Since the dc bus capacitor of a voltage source inverter is substituted by an inductor in a current source inverter, the issues presented above are significantly reduced since the inductor is mechanically more robust and can be designed to withstand high temperatures [16]–[19]. In addition, there is a potential risk of overcurrent due to the phase-leg short circuit, which reduces the system reliability [20], [21]. On the contrary, the current source inverters have the inherent current limiting capability and thus enhance the reliability [22], [23]. In fact, the current source inverters have been used for the PV systems in the last decades [24]–[28]. However, the conventional

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single-phase four-switch current source inverter suffers from the high leakage currents, mainly due to the high-frequency common mode voltages. Therefore, the undesired feature restricts its application to the single-phase transformerless PV systems. In order to reduce the common mode voltage, a novel modulation strategy has been reported in [29], and a four-leg current source inverter is presented in [30] for three-phase inverter. A recent advancement for the current source inverter is presented in [31]. However, it is only done in the stand-alone mode. And the leakage current reduction capability in grid-connected mode is unclear. Therefore, the new current source inverter needs further investigation.

The objective of this paper is to present a new single-phase six-switch current source inverter. Only two additional switches are installed in dc side, the high-frequency common mode voltage can be effectively eliminated with a novel space vector modulation. The theoretical analysis and experimental verification are presented. The performance comparison with the conventional four-switch and CH5 topologies is also provided to highlight the advantages of the proposed topology.

II. PROPOSED SOLUTION

The schematic diagram of the conventional and proposed current source inverters is illustrated in Fig. 1. Note that the additional switches S_5 and S_6 have another interesting function to avoid overvoltage. If the overvoltage is detected, the switches S_5 and S_6 will be turned on until the fault is clear. In this way, there are the freewheeling paths for the continuous dc-link inductor current. Therefore, there is no risk of open-circuit at dc side and the overvoltage can be avoided.

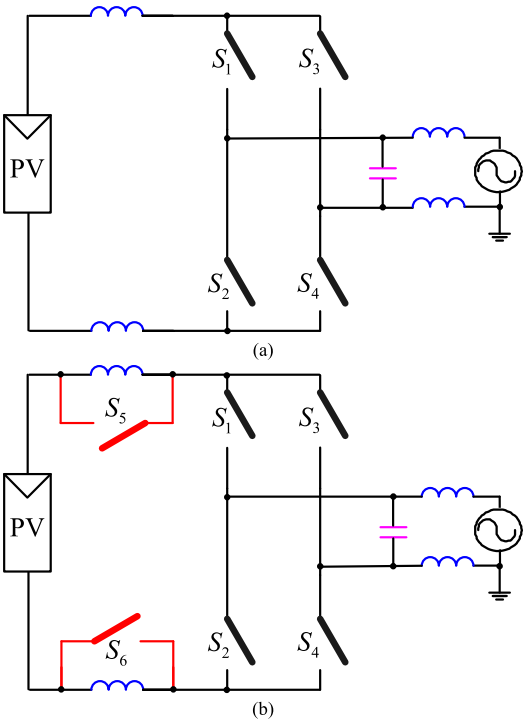

FIGURE 1. Schematic diagram. (a) Conventional current source four-switch inverter. (b) Proposed current source six-switch inverter.

A. CONVENTIONAL INVERTER

In order to clarify the operation mechanism of the current source inverter, the detailed schematic diagram is shown in Fig. 2, where I_{dc} is the dc-link current, L_{dc1} and L_{dc2} are the DC side inductors, C_{PV} is the parasitic capacitance between the PV panel and ground, the value of the parasitic capacitance depends on factors such as the external environment, the size and structure of the photovoltaic panel. In this paper, it is assumed that the parasitic capacitances of the positive and negative terminals of the photovoltaic panel that relative to ground are equal. S_1-S_4 are the switches, V_g is the voltage of grid, C_f and L_f are filter capacitor and filter inductor, respectively. If the parasitic capacitance exists between the PV panel and ground, the leakage current will arise since the common mode voltage is time-varying. Therefore, the high-frequency common mode voltage should be eliminated. It should be noted that the frequency range of the leakage current is around the switching frequency, which is 10 kHz in the paper. And the other common-mode capacitances are small in this range and thus ignored.

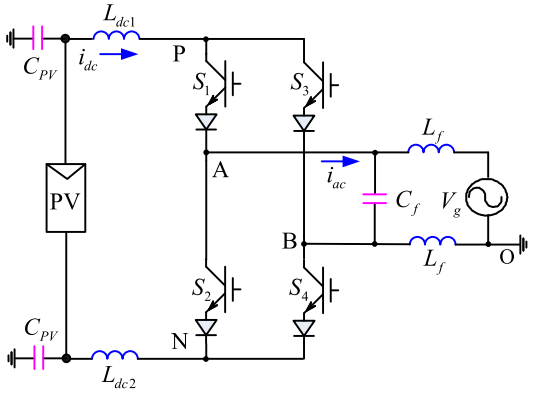

FIGURE 2. Conventional single-phase current source inverter.

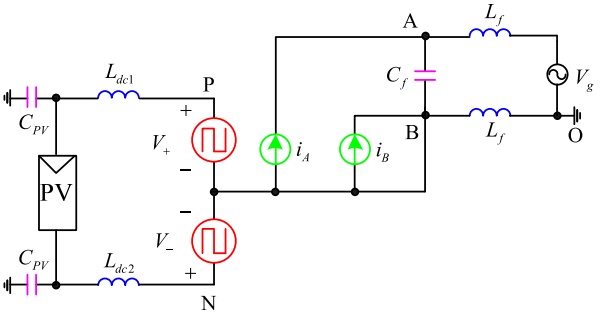

FIGURE 3. Equivalent circuit diagram of single-phase current source inverter.

In order to analyze the common mode voltage, the equivalent circuit diagram of single-phase current source inverter is established as shown in Fig. 3. Since the leakage current is mainly affected by the high frequency component of the common mode voltage, the filter capacitor can be regarded as short circuit. For simplicity, the simplified equivalent circuit is obtained as shown in Fig.4 after ignoring the effects of filter

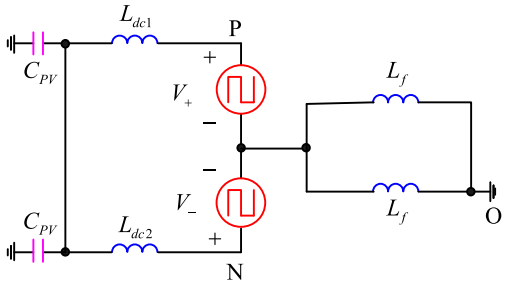

FIGURE 4. Simplified equivalent circuit diagram.

capacitor and power supplies. The voltage V_+ and V_- can be expressed as follows,

$$V_+ = \begin{bmatrix} S_1 & S_3 \end{bmatrix} \begin{bmatrix} V_A \\ V_B \end{bmatrix} \tag{1}$$

$$V_- = \begin{bmatrix} S_2 & S_4 \end{bmatrix} \begin{bmatrix} V_A \\ V_B \end{bmatrix} \tag{2}$$

where, V_A represents the voltage between point A and ground, V_B represents the voltage between point B and ground.

The current i_A and i_B can be expressed as follows,

$$i_A = S_1 i_{dc} - S_2 i_{dc} \tag{3}$$

$$i_B = S_3 i_{dc} - S_4 i_{dc} \tag{4}$$

where

$$S_i = \begin{cases} 1 & \text{when ON} \\ 0 & \text{when OFF} \quad (i = 1,\ 2,\ 3,\ 4) \end{cases} \tag{5}$$

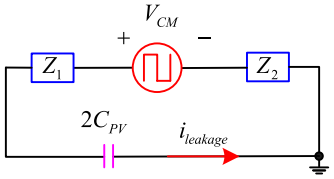

FIGURE 5. Simplified common mode model.

The common mode model as shown in Fig. 5 can be derived from Fig. 4. The common mode voltage V_{CM}, impedance Z_1 and Z_2 are expressed as

$$V_{CM} = \frac{L_{dc2}V_+ + L_{dc1}V_-}{L_{dc1} + L_{dc2}} = \frac{V_+ + V_-}{2} + \frac{(L_{dc2} - L_{dc1})(V_+ - V_-)}{2(L_{dc1} + L_{dc2})} \tag{6}$$

$$Z_1 = \frac{sL_{dc1}L_{dc2}}{L_{dc1} + L_{dc2}} \tag{7}$$

$$Z_2 = sL_f/2 \tag{8}$$

As described in (6), the common mode voltage depends not only on the voltage V_+ and V_- but also on the DC side inductances. Suppose L_{dc1} and L_{dc2} have an equal value L_{dc}, then the common mode voltage V_{CM} becomes

$$V_{CM} = \frac{V_+ + V_-}{2} \tag{9}$$

From Fig. 4 and (9), it can be concluded that the voltage V_+ is equal to V_{PO} and V_- is equal to V_{NO} when the voltage across the ac side filter inductor is ignored. For the sake of analysis, the common mode voltage is defined as

$$V_{\mathrm{CM}} = \frac{V_{PO} + V_{NO}}{2} \tag{10}$$

As is shown in Fig. 5, the leakage current $i_{leakage}$ can be defined as follows,

$$i_{leakage} = 2C_{PV}\frac{dV_{CPV}}{dt} \tag{11}$$

where V_{CPV} represents the voltage of C_{PV}. Assume that the transfer function between V_{CPV} and V_{CM} is,

$$V_{CPV} = G_0(s)\ V_{CM} \tag{12}$$

where,

$$G_0(s) = \frac{1}{2sC_{PV}(Z_1 + Z_2) + 1} \tag{13}$$

Therefore, the relationship between the leakage current $I_{leakage}$ and the common mode voltage V_{CM} is,

$$I_{leakage}(s) = G_1(s)V_{CM} \tag{14}$$

where,

$$G_1(s) = \frac{2sC_{PV}}{2sC_{PV}(Z_1 + Z_2) + 1} \tag{15}$$

It can be observed from (11) to (15) that the leakage current is related to the impedance of the common mode loop and the rate of change of the common mode voltage. It can be seen from Fig. 2 to Fig. 5 that the leakage current has an adverse effect on the grid current. The more serious the leakage current is, the greater the impact on the grid current. And the total harmonic distortion (THD) of the grid current will also increase. This will be verified in the experimental section. Therefore, the leakage current should be reduced by increasing the impedance of the common mode loop, or can be reduced by decreasing the rate of change of the common mode voltage.

Using the concept developed in [24], the current vector of the conventional single-phase current source inverter can be derived. The current vectors, switching states and its corresponding common mode voltage of the traditional single-phase current source inverter are listed in Table 1, where $\vec{I}_1 = I_{dc}\angle 0°$, $\vec{I}_2 = 0$, $\vec{I}_3 = I_{dc}\angle 180°$, $\vec{I}_4 = 0$. The current vectors schematic diagram is shown as Fig. 6, where $\vec{I}_{ref}$ is the reference current vector. In the positive half cycle, the common mode voltage varies from 0.5 V_g to V_g since the vector I_1 and I_2 are adopted. In the negative half cycle, the common mode voltage varies from 0 to V_g since the vector I_3 and I_4 are adopted.

TABLE 1. Switching states, space vectors, and CMV.

Vector	Switching states				CMV
	S_1	S_2	S_3	S_4	V_{CM}
I_1	1	0	0	1	$0.5V_g$
I_2	1	1	0	0	V_g
I_3	0	1	1	0	$0.5V_g$
I_4	0	0	1	1	0

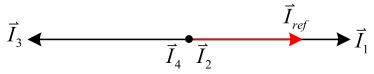

FIGURE 6. Current vectors schematic diagram.

It can be observed that the common mode voltage V_{CM} is time-varying in a high-frequency manner. And the leakage current is related to V_{CM}, as shown in (14). Therefore, the leakage current is high and not able to be reduced by the conventional solution.

B. PROPOSED INVERTER

As indicated by (11) to (15) and Fig. 5, the leakage current is related to the rate of change of the common-mode voltage V_{CM}. Therefore, the leakage current can be significantly reduced if the rate of change of the common-mode voltage is small, that is, eliminating the high-frequency components of common-mode voltage is an effective way for the leakage current reduction.

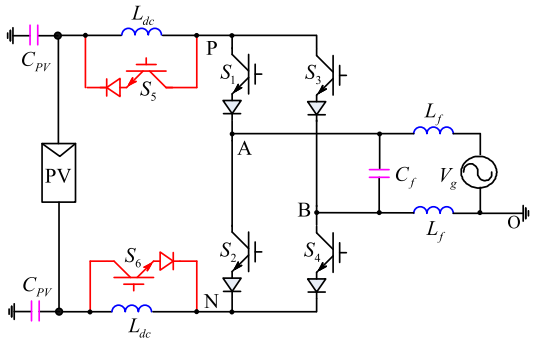

FIGURE 7. Proposed single-phase current source inverter.

In order to eliminate the undesirable high-frequency common mode voltage, a new current source inverter is proposed, as shown in Fig. 7. Two additional switches are connected in parallel with the DC side inductances. In the zero state, switches S_5 and S_6 are turned on for freewheeling of the inductances.

In the same time, a space vector modulation method capable of reducing common mode voltage variation is proposed in this paper. There are three operation modes of the proposed method over a period of grid voltage for the proposed modulation method. In the positive half cycle, the vectors, I_1 (when S_1 and S_4 are on) and I_5 (when S_5 and S_6 are on), are used to synthesize the reference current vector. The current path in the inverter is illustrated in Fig. 8 (a). When S_1 and S_4 are on, $V_{PO} = V_{AO}$, $V_{NO} = V_{BO}$. The common mode voltage is

$$V_{CM} = \frac{V_{PO} + V_{NO}}{2} = \frac{V_{AO} + V_{BO}}{2} = \frac{V_g}{2} \tag{16}$$

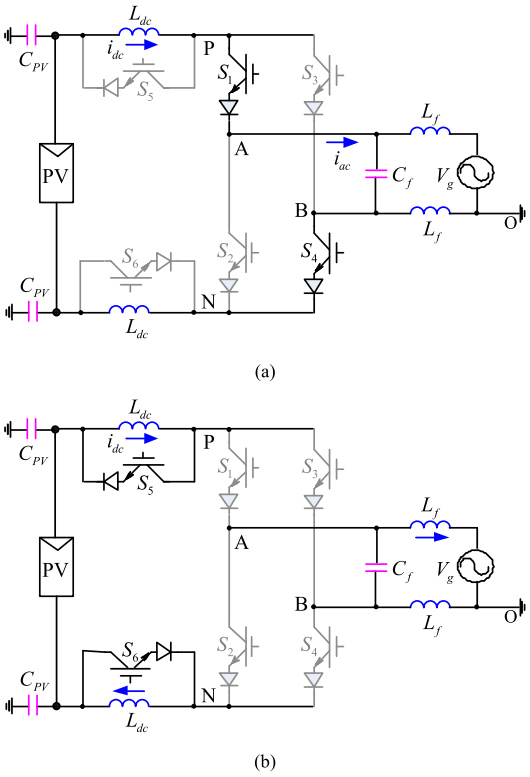

FIGURE 8. Operation modes of proposed inverter in the positive half cycle. (a) Active mode for positive half cycle (b) freewheeling mode for positive half cycle and negative half cycle.

When S_5 and S_6 are on, the circuit works in the freewheeling state as shown in Fig. 8 (b). It can be observed that the DC side inductances are freewheeling through switches, S_5 and S_6. The common mode voltage in this mode is

$$V_{CM} = \frac{V_{PO} + V_{NO}}{2} = \frac{V_g}{2} \tag{17}$$

In the negative half cycle, the vectors, I_3 (when S_2 and S_3 are on) and I_5 (when S_5 and S_6 are on), are adopted. The freewheeling state of the negative half cycle is the same as that of the positive half cycle shown in Fig. 8 (b). The active mode in the negative half cycle is shown in Fig. 9. When S_2 and S_3 are on, $V_{PO} = V_{BO}$, $V_{NO} = V_{AO}$. The common mode voltage is still $V_g/2$ as calculated by (16).

$$V_{CM} = \frac{V_{PO} + V_{NO}}{2} = \frac{V_{AO} + V_{BO}}{2} = \frac{V_g}{2} \tag{18}$$

The pulse pattern arrangement of the proposed space vector modulation is I_1 - I_5 - I_5 - I_1 in the positive half cycle, while I_3 - I_5 - I_5 - I_3 in the negative half cycle. The dwell times of I_1, I_3 and I_5 can be calculated by ampere-second balance principle.

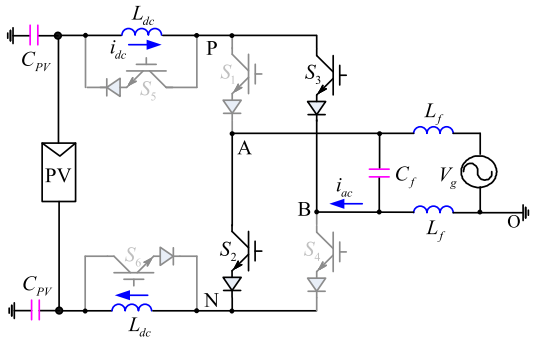

FIGURE 9. Active mode of proposed inverter in the negative half cycle.

According to the above analysis, the switching states, space vectors and common mode voltage (CMV) of the proposed single-phase current source inverter are shown in Table 2.

TABLE 2. Switching states, space vectors, and CMV.

Vector	Switching states						CMV
	S_1	S_2	S_3	S_4	S_5	S_6	V_{CM}
I_1	1	0	0	1	0	0	$0.5V_g$
I_3	0	1	1	0	0	0	$0.5V_g$
I_5	0	0	0	0	1	1	$0.5V_g$

From Table 2, it can be observed that if the three vectors of I_1, I_3 and I_5 are used, the common mode voltage is kept at half of the grid voltage. Note that the frequency of grid voltage V_g is much lower than the switching frequency, so the effect of low-frequency grid voltage on the high-frequency common mode behavior can be neglected. Compared with the conventional single-phase four-switch current source inverter, the proposed topology and modulation method have an additional degree-of-freedom for eliminating the high-frequency common mode voltage. Therefore, the leakage current can be significantly reduced, as expected by (11) to (15) and Fig. 5. It is worth noting that the leakage current cannot be completely eliminated in practice due to the junction capacitances of the switches and the differences of the passive components of the circuit, but the current source inverter topology and the corresponding modulation method proposed in this paper can effectively reduce leakage current compared with the traditional single-phase current source inverter.

TABLE 3. Action vector and operation time.

Parameters	Action vector	Dwell time
In the positive half cycle	I_1 (when S_1 and S_4 are on)	$T_1 = T_s \cdot m \cdot \sin\theta$
	I_5 (when S_5 and S_6 are on)	$T_5 = T_s - T$
In the negative half cycle	I_3 (when S_2 and S_3 are on)	$T_3 = T_s \cdot m \cdot \sin(\theta - \pi)$
	I_5 (when S_5 and S_6 are on)	$T_5 = T_s - T_3$

The information listed in Table 3 is the action vector and its corresponding vector operation time in one fundamental period. T_s represents the switching period, T_i represents the operation time of I_i ($i = 1, 3, 5$), m represents the modulation index and θ represents the vector angle. Another consideration that should be noted is how to control grid current by taking the resonance into account. In order to solve the problem, the passive damping is adopted in this paper, as shown in Fig. 10. The zero-crossing detection is used for grid synchronization and obtaining the phase of the reference current so that the grid current is in phase with the grid voltage. Then the error of the grid current is adjusted by the PR regulator with zero steady-state error. Finally, the pulse modulation signals of the switches are obtained by the distribution of the current vectors.

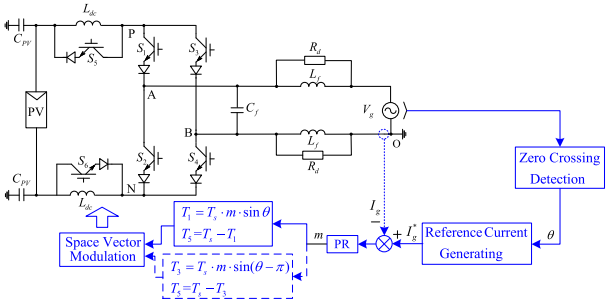

FIGURE 10. Proposed control structure.

The mathematical model for the control structure is shown in Fig.11, where K is the PWM gain, $G(s)$ is the current controller, R_d is the damping resistor.

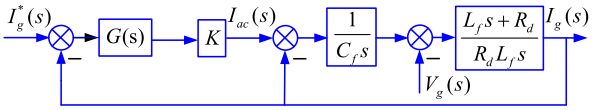

FIGURE 11. Mathematical model for the control structure.

Equation (19) shows that the instability will occur without any damping control. With the proposed solution in Fig. 10 and Fig .11, the transfer function can be rewritten as (20).

$$F(s) = \frac{I_g(s)}{I_{ac}(s)} = \frac{1}{L_f C_f s^2 + 1} \tag{19}$$

$$F_{pd}(s) = \frac{L_g(s)}{I_{ac}(s)} = \frac{L_f s + R_d}{R_d L_f C_f s^2 + L_f s + R_d} \tag{20}$$

It can be observed that the denominator of issue (20) has positive coefficient if R_d is not equal to zero. Based on the Routh-Hurwitz criterion, the stability can be ensured if the damping resistor R_d is chosen reasonably. So the stability is enhanced with the proposed approach. The next section will present the verification of the proposal.

III. SIMULATION RESULTS

In order to verify the effectiveness of the proposed solution, the performance test of both conventional single-phase four-switch and proposed six-switch current source inverters are

carried out. The system parameters are listed below. The system power rating is 500 W, grid voltage is 120V/50Hz, dc-link current is 10 A, dc-link inductance (L_{dc}) is 5 mH, switching frequency is 10 kHz, filter capacitor (C_f) is 9.4 μF, filter inductor (L_f) is 2.5 mH. The simulation results are shown as follows.

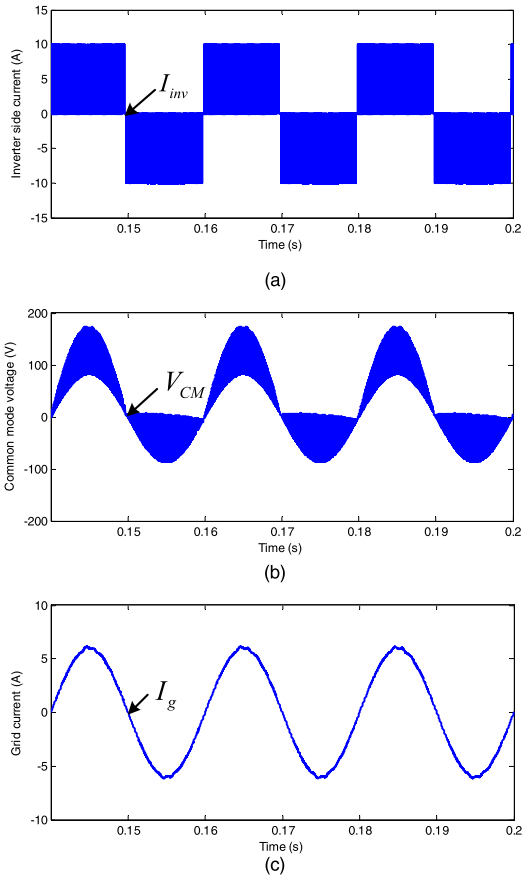

FIGURE 12. Simulation results of conventional single-phase four-switch current source inverter. (a) Inverter-side current. (b) Common mode voltage. (c) Grid current.

First of all, the conventional passive damping is used for both inverters. From Fig. 12, it can be observed that in case of conventional single-phase current source inverter, the common mode voltage is time-varying in a high-frequency way. As shown in Fig. 12 (b), the common mode voltage varies from $V_g/2$ to V_g in the positive half cycle while it varies from 0 to $V_g/2$ in the negative half cycle, which is consistent with the common mode voltage listed in Table 1.

Fig. 13 shows the simulation results of the proposed inverter, it can be observed that the value of the common mode voltage is always the half of the grid voltage ($V_g/2$). The leakage current is mainly caused by high frequency components of the common mode voltage, so the frequency of grid voltage can be ignored. In this way, the proposal eliminates the high-frequency common mode voltage, and the leakage current can be significantly suppressed. The experimental verification will be carry out in the next section.

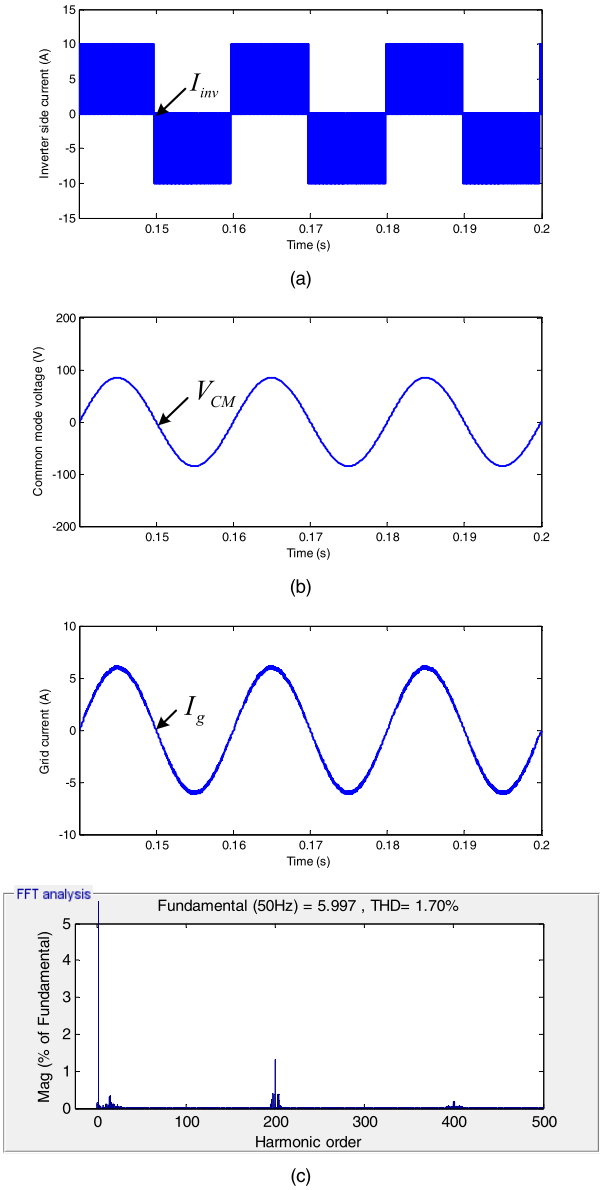

FIGURE 13. Simulation results of proposed single-phase current source inverter. (a) Inverter-side current. (b) Common mode voltage. (c) Grid current and its spectrum.

IV. EXPERIMENTAL RESULTS

The experimental setup has been built in the lab. The control is implemented with TMS320F28335 DSP and Xilinx XC6SLX9 FPGA. The system parameters are listed in Table 4. The experimental results are shown as follows.

Fig. 14 shows the experimental results of the conventional single-phase four-switch inverter. Note that passive damping control strategy is adopted in all the inverter topologies mentioned in this paper. As shown in Fig. 14(a), it can be observed that the grid voltage V_g and the grid current I_g are in the same phase. And the unipolar current pulse can be achieved. The grid current THD (Total Harmonic Distortion) of the conventional single-phase four-switch inverter is 7.27%. The waveforms of the voltage V_{PO}, the voltage V_{NO}, the common

TABLE 4. Experimental parameters.

Parameters	Value
Rated power	720 W
Grid voltage	120 V (RMS) / 50 Hz
Grid current	6 A
DC link current	8 A
DC link inductance (L_{dc})	5 mH
Switching frequency	10 kHz
filter capacitor (C_f)	9.4 μF
filter inductor (L_f)	2.5 mH
Parasitic capacitance (C_{PV})	75 nF

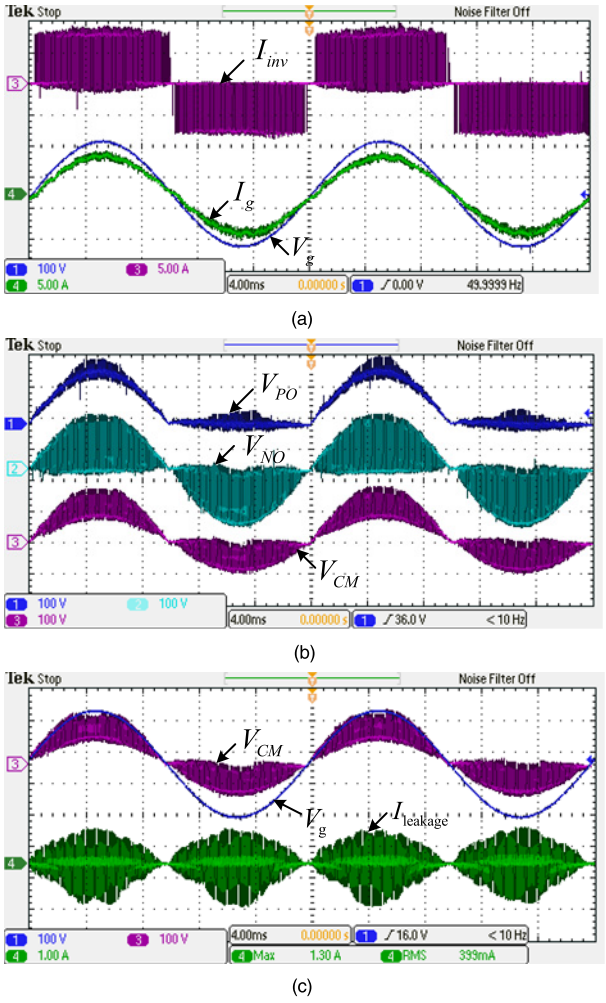

FIGURE 14. Experimental results of the conventional single-phase four-switch inverter. (a) Grid voltage V_g, grid current I_g, and the current of inverter side I_{inv}. (b) Common mode voltage V_{CM}, the voltage V_{PO}, and the voltage V_{NO}. (c) Common mode voltage V_{CM}, the grid voltage V_g, and the leakage current $I_{leakage}$.

mode voltage V_{CM} and the leakage current $I_{leakage}$ for the conventional single-phase four-switch inverter are shown in Fig. 14(b) and Fig. 14(c). The maximum and RMS values of leakage current for the conventional single-phase four-switch are 1.3 A, and 399 mA, respectively. The high frequency variation of common mode voltage results in large leakage current for the conventional single-phase four-switch inverter topology.

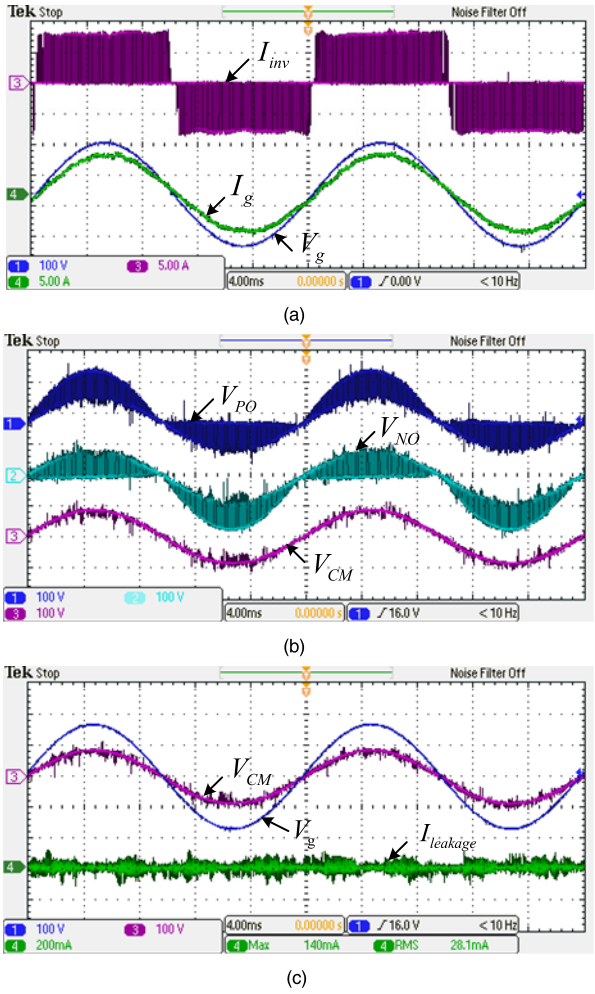

FIGURE 15. Experimental results of the proposed six-switch current source inverter. (a) Grid voltage V_g, grid current I_g, and the current of inverter side I_{inv}. (b) Common mode voltage V_{CM}, the voltage V_{PO}, and the voltage V_{NO}. (c) Common mode voltage V_{CM}, the grid voltage V_g, and the leakage current $I_{leakage}$.

Fig. 15 shows the experimental results of the proposed six-switch current source inverter. For the proposed six-switch current source inverter, the common mode voltage is always half of grid voltage. The grid current THD of the proposed six-switch current source inverter is 3.77%. The proposed topology yields lower THD. And the grid current THD of the proposed inverter meets the IEEE 519-2014 standard [32]. The maximum and RMS values of leakage current for the proposed six-switch current source inverter are 140 mA and 28.1 mA, respectively. The leakage current for the proposed topology is far less than the conventional topology, which complies with VDE-0126-1-1 standard. The experimental

results confirm that the proposed topology is able to achieve the significant reduction of the leakage current.

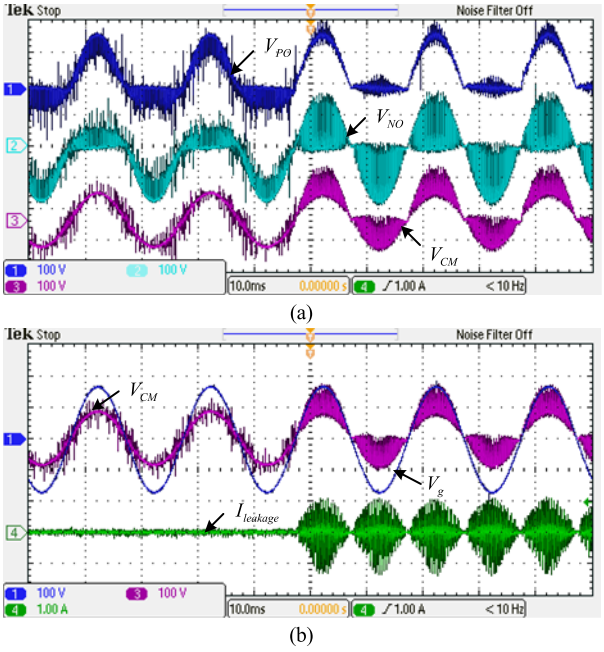

FIGURE 16. Dynamic test results in experimental. (a) Common mode voltage V_{CM}, the voltage V_{PO}, and the voltage V_{NO}. (b) Common mode voltage V_{CM}, the grid voltage V_g, and the leakage current $I_{leakage}$.

Fig. 16 shows the dynamic experimental results of the proposed solution. From 0 to 50ms, the switches, S_5 and S_6, are enabled. The tested circuit operates as a proposed single-phase six-switch current source inverter. From 50ms to 100ms, the switches, S_5 and S_6, are disabled. It operates as a conventional single-phase four-switch current source inverter. From Fig. 16, It can be observed that, compared with the conventional single-phase four-switch current source inverter, the proposed single-phase six-switch current source inverter and its modulation strategy are able to suppress leakage current effectively, which verifies the effectiveness of the proposal.

In order to compare the proposal with the recent advancement in [31], the further experimental test of CH5 inverter is carried out. The experimental results of CH5 inverter when it is connected to the grid is shown in Fig. 17. The grid current THD of the CH5 inverter is 5.3%. It can be observed that the high frequency component of the common mode voltage of the CH5 inverter is higher than the proposed inverter in this paper. The maximum and RMS values of leakage current for the CH5 inverter are 276 mA and 47.7 mA, which are both larger than that of the proposed inverter in this paper.

The above experimental results illustrate the effectiveness of the proposed method. The leakage currents of different inverters are listed in Table 5. It can be clearly seen from Table 5 that the method proposed in this paper has the best ability to suppress leakage current.

TABLE 5. Comparison of leakage currents for different inverters.

Leakage current	Conventional four-switch inverter	Five-switch inverter	Proposed six-switch inverter
Maximum	1.3A	276 mA	140 mA
RMS	399mA	47.7 mA	28.1 mA

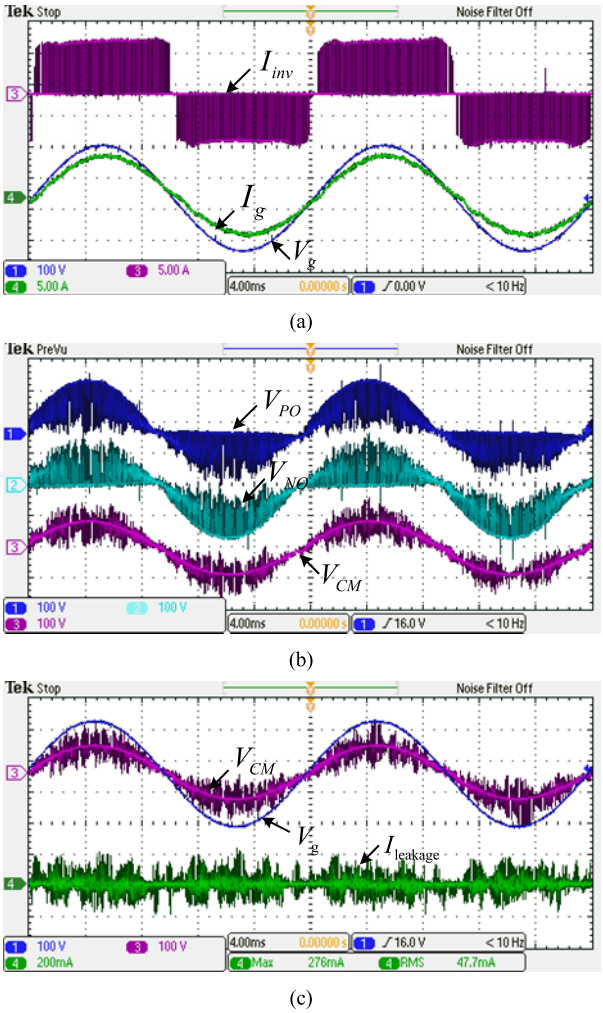

FIGURE 17. Experimental results of the CH5 inverter. (a) Grid voltage V_g, grid current I_g, and the current of inverter side I_{inv}. (b) Common mode voltage V_{CM}, the voltage V_{PO}, and the voltage V_{NO}. (c) Common mode voltage V_{CM}, the grid voltage V_g, and the leakage current $I_{leakage}$.

V. CONCLUSION

This paper has presented a novel single-phase six-switch current source inverter. Also, a new space vector modulation is presented for proposed six-switch current source inverter. Theoretical analysis and performance test results show that the conventional single-phase four-switch current source inverter suffers from high-frequency common mode voltage and larger leakage current. Compared with the conventional single-phase four-switch and five-switch current source inverter, the proposal is able to eliminate the

high-frequency common mode voltage. Therefore, the leakage current can be suppressed effectively. The maximum and RMS values of leakage current for the proposed six-switch current source inverter are 140 mA and 28.1 mA, which complies with VDE-0126-1-1 standard [33]. The new single-phase six-switch current source inverter tends to be more attractive for transformerless PV system.

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