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A PVT-Robust Analog Baseband With DC Offset Cancellation for FMCW Automotive Radar

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ABSTRACT This paper presents a process-voltage-temperature (PVT)-robust analog baseband with DC offset cancellation (DCOC) for automotive radar applications. The baseband is composed of three stages of programmable gain amplifier (PGA) and an embedded fifth-order Butterworth filter. A novel embedded G_m-cell based DCOC feedback loop is proposed to achieve fine DC offset rejection and a low high-pass the cut-off frequency with an economic chip area. The proposed embedded G_m-cell based DCOC feedback topology is capable of improving gain error and loop stability simultaneously. Besides, a constant overdrive biasing technique is proposed to strengthen PVT robustness. Implemented in 65-nm CMOS technology, the measured results show that the analog baseband can provide a programmable gain range from 18.2 to 70.6 dB with 5.8 dB per step with a gain error of <0.2 dB, while the 1-dB bandwidth range is from 200 kHz to 10 MHz. An OIP3 of 7.8 dBm and an input referred noise (IRN) of 15.8 nV/$\sqrt{}$Hz are obtained. The gain deviation is lower than 2.2 dB across all PVT corners. The core circuit consumes a dc power of 6 mW from a 1.2-V supply and occupies a chip area of 0.1 mm^2.

INDEX TERMS Analog baseband, automotive radar, DC offset cancellation (DCOC), filter, process-voltage-temperature (PVT)-robust, programmable gain amplifier (PGA).

I. INTRODUCTION

In recent years, automotive millimeter-wave (mm-wave) radars develop rapidly due to their low cost and robustness under harsh weather conditions [1]. Radars based on frequency-modulated continuous-wave (FMCW) technique can achieve large distance range and precise velocity simultaneously [2]. State-of-the-art mm-wave FMCW radar transceivers have been presented in literature [1]–[4].

The received power of automotive radar is inversely proportional to the fourth power of the distance [5]. To accommodate the wide power range, the dynamic range of the receiver should be sufficiently large, which is achieved by programmable gain amplifiers (PGA). A common specification of PGA is accurate dB-linear characteristic, which can be obtained by several techniques. The pseudo-exponential function approximation is a typical one [6]–[8]. This method provides an accurate gain control at a small gain range. In order to obtain a large gain range, multi-stages can be cascaded, however, coming up with gain error accumulation and apparent bandwidth dropping. Current steering PGA is another solution [9]–[11], however, noise on the control word is directly coupled to the output. Besides, the linearity is degraded due to square-law MOS device characteristic and the DC operating point also varies with gain settings. Transconductance-based PGA is also proposed in recent years [12]. However, the gain is closely related to the absolute value of the transconductance and output impedance, therefore exhibiting poor process-voltage-temperature (PVT) robustness. Meanwhile, the intermediate frequency (IF) of FMCW radar is also closely related to distance and velocity, thus the cut-off bandwidth should be tunable at different application to reject out-off band noise effectively.

Besides, DC offset cancellation (DCOC) is necessary in mm-wave radar inherited from the direct conversion architecture. In priors arts, several DCOC techniques have been proposed, such as AC coupling [13]–[15], digital-assisted cancellation [16], [18], [19], sub-harmonic mixers [20]–[24], and feedback DCOC [28]. In FMCW radar, the high-pass cut-off frequency of DCOC should be sufficiently low to achieve precise measurement. Furthermore, AC coupling usually employs large resistors and capacitors which are

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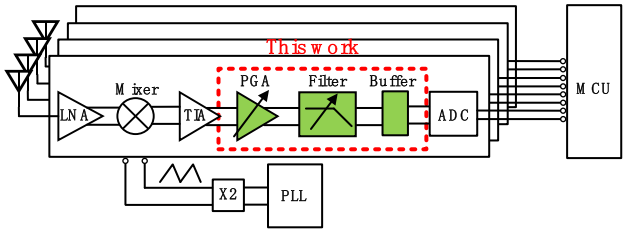

FIGURE 1. A multi-channel direct conversion mm-wave radar receiver.

inappropriate for monolithic integration. Meanwhile, the high-pass cut-off frequency of AC coupling is also related to the input impedance of the following stage, thus improper to embedded between amplifiers with low input impedance. Digital-assisted cancellation exhibits extremely low high-pass cut-off frequency, but extra quantizer and digital-to-analog converters (DAC) are required, while it also suffers from poor resolution. The feedback DCOC technique introduces feedforward path and load effect to the input which deteriorates the loop stability and the dB-linear characteristic of the PGA. Finally, since automotive radars typically work in serious environment, PVT robustness becomes more critical versus other applications.

In this paper, the proposed baseband is composed of three stages of programmable gain amplifier (PGA) and an embedded fifth-order Butterworth filter. The PGA is based on resistive feedback topology because of its natural PVT robustness [28]–[31], large gain range and fine linearity. Moreover, a novel embedded G_m-cell DCOC feedback loop is proposed to achieve fine DC offset performance with economic chip area. Meanwhile, the novel loop is capable of removing the load effect as well as feedforward path, and hence the dB-linear accuracy and loop stability is promoted. Finally, a constant overdrive biasing technique is also proposed to further improve the PVT robustness.

The paper is organized as follows. The architecture of the receiver and proposed analog baseband are explained in section II, while the circuit design techniques are discussed in section III. Section IV presents the measured results, and a conclusion is drawn in section V.

II. ARCHITECTURE OF THE RECEIVER AND ANALOG BASEBAND

A. RECEIVER ARCHITECTURE

Fig. 1 shows the block diagram of a multi-channel direct conversion mm-wave radar receiver. Multiple receiver channels are adopted to improve the angle resolution and to adapt different applications as well. The local oscillation (LO) signal is generated by a fractional-N phase-locked loop (PLL) frequency synthesizer and a frequency doubler. The received weak signal is firstly amplified by a low noise amplifier (LNA), and then subsequently mixed with the LO signal. A transimpedance amplifier (TIA) is introduced in front of the PGA to convert the current signal from the passive mixer to voltage signal. Due to even order nonlinearity and LO leakage, the output of mixer always contains large DC offset,

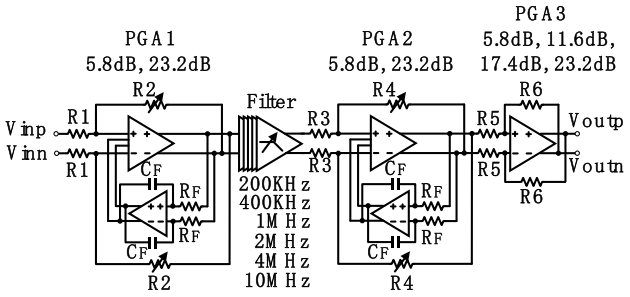

FIGURE 2. Architecture of the proposed analog baseband.

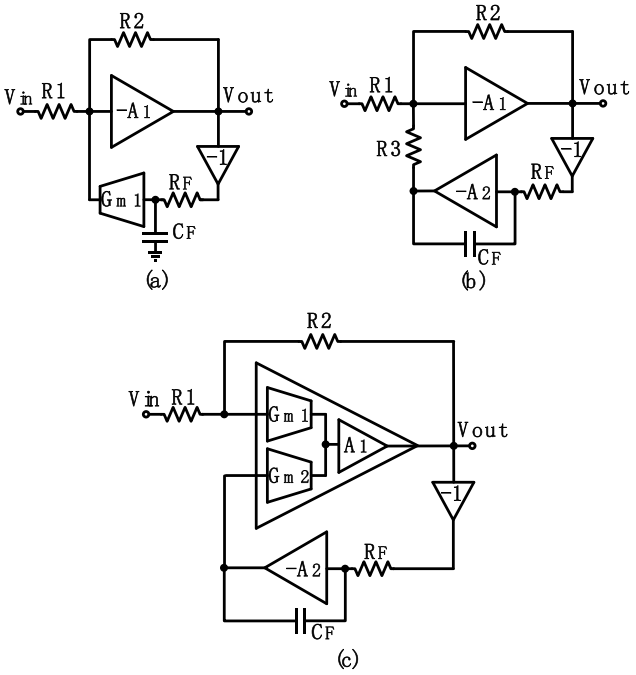

FIGURE 3. Negative feedback DCOC loop in resistive feedback PGA. (a) Basic topology. (b) Modified topology. (c) Proposed topology.

which will degrade the sensitivity and dynamic range or even saturate the following stages. Therefore, DCOC is indispensable in the analog baseband.

B. ANALOG BASEBAND ARCHITECTURE

Fig. 2 shows the architecture of the proposed baseband which is composed of a cascade of three PGA stages, an embedded fifth-order Butterworth filter and a buffer for measurement (not shown). The first and second PGA are both coarse gain adjustment (CGA) stage with only 5.8 dB step and 23.2 dB step, respectively, while the third PGA is a fine gain adjustment (FGA) stage with 5.8 dB, 11.6 dB, 17.4 dB, and 23.2 dB steps, respectively. The combination of these three PGAs achieves gain range from 17.4 dB to 69.6 dB with 5.8 dB per step, with 5 digital control bits. The proposed embedded G_m-cell based DCOC feedback loops are applied in the first and second PGA stages for cancellation of the DC offset.

The filter is embedded in the chain between the first and second stage PGA, rejecting out-of-band noise and interference introduced by RF frontend and the first stage PGA.

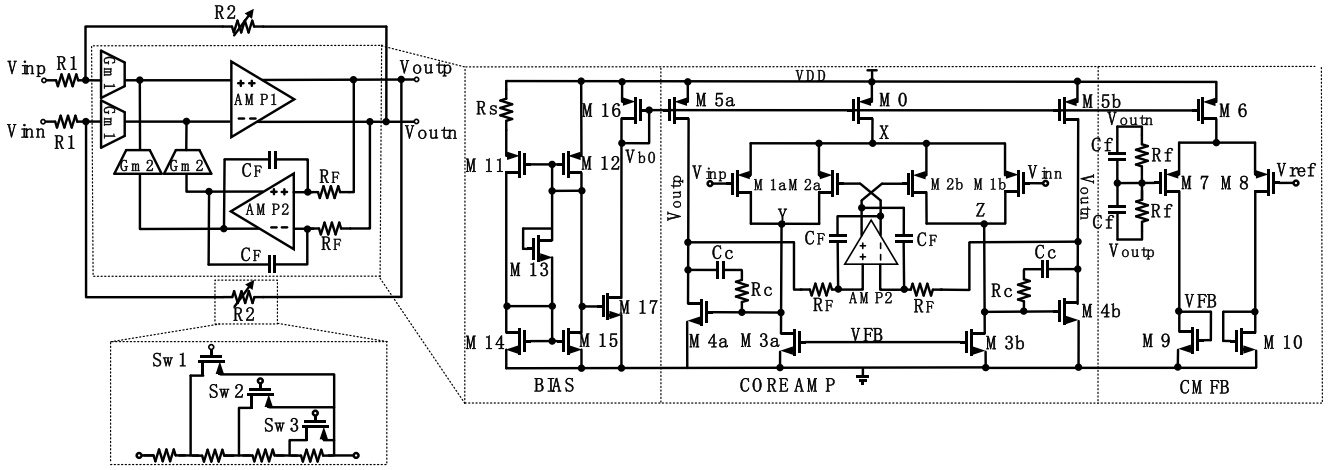

FIGURE 4. Implementation of the proposed PGA with DCOC.

The filter provides a sharp filtering property of −100 dB/dec as well as six bandwidth control steps, namely, 200 kHz, 400 kHz, 1 MHz, 2 MHz, 4 MHz and 10 MHz, respectively.

III. CIRCUIT DESIGN OF THE ANALOG BASEBAND

A. PGA AND DCOC LOOP

In the proposed baseband, the resistive feedback PGA is adopted due its natural PVT robustness. The most common approach to cancel DC offset in resistive feedback PGA is employing negative feedback DCOC loop [25]–[28]. The basic topology is showed in Fig. 3(a). The DC offset voltage is firstly extracted by the low pass filter consisted of R_F and C_F, and subsequently converted to current by G_{m2} to neutralize the DC offset. The high-pass cut-off frequency of the PGA can be described as

$$f_{HP1} = \frac{1 + R_2 G_{m1}}{2\pi C_F R_F} \tag{1}$$

Because $1 + R_2 G_{m1} > 1$, f_{HP1} is always larger than that of AC coupling which results in larger capacitor C_F and resistor R_F. Therefore, a modified topology is proposed as showed in Fig. 2(b) [28]. The high-pass cut-off frequency can be expressed approximately as

$$f_{HP2} = \frac{R_2}{2\pi C_F R_F R_3} \tag{2}$$

Equation (2) indicates that the high-pass cut-off frequency is lower than that of AC coupling if R_3 is larger than R_2. But larger R_3consumes a large chip area. Besides, R_3 introduces a feedforward path which deteriorates the loop stability, and the load effect at input node causes a large gain error.

To solve the above issues, an embedded G_m-cell based DCOC feedback loop is proposed as shown in Fig. 3(c). Firstly, a G_m-cell is used to convert DC offset voltage to current instead of resistors to save chip area. Secondly, the G_m-cell achieved by MOSFETs is completely embedded into core amplifier, thus load effect introduced by DCOC loop can be removed and the gain error would be promoted. Thirdly, the excellent reverse isolation of the G_m-cell will remove the feedforward path naturally, and hence promotes the loop stability. Finally, an appropriate proportion of G_{m1} and G_{m2} can be selected to reduce high-pass cut-off frequency as well as chip area, which will be explained in detail.

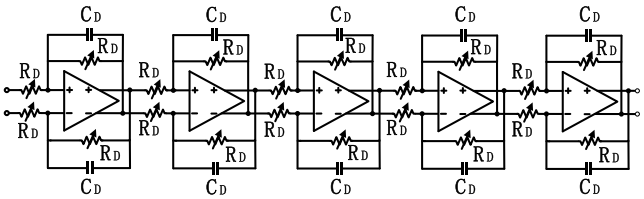

FIGURE 5. Implementation of the fifth-order Butterworth filter.

At the frequency near DC, the DC rejection ratio (DCRR) can be expressed as

$$A_{DCRR} = \frac{V_{out,DC}}{V_{in,DC}} \approx -\frac{G_{m1}}{G_{m1} + G_{m2}} \cdot \frac{R_2}{R_1 + R_2} \cdot \frac{1}{A_{v2}} \tag{3}$$

And the high-pass cut-off frequency can be described as

$$f_{HP3} \approx \frac{1}{2\pi} \cdot \frac{1}{C_F R_F} \cdot \frac{G_{m2}}{G_{m1}} \cdot \left(1 + \frac{R_2}{R_1}\right) \tag{4}$$

According to (3) and (4), a fine DCRR and a low high-pass cut-off frequency can be achieved simultaneously by increasing A_{v2} and decreasing G_{m2}. C_F and R_F can also be reduced to save chip area if G_{m2} is much smaller than G_{m1}. Therefore, the proposed embedded G_m-cell based DCOC feedback is capable of reducing high-pass cut-off frequency as well as chip area.

The implementation of the proposed PGA with DCOC is shown is Fig. 4. The two G_m-cells and AMP_1 are combined into a two stage Miller amplifier composed of $M_0 \sim M_5$, where M_1 and M_2 represent G_{m1} and G_{m2}, respectively. $M_6 \sim M_{10}$ compose a common-mode feedback (CMFB) network while $M_{11} \sim M_{17}$ and $R_S$provide a constant overdrive biasing to enhance the PVT robustness. The tunable resistor R_2 is achieved by a switch resistor array.

The transfer function of the first stage PGA can be derived as (5), as shown at the bottom of the next page, with one pole

and one zero, where $R_{out1} = r_{o1}//r_{o2}//r_{o3}$,$R_{out2} = r_{o4}//r_{o5}$, $r_{o1} \sim r_{o5}$ are the output resistance of $M_1 \sim M_5$ respectively, and $g_{m1} \sim g_{m4}$ are the transconductances of $M_1 \sim M_4$. From the analysis, DCRR and the high-pass cut-off frequency agree well with (3), (4). The transfer function of the second PGA is identical to that of the first stage. Since there is no DCOC loop in the third PGA, the transfer function can be simply expressed as

$$A_{PGA,3}(j\omega) \approx -\frac{R_6}{R_5} \tag{6}$$

where R_5 and R_6 are the feedback resistors of the third PGA.

B. FILTER

To satisfy a wide detection range and suppress out-of-band noise effectively, in this design, the cut-off frequency of the filter can be reconfigured over six levels, i.e. 200 kHz, 400 kHz, 1 MHz, 2 MHz, 4 MHz and 10 MHz, respectively.

Fig. 5 shows the architecture of the filter which is composed of five identical active RC filter stages. The transfer function of the filter can thus be described as

$$A_{filter}(j\omega) \approx -\frac{1}{(1+j\omega C_D R_D)^5} \tag{7}$$

where C_D and R_D are the feedback capacitance and resistor, respectively. The reconfigurable bandwidth can be achieved by tunable resistor realized by switched resistor array as that in the design of PGA. The complete transfer function of the analog baseband can thus be derived as

$$A_{BB}(j\omega) = A_{PGA,1}(j\omega) A_{PGA,2}(j\omega) A_{PGA,3}(j\omega) \frac{1}{(1+j\omega C_D R_D)^5} \tag{8}$$

The theoretical analysis of the analog baseband is compared with the post-layout simulated results as shown in Fig. 6. It can be seen that the theoretical analysis accurately estimates the performance of the analog baseband with little deviation, which is caused by three main reasons. Firstly, the above analysis assumes ideal gain and bandwidth of the amplifier. Secondly, the equivalent circuit model for the MOSFET is simplified. Thirdly, the layout parasitic is not involved in the theoretical analysis.

C. PVT ANALYSIS AND THE CONSTANT OVERDRIVE BIASING

Since the closed loop gain of the PGA and filter are both ratio quantity, as shown in (5), (6) and (7), they are naturally PVT robust if open loop gain is extremely large. In fact, it is difficult to realize high gain and wide bandwidth simultaneously. Therefore, when the open loop gain of the core amplifier varies with PVT corners, the closed loop gain changes

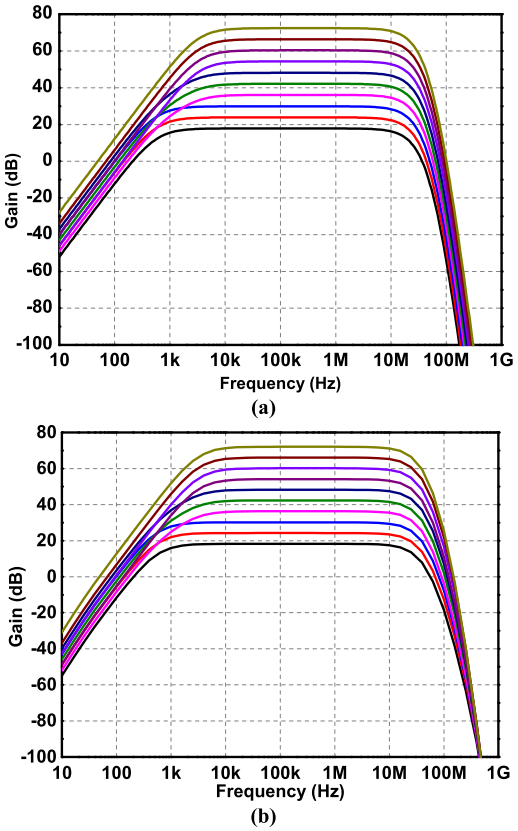

FIGURE 6. Frequency response of the analog baseband. (a) Theoretical analysis. (b) Post-layout simulated results.

slightly as well, which maybe more serious for multi-stages cascade. Instead of focusing on increasing the open loop gain, it is more critical to keep the open loop gain stable among PVT corners.

The open loop gain mainly depends on the intrinsic gain of MOSFET, which can be described as

$$g_m r_o \approx -\frac{2(1+\lambda V_{DS})}{(V_{GS}-V_{TH})\lambda} \tag{9}$$

where V_{GS}-V_{TH} is overdrive voltage, λ is the channel length modulation coefficient and V_{DS} is the drain-source voltage. λ is nearly temperature independent while V_{DS} is a constant with the help of CMFB network. Thus a constant overdrive voltage is mandatory to obtain the constant intrinsic gain.

Apparently, a constant voltage biasing could not meet the demand because V_{TH} is temperature dependent. A constant current biasing may induce an overdrive voltage as follow,

$$(V_{GS}-V_{TH}) \approx \sqrt{\frac{2I_D}{\mu C_{ox}\frac{W}{L}}} \tag{10}$$

$$A_{PGA,1}(j\omega) = \frac{-R_2 g_{m1} R_{out1} g_{m4} R_{out2} (2 - j\omega C_F R_F A_{v2})}{(R_1+R_2) g_{m2} R_{out1} g_{m4} R_{out2} A_{v2} + [R_1 + R_2 + R_1 g_{m1} R_{out1} g_{m4} R_{out2}](2 - j\omega C_F R_F A_{v2})} \tag{5}$$

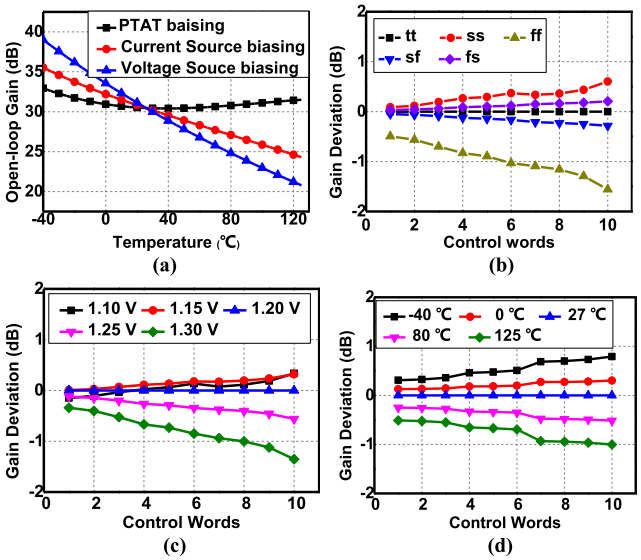

FIGURE 7. Simulated results. (a) Open-loop gain variation over different biasing. (b) Gain deviation over process corner. (c) Gain deviation over different supply voltage. (d) Gain deviation over temperature.

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area. However, since μ is temperature dependent, so is the overdrive voltage.

In this paper, a constant overdrive biasing technique is proposed, which is achieved by $M_{11} \sim M_{17}$ and R_S in Fig. 4. The overdrive voltage of M_{16} can be expressed as

$$V_{ov,16} \approx [V_{DD} - |V_{TH12}| - V_{TH17} - \frac{2\left(M - \sqrt{\frac{M}{N}}\right)}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{12} R_s}] \sqrt{\frac{\mu_n C_{ox}\left(\frac{W}{L}\right)_{17}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{16}}} \quad (11)$$

where $M = (W/L)_{15}/(W/L)_{14}$, $N = (W/L)_{11}/(W/L)_{12}$. Since $|V_{TH12}|$, $V_{TH17}$and μ_p are all inversely proportional to the temperature, a nearly constant overdrive voltage can be achieved by appropriately choosing M, N and R_S.

To compare different biasing techniques, two-stage Miller amplifiers with voltage biasing, current biasing and constant overdrive biasing are simulated and compared. The result is shown in Fig. 7(a), where it can be known that the fluctuation of the open loop gain has been minimized by the proposed constant overdrive biasing technique. Therefore, temperature compensation can be achieved without any proportional to absolute temperature (PTAT) bandgap [32], [7], or temperature sensitive loop [33].

Besides, the CMFB and resistive feedback topology further enhance the PVT robustness. The gain deviation of the entire analog baseband at different PVT corners is shown in Fig. 7(b)∼Fig. 7(d). It can be seen that the gain deviation is lower than 1.5 dB over all PVT conditions. Furthermore, a detailed Monte Carlo analysis has been implemented, which includes both process and mismatch statistical variables for 500 samples. The simulations are accomplished at all gain settings and the results of lowest and highest gain settings are showed in Fig. 8. It can be seen that the standard deviation of

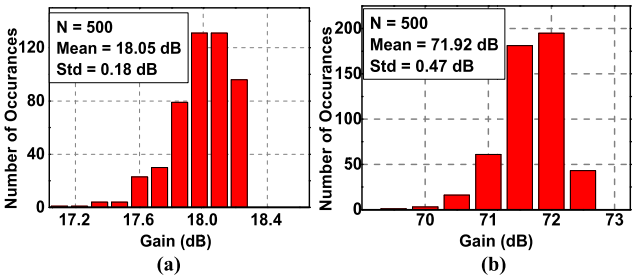

FIGURE 8. Monte Carlo analysis of the voltage gain. (a) At lowest gain setting. (b) At highest gain setting.

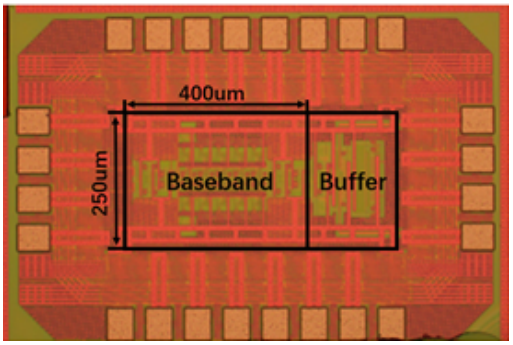

FIGURE 9. Die photo of the proposed analog baseband.

the gain is only 0.47 dB even in the highest gain setting, and 99% of the total samples are within ±1 dB of the mean value. Therefore, the proposed baseband is immune to the process variation and device mismatch.

IV. MEASUREMENT RESULTS

The proposed analog baseband has been fabricated in a 65-nm CMOS technology. To drive 50-Ω network analyzer, a differential output buffer is integrated after the analog baseband. Thanks to the proposed DCOC topology, the core chip exclude output buffer occupies only 0.1 mm^2 and the chip micrograph is shown in Fig. 9. The DC power consumption is 6 mW from a 1.2 V supply voltage without output buffer.

The DCOC characteristic is measured by a voltmeter and an oscilloscope. Firstly, a DC offset voltage from 0 to 200 mV is intentionally applied to the input of the analog baseband, and the DC offset at the output is measured. The measured result is showed in Fig. 10(a), from which it can be seen the output DC offset varies slightly with the input DC offset voltage among the range of 200 mV. It should be noted that even the input offset is 0 mV, an output offset around 9 mV also occurs due to the mismatch of the output buffer and the last stage PGA. Secondly, a 200 mVpp 1 Hz sinusoidal signal is injected to the baseband, the output offset is lower than 5 mV as showed in Fig. 10(b), implying that the DC offset has been rejected by over −30 dB. Therefore, the proposed DCOC loops are capable to eliminate DC offset effectively.

The frequency response is measured by a vector network analyzer (VNA), and the results are shown in Fig. 11. Comparing Fig. 11 with Fig. 6, it is clearly seen that the measured results are close to the theoretical analysis and

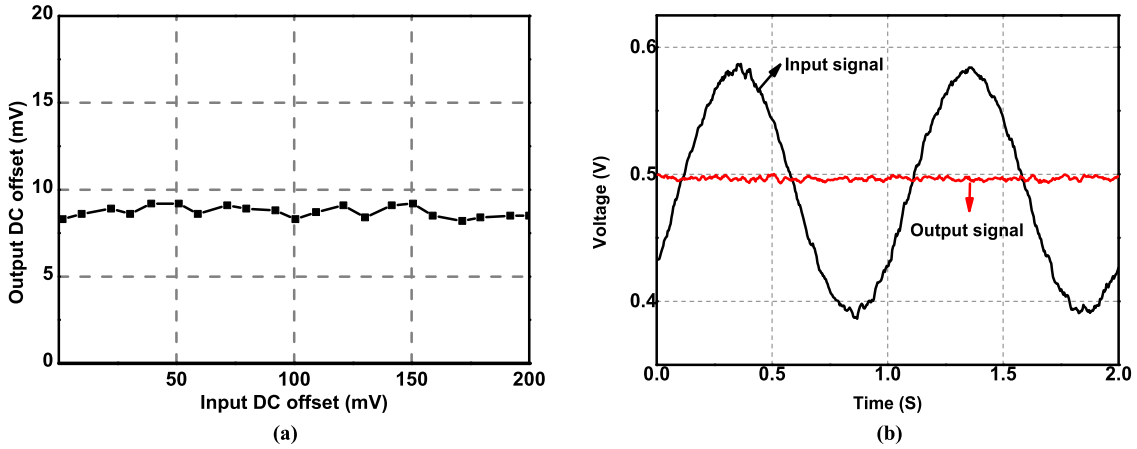

FIGURE 10. Measured DCOC performance. (a) Injecting DC offset from 0 to 200 mV. (b) Injecting a 200 mVpp 1 Hz sinusoidal signal.

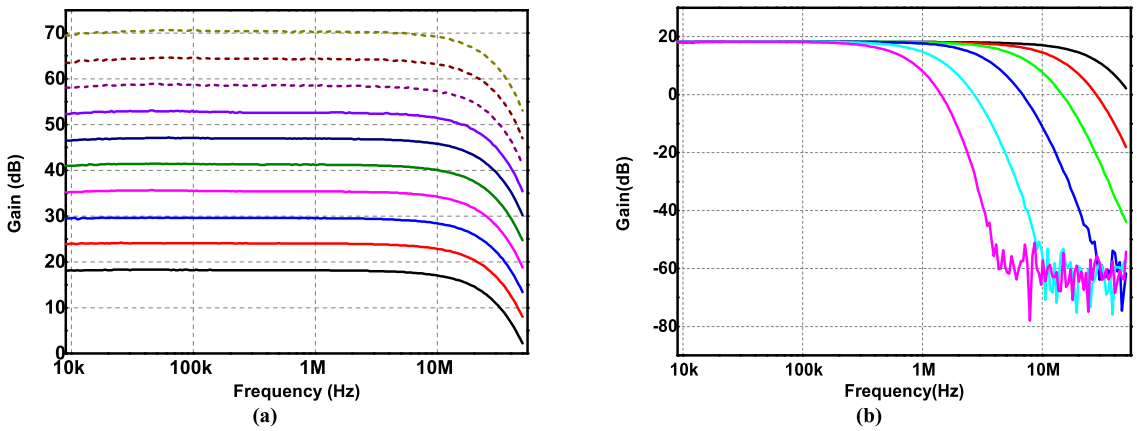

FIGURE 11. Measured frequency response. (a) Different gain steps @10 MHz bandwidth. (b) Different bandwidth steps @minimum gain.

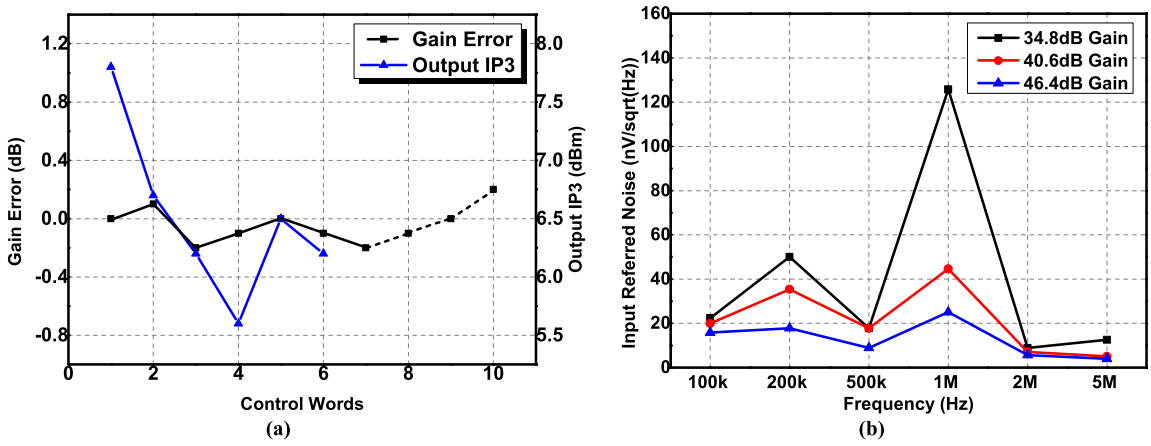

FIGURE 12. (a) Measured gain error and OIP3. (b) Measured input-referred noise.

post-layout simulation. A gain range from 18.2 dB to 70.6 dB is realized, with the 1-dB bandwidth of 200 kHz, 400 kHz, 1 MHz, 2 MHz, 4 MHz and 10 MHz, respectively.

Fig. 12(a) shows the gain error and output third-order intercept point (OIP3) characteristics. The gain error of the complete baseband including three PGAs and the fifth-order filter is always lower than 0.2 dB, with the OIP3 of 7.8 dBm at the lowest gain step. Fig. 12(b) exhibits the input-referred noise (IRN) at different gain steps. The larger the gain, the lower the IRN, being consistent with the Friis theory [34]. The IRN is 15.8 nV/$\sqrt{}$Hz at 100 kHz at the 46.4 dB gain step.

Fig. 13(a) and (b) show the measured gain characteristic at various supply voltages and temperatures. When the supply varies from 1.1 V to 1.3 V, the gain deviation from

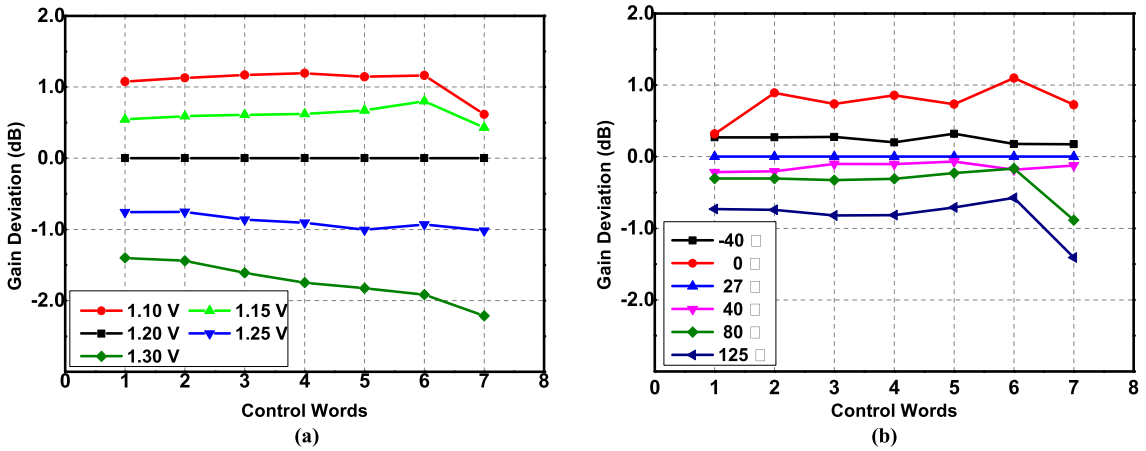

FIGURE 13. Gain deviation over (a) supply voltage corner, (b) temperature corner.

TABLE 1. Summary and comparisons with state-of-the-art.

Reference	JSSC 2013 [12]	TMTT 2013 [15]	JSSC 2016 [36]	JSSC 2015 [38]	TMTT 2012 [39]	This work
Technology	65-nm CMOS	180-nm SiGe BiCMOS	65-nm CMOS	180-nm CMOS	130-nm CMOS	65-nm CMOS
Topology	3 VGAs	1 PGA	3 PGAs + 5th filter	15 Cell-based	2 PGAs	3 PGAs + 5th filter
Supply (V)	1.2	1.8	1.2	1.8	1	1.2
Power (mW)	3.84	12.2	17.1	1.12	1.2	6.0
Gain range (dB)	-13~63	-10.6~7.8	16.8~68.2	3.6~59.6	-16~32	18.2~70.6
Gain error (dB)	0.5	N/A	N/A	0.3	0.35	**0.2**
BW (MHz)	14.8	2~1900	0.5~5	63.5	60	0.07~10
OIP3 (dBm)	11.5	4.9	N/A	6.6	6.6	7.8
IRN (nV/√Hz) @max gain	3.5	NF=21.4~27.1 dB	N/A	10.6	NF=12 dB	15.8
Area (mm^2)	0.01	0.048	0.65	0.07	0.1	0.1
DCOC	No	AC coupling	Modified DCOC	No	Basic DCOC	Proposed DCOC
High-pass cut-off Frequency (kHz)	N/A	2000	< 10	N/A	N/A	**7**
Temperature (°C) Gain Deviation (dB)	N/A	-25~85 2.0	N/A	-20~80 3.8 *	0~80 3.2 *	**-40~125 1.4**
Process Corner Gain Deviation (dB)	N/A	N/A	N/A	TT/SS/FF/ SF/FS 1.2 *#	TT/SS/FF 3 *	**TT/SS/FF/ SF/FS 1.6 ***
Monte Carlo Standard Deviation (dB)	1.27	N/A	N/A	N/A	N/A	**0.47**

* Simulated Results. # External calibration for process corners is required.

the normalized gain at 1.2 V is always lower than 2.2 dB. Similarly, the gain deviation from the normalized gain at 27 °c across −40 °c to 125 °c is lower than 1.4 dB.

Table 1 gives a summary and comparisons between the proposed baseband and the state-of-the-art. A key advantage of the analog baseband is its excellent PVT robustness. Moreover, thanks to the embedded G_m-cell based DCOC feedback loop, dB-linear accuracy is promoted and extremely low high-pass cut-off frequency is achieved with economic chip area.

V. CONCLUSION

In this paper, a PVT-robust analog baseband with DCOC for automotive radar applications is presented. The proposed embedded G_m-cell based DCOC feedback loop can achieve excellent DCOC without incurring a large chip area, extra digital circuits, and a load effect to the input, which is beneficial to promote dB-linear accuracy and loop stability. Besides, the constant overdrive biasing technique also helps improve the PVT robustness. The measurement results show that the proposed analog baseband achieved a gain range from 18.2 dB to 70.6 dB with a flatness of <0.2 dB, and a 1-dB bandwidth range from 200 kHz to 10MHz, while with a power consumption of 6 mW from a 1.2 V supply and a core chip area of only 0.1 mm^2. The gain variation is lower than 2.2 dB across all PVT corners.

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