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Modeling, Analysis, and Control of an Integrated Hybrid Energy Storage System

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ABSTRACT In traditional hybrid energy storage system (HESS), separated bidirectional dc/dc converter is usually used to interface energy storage system with dc bus. Though it has an advantage in flexibility of control system design using separated power converters, it results in more switches, auxiliary components, and cost for the whole system development. Particularly, since the energy storage system (ESS) designed for high dynamic compensation (e.g., supercapacitor) is mainly used to provide high-dynamic compensation in transient state process, the utilization rate of the corresponding interface dc/dc converter is relatively low. On the other hand, the dc bus voltage compensation performance will be discounted due to the inherent time delay for the current reference signal production of HESS with outer loop voltage control. In this paper, to address these two issues, an integrated topology of the hybrid energy storage system is proposed, and an improved control method that has the ability to enhance the control performance of HESS to compensate the dc bus voltage is developed too. The experimental test results are provided to validate the correctness and effectiveness of the proposed methods.

INDEX TERMS Hybrid energy storage, multi-port converter, phase shifted full bridge, feedforward compensation.

I. INTRODUCTION

The solar, wind, ocean wave and ocean tidal current etc. are environment friendly renewable energy generations (REG) [1]–[4], the consumption of fossil fuel can be greatly reduced by the utilization of these renewable energies. However, renewable energy generations are greatly affected by environmental factors, usually, the generation plan cannot be formulated very accurately, instability and intermittence are two prominent characteristics of REG [5]–[6].

Energy storage systems are usually configured to enhance the reliability and dynamic characteristics of the REG. Battery is very commonly used in ESS, though it has advantages in cost and energy density, it also has obvious defects in relatively short cycle life and power density etc. [7]. Furthermore, since many energy storage systems cannot simultaneously meet the requirements in both power density and energy density, hybrid energy storage system is proposed as a compromised scheme in a lot of applications [8]–[9]. For example, for the HESS using battery and supercapacitor, the battery is used to supply relatively low dynamic and steady state power for the load, while the supercapacitor can be utilized to provide high power in transient state process due to its excellent power density and high current tolerance characteristics [10].

Generally, the HESS can be interfaced to the DC bus by three connection modes, passive [11], semi-active [12] and active modes [13]. Taking battery and supercapacitor based HESS as an example, in passive mode, the battery and the supercapacitor are directly connected to the DC bus, therefore, they have the same terminal voltage, while their input and output currents are determined by their internal impedance [14], the superiorities by combining supercapacitor with battery cannot be manifested by this way. In semi-active mode, the battery or the supercapacitor will be connected to the DC bus via a bidirectional DC/DC converter, the input and output current of the one connected with the converter can be controlled flexibly. While the other one is

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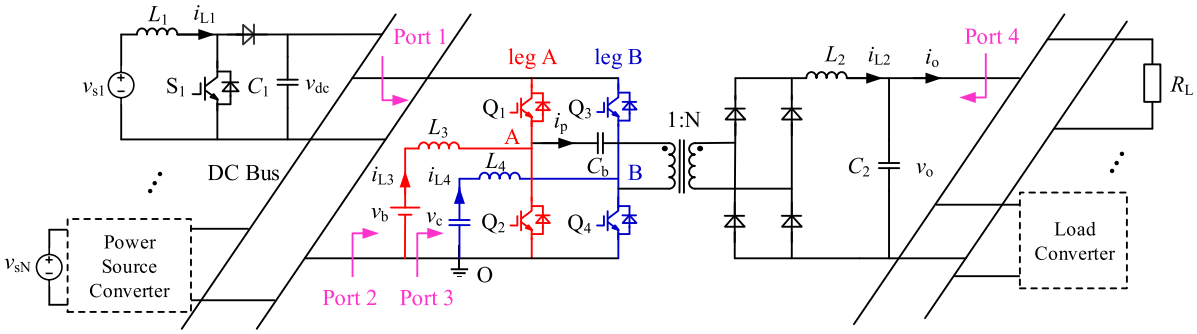

FIGURE 1. The topology of the proposed power conversion system.

still directly paralleled on the DC bus in a passive manner, and it might be needed to withstand high value of ripple current [15]. In the active mode, the supercapacitor and the battery are all connected to the DC bus through separated bidirectional DC/DC converters [16]–[18], charging and discharging are decoupled for supercapacitor and battery.

The prominent property of active connection HESS is that the control system can allocate current or power reference signals with different frequency characteristics to the corresponding ESS having different compensation abilities. Linear filter based frequency component allocation method is often used in HESS [19]. However, since the current reference signal of HESS is produced by the outer loop voltage controller according to the voltage change in the DC bus, the dynamic compensation performance will be impacted due to the inherent and inevitable time delay of voltage control loop. On the other hand, though the utilization of separated bidirectional DC/DC converters for ESS has flexibility in control system design, more switches and relatively high cost will be resulted in practice. Particularly, compared to battery energy storage system, the supercapacitor is mainly used to provide high dynamic compensation in a short duration, therefore, the utilization rate of the interface DC/DC converter is relatively low.

In order to address the aforementioned issues, a novel HESS scheme through multiplexing utilization of existent switches of full bridge converter [20] is proposed in this paper. In this method, the topology of HESS is integrated into an isolated phase shifted full bridge (PSFB) converter, the resulted converter behaves like a semi-isolated four-port converter (the four ports are denoted in Fig. 1). Furthermore, an improved DC bus voltage control method is developed to enhance the dynamic compensation performance for DC bus voltage change. An energy based DC bus voltage square control method is adopted in this scheme, in contrast to traditional voltage based control strategy, an analytical feedforward compensator can be formulated, the load power is used for feedforward compensation, which is beneficial to enhance dynamic compensation performance using HESS.

The rest of the paper is organized as follows. In section II, the topology, modulation scheme and work principle of the proposed system are presented. The control-oriented small signal models, control scheme and control system design are given in section III. The experiment results and brief analysis are given in section IV. Finally, the conclusion is drawn in section V.

II. TOPOLOGY AND MODULATION METHOD

The topology of the proposed integrated HESS along with the rest of a power conversion system is shown in Fig. 1. The switches Q_1-Q_4 are applied to constitute a phase shifted full bridge converter that is utilized to deliver the electric power from the DC bus to the load by regulating the phase shifting between leg A and leg B. The turns ratio of the high frequency transformer (HFT) is 1:N. L_2 and C_2 are output filter inductor and capacitor respectively. The output voltage of this PSFB converter can be used to supply different loads such as resistor and other load converters. The switches, Q_1 and Q_2 on leg A and an inductor, L_3 together with the battery (the voltage is v_b) form a bidirectional Buck/Boost power conversion system. The switches Q_3 and Q_4 on leg B and an inductor, L_4 together with the supercapacitor (the voltage is v_c) constitute another bidirectional Buck/Boost power conversion system. In the following sections, ESS1 and ESS2 are used to represent the battery and the supercapacitor energy storage systems respectively.

As shown in Fig. 1, the PSFB converter gets electric power from DC bus which is supplied by different power source converters (such as the Boost converter shown in this figure), while these power source converters are powered by v_{s_j} ($j = 1, 2, \ldots, N$). Here, v_{s_j} is used to represent the$j$th DC power source (or a rectified DC power source) produced by renewable energy generations (for example, photovoltaic generation). In normal condition, the renewable energy generations can be controlled in maximum power point tracking (MPPT) mode [21], for example, if v_{s1} is produced by solar panels, MPPT can be realized by using the hill climbing algorithm to control the average value of inductor current, i_{L1}.

The driving signals of the PSFB converter are shown in Fig. 2. In this figure, φ denotes the phase shifting between the switching signals of leg A (leading) and leg B (lagging), assuming the duty cycle of leg A is d_1 (the duty cycle of Q_2), and the duty cycle of leg B is d_2 (the duty cycle of Q_4) respectively. The duty cycles of leg A and leg B can

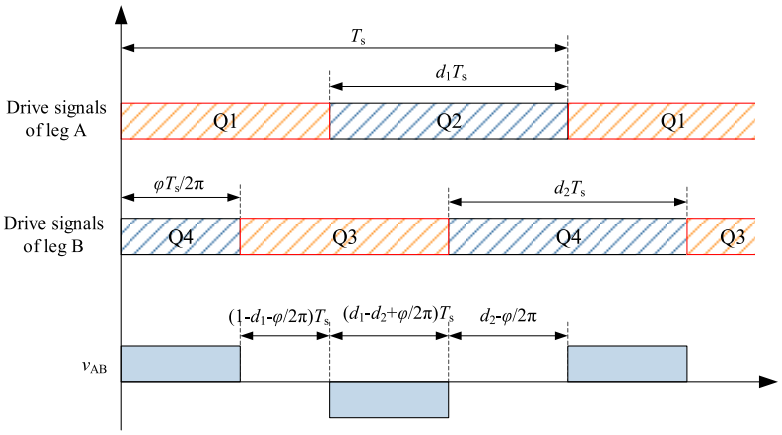

FIGURE 2. The phase shift pulses of the full bridge converter.

be regulated to charge or discharge the HESS to keep v_{dc} constant.

According to Fig. 1 and Fig. 2, the steady state voltages of ESS1 and ESS2 can be written as (1).

$$\begin{cases} V_b = (1 - D_1)V_{dc} \\ V_c = (1 - D_2)V_{dc}. \end{cases} \tag{1}$$

In (1), V_b and V_c are the steady state values of v_b and v_c respectively. D_1 and D_2 are the steady state values of d_1 and d_2 respectively. Since the values of v_b and v_c cannot be exactly the same, there is always deviation between d_1 and d_2, DC bias current will be produced in the transformer winding which will degrade transformer efficiency and even cause damage in transformer, therefore, a capacitor, C_b is necessary in series with the primary winding of HFT to block the DC component of winding current, i_p.

By applying the volt-second balance principle on the transformer, the steady state voltage of C_b, V_{cb} can be expressed as (2).

$$V_{cb} = V_{dc}(1-D_1) - V_{dc}(1-D_2) = V_{dc}(D_2 - D_1) \tag{2}$$

If the volt-second balance principle is applied to the output filter inductor L_2 in the PSFB converter, then, the steady state value of output voltage v_o can be expressed by (3).

$$\begin{aligned} V_o &= \left[N\frac{\varphi}{2\pi}(V_{dc} + V_{cb}) + (D_2 - D_1 + \frac{\varphi}{2\pi})(V_{dc} - V_{cb}) \right. \\ &\quad \left. + (1 - \frac{\varphi}{\pi} + D_1 - D_2)\,|V_{cb}|\right] \\ &= \begin{cases} NV_{dc}\left[\frac{\varphi}{\pi}(1 - \delta_d) + 2\delta_d - 2\delta_d^2\right], & \delta_d > 0 \\ NV_{dc}\left[\frac{\varphi}{\pi}(1 + \delta_d)\right], & \delta_d < 0 \end{cases} \end{aligned} \tag{3}$$

In (3), $\delta_d = D_2D_1$, and $V_{cb} = \delta_d V_{dc}$.

According to Fig. 2, if the condition given by (4) is met, then the phase shifting between the leg A and leg B will be less than $2\pi D_1$ and $2\pi(1\text{-}D_2)$.

$$\frac{\varphi}{2\pi} < D_1, \quad \text{and} \frac{\varphi}{2\pi} < 1 - D_2 \tag{4}$$

Otherwise, if this constrain is not held, the width of $v_{AB}$is only defined by the values of d_1 and d_2, that means the phase shifting, φwill lost control for the output voltage v_o [22]. However, it can be concluded from (3) that the output voltage is not only affected by φ, but also influenced by the duty cycles of leg A and leg B under the condition given in (4). Therefore, small δ_d is desired to reduce the impact of duty cycle change on the output voltage in transient state process. In steady state, the impact of δ_d behaves as a constant disturbance for the output voltage control system of PSFB converter, and it can be compensated by a properly designed voltage control loop of PSFB converter.

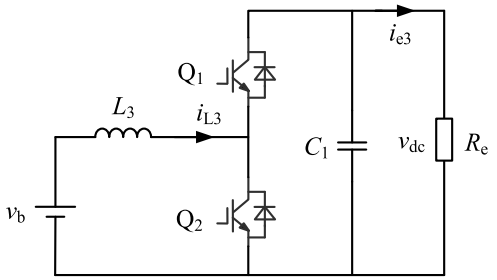

FIGURE 3. The topology of bidirectional Buck/Boost converter.

III. MODELING AND CONTROL SCHEME

A. SMALL SIGNAL MODEL OF HESS

In the proposed method, the two integrated bidirectional Buck/Boost converters can work in Buck or Boost mode to charge or discharge the HESS. By multiplexing utilization of Q_1 and Q_2, the topology of ESS1 is shown in Fig. 3. R_e represents an equivalent load.

Taking Q_2 as the main switch in Fig. 3, the large signal model of Fig. 3 can be derived in (5) according to the switching mode of Buck/Boost converter.

$$\begin{cases} L_3\dfrac{di_{L3}}{dt} &= v_b - (1 - d_1)v_{dc} \\ C_1\dfrac{dv_{dc}}{dt} &= (1 - d_1)i_{L3} - \dfrac{v_{dc}}{R_e} \end{cases} \tag{5}$$

By introducing small signal disturbance$\tilde{i}_{L3}$, $\tilde{v}_{dc}$ and $\tilde{d}_1$, of i_L, $v_o$and d_1 respectively, the small signal model of the

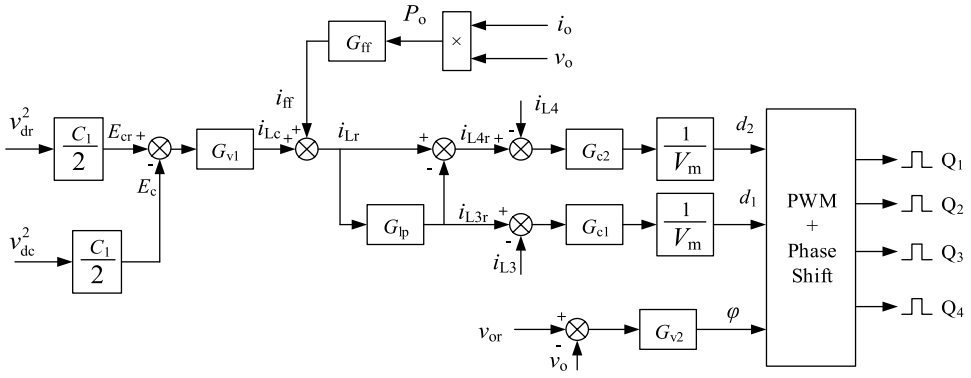

FIGURE 4. The control scheme of the proposed system.

converter in Fig. 3 can be expressed in (6).

$$\begin{cases} L_3 \dfrac{d\tilde{i}_{L3}}{dt} = -(1-D_1)\tilde{v}_{dc} + \tilde{v}_b + \tilde{d}_1 V_{dc} \\ C_1 \dfrac{d\tilde{v}_{dc}}{dt} = (1-D_1)\tilde{i}_{L3} - \dfrac{\tilde{v}_{dc}}{R_e} - \tilde{d}_1 I_{L3} \end{cases} \tag{6}$$

In (6), D_1, V_{dc} and I_{L3} are the steady state value of d_1, v_{dc} and i_{L3} respectively.

There is a non-minimum zero in the $\tilde{d}_1$-to-$\tilde{v}_{dc}$ small signal transfer function of the bidirectional Buck/Boost converter [23] which has negative impact on voltage control stability and dynamic performance. In steady state, the energy storage of the capacitor, C_1 can be expressed in (7).

$$E_c = \frac{1}{2} C_1 v_{dc}^2 \tag{7}$$

Equation (8) can be obtained by combining (5) and (7)

$$v_b i_{L3} = P_o + \frac{dE_c}{dt} + P_L \tag{8}$$

In (8) P_o represents load power, P_L represents inductor power, the expressions of P_o and $P_L$are given in (9).

$$\begin{cases} P_o = \dfrac{v_{dc}^2}{R_e} \\ P_L = \dfrac{L_3}{2} \dfrac{di_{L3}^2}{dt} \end{cases} \tag{9}$$

By introducing small signal disturbance, $\tilde{v}_b$, $\tilde{i}_{L3}$, $\tilde{P}_o$,$\tilde{P}_L$ and $\tilde{E}_c$ of the corresponding variables in (8), the small signal based differential equation of (8) can be written as (10).

$$\frac{d\tilde{E}_c}{dt} = V_b \tilde{i}_{L3} + \tilde{v}_b I_{L3} - \tilde{P}_o - \tilde{P}_L \tag{10}$$

It can be seen from (10) that E_c can be controlled by the inductor current. Therefore, the control scheme by employing inductor current inner loop plus capacitor energy storage outer loop can be developed, the DC bus voltage can be indirectly governed by controlling the energy storage of capacitor. The control plant (the transfer function of $\tilde{d}_1$-to-$\tilde{i}_{L3}$) of inner current control loop can be deduced as (11) according to (6).

$$G_{ld1} = \frac{\tilde{i}_{L3}}{\tilde{d}_1} = \frac{V_{dc} R_e C_1 s + 2V_{dc}}{R_e L_3 C_1 s^2 + L_3 s + R_e D_1'^2} \tag{11}$$

In (11)$D_1' = 1 - D_1$.

Similarly, the corresponding transfer function of $\tilde{d}_2$-to-$\tilde{i}_{L4}$ for the ESS2 can be derived as (12).

$$G_{ld2} = \frac{\tilde{i}_{L4}}{\tilde{d}_2} = \frac{V_{dc} R_e C_1 s + 2V_{dc}}{R_e L_4 C_1 s^2 + L_4 s + R_e D_2'^2} \tag{12}$$

Furthermore, the $\tilde{\varphi}$-to-$\tilde{v}_o$ transfer function of PSFB converter is given in (13) [24].

$$G_{\phi v} = \frac{\tilde{v}_o}{\tilde{\phi}} = \frac{NR_L V_b / \pi}{R_L L_2 C_2 s^2 + (L_2 + R_L R_d C_2)s + R_d + R_L} \tag{13}$$

In (13), $R_d = 4N^2 L_{lk} f_s$ represents duty cycle loss, where L_{lk} is the leakage inductance of the high frequency transformer, f_s is the switching frequency respectively.

B. CONTROL SCHEME

According to the earlier analysis, the developed control scheme for the HESS and the PSFB converter is presented in Fig. 4. In this figure, v_{dr} is the reference signal of DC bus voltage (v_{dc}), capacitor energy based voltage square outer loop control is developed for the DC bus voltage, G_{v1} is the corresponding voltage controller. G_{ff} is load power feedforward compensator. The reference current, i_{Lr} that should be provided by the HESS is the summation of i_{Lc}(the output of G_{v1}) and i_{ff} (the output of G_{ff}). G_{lp} is a low pass filter, it can be a first order filter shown in (14).

$$G_{lp}(s) = \frac{\omega_b}{s + \omega_b} \tag{14}$$

In (14), ω_b represents the bandwidth of G_{lp}. G_{lp} is used to extract the low frequency component, i_{L3r} of i_{Lr} as the inductor current reference signal for ESS1, and the high frequency component of i_{Lr} ($i_{L4r} = i_{Lr}$-i_{L3r}) is used as the inductor current reference signal for the ESS2. $G_{c1} = G_{c2} = G_c$are the inner loop current controller. $1/V_m$ is the model of modulator, V_m is the amplitude of carrier wave. G_{v2} is the output voltage controller of PSFB converter.

Since the ESS1 and ESS2 share the common voltage square controller, G_{v1}, and their inner inductor current control loops have the same current controller, G_c, the control system design can be addressed base on any one of these two energy storage systems. According to Fig. 4, the control

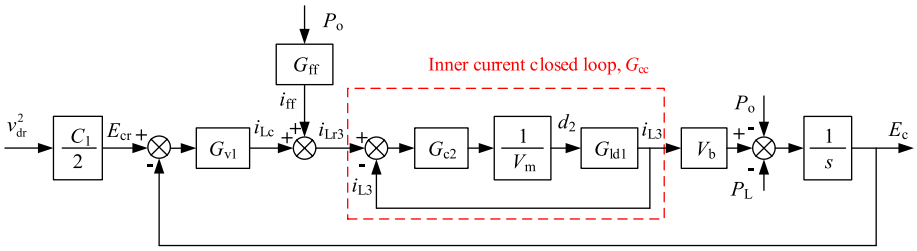

FIGURE 5. The control block diagram of ESS1.

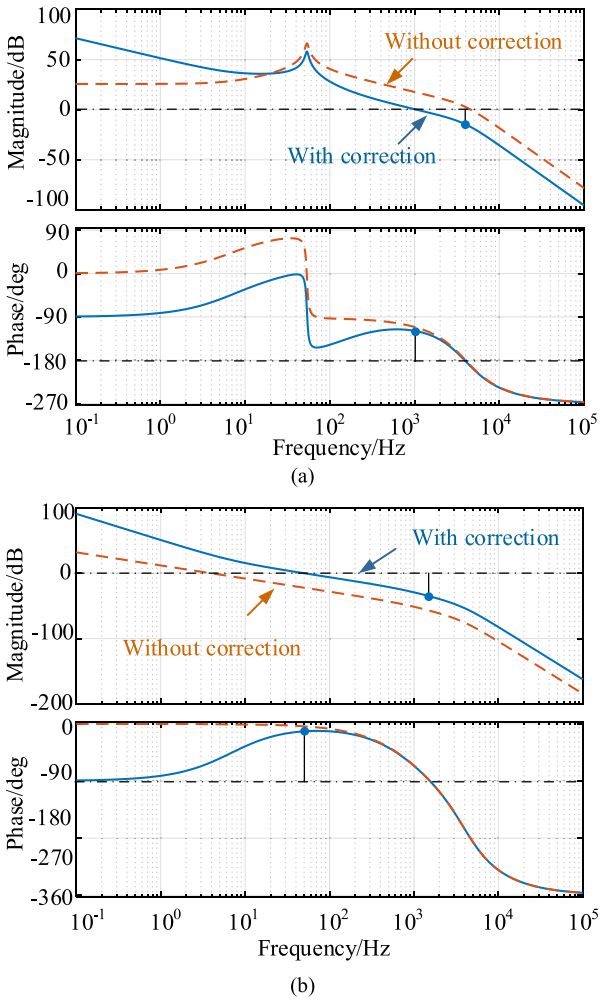

FIGURE 6. The bode plots of the corrected ESS control system (a) inner inductor current control loop and (b) outer capacitor energy control loop.

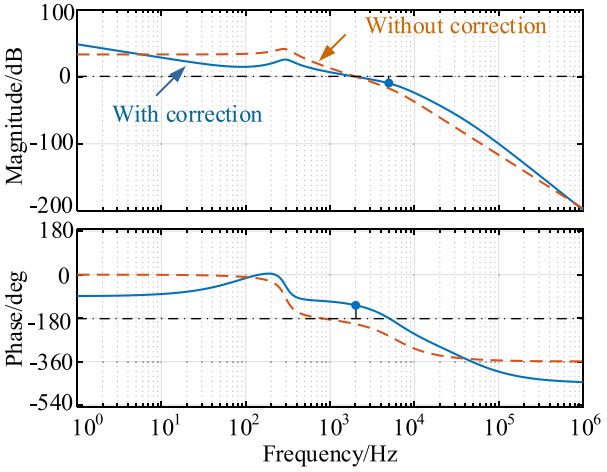

FIGURE 7. The bode plots of voltage control loop for the PSFB converter.

TABLE 1. Parameters of the hardware circuit.

Symbol	Name	Value
v_{s1}	DC input voltage	24V
v_b	Voltage of ESS1	24.5V
v_c	Voltage of ESS2	24.9V
v_{dc}	DC bus voltage	48V
v_o	Output voltage	20V
C_1	DC bus capacitor	2200μF
C_2	Output filter capacitor	1000μF
L_1	Output filter inductor	0.3mH
L_2	Filter inductor of Boost converter	2mH
L_3	Filter inductor of ESS1	1mH
L_4	Filter inductor of ESS2	1mH
f_s	Switching frequency	20kHz

block diagram of an individual ESS can be presented in Fig. 5 (by employing ESS1 as an example). As shown in this figure, a load power feedforward compensation is introduced to improve the load disturbance rejection ability of voltage square control loop. Assuming the transfer function of the inner current closed loop is G_{cc} (denoted by the dash line rectangle in Fig. 5), an analytical expression of G_{ff} can be designed as (15) to cancel the negative impact caused by the change of P_o.

$$G_{ff} = \frac{1}{V_b G_{cc}(T_p s + 1)} \tag{15}$$

In (15), the term $(sT_p + 1)$ in denominator is introduced to attenuate the high frequency noise and make (15) a rational fraction. And G_{cc} can be replaced by an equivalent first order system for simplification in practices.

Using the parameters listed in Table 1, the bode plot of the corrected ESS1 control system is shown in Fig. 6. It can be seen that the cross frequency of the corrected current loop is about 1kHz, the gain margin is about 14.5dB and the phase margin is about 61°. The cross frequency of the voltage

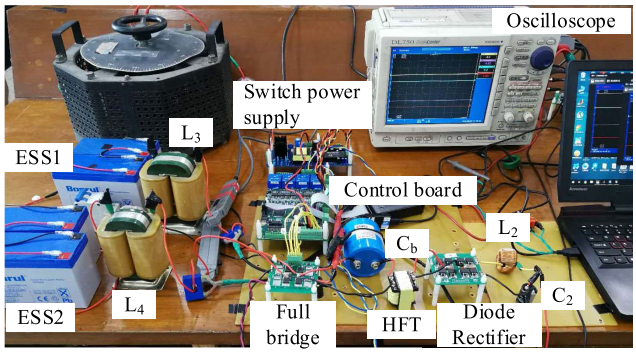

FIGURE 8. The experiment hardware circuit.

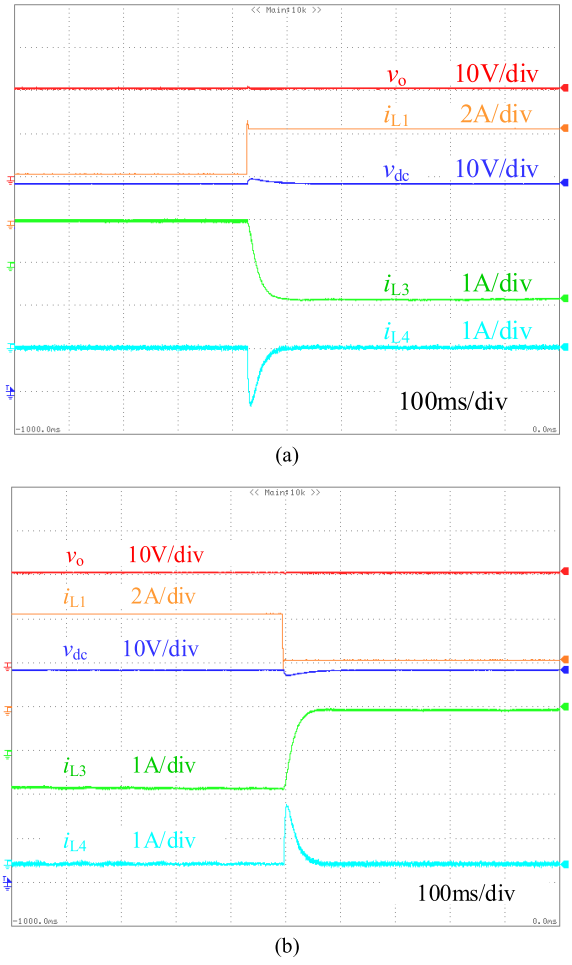

FIGURE 9. The experimental results with sudden change of i_{L1} (a) i_{L1} increase, (b) i_{L1} decrease.

square (energy) control loop is about 50Hz, the corresponding gain margin (GM) and the phase margin (PM) are about 14.5dB and 61° respectively.

Fig. 7 shows the bode plot of the voltage control loop for PSFB converter. In this figure, the controller shown in (16) is used to make the corrected voltage control loop has relatively high cross frequency which is beneficial to attenuate the impacts caused by the duty cycles regulation in dynamic process. It can be seen that the cross frequency of

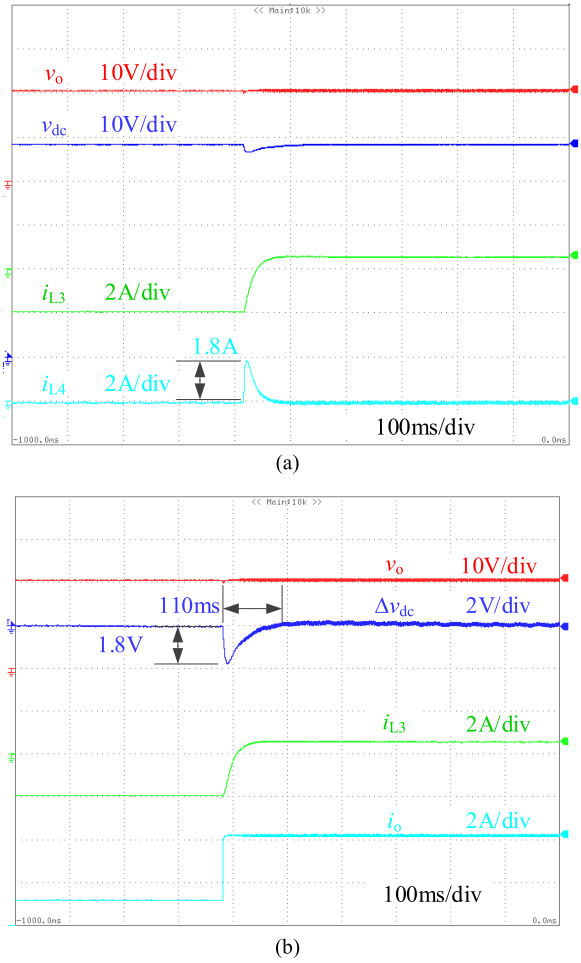

FIGURE 10. The experimental results of sudden load increase without feedforward compensation (a) v_o, v_{dc}, i_{L3} and i_{L4} (b) the fluctuation component of v_{dc} and i_o.

the corrected system is about 2kHz with GM=9.6dB and PM=51.3° respectively.

$$G_{v2}(s) = \frac{4.96 \times 10^6 (s + 676.5)(s + 676.5)}{s(s + 2.513 \times 10^5)(s + 2.513 \times 10^5)} \quad (16)$$

IV. EXPERIMENTAL RESULT

In order to verify the theoretical analysis and design results of the proposed method, an experimental platform was developed as shown in Fig. 8, the main parameters of the experiment circuit are listed in Table 1. The control board is equipped with a 32-bit ARM Cortex-M4 core STM32F407IGT6 Microprocessor with 168MHz clock frequency and floating point unit (FPU) which is very suitable to implement the proposed control scheme. Four Infineon MOSFET modules (IPT059N15N3) are utilized to formed the power circuit of PSFB converter, and two chips of IRS2183 are used as driver circuits for the four MOSFETs. Furthermore, in the experiment circuit, another MOSFET IPT059N15N3 together with its driver circuit, inductor (L_1 in Fig. 1) and capacitor (C_1 in Fig. 1) components constitute a Boost converter which is performed as a power source con-

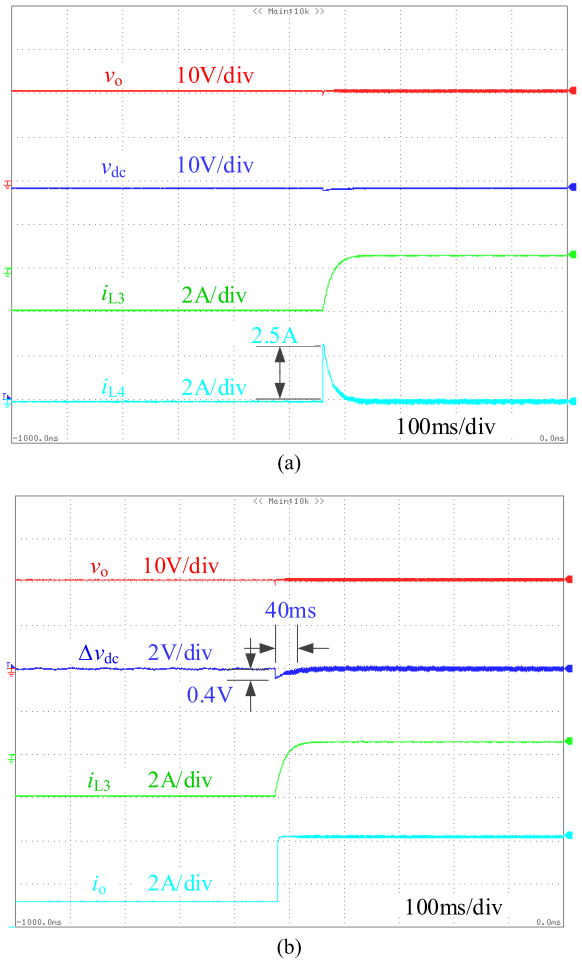

FIGURE 11. The experimental results of sudden load increase with feedforward compensation (a) v_o, v_{dc}, i_{L3} and i_{L4} and (b) the fluctuation component of v_{dc} and i_o.

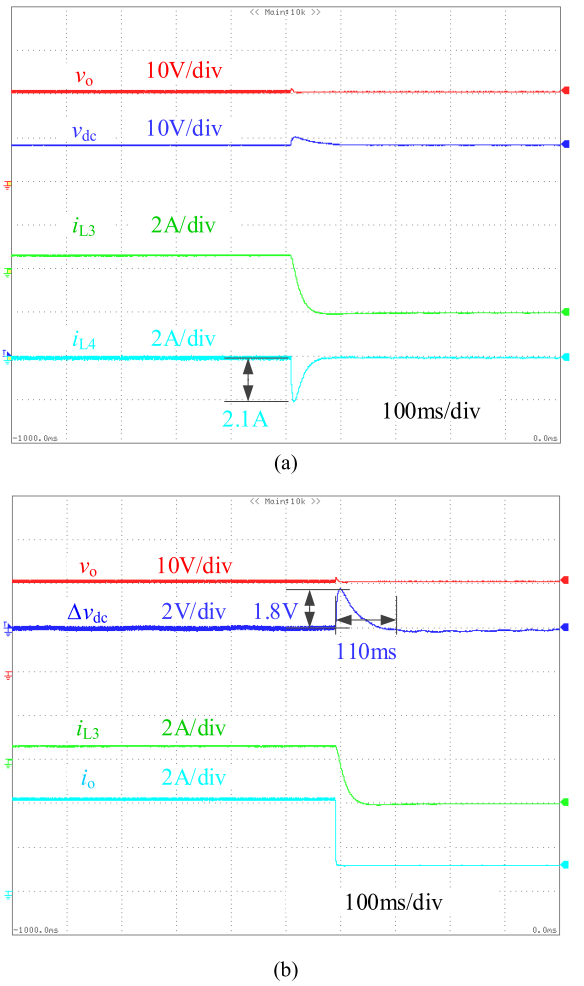

FIGURE 12. The experimental results of sudden load decrease without feedforward compensation (a) v_o, v_{dc}, i_{L3} and i_{L4} and (b) the fluctuation component of v_{dc} and i_o.

verter and operated in average inductor current control mode to supply the DC bus (e.g., emulating solar panel in MPPT mode). As shown in Fig. 8, there is no real supercapacitor used in the hardware circuit, two groups of lead-acid batteries are used as ESS1 and ESS2, however, this configuration has little influence on the validation of the proposed control scheme. The experimental results are shown in Fig. 9–13.

Fig. 9 shows the experiment results with sudden change of input current, i_{L1}. In Fig. 9 (a), the initial value of i_{L1} is 2.2A and the load power is about 67W ($R_L = 6\Omega$), the value of ω_b in (14) is designed as 62.8rad/s (10Hz), as it can be seen that the ESS1 is discharged in this initial condition to supply the load. When i_{L1} is suddenly controlled to be 4.2A, there is a very steep undershoot in i_{L4} of ESS2, while the current of the ESS1,i_{L3} is changed smoothly. Furthermore, since there has excess power delivered to the DC bus with the sudden increase of i_{L1}, the ESS1 is charged in this condition. The experiment result with sudden reduction of i_{L1} is shown in Fig. 9 (b), in this case, $i_{L1}$is controlled from 4.2A to 2.2A, there is a very steep overshoot in i_{L4} of ESS2, that means the ESS2 provide high dynamic current compensation in transient state process as desired. While the ESS1 smoothly transitions from the charge state to the discharge state again. These experiment results show that the proposed integrated HESS scheme can be performed well both in steady and transient state process, and it can stabilize the DC bus voltage when the input power provided by the power source is varied.

Fig. 10 shows the experiment results on performance investigation of the proposed load power feedforward compensation method. In Fig. 10 (a), the initial value of $i_{L1}$is controlled to be 3A, and the load power is about 22W (the value of $R_L$is about 18Ω), the load resistor and the ESS1 get electric power from v_{s1} in this condition. If the load power is suddenly increased to 88W (R_L is decreased to 4.7Ω) without adopting the proposed feedforward scheme, there is an obvious voltage drop (about 1.8V, 3.75% of v_{dc}) in v_{dc}, though the HESS provides electric power to the DC bus according to the frequency based current allocation rule in Fig. 4. It can be seen that the peak value of inductor current (i_{L4}) in ESS2 is about 1.8A in Fig. 10 (a), and the transient recovery time of v_{dc} is about 110ms in Fig. 10 (b).

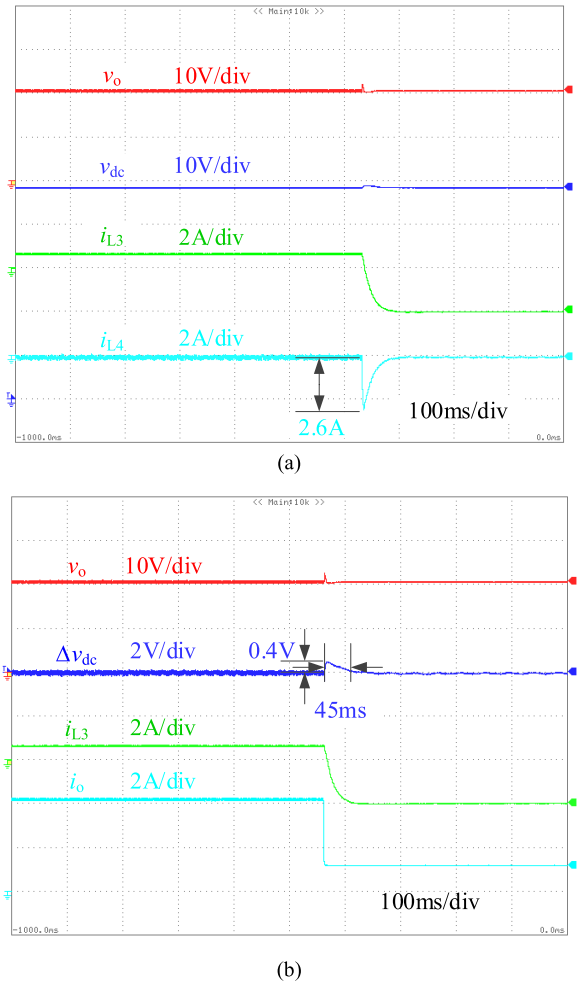

FIGURE 13. The experimental results of sudden load decrease with feedforward compensation (a) v_o, v_{dc}, i_{L3} and i_{L4} and (b) the fluctuation component of v_{dc} and i_o.

As shown in Fig. 11, if the proposed feedforward compensation method is utilized, the voltage drop in v_{dc} is reduced to 0.4V (0.83% of v_{dc}) with the same load change in Fig. 10, the transient recovery time is decreased to about 40ms and the peak value of inductor current (i_{L4}) in the ESS2 is about 2.5A, that means the ESS2 has provided more prompt and effective compensation to reduce the DC bus voltage change in the transient state under this condition.

The experiment results of sudden load decrease with feedforward control are shown in Fig. 12 and Fig. 13, in these two figures, the load power is decreased from 88W to 22W suddenly (the load current, i_o is changed from about 4.2A to 1.1A). Without the proposed feedforward power compensation, the overshoot in v_{dc} is about 1.8V in Fig. 12 (b), and the corresponding transient state recovery time of v_{dc} is about 110ms, the peak value of i_{L4} is about 2.1A in this case. While the voltage overshoot in v_{dc} is decreased to 0.4V, the peak value of i_{L4} is increased to about 2.6A, and the transient state recovery time is reduced to about 45ms in Fig. 13 (b), if the proposed load power compensation method is employed.

V. CONCLUSION

In this study, an integrated hybrid energy storage system scheme is proposed by multiplexing utilization of the full bridge switches at the primary side of a phase shifted full bridge converter, the converter behaves like a semi-isolated four-port converter in this condition, which can reduce the number of power switches and cost, and the topology of the whole power conversion system can be more compact. The constraint condition between phase shifting and duty cycle are discussed to guarantee this four-port converter can perform hybrid energy storage control and output voltage control harmonically. Furthermore, an improved voltage control method that is based on voltage square (that means capacitor energy storage) feedback and load power feedforward is developed for hybrid energy storage system to enhance the voltage compensation performance on DC bus. The effectiveness of the proposed integrated scheme and control method are demonstrated by the obtained experimental results.

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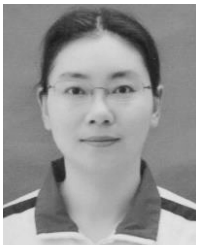

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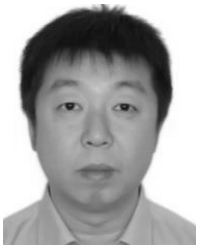

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