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Implementation of a Low Noise Amplifier With Self-Recovery Capability

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ABSTRACT In this paper, an RF low noise amplifier (LNA) with self-recovery capability has been designed and implemented. A degradation model of hot carrier injection (HCI) of n-channel MOSFETs is proposed to simulate the aging process of the RF circuits, and a method for monitoring the HCI degradation in the RF circuits has been developed. Self-recovery mechanism of the LNA is triggered automatically by monitoring the HCI degradation to compensate for the HCI degradation. With the self-recovery capability, the LNA can maintain its performance under HCI stress over time. The proposed LNA has been fabricated with a $0.13\mu m$ CMOS technology and the self-recovery capability has been experimentally demonstrated.

INDEX TERMS LNA, HCI, self-recovery, self-monitoring, built-in compensation, degradation model.

I. INTRODUCTION

In recent years, the popularity of mobile communications has promoted the rapid development of RF circuits. At the same time, chip manufacturing technologies are also rapidly advancing, and more and more RF circuits and digital circuits are integrated on the same chip. As a result, reliability of the RF circuits has become an important concern.

With decrease of transistor geometry size and increase of operating frequency, aging problems of the RF circuits have become more and more severe. Many previous studies have discussed various aging mechanisms and their negative impacts on the circuits. Common aging mechanisms for MOSFETs include hot carrier injection (HCI) [1]–[3], oxide breakdown (OBD) [4]–[6] and negative bias temperature instability (NBTI) [7]–[9]. The influence of HCI on CMOS low noise amplifier (LNA) performance was analyzed in [10]. The authors concluded that HCI reduces the transconductance of transistors, leading to decrease of the gain of LNA and increase of the noise figure. The influence of NBTI on LNA and Voltage Controlled Oscillator (VCO) were reported in [11]. The above research shows that the performance parameters of the RF circuits can be significantly affected by HCI and NBTI.

Models for the aging mechanisms of RF circuits have been reported in literature in detail. In this paper, we employ these models to design a 2.4 GHz LNA with self-recovery capability using the self-monitoring and built-in compensation technology. Once the monitoring circuit detects noticeable performance degradation of the RF circuit, the performance recovery of the RF circuit is realized by a built-in compensation circuit. The self-monitoring circuit and built-in compensation circuit should be designed together with the RF circuit to facilitate the degradation monitoring and performance recovery.

A suitable HCI degradation model is employed to describe the degradation of the key transistors used in the LNA. By monitoring the DC status of the LNA, it can be determined whether to start the biasing or transconductance (g_m) compensation process. With the self-recovery capability, the performance of the LNA can be maintained after a long time of HCI stress.

In this paper, we will present the design of the power-constrained simultaneous noise and input matching (PCSNIM) LNA followed by the techniques for the HCI degradation monitoring and self-recovery realization.

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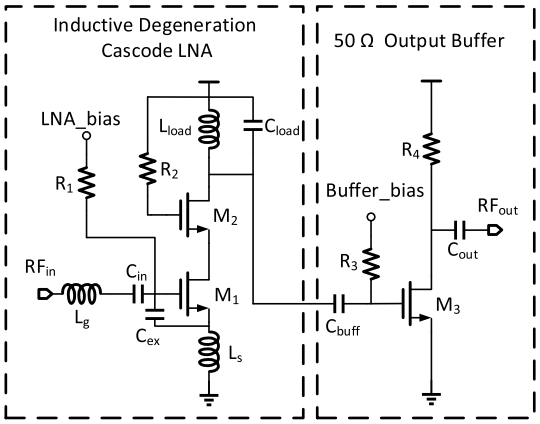

FIGURE 1. Schematic of PCSNIM LNA with a 50 Ω output buffer.

TABLE 1. Specifications of low noise amplifier.

Specifications	S_{11}	S_{21}	S_{22}	NF
Targets	$< -10dB$	$> 18dB$	$< -10dB$	$< 1.5dB$
Simulation Results	$-16dB$	$19.8dB$	$-12dB$	$1.05dB$

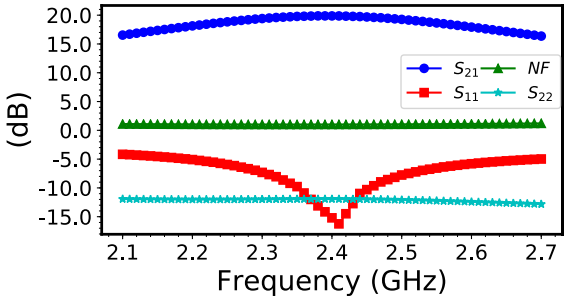

FIGURE 2. Simulation results of the PCSNIM LNA.

Experimental results are shown to prove the effectiveness of the methodology proposed in this paper.

II. LNA DESIGN

The LNA topology is presented in Figure 1. The power-constrained simultaneous noise and input matching (PCSNIM) technique is used [12]. The inductive degenerated cascode structure is commonly used in narrow band applications [13], [14]. It is composed of cascoded transistors M_1 and M_2 to obtain a high gain, a L_{load} C_{load} tank resonator to tune the gain at 2.4 GHz. Inductors L_g and L_s and capacitor C_{ex} are used to provide the input match; while a 50 Ω output buffer is used for measurement [15]–[17].

Using the above topology, the 50 Ω input match is obtained without adding noise to the design [18]. This is realized by carefully selecting the input inductor L_g, the degenerated inductor L_s, the extra capacitor C_{ex} and transistor M_1 with desirable transconductance g_m and gate-source capacitor C_{gs}. Therefore, in the PCSNIM LNA, by adding an extra capacitor C_{ex}, the simultaneous noise and input matching (SNIM) can be achieved at a lower level of power dissipation.

Table 1 and Figure 2 present the simulation results of the LNA. The simulator used for the simulation is Spectre RF. As can be seen in Figure 2, the LNA shows an input return loss (S_{11}) of −16 dB, gain (S_{21}) of 19.8 dB, output return loss (S_{22}) of −12 dB and noise figure (NF) of 1.05 dB, respectively, at 2.4 GHz.

III. SELF-RECOVERY CIRCUIT DESIGN

The LNA with self-recovery capability based on the degradation monitoring and compensation technique is described in this section. With this technique, the HCI degradation of transistors is monitored, and a mechanism to compensate for the g_m shift caused by the degradation is employed to maintain the LNA performance.

A. MODEL OF NMOS AGING BY HCI

The continuous development of CMOS technology inevitably leads to a variety of reliability problems, such as hot carrier injection (HCI), which is prominent in NMOS devices [19]–[22]. When the gate of NMOS is switched on, HCI generates interface traps at the Si/SiO_2 interface near the drain terminal, which leads to an increase in the threshold voltage (V_{th}) of the MOSFETs and a decrease in the MOSFETs' channel mobility μ_n. The degradation may lead to a significant decrease in the transconductance g_m of the transistors concerned. As the matching and gain of RF circuits are significantly affected by the drain current I_d and g_m of the transistors, the effects of HCI on RF circuits are significant. The influence of HCI on RF characteristics of single MOSFET has been studied in literatures [6], [23].

HCI can be physically described as charge generation in the region near the Si/SiO_2 interface. A previous study [24] proposed a general theoretical framework, namely the R-D model, to explain this effect. The model of threshold voltage shift ΔV_{th} and carrier mobility μ_n as a function of HCI stress time can be expressed as follows:

$$\Delta V_{th} = \frac{q}{C_{ox}} K \sqrt{Q_i} exp(\frac{E_{ox}}{E_o}) exp(-\frac{\varphi_{it}}{q\lambda E_m}) t^n \quad (1)$$

$$\mu_n = \mu_{n0}/(1+\alpha N_{it})^m \quad (2)$$

where $N_{it} = \Delta V_{th} C_{ox}/q$ is the number of the charged interface states; $Q_i = C_{ox}(V_{gs} - V_{th})$ is the inversion charge; $E_{ox} = (V_{gs} - V_{th})/t_{ox}$ is a vertical electric field (due to V_{gs}) in the gate oxide; $E_m = (V_{ds} - V_{dsat})/l$ is a transverse electric field in the channel; E_o is the activation energy; φ_{it} is the minimum energy required for thermal electron collision ionization; K is a fitting parameter; n is the time exponent; and m is a fitting parameter for carrier mobility.

Based on the study reported in [25] we have developed a more precise degradation model of V_{th} and μ_n. From the model I_d can be expressed as:

$$I_d = \theta \mu_{n0} C_{ox} \frac{W}{L} (V_{gs} - (V_{th} + \Delta V_{th}))^2 \quad (3)$$

$$\theta = 1/(1+\alpha N_{it})^m \quad (4)$$

θ is the attenuation factor of carrier mobility.

I_d can further be expressed as:

$$I_d = \mu_{n0} C_{ox} \frac{W}{L}(V_{gs} - (V_{th} + \Delta V_{th}))^2 - (1-\theta)\mu_{n0} C_{ox} \frac{W}{L}(V_{gs} - (V_{th} + \Delta V_{th}))^2 \quad (5)$$

$$= I_{d0} - (1-\theta) I_{d0} \quad (6)$$

$$= I_{d0} - \Delta I_{d0} \quad (7)$$

HCI stress causes an increase in the threshold voltage V_{th}, leading to a decrease in the drain current. ΔV_{th} can be seen as a "voltage source" in the Modeling language "Verilog-A". As can be seen in Equation (7), the degradation of μ_n could be described as a current source in "Verilog-A", which is affected by θ and I_{d0}. As shown in Figure 3, the aging model can be built in the SPICE environment for simulation. The simulators used for the simulation of the LNA degradation with the aging model are Spectre RF and AMS (Analog Mixed-Signal Simulation). From the aging simulation, the effect of transistor degradation on LNA performance can be revealed.

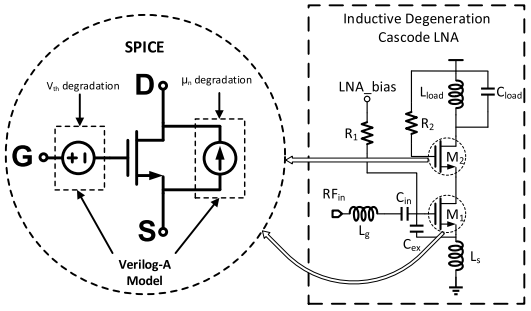

FIGURE 3. Circuit implementation of the aging model.

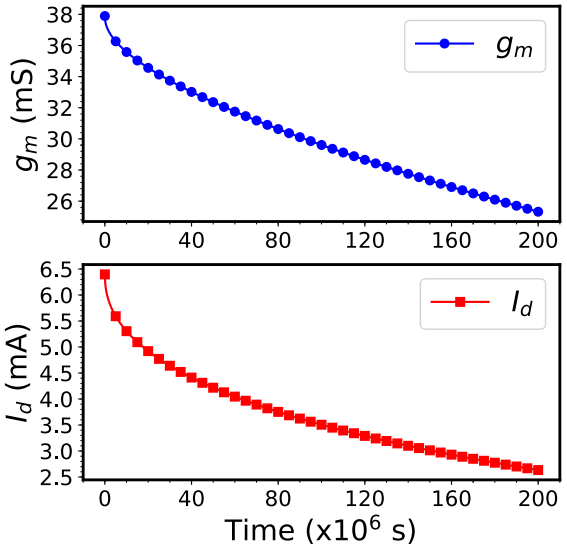

FIGURE 4. Simulated degradation of g_m and drain current (I_d) versus aging time.

Figure 4 shows the simulation results of HCI degradation of transconductance g_m and drain current I_d of transistor M_1 used in the LNA. As observed in Figure 4, due to the HCI effect, g_m and I_d undergone a large degradation.

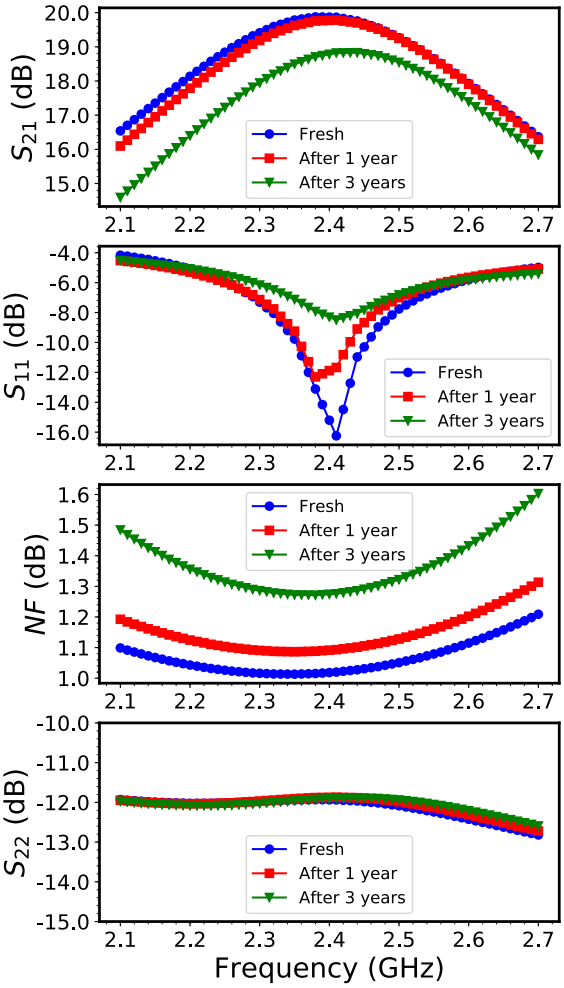

FIGURE 5. Simulated performance degradation of the LNA. S_{21}, S_{11}, NF and S_{22} of the LNA due to HCI effect after 1 and 3 years of operation.

g_m decreases by more than 30% while I_d decreases by more than 50% for HCI stress time of 2×10^8 seconds.

Figure 5 shows the simulation results of the performance parameters of the LNA at 2.4 GHz frequency after 1-year and 3-year HCI stress. The gain (S_{21}) of LNA decreases; the noise figure (NF) increases; and the input return loss (S_{11}) increases and the output return loss (S_{22}) remains constant. After 3-year degradation, the S_{21}, NF and S_{11} degraded 1.1 dB, 0.2 dB and 8 dB respectively. Overall, the performance of the 2.4 GHz LNA may significantly degrades under HCI stress.

B. MONITORING AND CALIBRATION TECHNIQUE

The self-recovery capability of the LNA is realized by monitoring, calibration and compensation, as shown in Figure 6. The monitoring circuit monitors the I_d degradation and works together with the calibration circuit to control the compensation switch with the objective to keep I_d constant.

The self-recovery LNA has working mode and recovery mode as shown in Figure 7. During operation, the monitoring circuit should be activated periodically. In the working mode,

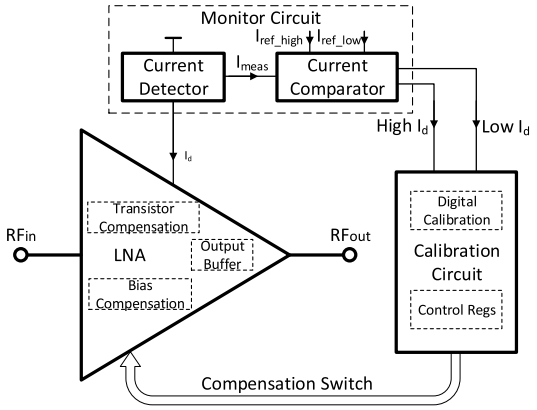

FIGURE 6. Structure of the self-recovery LNA.

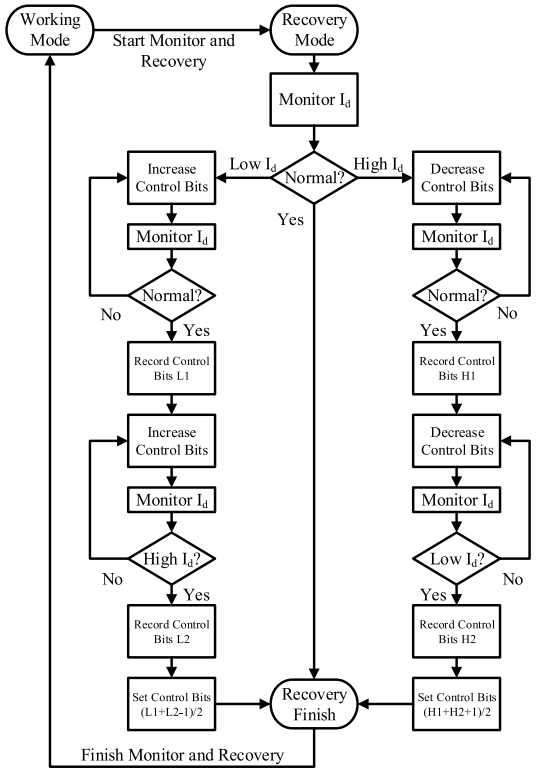

FIGURE 7. Workflow of the self-recovery mechanism.

the monitoring and calibration circuit are switched off and the LNA works normally.

In the recovery mode, the current detector monitors the biasing current of LNA, I_{meas}. The current detector is designed and implemented as shown in Figure 8. This current detector requires a small series resistance on the LNA current path. The value of the resistance must be low enough to prevent a significant impact on the performance of the LNA. The series resistance of the current detector is 1 Ω, and the bias current I_d of the LNA is 6.4 mA under normal working conditions. Therefore, the voltage drop on the series resistance R_{10} is 6.4 mV, which is much smaller than the power supply voltage of 1.2 V. The influence of the series resistance can be neglected. V_{bias_p} and V_{bias_n} can turn off the current

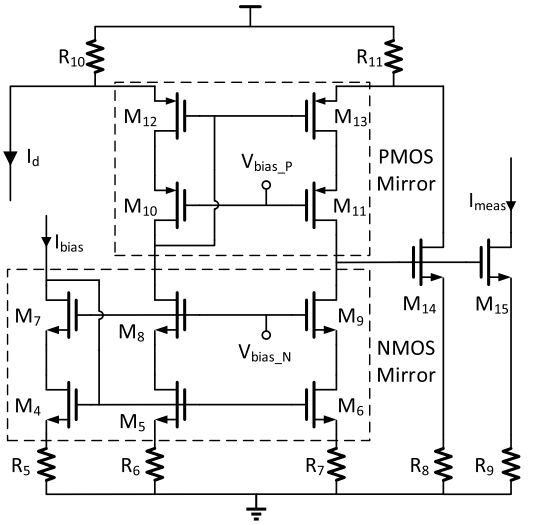

FIGURE 8. Schematic of the proposed current detector.

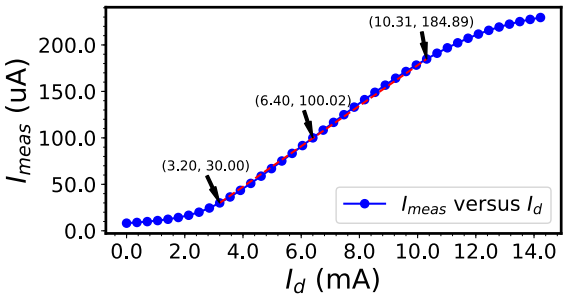

FIGURE 9. Output current of the current detector versus I_d.

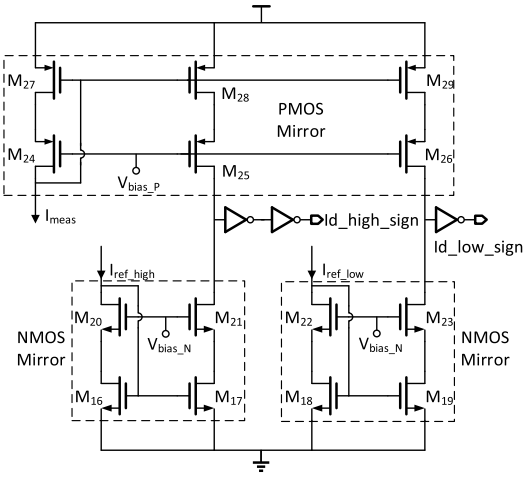

FIGURE 10. Schematic of the proposed current comparator.

monitor under normal working condition. The characteristics of the current detector is shown in Figure 9. I_{meas} is a linear function of I_d when I_d is between 3.2 mA and 10.31 mA.

The structure of current comparator is shown Figure 10. The current comparator determines whether I_d is normal by comparing I_{meas} with I_{ref_high} and I_{ref_low}. We set the normal working range of the current comparator to be within ±10%. Two reference currents I_{ref_high} and I_{ref_low} for the current comparator represent ±10% variation from the measured

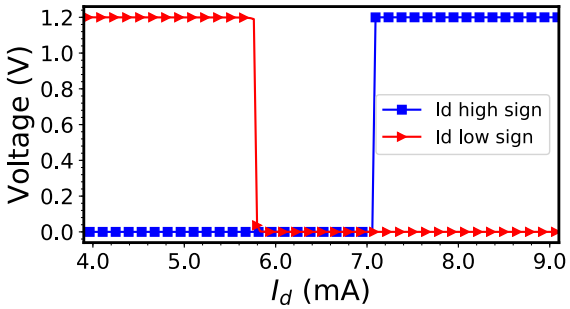

FIGURE 11. Output of the current comparator versus I_d.

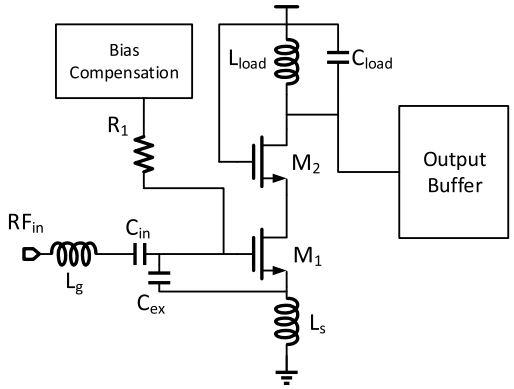

FIGURE 12. PCSNIM LNA with biasing compensation.

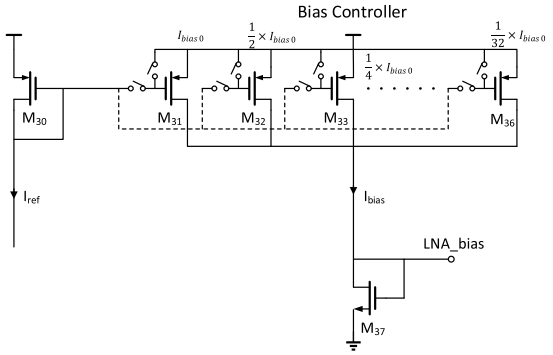

FIGURE 13. Circuit schematic of biasing compensation.

current I_{meas}, respectively. When $I_{ref\_low} \leq I_{meas} \leq I_{ref\_high}$, LNA is considered to be in the normal state. The compensation mechanism will be triggered if the current was out of the range, i.e., $I_{meas} < I_{ref\_low}$ or $I_{meas} > I_{ref\_high}$. Simulation result of the current comparator is shown in Figure 11. When $I_{meas} < I_{ref\_low}$, Id_low_sign is set to 1.2 V. On the other hand, Id_high_sign is set to 1.2 V when $I_{meas} > I_{ref\_high}$.

C. COMPENSATION

A biasing compensation circuit (Figure 12), which adjusts the biasing current and g_m of transistor M_1 by adjusting the biasing voltage of transistor M_1, and thus realizing the performance compensation. The biasing circuit is shown in Figure 13. It consists of a current mirror controlled by a reference current plus switch. By gradually turning on the current mirror M_{31}-M_{36}, a biasing current change of 1-1.97 times can

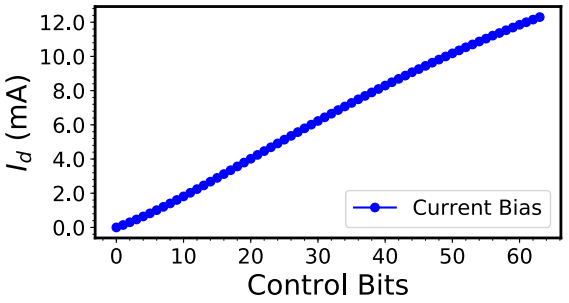

FIGURE 14. DC current I_d versus control bits under normal operation state.

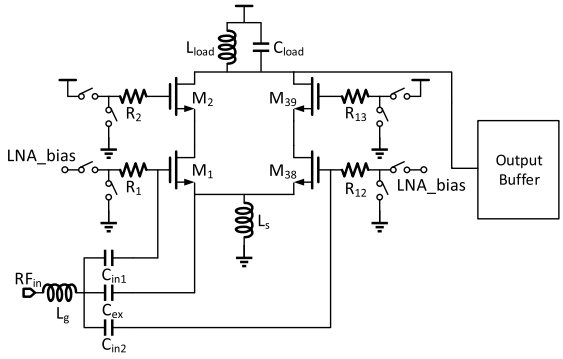

FIGURE 15. Circuit schematic of transistor compensation.

be achieved. We use the M_{31}-M_{36} current mirrors according to the 6-bit binary code. The M_{31} weight is the largest, and the M_{36} weight is the smallest. A binary-weighted current source can determine the total biasing current. The simulation of biasing current is shown in Figure 14.

The biasing compensation has a limit. It can only compensate for the shift of the threshold voltage, but it cannot compensate for the decrease of the carrier mobility. With the transistor aging, the biasing voltage increases progressively, causing the static operating point of the transistor enter into the unsaturated region. Then the biasing method cannot be used for compensation. In this case, the method of transistor replacement is used in this work. When the biasing compensation fails to compensate the current to the normal level, the replacement transistor will be turned on, and thus the performance of LNA will be compensated. The circuit schematic of the transistor compensation is shown in Figure 15. At the beginning, transistors M_1 and M_2 are on, while M_{38} and M_{39} are off. When the switch of the transistor compensation is turned on, M_1 and M_2 are off, while M_{38} and M_{39} are on. The simulation result of the LNA with the transistor replacement compensation circuit is shown in Figure 16. The transistor replacement compensation circuit almost has no effect on the performance of the LNA.

The collaborative workflow of monitoring, calibration and compensation is shown in Figure 7. The calibration circuit will select the best control bits for the compensation circuit to ensure the LNA is in the normal state. The simulation results of the LNA biasing current I_d and g_m of transistor M_1 are shown in Figure 17. As can be seen in Figure 17, g_m and I_d

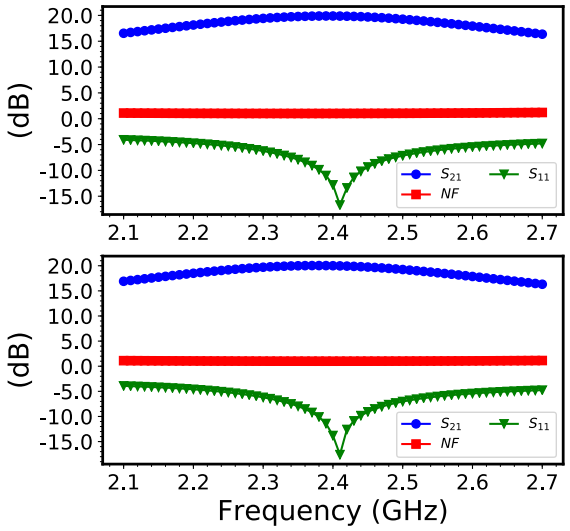

FIGURE 16. Simulated results of LNA without and with transistor compensation.

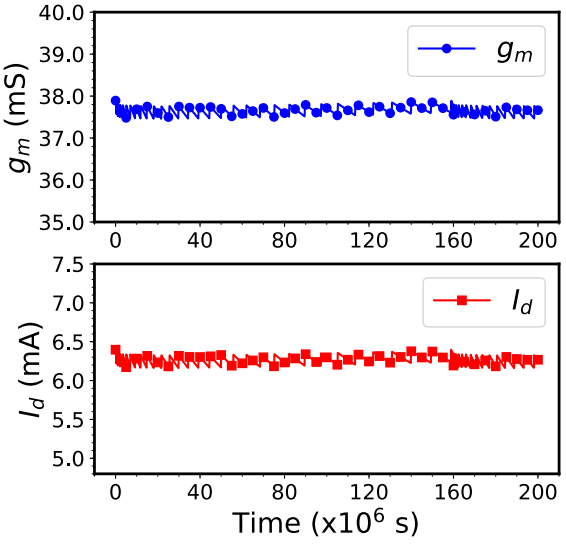

FIGURE 17. Simulated results of g_m and I_d versus aging time with compensation.

are almost constant, and no significant degradation occurs when the compensation module is in operation. The simulated performance of the LNA is shown in Figure 18. S_{21} and *NF* remain 19.8 dB and 1.05 dB respectively. S_{11} fluctuates between −16 dB and −14 dB. To summarize, S_{11}, S_{21}, and *NF* of LNA do not deteriorate significantly after the monitoring recovery circuit turns on.

IV. MEASUREMENT RESULTS

The proposed self-recovery capability was verified on a 2.4 GHz CMOS LNA manufactured with a 130 nm CMOS technology. Figure 19 shows the die photograph of the LNA with the monitoring and self-recovery circuits. The chip area is 1.14 mm×0.82 mm. Accelerated aging tests at a high temperature with voltage overstress [26], [27] were carried out. The chips were stressed with the bias voltage of 1.44 V, which is 120% of the supply voltage, at the temperature of 120°C

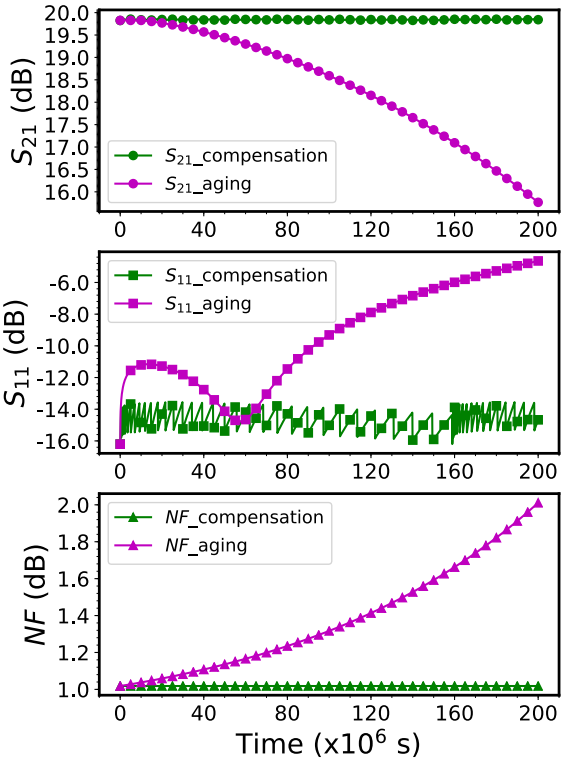

FIGURE 18. Simulated results of S_{21}, S_{11} and *NF* versus aging time.

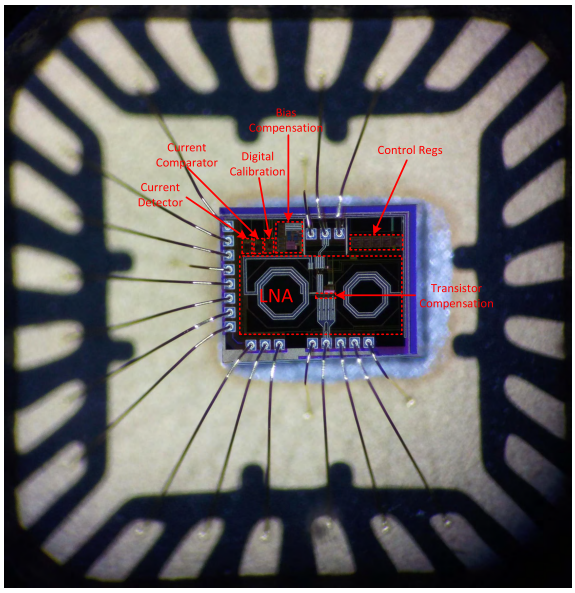

FIGURE 19. Die photograph of the LNA with self-monitoring and self-recovery circuits.

for 400 hours. The measurement results of the fabricated chips are summarized in Table 2.

The degradation and compensation experimental results of LNA are shown in Figure 20. As can be seen in Figure 20, after 400 hours of stress, without the compensation mechanism, the parameters including S_{21}, S_{11}, and *NF* of LNA have undergone a significant degradation, i.e., S_{21}, S_{11}, and *NF* deteriorates 1.9 dB, 6.1 dB and 0.57 dB respectively.

TABLE 2. Summary of chip measurements.

Technology	GSMC 7RF 130nm CMOS
Power Supply(nominal/stressed)	1.2 V / 1.44 V
Temperature(nominal/stressed)	27 °C / 120 °C
S_{11}(nominal/stressed)	-14.2 dB / -8.1 dB
S_{21}(nominal/stressed)	18.2 dB / 16.3 dB
NF(nominal/stressed)	1.45 dB / 2.02 dB
S_{22}(nominal/stressed)	-12.1 dB / -12.1 dB
Power consumption(nominal/stressed)	8.07 mW / 3.75 mW
Chip area	1.14 mm*0.82 mm

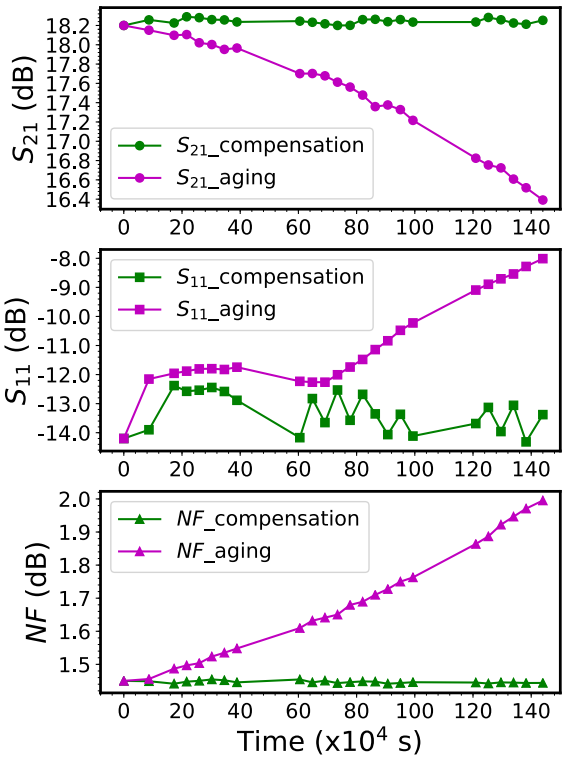

FIGURE 20. Experimental demonstration of the compensation effect of the proposed self-recovery technique. S_{21}, S_{11} and NF of the LNA.

However, when the monitoring and recovery circuits are turned on, S_{21}, S_{11}, and NF of LNA remain almost constant, showing the excellent self-recovery capability.

V. CONCLUSION

In this paper, we propose a LNA having the self-recovery capability to counter the HCI degradation. The self-recovery module has both the degradation monitoring and compensation functions. The compensation function can be triggered automatically based on the result of the monitoring process. With the self-recovery capability, the performance of LNA can be maintained over time under HCI stress. This technique has been proved to be efficient by the experiment carried out with the LNA fabricated with a 0.13 μm CMOS process.

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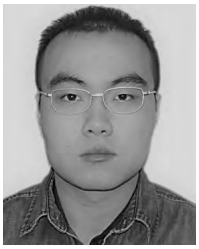

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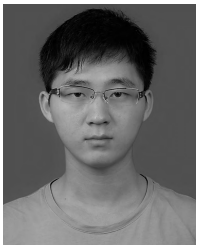

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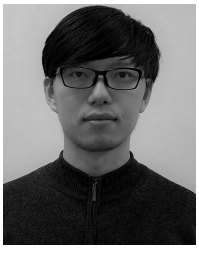

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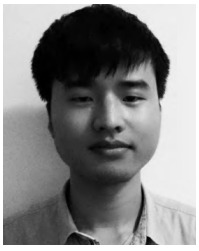

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