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Realization of a Large Values Floating and Tunable Active Inductor

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ABSTRACT This paper presents a new design for active inductor (AI) realization in addition to capacitance and resistance multipliers. The design uses one current conveyor (CCII±) and one dual-output transconductance amplifier(DO-OTA) and a grounded capacitor. The functionality of the design is confirmed using experimental verification and simulation. Simulation results show that the realized inductance is tunable be tuned from few mH to 2H and more and the multiplication factor for the resistance multiplier is more than 2200 while the capacitance multiplication factor is around 500. A CMOS version of the AI is designed and simulated using Tanner Tspice in 0.18μm CMOS technology. The simulation results confirm the functionality of the design.

INDEX TERMS Tunable active inductance, resistance multiplier, capacitance multiplier, integrated circuits.

I. INTRODUCTION

Active inductors are used in many applications such as Wilkinson power drives, phase shifters, active filters, oscillators, low noise amplifiers and matching networks [1]. There are many existing approaches to design floating inductors [1]– [15]. For example, the design in [1] used the Gyrator approach and the range of the active inductor was 6-284nH. In [2], the authors presented a grounded and floating active inductance simulator. Three Voltage Differencing Differential Input Buffered Amplifiers (VD-DIBAs) are used to realize the floating inductance. Each VD-DIBA requires three Operational Transconductance Amplifiers (OTA) and one current conveyor, in addition to a 2.2kΩ resistor. The design in [3] used two Z-copy Current Follower Current Controlled Conveyors (ZC-CFCCCs). A negative floating inductance was presented in [4]. It used three Current Feedback Operational Amplifiers (CFOA) and three passive components, two of which will control the value of the simulated impedance. The authors in [5] presented two floating inductance simulators. The main drawback of these two designs is the use floating capacitor between terminals X and Y and the maximum inductance in both designs is 1.1mH. The design in [6] proposed a CMOS floating inductor using the intrinsic capacitance of the transistor. The realized inductance was in the range 249nH-394nH. The design in [7] used Dual X Current Conveyor Differential Input Transconductance Amplifier (DXCCDITA) and two passive elements. The maximum inductance realized was 23.25mH. In [8] a new positive/negative floating inductance simulator is presented. Equation (8) in this design indicates that the inductance is proportional to the square of the temperature. In addition, the maximum inductance is 0.084mH. The design in [9] presented a novel floating lossy-inductance realization using two negative impedance converters and three passive elements. The work in [1] presented a floating inductance simulator. The design is based on using the parasitic capacitance of the MOSFETs and the maximum inductance was 300nH, which is suitable for high frequency applications. In [10], a general floating impedance simulator is presented. The design used two voltage difference current conveyors and five passive components. A grounded and floating inductance simulator is presented in [11]. The design used two-voltage differencing transconductance amplifier and requires matching conditions. In [12], a floating impedance simulator using grounded passive elements is presented. This work used four CCCII- and four passive elements and the maximum inductance is 0.5mH. A new floating inductor circuit is presented in [13]. It used two differential voltage current conveyor and two resistor and one capacitor. The inductance value was tuned by varying the resistor. In [14], a CCII based floating inductance simulator was presented. The design used four CCII and three

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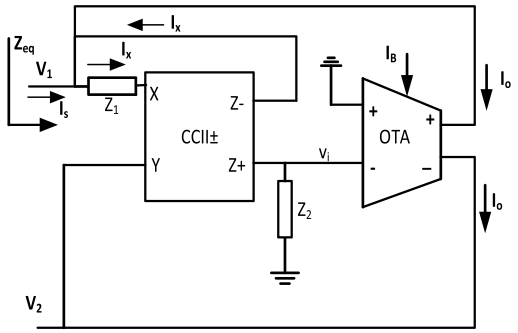

FIGURE 1. The circuit diagram of the proposed active inductor.

passive elements and the maximum inductance is 57.4μH. A tunable floating active inductor was presented in [15]. The design used three CCCII and floating capacitor and the maximum inductance was 100mH.

This paper presents a new design to realize a large value floating and tunable active inductor. The circuit can also be used as a capacitance and resistance multiplier with large multiplication factors. The developed circuit employs minimum number of passive components.

The rest of the paper is organized as follows: Section II presents the proposed design and mathematical analysis. Simulation and experimental results are given in section III. In section IV non-ideal analysis is presented. The paper conclusion is presented in section V.

II. PROPOSED DESIGN

The proposed design consists of CCII± and DO-OTA as shown in Figure 1.

With reference to Figure 1, assuming ideal devices, with $I_x = I_{z+} = -I_{z-}$ and the OTAs output currents are the same, the impedance seen between nodes V_1 and V_2 is given by:

$$Z_{eq} = \frac{V_1 - V_2}{I_s} = \frac{V_1 - V_2}{I_o} \tag{1}$$

$$I_o = -g_m \times V_i \tag{2}$$

$$V_i = -I_Z \times Z_2 = -I_x \times Z_2 \tag{3}$$

$$I_x = \frac{V_1 - V_2}{Z_1} \tag{4}$$

Combining equations 1-4, the equivalent impedance seen between terminals V_1 and V_2 is given by:

$$Z_{eq} = \frac{Z_1}{g_m Z_2} = \frac{2V_T Z_1}{I_B Z_2} \tag{5}$$

where $g_m = \frac{I_B}{2V_T}$ is the transconductance for BJT-based OTA, V_T is the thermal voltage and I_B is the bias current of the OTA (I_{abc}).

If Z_1 is replaced by a resistor R_1 and Z_2 is replaced by a capacitor C, then a tunable active inductor is realized and the equivalent impedance is given by:

$$Z_{eq} = \frac{s2V_T R_1 C}{I_B} = sk(2V_T c) = sL \tag{6}$$

where $L = k(2V_T c)$ and k is the multiplication factor $k = \frac{R_1}{I_B}$

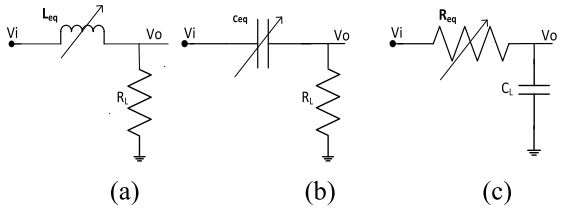

FIGURE 2. Circuits used to simulate the proposed design (a) Active inductor (b) Capacitance multiplier (c) Resistance multiplier.

It is clear that equation (6) realizes an active inductor whose inductance can be tuned using the bias current I_B and/or the resistor R_1. The bias current of the OTA can be varied from 2.5μA to 2000μA. If $R_1 = 10$k, using equation (6), the simulated inductance will be in the range of 2.5mH-2H. Higher inductance can be achieved by increasing the value of R_1.

On the other hand, if Z_1 is replaced by a capacitor C, and Z_2 by a resistor R_2, then a tunable capacitor multiplier is obtained and the equivalent impedance is given by:

$$Z_{eq} = \frac{2V_T}{I_B R_2 sC} = \frac{1}{skC} \tag{7}$$

where $k = \frac{I_B R_2}{2V_T}$, the bias current I_B and/or R_2 are used to tune the simulated capacitance.

Finally, if Z_1 is replaced by resistor R to be scaled and resistor R_2 replaces Z_2, a resistance multiplier is achieved and the equivalent impedance is given by:

$$Z_{eq} = \frac{2V_T R}{I_B R_2} = kR \tag{8}$$

where $k = \frac{2V_T}{I_B R_2}$

It is worth mentioning here that the equivalent impedance is proportional to temperature if BJT based OTA is used. If CMOS OTA is used, then the equivalent impedance will be less sensitive to temperature variation.

III. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

Simulation using PSPICE is used to confirm the functionality of the proposed circuit. The realized impedances are used in the design of filters with tunable cut-off frequencies as shown in Figure 2.

1) ACTIVE INDUCTOR

The proposed active inductor is used in the design of low pass filter with Z2 replaced by 10nF capacitor and Z1 = RL = 10Ω. The bias current I_B is swept from 2.5μA to 2000μA. The frequency response of the filter shown in Figure 3 confirms the functionality of the realized tunable inductor.

To compare the proposed design with the ideal design, the circuit was simulated with $I_B = 2.5\mu$A, $Z_1 = 10k\Omega$, to realize a 2H inductor and compared with the ideal one. The simulation results shown in Figure 4 indicate that the simulated inductor is in excellent agreement with the ideal one.

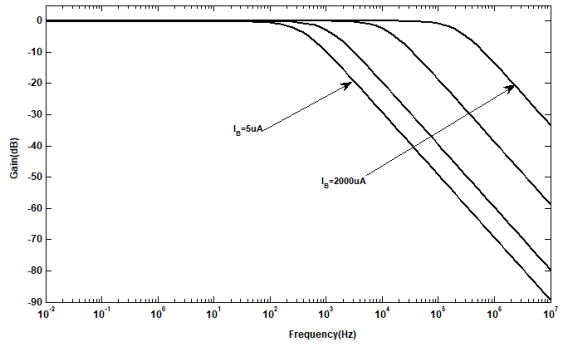

FIGURE 3. Frequency response of low pass filter using active inductor.

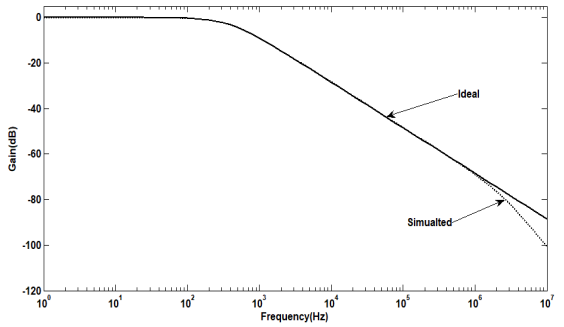

FIGURE 4. Frequency response for low pass filter using the realized and the ideal inductor.

It is well known that the current conveyor input resistance (r_x) is finite. This resistance can replace Z_1 if only one passive element is to be used. In this case the realized inductance will be in mH range because r_x is small (50Ω for AD844). The inductance value is given by:

$$L = \frac{2V_T r_x C}{I_B}. \tag{9}$$

2) CAPACITANCE MULTIPLIER

Similarly, for the capacitance multiplier, the design of a tunable RC high pass filter is used with Z_1 being replaced by a10nF capacitor and $Z_2 = R_L = 10k\Omega$. The bias current is swept from 2.5μA to 2000μA. Simulation results shown in Figure 5 confirm the functionality of the capacitance multiplier with maximum multiplication factor of 500.

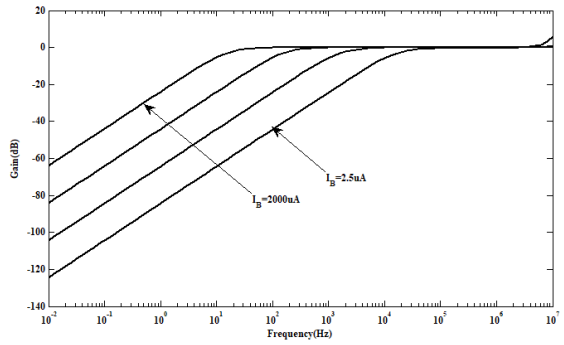

FIGURE 5. Frequency response for the tunable RC high pass filter using capacitance multiplier.

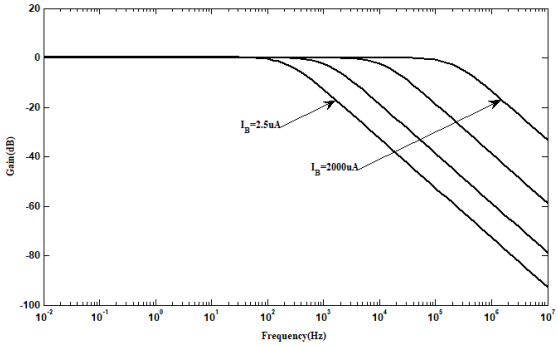

FIGURE 6. Frequency response for low pass filter using resistance multiplier.

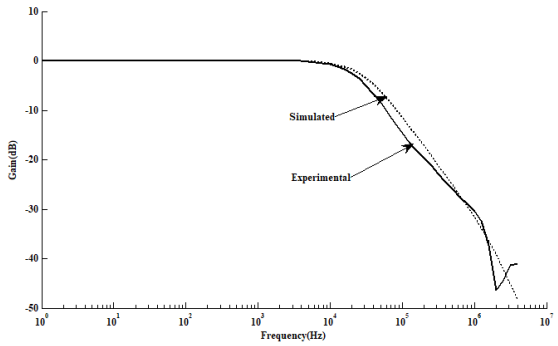

FIGURE 7. Experimental and simulated frequency response for low pass filter using the proposed inductor.

3) RESISTANCE MULTIPLIER

The resistance multiplier is used in the design of a tunable low pass filter with the resistance to be scaled $Z_1 = 100\Omega$, $Z_2 = 10\Omega$ and $C_L = 10$nF. The frequency response of the filter shown in Figure 6 confirms the functionality of the design. It is found that, for $I_B = 5uA$, a 100 Ω resistor is scaled up to 221kΩ(2210 time.

B. EXPERIMENTAL RESULTS

A low pass filter was implemented using AD844 and LM13700AN, $R_1 = R_L = 10K\Omega$, C=10nF and the supply voltage is ±5V. Since there is no commercially available CCII±, three AD844 are used to implement this device. The bias current was fixed to 180μA to realize 27.7mH inductor. The experimental and simulated frequency response of the filter are shown in Figure 7. It is found that the cut-off frequencies for the experimental and simulation results are 22KHz and 27KHz respectively. The sources of the error are the non-ideal behavior of the current conveyor and the OTA, in addition to the tolerance in the passive components used in the experiment.

The new active inductor is used in the design of a tunable band-reject filter with $C_1 = 10$nF, $R_L = 10k\Omega$ as shown in Figure 8.

Plots of the frequency response of the notch filter are shown in Figure 9. It is clear from figure 9 that the filter is functioning properly with tunable notch frequency.

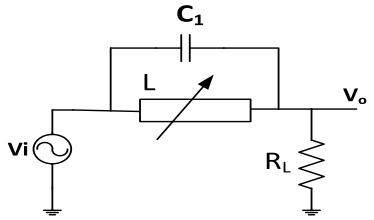

FIGURE 8. Circuit used to implement notch filter using the realize inductor.

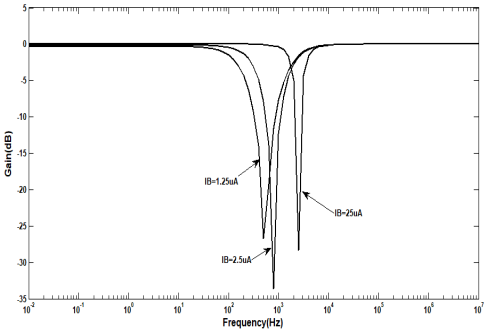

FIGURE 9. Frequency response for band reject filter using the prosed inductor.

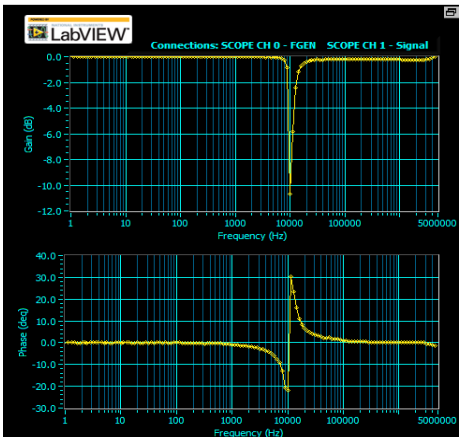

FIGURE 10. The experimental frequency response for notch filter using the proposed active inductor.

The notch filter was implemented using the same components used in simulation with $I_B = 583\mu$A. The experimental results shown in Figure 10 confirm the functionality of the design. It is clear from the figure that the notch frequency is 10KHz while the simulated frequency for the same bias current is 12KHz. The error is due the non-ideality and tolerance in the components used in the hardware implementation.

IV. NON IDEAL ANALYSIS

Assuming that the output currents of the current conveyor are not tracking the input current, that is

$I_{Z-} = -\propto I_x$ and $I_{Z+} = \propto I_x$, the equivalent impedance of figure1 is given by:

$$\frac{1}{Z_{eq}} = \frac{1-\propto}{Z_1} + \frac{\propto g_m Z_2}{Z_1} \tag{10}$$

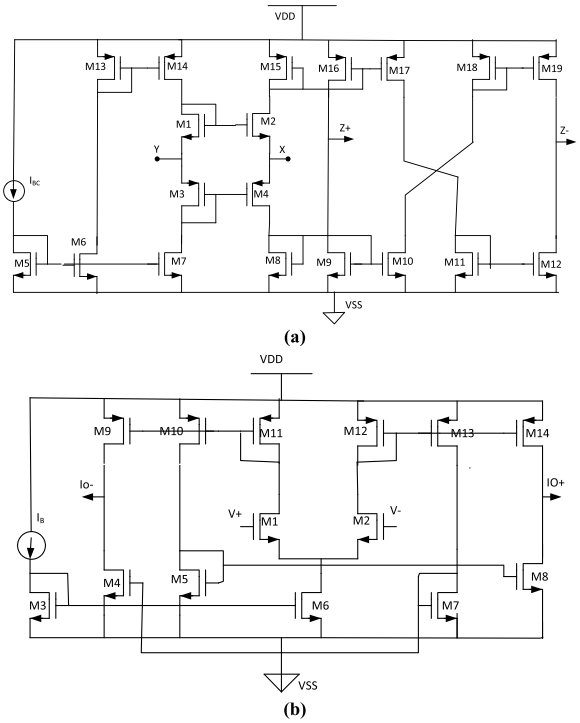

FIGURE 11. CMOS Cells (a) CCII± (b) DO-OTA.

If Z_1 is replaced by a resistor R_1, and Z_2 is replaced by a capacitor C, then equation (10) is rewritten as:

$$\frac{1}{Z_{eq}} = \frac{1-\propto}{R_1} + \frac{\propto g_m}{R_1 sC} = \frac{1-\propto}{R_1} + \frac{1}{sL} = \frac{1}{\frac{R_1}{1-\propto}} + \frac{1}{sL} \tag{11}$$

where $L = \frac{R_1 C}{\propto g_m} = \frac{2V_T R_1 C}{\propto I_B}$

Equation (11) indicates that the equivalent impedance consists of an inductor in parallel with a resistor. If $\propto = 1$, then equation (11) is reduced to equation (6). On the other hand, if $\propto$ varies by 1%, then a resistor in parallel with L exists and the value of this resistor equal to $\frac{R_1}{1\pm 0.01} = 0.99R_1$ or $1.01R_1$. By making R_1 large, it will have no effect in low frequency range.

If we consider the effect of r_x, then Z_1 is replaced by $R_1 + r_x$ and Z_2 is replaced by a capacitor C, then equation (10) is rewritten as:

$$\frac{1}{Z_{eq}} = \frac{1-\propto}{R_1 + r_x} + \frac{\propto g_m}{(R_1 + r_x)\, sC} = \frac{1}{\frac{R_1 + r_x}{1-\propto}} + \frac{1}{sL} \tag{12}$$

where $L = \frac{2V_T (R_1 + r_x) C}{\propto I_B}$

It is clear from equation (12) that the non-ideal behavior of the current conveyor will be the main source of the error, in addition to the inequality of the output currents of the OTA.

The CMOS version of the CCII± and the DO-OTA cells used in the design of the proposed active inductor are shown in Figures 11a and b respectively. The aspect ratio of all transistors are given in Table 1.

A CMOS based active inductor notch filter is designed using the above cells. The filter was simulated using Tanner Tspice simulation tools in 0.18μm TSMC CMOS technology.

TABLE 1. Transistors aspect ratios.

CCII±	M1-M2	6.1/.18	M5-MN128	3.1/1
	M3-M4	18.5/0.18	M13-M19	9.25/1
DO-OTA	M1, M2, M3	4/1	M4-M6	10/1
	M9-M14	10/1		

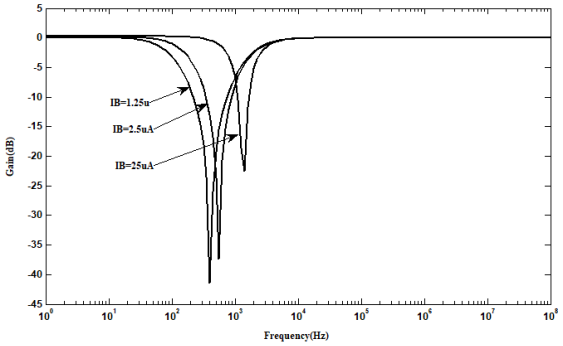

FIGURE 12. Frequency response for notch filter using TSMC 0.18μm CMOS technology.

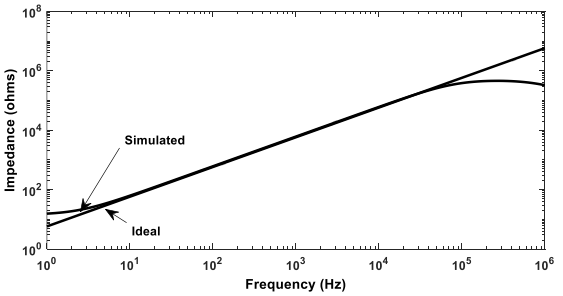

FIGURE 13. The magnitude of the active inductor as a function of frequency.

The frequency response of the filter shown in Figure 12 confirms the functionality of the design. It is worth mentioning here that the values of the inductance will not be the same because the transconductance of the CMOS OTA operating in saturation region is proportional to $\sqrt{I_B}$ and equation (6) becomes

$$Z_{eq} = \frac{sCR_1}{\sqrt{K_n I_B}} = sL \tag{13}$$

where $L = \frac{CR_1}{\sqrt{K_n I_B}}$

Consequently, the notch frequencies will not be the same as the ones in Figure 9.

In order to investigate the performance of the proposed inductor as a function of the frequency, the frequency response of the simulated and ideal inductor was measured. Figure 13 shows that the simulated inductor works properly in the frequency range 5Hz –to−80kHz.

V. CONCLUSION

A new design to realize a large active inductor with wide tuning range has been presented. The proposed circuit can be used as a resistance and capacitance multiplier with large multiplication factors. Simulation and experimental results to confirm the functionality of the proposed design are also presented. The design functionality is confirmed using commercially available integrated circuits and simulated using 0.18μm TSMC CMOS technology. The proposed circuit can find many applications in analog filters and in applications requiring the implementation of large time constant values in small silicon area or application where large active inductor is required.

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