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Capacitor Balancing and Common-Mode Voltage Reduction of a SiC Based Dual T-Type Drive System Using Model Predictive Control

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ABSTRACT The dual T-type multilevel converter (MLC) is an advanced topology with a reduced switching device count compared to a conventional diode clamped converter. This paper proposes a reduced switching state model predictive control (MPC) of a dual T-type drive system considering the DC link capacitor balancing, the common-mode voltage (CMV) along with torque control of an open-ends induction motor. The proposed study addresses the CMV in two different scenarios; i.e., the CMV reduction (CMVR) and CMV elimination (CMVE). A Matlab simulation for the proposed drive system is presented. A dual T-type converter prototype based on Silicon-Carbide discrete MOSFET switch is designed, implemented, and tested in the laboratory. The proposed MPC scheme achieves the torque command as well as balances the dual DC links in an efficient manner. It is observed that the CMVE has some limitation compared to CMVR, particularly at rated speed operation. It is worth mentioning that the proposed reduced switching states technique could reduce the computation time from 5.5 ms to 140 μs for CMVR and 70 μs for CMVE. In addition, the results demonstrate the effectiveness of CMVR scheme in reducing the harmonic contents, the torque and flux ripples, and converter switching loss compared to the CMVE scheme.

INDEX TERMS Multilevel converter, model predictive control, capacitor balancing, common-mode voltage.

I. INTRODUCTION

T-type multilevel converters (MLCs) are the developed reduced switching element topologies of the conventional diode clamped converter (DCC). Compared to two-level (2L) voltage source converters (VSCs), the T-type MLC is preferred due to lower harmonic contents which is essential in any industrial drive application [1]. Furthermore, compared to conventional DCCs, the T-type reduces the converter losses by 30-40 % at a certain switching frequency range (up to 12 kHz)[2]–[5].

Recently, model predictive control (MPC) proved its efficiency and competence to classical control methods for drive power converters [6]–[8]. In particular, finite control set MPC (FCS-MPC) suits the discrete nature of power converter and represents a potential alternative to avoid sophisticated pulse width modulation techniques required for complex power converters [9], [10]. In FCS-MPC, the converter voltage vectors (VVs) are tested individually in a predefined cost function. The VV that minimizes the cost function will be selected as the optimal one and applied on the next control sample. The cost function normally consists of summations of predicted deviations of the controlled variables compared with their reference values. Therefore, not only torque and flux can be controlled in electrical motor drives, but also capacitor balancing and common-mode voltage (CMV) mitigation of multilevel converters can be realized in the same cost-function.

The three-level (3L) T-type capacitor voltage balancing has been investigated using pulse-width modulation (PWM) technique in [11]–[14] and using MPC in [9]. However, the extension of these techniques to five-level (5L) converters

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has some technical limitations in terms of computation and execution times. A 5L Nested DCC capacitor balancing has been studied using MPC in [15], [16]. As far as the authors know, only one study in [17] has investigated the capacitor balancing of the dual T-type topology using switching state redundancy based on off-line study.

Another related important problem in AC drives is the CMV. This CMV affects the bearing of the induction motor (IM) and reduces its lifetime [17], [18]. Two well-known approaches were presented to solve this problem, namely CMV reduction (CMVR) and CMV elimination (CMVE). The CMVE method is based on selecting the VVs that produce zero CMV. This technique reduces the number of possible VVs for the drive system control. On the other hand, the CMVR decreases the CMV value by PWM techniques or using MPC technique [20]. Some studies investigated the CMVR using PWM techniques for different converters. In [21], synchronous optimal PWM technique was used to reduce the CMV of a modular MLC connected to an open ends induction motor (OEIM). However, this MLC topology has the drawback of having separate capacitors for each switching module (half H-bridge topology) which increases the power circuit complexity. In [22], a carrier based PWM is used to reduce the CMV of a 2L matrix converter. However, due to its protection issues, the matrix converter is not widely used in industrial drive applications. The study in [23] introduced the CMVR and capacitor balancing of 3L T-type MLC using finite control set (FCS) MPC. The study presented 19 switching states to mitigate CMV. It was reported that the MPC code consumes 100 μs, which is considered high for 3L converters. Although CMVE reduces the eddy currents in bearings, a little work in literature has addressed its impact on core losses. It was demonstrated that CMVE has a negative impact on core losses due to harmonic increase in the absence of some voltage vectors at the CMVE technique [24]. Therefore, the CMVR will be investigated in this study to achieve better drive system performance and lower harmonic contents.

To perform the MPC for the proposed topology, 729 switching states have to be considered in the MPC code to select the optimum cost function solution. This test is performed within this study and it was observed that the execution time was 5.5 ms, which is not suitable for this application. To the best of authors' knowledge, no detailed study on the CMVR or CMVE for the dual T-type drive system has been introduced. Furthermore, there is a lack of comprehensive studies on balancing the DC link capacitors of the proposed converter using MPC.

Recently, Silicon Carbide (SiC) MOSFET has been used in power electronic converters. This technology gives the MOSFETs device the advantages of lower energy consumption during turning on/off transitions as well as lower turning-on resistance compared to silicon IGBT switches [20]. However, the fast on/off transitions affect the edging of the converter output voltage if the electromagnetic interference (EMI) is not considered during the converter design. Therefore, the use of the SiC MOSFETs in complicated power circuits, as the case in 5L converters, needs deep investigations.

In view of the aforementioned issues, the target of this paper is to develop a reduced switching state MPC technique considering CMVE/CMVR, DC link capacitor balancing along with machine torque control. The proposed switching state model aims to reduce significantly the computation time and to improve substantially the MPC performance. This study is conducted on a dual T-type topology connected to an OEIM coupled with a DC generator as a mechanical load. The effectiveness of the proposed MPC technique is assessed in terms of torque and flux ripples, capacitor voltage deviation, and harmonic analysis of the generated voltage and current. A laboratory prototype has been designed and built using the advanced semiconductor technology of SiC MOSFET. The close agreement between the simulation and experimental results confirm the efficacy of the proposed approach. Hence, the contributions of this study can be summarized as follows:

- A fast MPC technique with reduced switching states has been developed for torque control, capacitor balancing, and CMVR/CMVE for the dual T-type 5L converter.
- A SiC-based 5L dual T-type MLC has been designed, tested, and implemented.
- A comprehensive comparison between CMVR and CMVE in the dual T-type topology has been carried out. The results confirm the superiority of CMVR technique.

This paper is organized as follows: a brief description for the dual T-type topology modeling and operation is presented in section II. Investigations of capacitor balancing and CMV for the dual T-type topology are discussed in Section III. In Section IV, the MPC of the three-phase OEIM considering capacitor balancing, CMVE and CMVR is presented. The experimental setup for the proposed drive system is demonstrated in Section V. The simulation as well as the experimental results for the proposed study are discussed and analyzed in Section VI. Finally, the study conclusion is derived in Section VII.

II. MODELING AND OPERATION OF A DUAL T-TYPE MLC

Fig. 1 shows the power circuit of a dual T-type 5L converter topology connected to a three-phase OEIM. Each 3L T-type topology consists of twelve semiconductor switches and can be classified as horizontal switches (Q_{2x} and Q_{4x}; x is a, b and c) and vertical switches (Q_{1x} and Q_{3x}). The following subsections describe the operation and the mathematical modeling of the dual T-type topology.

A. MATHEMATICAL MODEL OF A DUAL T-TYPE CONVERTER

The switching function model is a mathematical representation for the voltage source converters that aims to obtain a clear vision of the converter switching states (SS) [25]. Based on switching functions, a proposed model for the dual T-type advanced topology is derived as follows. The modes of operation of the dual T-type converter is summarized in TABLE 1. Assuming m_X is the switching function to connect

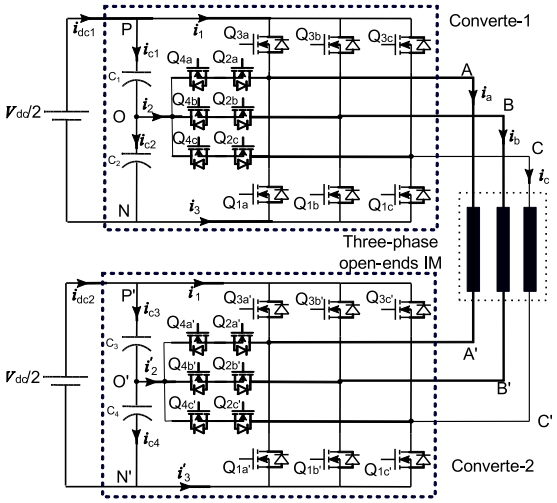

FIGURE 1. Wiring diagram of a dual T-type 5L converter connected to three-phase OEIM.

TABLE 1. Modes of operation of a dual T-TYPE: Phase AA.

Converter-1	m_A	point	Converter-2	m_A'	point
Q_{3a},Q_{4a}	1	P	Q_{3a}',Q_{4a}'	1	P′
Q_{2a},Q_{4a}	0	O	Q_{2a}',Q_{4a}'	0	O′
Q_{1a},Q_{2a}	-1	N	Q_{1a}',Q_{2a}'	-1	N′

phase X to P, N or O (Fig. 1), where X is A, B or C for converter-1, while converter-2 has the same symbols with a prime. This switch function can be 1, −1 or 0 as clarified in TABLE 1. The phase voltages for each T-type converter can be described by

$$v_{XO} = 0.25\, m_X V_{\rm dc},\ v_{X'O'} = 0.25\, m'_X V_{\rm dc} \quad (1)$$

Applying KVL, the voltage across AA′ can be described by:

$$v_{AA'} = v_{AO} + v_{OO'} - v_{A'O'} \quad (2)$$

For a balanced load, the summation of the three-phase voltages equals zero. The voltage $v_{OO'}$ can be described by:

$$-v_{OO'} = \frac{1}{3}\left(v_{AO} + v_{BO} + v_{CO} - v_{A'O'} - v_{B'O'} - v_{C'O'}\right) \quad (3)$$

By substituting (1) and (3) into (2), the phase voltage $v_{AA'}$ can be expressed as:

$$v_{AA'} = \frac{V_{dc}}{6}\left(m_A - m_{A'} - \frac{1}{2}(m_B - m_{B'} + m_C - m_{C'})\right) \quad (4)$$

The voltages $v_{BB'}$ and $v_{CC'}$ can be derived in the same way. By applying the switching function possibilities to (4), the phase-voltage can obtain 17 different voltage levels similar to any 5L converter.

B. OPERATION OF DUAL T-TYPE CONVERTER TOPOLOGY

The possible connections for phase A of one T-type converter can be described in TABLE 2. Similarly, the possible connections for phase $V_{AA'}$ for the dual T-type converter topology are described in TABLE 3. The possible SS for a 3L T-type converter can be calculated by m^3, where m is the number of voltage levels in the connected DC link, which gives 27 states in this case [10].

However, this relation is not applicable for the dual converter configuration as the DC links are isolated. The total number of SS for the dual T-type converter is $27^2 = 729$ states. By applying these 729 states, the vector diagram of this converter can be described by the hexagon as shown in Fig.2 (5L vector diagram). It consists of 61 vectors, i.e. O, a_1-a_6, b_1-b_{12}, c_1-c_{18}, and d_1-d_{24}. The summary of the 729 switching states and their corresponding voltage vectors is listed in TABLE 4. More details about the switching states of this converter can be found in [26].

TABLE 2. Possible Connections for Phase A of the 3-level T-type.

Level	Q_{1a}	Q_{2a}	Q_{3a}	Q_{4a}	V_{AO}
P	0	0	1	1	$+V_{dc}/2$
O	0	1	0	1	0
N	1	1	0	0	$-V_{dc}/2$

TABLE 3. Possible connections for phase A of the dual T-type.

Converter I	Converter II	Points	$V_{AA'}$
Q_{3a},Q_{4a}	$Q_{1a'}$,$Q_{2a'}$	P-N′	$+V_{dc}$
Q_{3a},Q_{4a}	$Q_{2a'}$,$Q_{4a'}$	P-O′	$+V_{dc}/2$
Q_{2a},Q_{4a}	$Q_{1a'}$,$Q_{2a'}$	O-N′	
Q_{3a},Q_{4a}	$Q_{3a'}$,$Q_{4a'}$	P-P′	0
Q_{2a},Q_{4a}	$Q_{2a'}$,$Q_{4a'}$	O-O′	
Q_{1a},Q_{2a}	$Q_{1a'}$,$Q_{2a'}$	N-N′	
Q_{2a},Q_{4a}	$Q_{3a'}$,$Q_{4a'}$	O-P′	$-V_{dc}/2$
Q_{1a},Q_{2a}	$Q_{2a'}$,$Q_{4a'}$	N-O′	
Q_{1a},Q_{2a}	$Q_{3a'}$,$Q_{4a'}$	N-P′	$-V_{dc}$

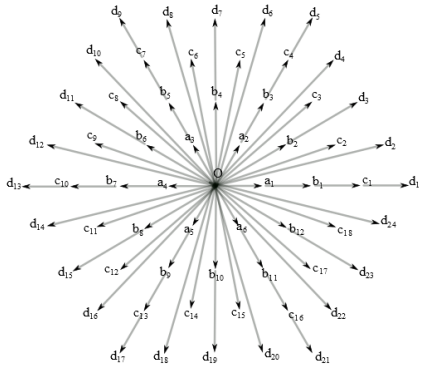

FIGURE 2. Vector diagram of the dual T-type MLC.

TABLE 4. CLASSIFICATION OF THE 729 SS ACCORDING TO THEIR GROUP EFFECTS.

Vectors	O	a_1-a_6	b_1-b_{12}	c_1-c_{18}	d_1-d_{24}
No-effect	45	-	132	-	24
High-effect	-	216	84	156	24
Medium-effect	-	-	48	-	-
No. of states/vector	45	216	264	156	48

III. CAPACITOR IMBALANCE OF DUAL T-TYPE TOPOLOGY

The switching state selection of the operating VV affects the capacitor charging state as well as the generated CMV value.

A. CAPACITOR BALANCING OF DUAL T-TYPE MLC

As the switching state affects the capacitor charging condition [20], an intensive study for all of the 729 states effect on the DC link capacitors is performed. A summary for the proposed study is illustrated in TABLE 4. The meaning of the group effect is described as follows: assuming the voltage imbalance is $\Delta V_c = V_{c1} - V_{c2}$ for Converter-1 and $\Delta V'_c = V_{c3} - V_{c4}$ for Converter-2. According to the imbalance value, the switching state effects can be classified as follows:

- High-effect group, in which ΔV_c or $\Delta V'_c$ tends to $V_{dc}/2$.
- Medium-effect group, in which ΔV_c or $\Delta V'_c$ tends to $V_{dc}/4$.
- No-effect group, in which ΔV_c or $\Delta V'_c$ tends to zero.

The use of the high- and medium-effect groups can change the capacitor balancing state. Hence, the high number of SS of these two groups (528 out of 729 states) gives high flexibility in selection decision to balance the four capacitors voltages. It is worth to mention that a proposed set of 219 SS, out of 528, is selected in such a way to represent all of the 61 VVs and include both of high- and medium-effect SS groups. Therefore, 219 out of 729 SS are sufficient to perform the capacitor balancing and reduce the MPC execution time.

B. CMV OF A DUAL T-TYPE MLC

CMV is a relatively high frequency voltage that appears between the two isolated ground systems [18]. In AC drives, this voltage appears between the machine neutral point and the connected inverter DC link midpoint [21]. For the dual T-type configuration, this voltage is the difference between the dual converter two mid-points [20]. The CMV cannot be eliminated by using 2L inverter SS. This results from the third harmonic component that exists at all the VVs of the 2L inverter. However, in MLCs, there are some VV produce zero CMV (ZCMV). If a converter is controlled to operate at these vectors, the CMV will not appear in the drive system.

The CMV for the dual T-type MLC can be calculated as:

$$\begin{aligned} v_{\mathrm{CM1}} &= 1/3\,(v_{AO} + v_{BO} + v_{CO}) \\ v_{\mathrm{CM2}} &= 1/3\,(v_{A'O'} + v_{B'O'} + v_{C'O'}) \\ v_{\mathrm{CM}} &= v_{\mathrm{CM1}} - v_{\mathrm{CM2}} \end{aligned} \tag{5}$$

A proposed intensive study for the different 729 SS is executed in order to reflect how each state and VV can contribute to the CMV. A summary for the proposed study is listed in TABLE 5. It can be observed that:

- 42 VVs, out of 61, can produce CMV with different values.
- The zero vector "O" can produce CMV with different values and can produce ZCMV.
- 18 VVs, out of 61, produce only ZCMV.

Hence, the CMV in dual T-type configuration is not a VV dependent like other DCCs. However, it is considered SS dependent. For instance, vector "O" can be represented by 45 SS. Only 27 SS produce ZCMV and the other 18 SS produce CMV value. A part of VVs produces ZCMV for all of SS. These ZCMV are described in TABLE 5 and shown in Fig.3. It can be observed that only 19 VVs can produce ZCMV while 42 VVs are not. The absence of the highest VVs, d's vectors, will affect the output voltage level, which requires extra DC link voltage.

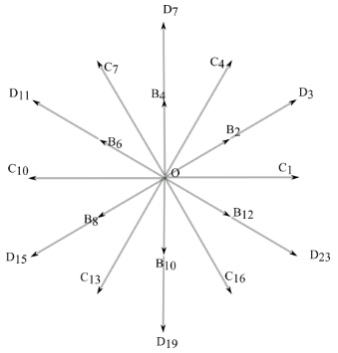

FIGURE 3. ZCMV vector diagram for dual T-type MLC.

TABLE 5. Classification of the 729 SS according to their CMV.

Vectors	O	a_1-a_6	b_1-b_{12}	c_1-c_{18}	d_1-d_{24}
Number of SS	45	216	264	156	48
CMV appear	18	216	192	132	30
ZCMV	27	0	72	24	18
ZCMV Voltage Vectors	O	-	b_s; s is even	c_1, c_4, c_7, c_{10}, c_{13}, and c_{16}	d_3, d_7, d_{11}, d_{15}, d_{19}, and d_{23}

IV. MODEL PREDICTIVE CONTROL OF DUAL T-TYPE DRIVE

Fig. 4 illustrates the schematic diagram of Torque Predictive Control (TPC) of IM drive. The torque reference is generated from the outer speed control loop via a proportional integral (PI) controller. Flux reference is assumed constant. The machine model is used for predicting the future torque and flux based on the measured and estimated states. Finally, an optimization step utilizes the reference and predicted quantities to generate the optimal gating signal for the next control sample, which will be applied to the converters. In this section, the mathematical models required for the estimation and prediction steps are explained.

A. INDUCTION MOTOR MODEL

The dynamic model of IM can be expressed using different representations depending on the reference frame used [27]. Considering stator reference frame with stator current and rotor flux as the state variables, the dynamic equations can be expressed using complex vector notation as follow [28]:

$$\dot{x} = Ax + Bu;$$

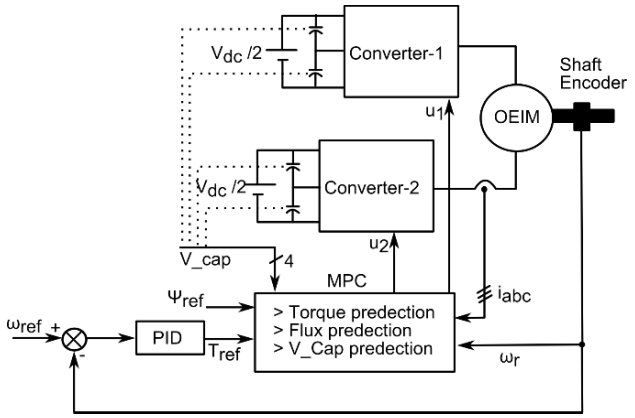

FIGURE 4. Schematic diagram of predictive torque control.

where:

$$A = \begin{bmatrix} \frac{-1}{\tau_\sigma} & 0 & \frac{k_r}{R_\sigma \tau_\sigma \tau_r} & \frac{k_r}{R_\sigma \tau_\sigma}\omega_r \\ 0 & \frac{-1}{\tau_\sigma} & -\frac{k_r}{R_\sigma \tau_\sigma}\omega_r & \frac{k_r}{R_\sigma \tau_\sigma \tau_r} \\ \frac{L_m}{\tau_r} & 0 & \frac{-1}{\tau_r} & -\omega_r \\ 0 & \frac{L_m}{\tau_r} & \omega_r & \frac{-1}{\tau_r} \end{bmatrix},$$

and

$$B = \begin{bmatrix} \frac{1}{R_\sigma \tau_\sigma} & 0 \\ 0 & \frac{1}{R_\sigma \tau_\sigma} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{6}$$

where $x = [i_s \psi_r]^T$ are the state variables, $u = u_s$ is the stator voltage vector, i_s is the stator current, ψ_r is rotor flux, R_s and R_r are stator and rotor resistances, L_s, L_r and L_m are stator, rotor, and mutual inductances, respectively. ω_r is electrical rotor speed. $k_r = L_m/L_r$ is the rotor coupling factor. $R_\sigma = R_s + k_r^2 R_r$ represents the equivalent resistance. $L_\sigma = L_s(1 - L_m^2/L_r)$ is the transient inductance of the machine. $\tau_r = L_r/R_r$ is the rotor time-constant. $\tau_\sigma = L_\sigma/R_\sigma$ is the stator transient time constant.

The electromagnetic torque can be calculated as:

$$T = 3/2 n_p(\psi_s \times i_s) \tag{7}$$

where n_p is the number of pole pairs and ψ_s is the stator flux.

The prediction step in MPC requires the knowledge of the discrete model of IM. Several discretization methods are available in literature [15]. For the sake of simplicity, Euler discretization method is used. The discrete state space model can be expressed using

$$\begin{aligned} x^{k+1} &= A_d x^k + B_d u^k \\ A_d &= I + T_s A \\ B_d &= T_s B \end{aligned} \tag{8}$$

where I is the identity matrix and T_s is the sampling time.

B. INVERTER OUTPUT VOLTAGE MODEL

Using the proposed switching-function model of the dual T-type converter, the applied stator voltage can be calculated as

$$u_s = u_{s\alpha\beta} = \mathrm{V}_{dc}/2(T_{Cl} S_{abc}^{Conv-1} - T_{Cl} S_{abc}^{Conv-2}) \tag{9}$$

where V_{dc} is the summation of the capacitor voltages, S_{abc}^{Conv-1} and S_{abc}^{Conv-2} are the switching function for the dual converters and T_{Cl} represents Clarke transformation.

$$T_{Cl} = \frac{2}{3}\begin{bmatrix} 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{10}$$

C. STATOR FLUX ESTIMATION

The rotor flux can be estimated from the rotor dynamics of IM expressed at the rotor reference frame as follows:

$$\psi_r + \tau_r d\psi_r/dt = L_m i_s \tag{11}$$

Then after using Euler discretization it can be expressed as:

$$\psi_r^k = \frac{L_r}{L_r + T_s R_r}\psi_r^{k-1} + \frac{L_m T_s R_r}{L_r + T_s R_r} i_s^k \tag{12}$$

D. TORQUE AND FLUX PREDICTION

Knowing the rotor flux and using current measurement, Eq. (8) can be used to predict rotor flux one-step ahead. Then stator flux can be calculated at the $k+1$ sample from:

$$\psi_s^{k+1} = k_r \psi_r^{k+1} + L_\sigma i_s^{k+1} \tag{13}$$

It should be noted that the variables in (8) and (13) are expressed in stator reference frame. Therefore, appropriate coordinate transformation should be considered. In order to compensate for the time delay caused by calculation process, the variables at sample $k+2$ can be calculated using the variables at instant $k+1$ as follows:

$$\begin{aligned} x^{k+2} &= \mathrm{A}_d x^{k+1} + \mathrm{B}_d u^{k+1} \\ \psi_s^{k+2} &= \mathrm{k}_r \psi_r^{k+2} + \mathrm{L}_\sigma i_s^{k+2} \\ T^{k+2} &= \frac{3}{2} n_p(\psi_s^{k+2} \times i_s^{k+2}) \end{aligned} \tag{14}$$

E. CAPACITOR VOLTAGE PREDICTION

For a capacitor, x:

$$dv_{Cx}/dt = i_{cx}/C_x \tag{15}$$

Using Euler discretization, the predicted capacitor voltage can be expressed as

$$v_{Cx}^{K+1} = v_{Cx}^K + i_{Cx}^{K+1}.T_s/C_x \tag{16}$$

The capacitor current can be obtained as a function of the three-phase currents and the SS.

Firstly, the capacitor currents can be expressed as a function of the currents i_1, i_2, and i_3 (See **Fig. 1**) as follows:

$$\begin{aligned} i_{C1} &= i_{dc1} - i_1 \\ i_{C2} &= i_{C1} - i_2 = i_{dc} - i_1 - i_2 \\ i_{C3} &= i_{dc2} - i'_1 \\ i_{C4} &= i_{C3} - i'_2 = i'_{dc} - i'_1 - i'_2 \end{aligned} \tag{17}$$

The objective of the controller is to maintain equal energy among the capacitors. Hence, the DC link currents $i_{dc1} = i_{dc2} = 0$ [29]. The capacitor currents can be written as

$$\begin{aligned} i_{C1} &= -i_1 \\ i_{C2} &= -i_1 - i_2 \\ i_{C3} &= -i'_1 \\ i_{C4} &= -i'_1 - i'_2 \end{aligned} \tag{18}$$

The currents i_1, i_2, i'_1 and i'_2 can be expressed as a function of the three-phase currents by means of SS as follows:

$$\begin{aligned} i_{1,2} &= m_A i_a + m_B i_b + m_C i_c \\ i'_{1,2} &= -m_A i_a - m_B i_b - m_C i_c \end{aligned} \tag{19}$$

where m_A, m_B and m_C are the switching functions. Similarly, the second horizon prediction can be performed similar to that of the flux and torque. The predicted currents can be obtained by the first relation in (14).

F. PROPOSED MPC TECHNIQUES

As mentioned earlier, the idea of the FCS-MPC is to calculate the model cost-function for all SS (729 in the dual T-type case). However, this huge number of SS needs long execution time for calculation (around 5.5 milliseconds using dSPACE 1103). This affects negatively on the performance of the drive system. In this work, two proposed scenarios are studied as follows.

Scenario-1: Consider the CMVR and use the proposed 219 SS for capacitor balancing.

Scenario-2: Consider CMVE switching states and investigate the performance of capacitor balancing using the proposed 115 CMVE SS only.

1) SCENARIO-1 (CMVR)

The target is to apply the capacitor balancing and the CMVR in the cost-function using the proposed 219 SS. As a result, the cost-function will include flux, torque, CMV and capacitor voltage deviations as:

$$\begin{aligned} J_1 &= \frac{\left|T^{ref} - T^{k+2}\right|}{T_{rated}} + K_\psi \frac{\left|\left\|\psi_s^{ref}\right\| - \left\|\psi_s^{k+2}\right\|\right|}{\|\psi_s\|_{rated}} \\ J_2 &= K_{dc}\left(\left|v_{C1}^{k+1} - v_{C2}^{k+1}\right| + \left|v_{C3}^{k+1} - v_{C4}^{k+1}\right|\right) \\ J_3 &= K_{cm}\left|v_{CM}\right| \\ J &= J_1 + J_2 + J_3 \end{aligned} \tag{20}$$

where T^{ref} and ψ_s^{ref} are the reference torque and stator flux respectively. T_{rated} is the rated torque and $\|\psi_{rated}\|$ is the rated stator flux magnitude. K_ψ, K_{dc}, and K_{CM} are the flux, capacitor voltage and CMV weighting factors. These factors determine the relative importance of flux, capacitor voltages and CMV errors. During the design process, these factors should be carefully tuned in order to obtain a satisfactory performance. The optimum vector is calculated by:

$$V_{opt} = \arg \min_{\{V_1..V_{219}\}} J\left(V_s^{k+1}\right) \tag{21}$$

A flow-chart for the proposed MPC technique is shown in Fig. 5. The MPC code is performed based on the following technique. Firstly, the flux and torque are predicted based on the proposed 219 SS. It is worth noting that the execution time for this code is 140 μS using dSPACE 1103 digital controller, which is still fast enough to operate 5L MLCs. However, this time is slightly high.

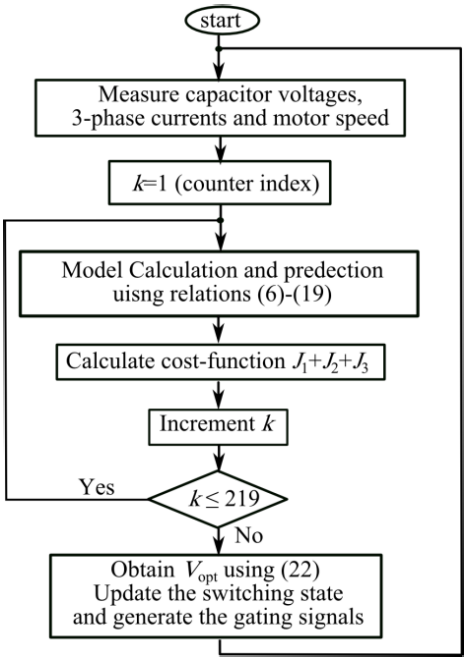

FIGURE 5. A flow-chart for the proposed MPC algorithm.

2) SCENARIO-2 (CMVE)

The proposed CMV study reflected that only 19 VVs can produce ZCMV, as listed in TABLE 5. These VVs can be achieved by 141 SS, and can be optimized to 115 SS as only one state for vector O is sufficient to be used for both achieving capacitor balancing and CMVE. Hence, the switching number of SS is reduced to 115.

Applying these SS to (20), while omitting J_3 term, then the optimum vector can be calculated as:

$$V_{opt} = \arg \min_{\{V_1..V_{115}\}} J\left(V_s^{k+1}\right) \tag{22}$$

It is worth noting that the execution time for this code is 71 microseconds using dSPACE 1103 digital controller which is fast enough to operate MLC drives.

V. EXPERIMENTAL SETUP OF DUAL T-TYPE DRIVE SYSTEM

The Silicon Carbide (SiC) semiconductor technology is preferred in power electronic converter as it decreases the converter switching losses. On contrary, the SiC MOSFET operation in MLCs faces some difficulties due to EMI. Due to large commutation paths in the MLCs printed circuit boards (PCBs) compared to 2L converter circuits, the stray inductance increases and hence the ringing (voltage overshoots at the instant of level transition) appears. The voltage overshoot results from the energy stored in the stray inductance L_s, $E_s = L_s i^2/2$ through the current path. This voltage overshoot is added to the DC link voltage and increases over the blocking voltage of the used semiconductors. For that reason, most of companies produced T-type modules for only one-phase to avoid EMI problems [30].

In the proposed test-setup, the three-phase T-type converter is designed and implemented on one PCB. The prototype of the dual T-type converter and the PCB layout are shown in Fig. 6-a,b. The tracks are kept as short as possible and the electrolytic capacitors are installed on the PCB. Some designs prefer the use of film capacitors, like the implemented converter in [31], in order to reduce the electromagnetic interference (EMI) and prevent edging (voltage spikes) during switching transitions. However, the film capacitors are quite expensive. In the proposed setup, the electrolytic capacitors are used. The distance between the driver and the discrete switches is kept small (around 4 centimeters for the gate current loop) to avoid the EMI problem. The gate to source pulses for one MOSFET are shown in Fig. 6-c. It can be observed that due to the well-designed PCB, there is no overshoots in the generated pulses.

The T-type converter is implemented in laboratory using SiC discrete switches metal-oxide semiconductor field-effect transistor (MOSFET) with the code number C2M0080120D. The converter power circuit board (PCB) is designed based on short traces between driver and discrete switches and short power traces as well. The power MOSFETs are derived using Cree driver with the code number CGD15HB62P1, which drives two SiC MOSFETs. The converter is interfaced to dSPACE 1103 digital controller through dead-band circuit.

It is worth mentioning that the, in principle, operating T-type SiC based MLC with high switching frequency is possible to be applied. However, the switching frequency of this work is limited by the MPC technique computation time, which is 70 μs for one of the case studies (corresponding to a maximum frequency of 14.3 kHz) using 1103 dSPACE digital controller.

The experimental test-setup, which is shown in Fig. 7, consists of dual T-type converters connected to an OEIM, which is mechanically coupled to a DC machine. The DC machine is loaded by a Chroma programmable load to adjust the required IM torque command. The dual converters are supplied from two single-phase rectifiers. Each rectifier is connected to two cascaded capacitors in order to attain the

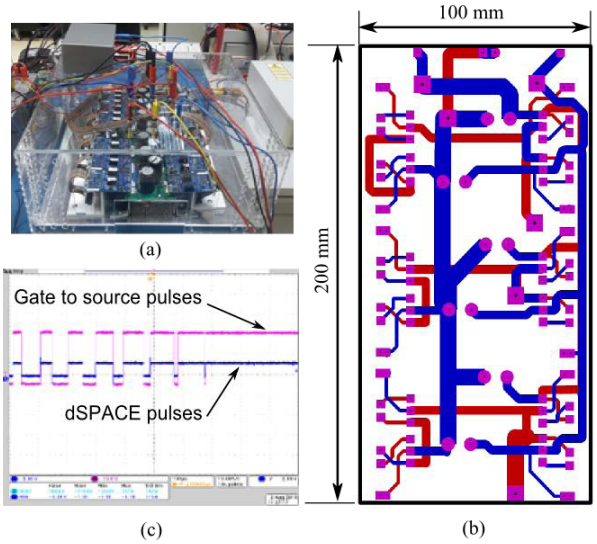

FIGURE 6. T-type MLC a) Dual T-type laboratory prototype b) double layers PCB layout, and c) Gate to source pulses vs. dSPACE pulses.

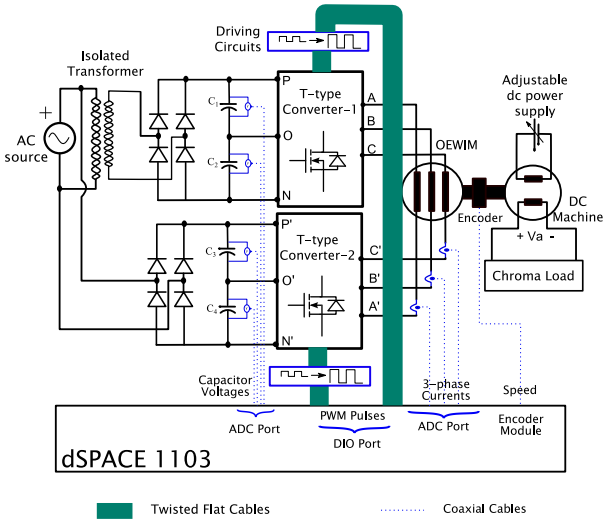

FIGURE 7. Block diagram for the experimental setup.

DC link mid-points O and O'. One isolated transformer is used to prevent zero-sequence current in the drive system.

The gating pulses are connected to the proposed converter using twisted ribbon cables in order to reduce the EMI effects in wiring. LEM modules voltage and current sensors are used to feedback the voltage and current signals to the digital controller. The three-phase currents, the capacitor voltages and the shaft encoder measured signals are transferred to dSPACE ports using coaxial cables.

VI. RESULTS AND DISCUSSIONS

The simulation of the proposed system is carried out using Matlab^{TM}\Simulink$^{®}$ software. The experimental test is performed in laboratory using the test-setup seen in Fig. 7 which is based on dSPACE 1103. The available programmable load

can only work when the generated voltage is attained from the DC machine. Then, the programmable load command can be applied. Hence, the simulation test is carried out in correspondence with the experimental tests extended period.

To test the proposed drive system properly, the following experiment sequence will be carried out. Firstly, the flux command will be applied at the instant $t = 0$ and reached to its rated value at $t = 0.1$ S, then the speed command can be applied. This pre-excitation process helps to reduce the starting current. Furthermore, in order to investigate the drive system performance under the different circumstances, i.e. capacitor balancing. CMVR, and CMVE, the following case studies were conducted:

- Case-1: This test aims to investigate the effect of ignoring the capacitor voltage balancing on the proposed drive. Therefore, the capacitor balancing is ignored while the CMV is considered in the drive system.
- Case-2: In this case, the capacitor voltage balancing and the CMVR (Scenario-1) are considered.
- Case-3: In this case, the capacitor balancing and the CMVE (Scenario-2) are considered.

A. CASE-1 (IGNORING CAPACITOR BALANCING)

This case involves two different tests.

- Firstly, the capacitor balancing technique will be ignored from the starting of the operation (at $t = 0$).
- Secondly, the effect of deactivating the capacitor balancing technique at steady-state will be inspected.

The first test results are shown in TABLE 2 where the machine torque follows the reference torque with peak-peak ripples of 1.594 N.m. (63.76 % of reference torque). In addition, the flux ripples reaches 44 mWb (5.39% of reference flux). The capacitor voltages deviation reached to 28 V (20 % of the capacitor reference voltage). The corresponding experimental results for Case-1 are shown in Fig. 9. Similar trend for torque and flux ripples can be observed in experimental test. The torque and flux ripples are 2.07 N.m. (82.9 % of reference torque) and 51 mWb (6.25 % of the reference flux) respectively. The capacitor voltage deviation reached 25 V (17.86 %) in experimental test.

Secondly, the effect of deactivating the capacitor balancing during steady state has been examined as follows. Fig.10 and Fig.11 show the simulation and experimental results respectively. The capacitor disabling instant is 10 s.

Comparing the steady-state torque and flux ripples for the intervals before and after disabling instant, the torque ripples increased from 0.525 to 1.427 N.m. for simulation results in Fig.10 Correspondingly, for simulation results as well, the flux ripples increased from 16 to 40 mWb. Similarly, the experimental results follow the same simulation trend. The torque ripples increased from 0.86 to 1.93 N.m. and the flux ripples increased from 26 to 51 mWb, respectively.

On the other hand, the effect of the capacitor unbalancing compared to normal operation (balanced capacitors case) on the motor voltage and current is observable.

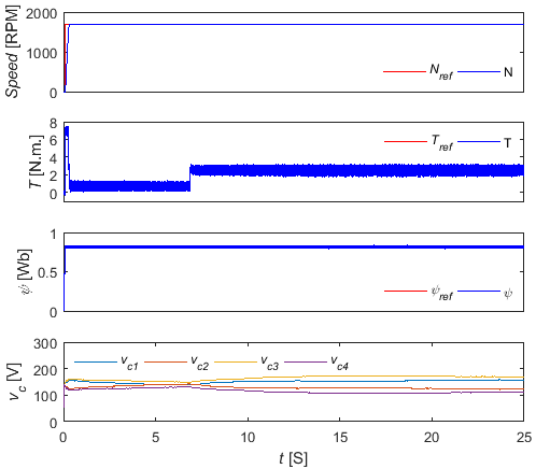

FIGURE 8. Motor speed, torque, flux and capacitor voltages without considering capacitor balancing (simulation).

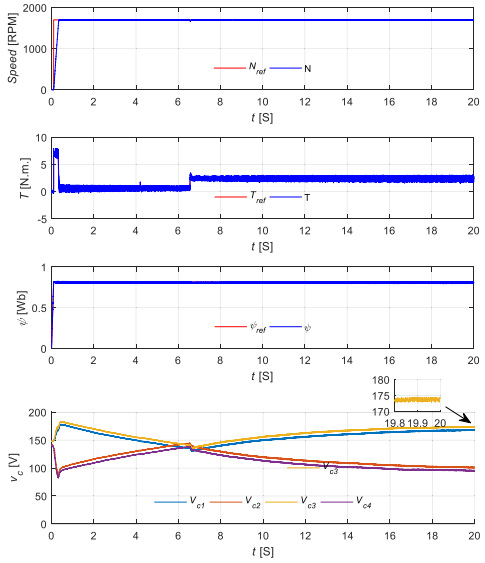

FIGURE 9. Motor speed, torque, flux and capacitor voltages without considering capacitor balancing (Experiment).

TABLE 6. Comparison between balanced and unbalanced THD values for both voltage and current.

Case	THD_i [%]		THD_v[%]	
	Sim.	Exp.	Sim.	Exp.
Unbalanced case	10.99	12.10	25.02	26.80
Balanced case	1.12	1.85	16.13	18.43

Fig.12 and Fig.13 show the voltage and current waveforms for the simulation and experimental tests respectively. The voltage levels and the current waveforms appear distorted for the unbalanced capacitor case. The *THD* values for normal and unbalanced voltage and current are listed in Table 6. Hence, losing capacitor balancing either at steady-state operation or from the starting of the drive operation have similar trend on the drive system.

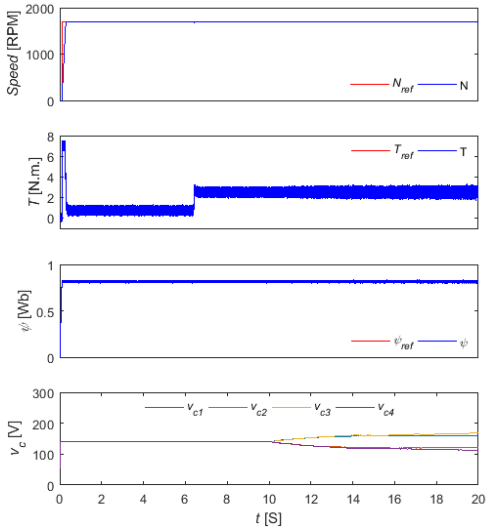

FIGURE 10. Motor speed, torque, flux and capacitor voltages without considering capacitor balancing at t=10 S (simulatio).

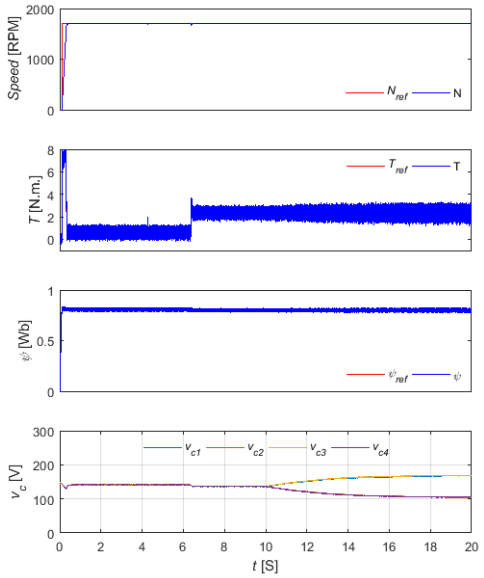

FIGURE 11. Motor speed, torque, flux and capacitor voltages while disabling capacitor balancing at t=10 S (Experiment).

B. CASE-2: CONSIDERING CMVR (SCENARIO-1)

In this test, the capacitor balancing is considered from the instant $t = 0$. The simulation results of the motor speed, torque, flux, capacitor voltages and CMV are shown in fig.14 The capacitor balancing weighting factor K_{dc} is set to 0.1 from $t = 0 - 10$s. This period, in which the capacitor balancing is considered and both CMVR and CMVE are ignored, is going to be referred as the *normal operation* in this article. During that period, the torque, flux, speed and capacitor voltages follow their references values appropriately. The torque ripple is 0.525 N.m. (21% of the reference torque). Correspondingly, the flux ripple is 16 mWb (1.9% of the reference flux). The maximum capacitor voltages ripple is 0.4 V (0.29 % of the desired capacitor voltage).

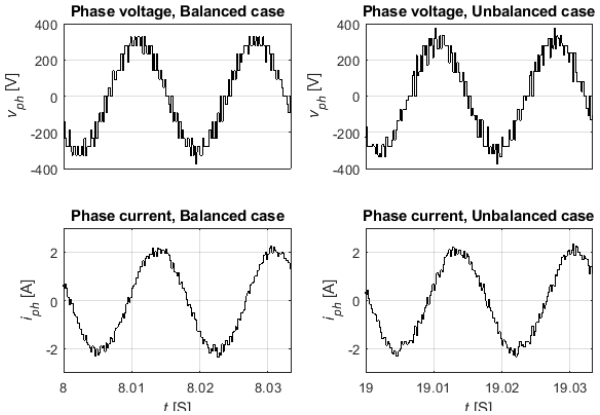

FIGURE 12. Phase voltage and current for balanced and unbalanced cases (simulation).

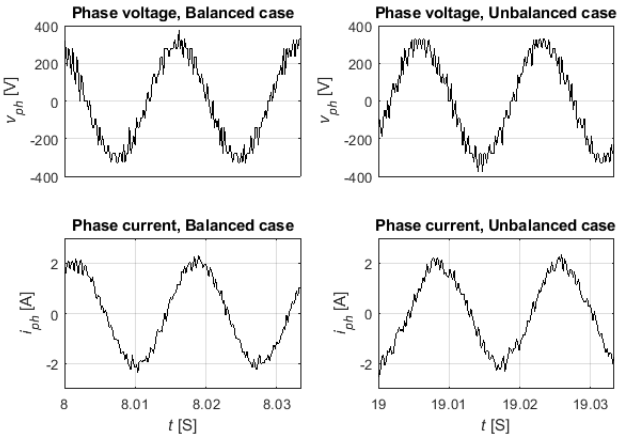

FIGURE 13. Phase voltage and current for balanced and unbalanced cases (Experimental).

In order to test the capability of the proposed MPC technique to restore balancing if the capacitor voltages are disturbed, the technique disabled the part of capacitor balancing for one second ($t = 10 - 11$ s). Successfully, the technique could achieve the capacitor balancing in a short period (0.23 s).

In order to test the CMVR, at the period $t = 13 - 15$ s, K_{cm} is set to 0.1. It could be observed that the torque and flux ripples are 0.699 N.m. and 18 mWb respectively. These ripples contribute increase of 33.14 % and 12.5 % of the normal operation torque and flux respectively. In addition, the maximum capacitor deviation increased to 0.5 V, which is 25%, compared to normal operation voltage deviation. In addition, it could be observed that the CMV is limited to 93 V instead of 140 V, which means a reduction of 33.5 % in the maximum CMV is achieved.

Similarly, the experimental test has achieved similar impact. fig.15 shows the drive system response for loading condition while CMVR and capacitor balancing are considered. The torque and flux ripples are 1.534 N.m. and 21 mWb respectively. In addition, the capacitor voltage deviation reached to 1.5 V to the reference voltage. Unlike simulation results, during the first 0.1 s while the machine is energized, the capacitor voltages drop because of high

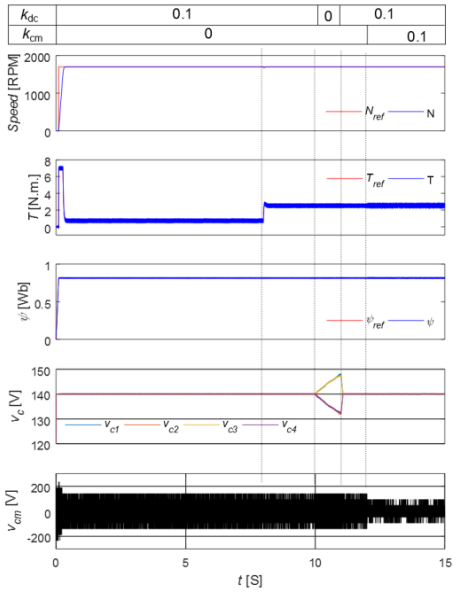

FIGURE 14. Simulation test for T-type drive system using CMVR, capacitor balancing, and TPC.

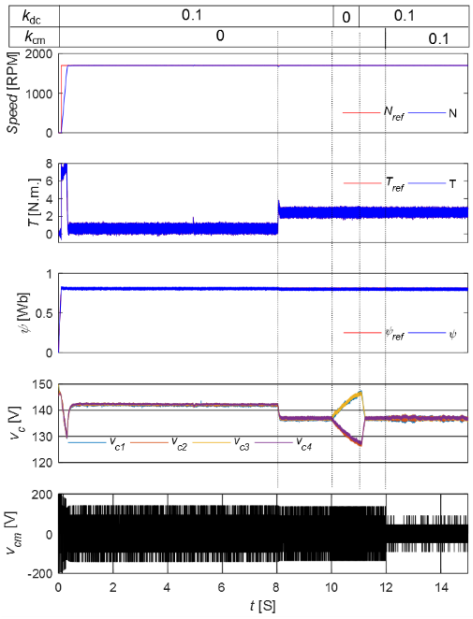

FIGURE 15. Experimental test for T-type drive system using CMVR, capacitor balancing, and TPC.

starting current. This appears only in experiments, as the supply is not regulated. Other results are similarly following the simulation results.

C. CASE-2: CONSIDERING CMVE (SCENARIO-2)

This test aims to investigate the performance of the T-type drive system while removing the CMV using the proposed 115 reduced number of SS that represent 19 VVs. The test has been carried out in the following sequence. Firstly, the capacitor balancing is considered during the first 10 s interval. Then, from t = 10-11 s, K_{dc} is set to zero. During this period, the unbalanced capacitors affect the torque and flux ripples

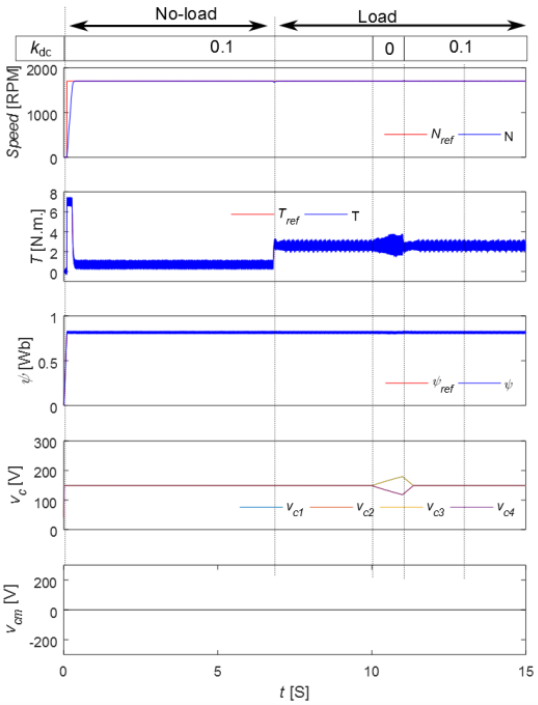

FIGURE 16. Simulation test for T-type drive system using CMVE, capacitor balancing, and TPC.

as shown in Fig. 16. Corresponding experimental results is shown in Fig.17

Similar notation for the capacitor voltage dip in the starting is observed as in Case-2. The simulation and experimental testes are well agreed. The CMV value is zero in both tests. The simulation results for torque and flux ripples are 1.017 N.m. and 28 mWb, respectively.

Corresponding experimental results for torque and flux ripples are 1.7 N.m. and 29.3 mWb, respectively. Comparing to normal operation, it can be observed that the torque and flux ripples have increased by 93.7 % and 75 % for simulation test and increased by 98.8 % and 39.5 % for experimental test respectively.

D. SUMMARY AND DISCUSSION

This subsection aims to conduct a comparison between CMVE, CMVR and normal operation. Due to the different number of SS and VVs used in the two studied scenarios and the normal operation, the performance of the T-type drive system is different. A summary for the torque and flux ripples as well as the capacitor voltage deviations are listed in TABLE 7. The CMVE case has higher torque and flux ripples. On contrary, the capacitor voltage deviations compared of the CMVE case are lower than that of CMVR case.

To observe the effect of the CMVR and CMVE on the motor phase voltage and current, a study for the harmonic contents in phase voltage and current for the two scenarios has been carried out. The simulation and experimental phase voltage and current are shown in Fig.18 and Fig.19 for CMVE and CMVR scenarios, respectively. Moreover, the phase voltage and current for the normal operation is shown in Fig.20 It

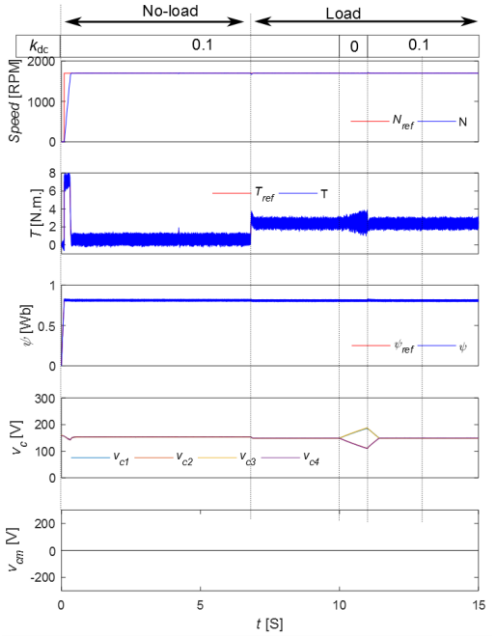

FIGURE 17. Experimental test for T-type drive system using CMVE, capacitor balancing, and TPC.

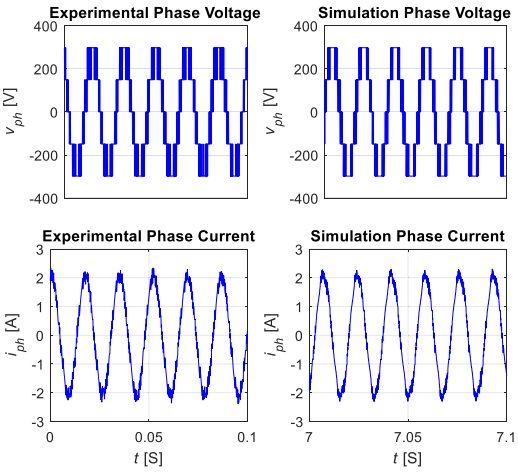

FIGURE 18. Phase voltage and current during CMVE.

TABLE 7. Summary for the machine variables performance for the different executed tests.

Case	$T_{ripples}$ [N.m.]		$\psi_{ripples}$ [mWb]		Cap. deviation [V]	
	Sim.	Exp.	Sim	Exp	Sim	Exp
Normal	0.525	0.861	16	26	0.4	1.0
Unbalanced	1.594	1.931	44	51	25.0	28.0
CMVR	0.699	1.534	18	21	0.5	1.5
CMVE	1.017	1.712	28	29	0.2	0.6

can be observed that the voltage shapes for the two scenarios are different due to the absence of some voltage vectors in CMVE case. Moreover, the voltage steps are also different due to the higher DC link voltage for the CMVE scenario.

Moreover, the absence of the greatest voltage vectors (d_1, d_5, d_9, d_{13}, d_{17}, and d_{21}) decreases the fundamental output voltage in this case. Hence, an increase in the DC link voltage was required in order to achieve the same loading

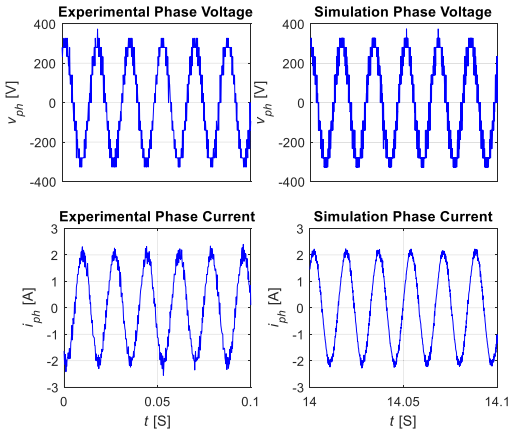

FIGURE 19. Phase voltage and current during CMVR.

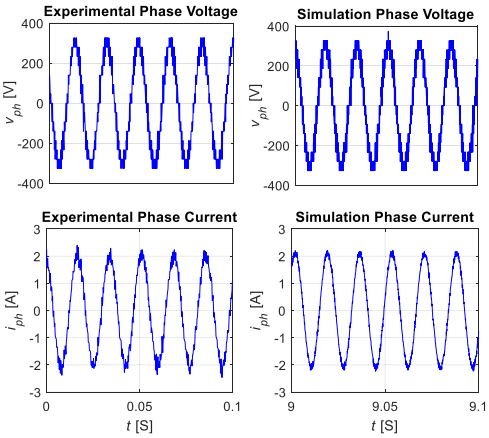

FIGURE 20. Phase voltage and current during normal operation.

TABLE 8. Comparison between CMVE, CMVR and normal operation.

Case	THD_i [%]		THD_v[%]	
	Sim.	Exp.	Sim.	Exp.
CMVE	4.60	6.45	25.50	27.75
CMVR	2.14	2.65	18.50	19.60
Normal operation	1.12	1.85	16.13	18.43

conditions of the normal and CMVR cases. This is considered one of the drawbacks of the CMVE in AC drive systems.

A summary for the total harmonic distortion factors for phase voltage and currents are listed in TABLE 8. It can be concluded that the higher voltage and current harmonic distortions of the CMVE case, compared to other cases, increase the torque and flux ripples. Although the CMVE is preferred in AC drives to reduce the bearing current and increase the machine lifetime, it has the following drawbacks:

- It utilizes extra DC link voltage that increase the converter switching losses, as the former depends on the DC link voltage level [4].
- It delivers extra harmonic contents that lead to increase the machine core losses [32], [33].
- It increases the torque and flux ripples.

VII. CONCLUSION

A new strategy for capacitor balancing and CMV reduction/elimination for a dual T-type drive system has been

proposed. MPC-based approach has been developed for controlling the machine torque, fulfilling capacitor balancing and reducing/eliminating the CMV of the proposed drive system. Two scenarios for the CMV along with balancing the DC link capacitor voltages have been discussed. The two proposed scenarios are based on reduced switching states models of 219 and 115 out of 729 for CMVR and CMVE, respectively. This reduces substantially the MPC execution time to 140 μs and 70 μs, respectively, compared to 5.5 ms of total 729 switching states. The results show the effectiveness of both scenarios to fulfill the capacitor voltage balancing. Moreover, it is concluded that the CMVR has lower torque and flux ripples compared to CMVE technique. In addition, the voltage and current harmonic distortions of the CMVE case are higher than that of CMVR case. The higher DC link voltage required for the case of CMVE increases the converter switching losses as well. Therefore, it can be concluded that considering CMVR has better compromise impact on the machine performance, harmonic contents, and switching losses.

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Authors' photographs and biographies not available at the time of publication.