IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received January 28, 2019, accepted March 8, 2019, date of publication March 22, 2019, date of current version April 5, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2905106

A Cavity-Backed Shorted Annular Patch (SAP) Array for Mid-Range V-Band Backhauling Applications

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ABSTRACT This paper presents a new improved gain array configuration well suited for mid-range V-band backhauling applications. The proposed solution is based on a cavity-backed shorted annular patch (SAP) antenna loaded with a parasitic patch element for gain maximization. This solution is proved by designing and measuring a 4 × 4 array which presents a reflection coefficient bandwidth covering the frequencies from 58.7 to 63.25 GHz (7.6% at 60 GHz). The experimentally validated array gain is equal to 18 dBi corresponding to 37.9% of aperture efficiency. The antenna and array configurations presented in this paper are optimized to minimize the manufacturing cost and complexity. This result is achieved through a novel beamforming network (BFN) configuration, implemented using a dual-layer substrate-integrated waveguide (SIW) technology, and partly integrated on the array aperture. The achieved results demonstrate how the performance of the cavity backed SAP array is comparable to the ones achieved with more complex and expensive solutions.

INDEX TERMS 5G mobile communication, antenna arrays, substrate integrated waveguide (SIW).

I. INTRODUCTION

Backhauling links are employed to implement the interconnections between the network core and the base stations. Into the hierarchy of the modern network infrastructures, they play a crucial role which will be further augmented with the forthcoming fifth generation mobile communication system that is referred to as 5G. Indeed, the need to face higher data rate per cell and the new frequency allocation of the 5G system will require the deployment of a higher number of cells. The capability to efficiently transfer the data from these pico-cells to the network core is regarded as one of the main cost drivers to be faced by operators. For this reason, several wireless systems operating at millimeter wave frequencies have been developed for backhauling applications [1]. The V band unlicensed spectrum provides an interesting opportunity as it offers up to 9 GHz of bandwidth around 60 GHz thus allowing multi-gigabit data rates. Several industrial and academic research efforts have been devoted to the development of V-band antenna. For medium to long range applications requiring peak antenna gains of more than 25 dBi parabolic reflectors, transmit-arrays [2], lens antennas [3], slot-waveguide arrays [4] or substrate integrated waveguide (SIW) arrays [5] have been proposed. In the case of shorter link distances, several investigations have been conducted on medium gain (10–20 dBi) antenna configurations [6]. The smaller gain value, makes the use of planar technologies preferable due to their ease of integration with the chipsets, lower manufacturing and installation costs. For instance, in [7] a 6×6 array on LTCC with a gain of 19 dBi is reported. A SIW slot configuration in printed circuit board (PCB) technology is presented in [8] where an array of 12×12 elements exhibits a gain of 22 dBi. The use of dense dielectric patch antennas allows in [9] the achievement of a gain of 16.5 dBi in a 4×4 array arrangement. The typical approach to increase the radiation efficiency is to limit the losses in the beam forming network (BFN) and to increase the gain of the array elements. An example of highly directive elements is shown in [10] where a SIW distribution network is used to feed cavity backed patch elements.

The associate editor coordinating the review of this manuscript and approving it for publication was Bora Onat.

This configuration, which requires an aluminum plate to realize the cavities, reaches a gain of 19.6 dBi with 16 elements. Another approach has been demonstrated in [11] where a combination of a one-wavelength bowtie and a double loop antenna are employed in a reflector-backed arrangement achieving a gain of about 20 dBi.

In this work, a new array configuration based on Shorted Annular Patch (SAP) antenna elements for V-band applications is presented [12]. This type of antenna has been studied in the past for its surface waves inhibition properties and due to its capability to provide higher gain if compared to a patch antenna element. Thanks to these properties, the SAP antenna has found application in global navigation satellite system (GNSS) applications [13]–[15] for low multipath applications. In [16] an all-metal SAP has been demonstrated as a parabolic reflector feed for Ku-band SatComs applications, while in the lower millimeter wave band, SAP antennas have been demonstrated for dual band operation [17].

The solution proposed in this work is obtained combining some of the aforementioned concepts to achieve a new architecture where in a four layer PCB stack-up are embedded cavity-backed SAP antennas fed using a dual-layer SIW beam forming network. Stacked SAP elements loaded with a parasitic ring are employed to improve the bandwidth and to increase the gain. The idea of loading a SAP element with a parasitic patch has been already proved in [18] where two shorted rings suspended though an aluminum solid block were employed for S band for satellite applications. At variance of this work, the intended approach is entirely based on standard PCB technology and it expands upon the feasibility study presented in [19]. The entire radiating element is embodied within a metal cavity which serves to enhance the gain. The proposed concepts are validated through the design and the experimental validation of a 4×4 array whose BFN is built using a two layer SIW network as described in Section III. Results of the experimental evaluation are illustrated and discussed in Section IV.

II. ANTENNA DESIGN

One of the key features of the proposed design is that the overall array structure can be fabricated using a low cost PCB process. As it can be observed in figure 1, the stack-up employed in this work makes use of four metal layers assembled using a sequential build-up procedure. The interconnections between the different layers and the shielding cavity requires the use of two metallized via typologies, namely a through via between M2 and M3 and a blind via between M1 and M2. D1 and D2 are used to implement the SIW BFN and the SAP elements, including the backing cavity. A foam layer, D3, acts as a spacer for the stacked patch which is printed on D4. The manufacturing process exploits a fusion bonding technique developed by Nuova Eurotar S.r.l., Italy. This approach allows to bond the different dielectric layers through high pressure and temperature thus allowing to avoid the use of prepreg materials. Therefore, a straightforward implementation of complex multilayer stack-ups is

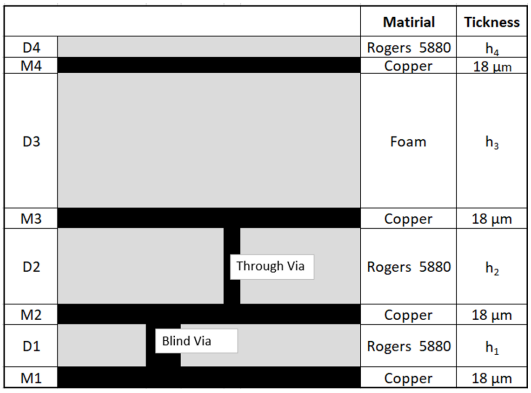

FIGURE 1. Side view of the PCB stackup. $h_1 = 0.254$ mm, $h_2 = 0.508$ mm, $h_3 = 1.9$ mm, $h_4 = 1.295$ mm. Conductor layers are depicted in black, dielectric substrates in gray.

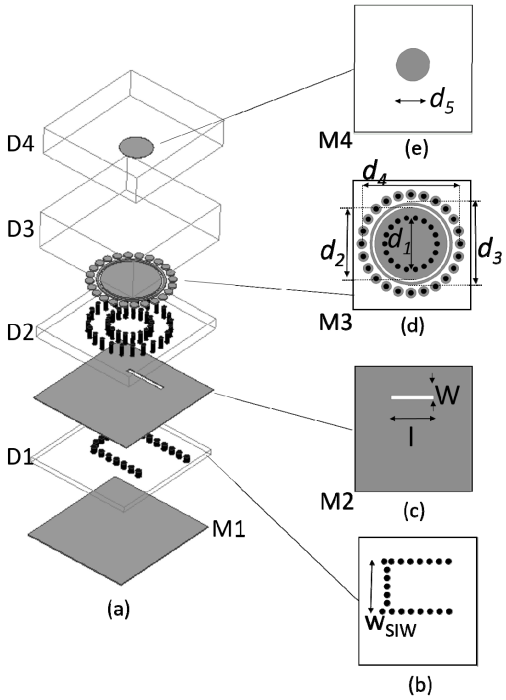

FIGURE 2. Representation of the shorted circular patch antenna printed on a multilayer PCB. (a) Exploded view; (b) feeding SIW; (c) ground with feeding slot; (d) shorted patch; (e) parasitic circular patch. $d_1 = 1.64$ mm, $d_2 = 2.49$ mm, $d_3 = 2.87$ mm, $d_4 = 3.4$ mm, $d_5 = 1.4$ mm, $l = 1.85$ mm, $w = 0.18$ mm, $w_{SIW} = 2.1$ mm.

made possible through a sequential build-up process which allows to have a through via type between M2 and M3 with a diameter $dvia_{23}$ equal to 0.2 mm.

The geometry of the stacked SIW SAP radiator is shown in figure 2. A circular patch having diameter d_2 is printed on M3 and it is short circuited through a concentric ring having a diameter equal to d_1. The shorter inner border is realized through a set of vias from M2 to M3. The SAP element is surrounded by a matching ring implemented through a 0.09 mm annular ring with an outer diameter of d_3. As it will be shown in the following paragraphs, this parasitic ring serves to enlarge the matching bandwidth. The entire

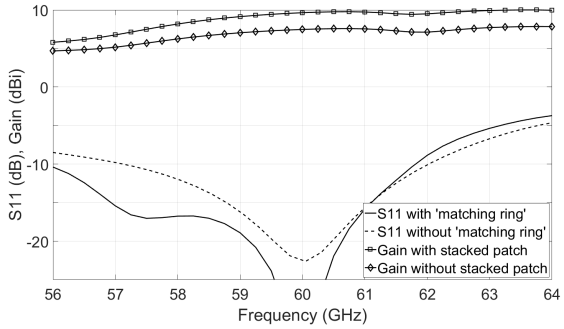

FIGURE 3. Simulated reflection coefficient and gain of the single antenna: the performance of the geometry presented in figure 2 is compared with the case without parasitic patch and without matching ring.

SAP structure, including the matching ring, is surrounded by a cavity formed by a cage of metallized via holes distributed along a concentric circle having a diameter equal to d_4. The via cage around the patch is helpful to improve the element gain and to minimize the mutual coupling effects thus limiting the insurgence of side lobes. A foam spacer of height h_3 is used to couple a parasitic circular patch whose diameter, d_5, can be optimized to further increase the gain of the cell. A w×l slot etched on M2 provides the electromagnetic coupling between the SAP cavity and a feeding SIW fabricated in the lower dielectric, D1. The feeding SIW has a width equal to W_{SIW} and it is fabricated using blind vias having a diameter equal to $dvia_{12}$ =0.25mm. The SAP antenna can be designed by selecting the outer radius and then optimizing the inner radius to excite the radiator at the desired frequency. For the case at hand, the design procedure started with the selection of the SAP outer radius, d_2, which was fixed to half a free space wavelength, i.e. 2.49 mm. This value provides high gain while avoiding grating lobes generated by the single array element. A first guess of the inner diameter, d_1, was analytically calculated as suggested in [20] (equation 2) obtaining a value of 1.71 mm. A finite element method (FEM) analytical model was implemented including all the antenna components as presented in the geometry shown in figure 2. Ansys HFSS [21] was used for the full-wave simulation and optimization. The height of the foam layer was fixed to 1.9 mm that is the thickness of a foam slab after the completion of the stack-up fabrication. The diameter of SAP cavity, d_4, was fixed at $0.68\lambda_0$, with λ_0 the free space wavelength. As it will be discussed in the next section, this choice is essential to have enough spacing for the array beam forming network. Each geometrical parameter was fine tuned to match the manufacturing constrains and to optimize the bandwidth and gain performance of the antenna. The optimized antenna, has a maximum gain of 9.6 dBi at 60 GHz that is about 30% higher with respect to the SAP gain without parasitic patch, as shown in figure 3. It is worth noticing that the two gain values was achieved adjusting each antenna configuration to its optimal performance. A similar comparison was done to evaluate the effect of the matching ring. This element creates an additional resonance in the cavity which, for the case at hand, was tuned to about 57.5 GHz thus enlarging the bandwidth of the unloaded SAP antenna from 7.9% to 10%.

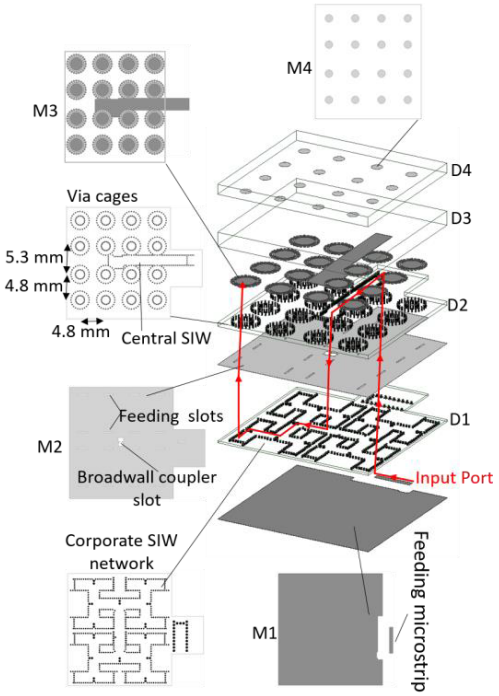

FIGURE 4. Representation of the proposed 4 × 4 array. The electromagnetic wave flows from the feed port to each array element as shown by the red arrows.

III. ARRAY DESIGN

The single element presented in the previous section was employed to design a 4×4 array using the same PCB stackup reported in figure 1. The designed array is shown in figure 4. One of the objectives of the proposed antenna configuration is to reduce the complexity of the stack-up by limiting the number of layers. For this reason, the array BFN is partly embedded in D2, which is the same substrate where the cavity backed SAP antennas are implemented. Specifically, the BFN is composed by a two layer full-corporate feeding network in SIW technology. The electromagnetic wave flows through the antenna array as shown by the red arrows in figure 4. The array is fed through a microstrip line printed in M1 that is slot coupled to the core part of the BFN which is a SIW integrated in D2. To accommodate this part of the BFN, the central elements of the array are spaced 5.3 mm apart while the inter-element spacing of the other radiators is equal to 4.8 mm ($0.96\lambda_0$).

The SIW section in D2 serves to direct the signal toward the center of the array where a broadwall coupler is used to couple the RF power downward into a SIW corporate feeding network integrated in D1. Due to the structure symmetry, the signal distribution across the array elements is uniform in amplitude and phase. H shaped power dividers are used in the corporate feeding network. Each power divider is the combination of three T-junctions. The coupling between the corporate BFN and each SAP cavity is achieved through a

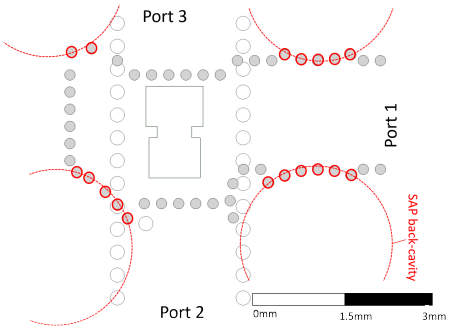

FIGURE 5. Top view of the broadwall cross coupler. Gray vias are fabricated on D2 while the other vias are located on the lower level (D1). The vias shared with the SAP back-cavity are circled in red. The H slot is etched on M2. Physical dimensions can be extrapolated using the provided scale.

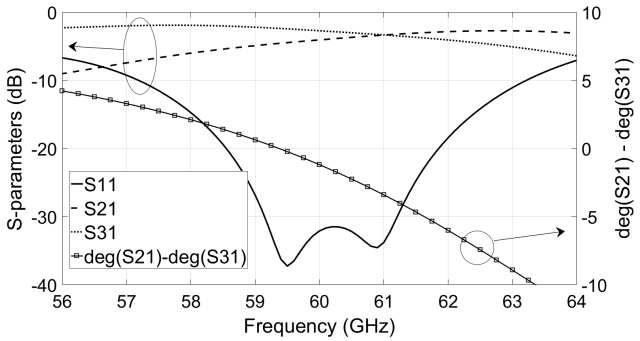

FIGURE 6. Simulated S-parameters of the broadwall cross coupler.

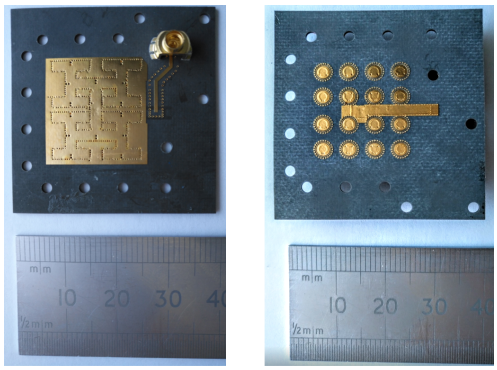

FIGURE 7. Manufactured 4x4 array. (a) Bottom view. (b) Internal layer M3.

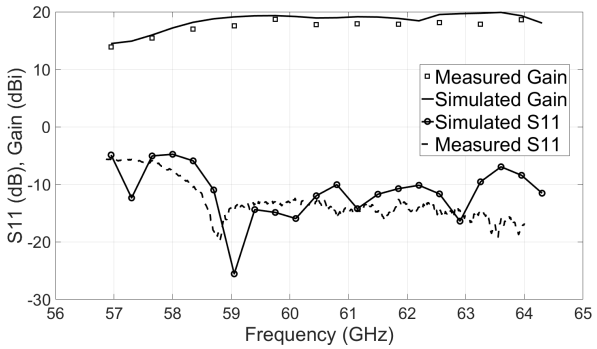

FIGURE 8. Simulated and measured antenna parameters: gain and reflection coefficient.

longitudinal slot etched in M2. It is worth noticing that the use of an additional dielectric layer, albeit it would increase the production costs, it would allow a further optimization of the antenna performance as a larger back-cavity could be employed thus increasing both gain and bandwidth.

The broadwall coupler is the key component for the vertical RF power transmission in the proposed multilayered structure. Figure 5 shows the geometry of the proposed coupler. The curved shape of the couplers in D2 serves to create room for the antenna's circular cavities. Indeed, the couplers and the SAP back-cavity share a sub-set of vias (see red circled vias in figure 5). The broadwall coupler was simulated including in the full-wave model two crossed SIWs, the central H shaped slot and three ports. The distance between the H slot and the end of the upper SIW is about $\lambda_g/4$ (λ_g is the guided wavelength). The metalized hole located at the junction of each T-branch is used for matching purposes. The width of the two SIWs is fixed to 1.9 mm in D2 and 2.2 mm in D1, to make sure that only the fundamental mode propagate within the waveguide. Simulated S parameters for the broadwall coupler are shown in figure 6.

The feeding network total losses are about 3dB. This value has been evaluated from simulations, considering the whole path followed by the electromagnetic wave from the input microstrip in M1 to the antenna input slot (see red arrows in figure 4). The maximum simulated gain of the array is 19.5 dBi at 63Ghz, at the same frequency the directivity is 20.85 dBi (76.3% of radiation efficiency).

IV. MEASUREMENT

Figure 7 shows the photograph of the fabricated 4×4 array which is fed exciting the microstrip line through an MMPX connector, visible in figure 7 (a) which reports the bottom side of the array. Figure 7 (b) shows the internal M3, before the integration of the upper dielectric layers (D3 and D4). The size of the radiation aperture is 17.9×18.5mm. The measured and simulated S11 of the whole structure are compared in figure 8 along with the array gain. The simulated antenna bandwidth (−10dB) covers the frequencies from 58.7 to 63.25 GHz which corresponds to almost 7.6% at 60 GHz. The bandwidth is comparable with the one of the isolated array cell as the BFN bandwidth is significantly higher.

The small difference between simulated and measured results can be ascribed to fabrication tolerances and, in particular, to alignment issues between layers. It has been verified that, although in the order of tens of microns, they might degrade the array performance. The measured array peak gain, observed at 63 GHz, is equal to about 18 dBi while the simulated one was equal to 19.5 dBi. The increased gain losses in the prototype are attributed to manufacturing losses and to additional losses caused by the BFN or by the connector itself whose effect was not de-embedded. The proper behavior of the array is confirmed by the cross-polar radiation levels which remain below −28 dBi over the entire band. Figure 9 presents the simulated and measured radiation patterns for the proposed array in the two main planes. The beam

TABLE 1. Comparison between proposed and reported 60 GHz antennas arrays.

Ref.	Tipology	Feeding Network	No. Of Element	Size (mm^2)	Impedance bandwidth (-10dB) %	Max gain (dBi)	Aperture efficiency (%)*
[7]	Slot coupled patch (LTCC)	Stripline	6×6	25×25	n.a.	19	25.3
[8]	SIW Slot Array (PCB)	SIW (series)	12×12	30.7×30.7	4.1	22	41.2
[9]	Patch (PCB)	Microstrip Line (parallel)	4×4	18×20	23.7	16.5	24.7
[10]	Cavity backed patch (PCB)	SIW (parallel)	4×4	16.3×17.1	22.6	19.6	65.1
[11]	Loop-loaded Dipole (PCB)	Microstrip Line (series)	14	20×20	22.1	20.1	50.9
[22]	Cavity (LTCC)	SIW (parallel)	64	24.6×31	17.1	22.1	42
[23]	Microstrip Patch (LTCC)	Stripline	2×2	10.1×8.5	27.3	10.5	26
[24]	Ridge Gap Waveguide (all metal)	RGW	8×8	33.6×33.6	17	27	88
[25]	Microstrip Patch	Microstrips	4×4	18×18	22	15.98	24
This Work	Cavity backed SAP (PCB)	SIW (parallel)	4×4	17.9×18.5	7.6	18	37.9

*Calculated using the published size and gain values.

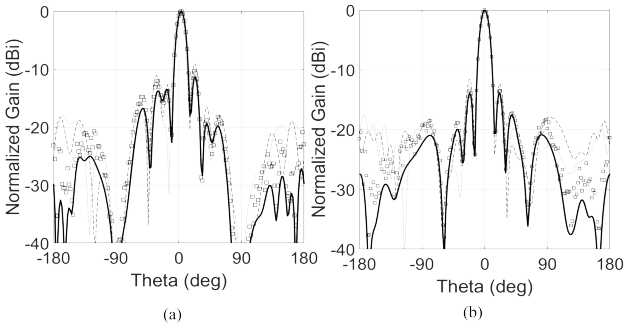

FIGURE 9. Measured (square) and simulated (continuous line) radiation patterns of the 4 × 4 antenna array at 61GHz. Also simulated pattern at 59GHz (dashed line) and 63GHz (dotted line) are shown. (a) E plane (b) H plane.

width measured at −3 dBi is about 8 degrees thus in good agreement with the simulated values. As it can be observed, a small asymmetry in the side lobes is visible in the E plane. This effect is generated by the BFN core branch embedded in D2 and it could be easily avoided by metallizing the M3 layer, outside the SAP cavities.

For comparison purposes, Table I reports the key parameters of some of the most recent works on a similar subject. As it can be observed, the most relevant scientific publications on planar V-band arrays for mid-range applications include configurations based on LTCC [7], [22], [23], hybrid PCB-metal [10] arrangements, metallic waveguides [24] and standard PCB [8], [9], [11], [25]. LTCC and PCB-metal solutions can provide better performance while having higher manufacturing costs. The increased costs are due to the inherently higher manufacturing costs in the case of LTCC. On the other hand, the use of different technologies, although simple for a limited number of prototypes is diriment in the case of mass production where the integration and assembly costs should be minimized. In this regard, the technology which is most suitable for massive production is PCB that is being currently used in a wide variety of applications having a wide diffusion. The performance of PCB arrays presented in Table I are worst than the previously proposed elements with the exception of the loop loaded dipole reported in [11]. This work exhibits an excellent behavior in terms of gain and bandwidth but it has a critical limiting aspect. Indeed, the radiating elements are suspended over a foam layer and the feeding microstrip lines are placed on the array aperture. As a consequence, their integration with the front end, usually located on the array back-side, would require a through via across a foam layer that is not compatible with currently available standard PCB processes.

V. CONCLUSIONS

A new highly integrated multilayer array based on SIW technology in V-band has been presented in this work. The proposed design is based on a SIW fed cavity backed shorted circular patch (SAP) antenna. The geometry of this radiator has been tailored to simplify the array design and fabrication process while maximizing its gain. To this end, a parasitic element placed above the driving SAP has been used to further increase its gain. A 4×4 array has been fabricated and measured. The array is fed through a two layer corporate SIW network which is partly embedded on the same dielectric layer where the array elements lie. This solution, although not allowing a full exploitation of the cavity backed SAP characteristics in terms of gain and bandwidth, it allows to limit the number of layers employed in the array manifold. The proposed array shows good matching over a 7.8 % bandwidth and a gain of about 18 dBi over the entire operational bandwidth.

The whole structure is compact and easy to build using standard PCB manufacturing process.

REFERENCES

[1] L. Verma, M. Fakharzadeh, and E. S. Choi, "Backhaul need for speed: 60 GHz is the solution," *IEEE Wireless Commun.*, vol. 22, no. 6, pp. 114–121, Dec. 2015.
[2] C. Jouanlanne *et al.*, "Wideband linearly polarized transmitarray antenna for 60 GHz backhauling," *IEEE Trans. Antennas Propag.*, vol. 65, no. 3, pp. 1440–1445, Mar. 2017.
[3] F. Pivit, E. Doumanis, D. Kozlov, M. Gueye, and E. M. Gimersky, "Compact 60-GHz lens antenna with self-alignment feature for small cell backhaul," in *Proc. IEEE-APS Topical Conf. Antennas Propag. Wireless Commun. (APWC)*, Sep. 2017, pp. 280–283.
[4] A. Vosoogh and P. S. Kildal, "Corporate-Fed Planar 60-GHz slot array made of three unconnected metal layers using AMC pin surface for the gap waveguide," in *Proc. IEEE Antennas Wireless Propag. Lett.*, vol. 15, Dec. 2016, pp. 1935–1938.
[5] Y. Li and K M. Luk, "60-GHz substrate integrated waveguide fed cavity-backed aperture-coupled Microstrip patch antenna arrays," *IEEE Trans. Antennas Propag.*, vol. 63, no. 3, pp. 1075–1085, Mar. 2015.
[6] C. Dehos, J. L. González, A. D. Domenico, D. Kténas, and L. Dussopt, "Millimeter-wave access and backhauling: The solution to the exponential data traffic increase in 5G mobile communications systems?." *IEEE Commun. Mag.*, vol. 52, no. 9, pp. 88–95, Sep. 2014.
[7] E. Cohen, M. Ruberto, M. Cohen, O. Degani, S. Ravid, and E. D. Ritter, "A CMOS bidirectional 32-element phased-array Transceiver at 60 GHz with LTCC antenna," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1359–1375, Mar. 2013.
[8] X.-P. Chen, K. Wu, L. Han, and F. He, "Low-cost high gain planar antenna array for 60-GHz band applications," *IEEE Trans. Antennas Propag.*, vol. 58, no. 6, pp. 2126–2129, Jun. 2010.
[9] Y. Li, and K.-M. Luk, "A 60-GHz dense dielectric patch antenna array," *IEEE Trans. Antennas Propag.*, vol. 62, no. 2, pp. 960–963, Feb. 2014.
[10] Y. Li, and K.-M. Luk, "Low-cost high-gain and broadband substrate-integrated-waveguide-fed patch antenna array for 60-GHz band," *IEEE Trans. Antennas Propag.*, vol. 62, no. 11, pp. 5531–5538, Nov. 2014.
[11] M. Li, and K.-M. Luk, "A low-profile unidirectional printed antenna for millimeter-wave applications," *IEEE Trans. Antennas Propag.*, vol. 62, no. 3, pp. 1232–1237, Mar. 2014.
[12] D. R. Jackson, J. T. Williams, A. K. Bhattacharyya, R. L. Smith, S. J. Buchheit, and S. A. Long, "Microstrip patch designs that do not excite surface waves," *IEEE Trans. Antennas Propag.*, vol. 41, no. 8, pp. 1026–1037, Aug. 1993.
[13] L. Boccia, G. Amendola, and G. D. Massa, "Performance evaluation of shorted annular patch antennas for high-precision GPS systems," *IET Microw. Antennas Propag.*, vol. 1, pp. 465–471, Apr. 2007.
[14] G. J. K. Moernaut and G. A. E. Vandenbosch, "The shorted annular patch as a multi-path suppressing antenna," in *Proc. 2nd Eur. Conf. Antennas Propag. (EuCAP)*, Nov. 2007, pp. 1–6.
[15] G. J. K. Moernaut and G. A. E. Vandenbosch, "Concept study of a shorted annular patch antenna: Design and fabrication on a conducting cylinder," *IEEE Trans. Antennas Propag.*, vol. 59, no. 6, pp. 2097–2102, Jun. 2011.
[16] Z. Yang, K. C. Browning, and K. F. Warnick, "High-efficiency stacked shorted annular patch antenna feed for ku-band satellite communications," *IEEE Trans. Antennas Propag.*, vol. 64, no. 6, pp. 2568–2572, Jun. 2016.
[17] E. Arnieri, L. Boccia, and E. G. Amendola, "A ka-band dual-frequency radiator for array applications," in *Proc. IEEE Antennas Wireless Propag. Lett.*, vol. 8, Jul. 2009, pp. 894–897.
[18] E. Arnieri, L. Boccia, G. Amendola, and G. Di Massa, "A high gain antenna for small satellite missions," in *Proc. IEEE Antennas Propag. Soc. Symp.*, vol. 2, Jun. 2004, pp. 1587–1590.
[19] E. Arnieri, G. Amendola, and E. L. Boccia, "Stacked shorted circular patch antenna in SIW technology for 60-GHz band arrays," in *Proc. IEEE Int. Symp. Antennas Propag. USNC/URSI Nat. Radio Sci. Meeting*, Jul. 2017, pp. 2675–2676.
[20] L. I. Basilio, J. T. Williams, D. R. Jackson, and E. R. L. Chen, "Characteristics of an inverted shorted annular-ring-reduced surface-wave antenna," in *Proc. IEEE Antennas Wireless Propag. Lett.*, vol. 7, pp. 123–126, May 2008.
[21] *High Frequency Surface Structure (HFSS) (15 ed.)*. [Online]. Available: http://www.ansys.com
[22] J. Xu, Z. N. Chen, X. Qing, and W. Hong, "Bandwidth enhancement for a 60 GHz substrate integrated waveguide fed cavity array antenna on LTCC," *IEEE Trans. Antennas Propag.*, vol. 59, no. 3, pp. 826–832, Mar. 2011.
[23] H. J. Lee, E. S. Li, H. Jin, C. Y. Li, and K. S. Chin, "60 GHz wideband LTCC microstrip patch antenna array with parasitic surrounding stacked patches," *IET Microw. Antennas Propag.*, vol. 13, no. 1, pp. 35–41, Jan. 2019.
[24] J. Liu, A. Vosoogh, A. U. Zaman, and J. Yang, "A slot array antenna with single-layered corporate-feed based on ridge gap waveguide in the 60 GHz band," *IEEE Trans. Antennas Propag.*, vol. 67, no. 3, pp. 1650–1658, Mar. 2019.
[25] B. Lee and Y. Yoon, "Low-profile, low-cost, broadband millimeter-wave antenna array for high-data-rate WPAN systems," *IEEE Antennas Wireless Propag. Lett.*, vol. 16, pp. 1957–1960, Apr. 2017.

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