

# A Novel Series-Connected Asymmetric Hybrid Modular Multilevel Converter for HVDC Tapping Application

CAN WANG<sup>1</sup>, (Member, IEEE), YUNMING YANG<sup>1</sup>, ZHILI LONG<sup>1,2</sup>,  
AND XUEWEI PAN<sup>1</sup>, (Member, IEEE)

<sup>1</sup>Department of Mechanical Engineering, Harbin Institute of Technology, Shenzhen 518055, China

<sup>2</sup>Key Laboratory of Precision Microelectronic Manufacturing Technology and Equipment of the Ministry of Education, Guangdong University of Technology, Guangzhou 510006, China

Corresponding author: Xuewei Pan (davidpeterpan@163.com)

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**ABSTRACT** In this paper, a three-phase series-connected asymmetric hybrid modular multilevel converter (SCAH-MMC) tap is proposed. The proposed SCAH-MMC reduces the requirement of switches by connecting phases in series to withstand the dc-bus voltage and possesses the dc fault ride-through capability by partially employing full bridge sub-modules. The system structure and operation principle of SCAH-MMC are presented in detail, which reveals the immunity of the SCAH-MMC from dc faults. In order to solve the third harmonic problem of SCAH-MMC, the interactions of harmonic components in arms are investigated. Based on that, two feed-forward third harmonic suppression methods are proposed. Furthermore, a control strategy for the SCAH-MMC is introduced to maintain dc voltage balancing in each phase under unbalanced ac fault conditions. The effectiveness of third harmonic suppression methods and the proposed control strategies of SCAH-MMC are validated by simulations using PSCAD/EMTDC. The proposed SCAH-MMC is compared with other MMC topologies in terms of cost and control to show the merits of it.

**INDEX TERMS** Modular multilevel converter (MMC), HVDC tap, fault ride-through, harmonic suppression, unbalanced fault.

## I. INTRODUCTION

Since modular multilevel converter (MMC) was first introduced in [1], [2], it has become a highly attractive topology with the merits of excellent output voltage waveforms and high efficiencies [3], [4]. MMC has been utilized in more and more medium- and high-voltage applications such as medium and high power motor drives [5], [7], STATCOMs [8], [9], and high-voltage direct current transmission (HVDC) [10]–[13].

The conventional parallel-connected MMC draws lots of attention in HVDC transmission industry with many advantages like bulk power transmission capability, independent controllability of active and reactive power, low output harmonics, low switching losses, and enhanced reliability, etc. [14]–[18]. Up to now, some main converter stations of MMC-based HVDC systems have already been put into operation, such as the Trans Bay Cable HVDC

project ( $\pm 200$ kV, 400MW) in U.S. and Xiamen Bipolar MMC-HVDC project ( $\pm 320$ kV, 1000MW) in China. In 2019, China South Grid (CSG) is constructing an HVDC project with parallel-connected MMC as the receiving end, which is named as Wudongde HVDC project (with the largest power rating so far,  $\pm 800$ kV, 8000MW).

Nevertheless, one major drawback of MMC is the high cost since it employs a large number of switching devices. The prohibitive cost of MMC prevents it from being widely applied to HVDC transmission system. To reduce the cost of MMC station while withstanding the high dc voltage, [20], [21] proposed a three-phase series-connected modular multilevel converter (SC-MMC) for HVDC tapping application, which is aiming at supplying power to rural areas though the existing HVDC transmission corridor. SC-MMC is capable of reducing the number of switching devices by one-third and that can save the cost of converter stations considerably. However, SC-MMC does not possess the capability to handle the dc-to-ground fault by itself

as its sub-modules are completely half-bridge sub-modules (HBSM).

Fault ride-through ability against the dc short-circuit fault is one of main concerns for an HVDC transmission system, especially in the case that the overhead lines are used. Some scholars present different types of topologies to ensure the MMCs with the capability to deal with dc faults [22]–[25]. The MMC based on full bridge sub-module (FBSM) is able to crack the weakness of HBSM-MMC by the self-control strategy. However, FBSM-MMC has much higher loss and cost. A symmetric hybrid modular multilevel converter (SH-MMC) is presented in [26]. Compared with FBSM-MMC, SH-MMC reduces the total loss and cost. Nevertheless, when the converter station is designed to work within full dc voltage range (from 0p.u.-1p.u.), at least 75% sub-modules have to be FBSM [27], which impairs the cost effectiveness of the SH-MMC. A new asymmetric hybrid modular multilevel converter (AH-MMC) is introduced in [28]. AH-MMC further reduces the requirement of FBSMs (the proportion of FBSM in the total number of sub-modules is 50%) and is more suitable for point-to-point or multi-terminal HVDC transmission system with overhead lines than SH-MMC due to the low cost and losses.

In this paper, the topology in [20], [28] is further extended, and a series-connected asymmetric hybrid modular multilevel converter (SCAH-MMC) tap is proposed, which incorporates the advantages of SC-MMC and AH-MMC. SCAH-MMC is suitable for long distance overhead-line transmission system and can be built alongside the existing HVDC transmission corridor to provide power to remote areas with low cost. The contributions of this paper are: 1) A novel SCAH-MMC topology for HVDC tapping is proposed; 2)The 3<sup>rd</sup> harmonic current inherent in SCAH-MMC is pinpointed from origin by applying harmonic function analysis [12]; 3)Two feed-forward control methods are proposed to suppress 3<sup>rd</sup> harmonic current; 4) Sequence control method is applied to balance dc voltage of each phase when unbalanced ac fault occurs.

This paper is organized as follows: In Section II, system structure and operating principle of the three-phase SCAH-MMC are introduced. Section III analyses the interaction between harmonic components of arms and proposes two feed-forward control methods for SCAH-MMC to suppress third harmonic current. In Section IV, a control strategy is introduced to balance the dc voltage in each phase under unbalanced fault conditions on the ac grid side. Section V presents simulation results of the proposed control methods for a SCAH-MMC working as an HVDC tap in a multi-terminal HVDC system. Conclusions are presented in Section VI.

## II. STRUTURE AND OPERATING PRINCIPLE OF THE PROPOSED SCAH-MMC

### A. STRUCTURE OF SCAH-MMC

The configuration of the proposed SCAH-MMC is shown in Fig. 1. SCAH-MMC consists of three single-phase MMCs

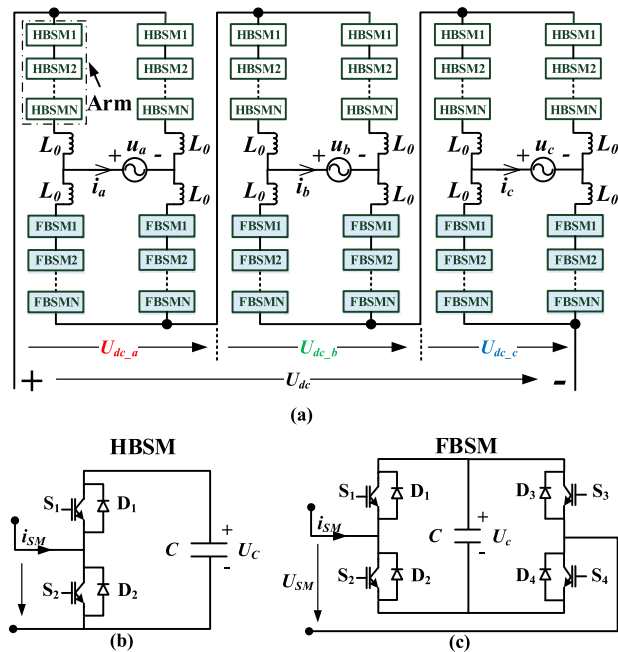


FIGURE 1. Structure of SCAH-MMC. (a) 3-phase SCAH-MMC; (b) half-bridge sub-module (HBSM); (c) full-bridge sub-module (FBSM).

connected in series. Each single-phase of it is composed of two upper arms (consist of series-connected HBSMs) and two lower arms (consist of FBSMs). Each arm includes sub-modules connected in series with the number of  $N$ . The output voltage  $U_{SM}$  of HBSMs in the upper arms can produce two values: (i)  $U_{SM} = U_C$  (ii)  $U_{SM} = 0$ . The output voltage  $U_{SM}$  of FBSMs in the lower arms can produce three values: (i)  $U_{SM} = U_C$ ; (ii)  $U_{SM} = -U_C$ ; (iii)  $U_{SM} = 0$ .  $L_0$  represents the arm inductor and  $C$  is the capacitor in each sub-module. During the operation, the dc voltage of each phase ( $U_{dc-j}$ ,  $j = a, b, c$ ) should be maintained as one-third of the dc bus voltage  $U_{dc}$ .

### B. SINGLE-PHASE SCAH-MMC

The schematic diagram of single-phase SCAH-MMC is shown in Fig. 2. In principle, each arm of MMC produces a controllable voltage, the reference of which can be expressed as:

$$u_{j1\_ref} = \frac{U_{dcrated\_j}}{2} - \frac{u_{ref\_j}}{2} \quad (1)$$

$$u_{j2\_ref} = \left( U_{dc\_j} - \frac{U_{dcrated\_j}}{2} \right) + \frac{u_{ref\_j}}{2} \quad (2)$$

$$u_{j3\_ref} = \frac{U_{dcrated\_j}}{2} + \frac{u_{ref\_j}}{2} \quad (3)$$

$$u_{j4\_ref} = \left( U_{dc\_j} - \frac{U_{dcrated\_j}}{2} \right) - \frac{u_{ref\_j}}{2} \quad (4)$$

where  $U_{dcrated\_j}$  is one-third of dc rated voltage,  $U_{dc\_j}$  represents the  $j$ -phase operating dc voltage and  $u_{ref\_j}$  is the reference of  $j$ -phase output voltage of SCAH-MMC.

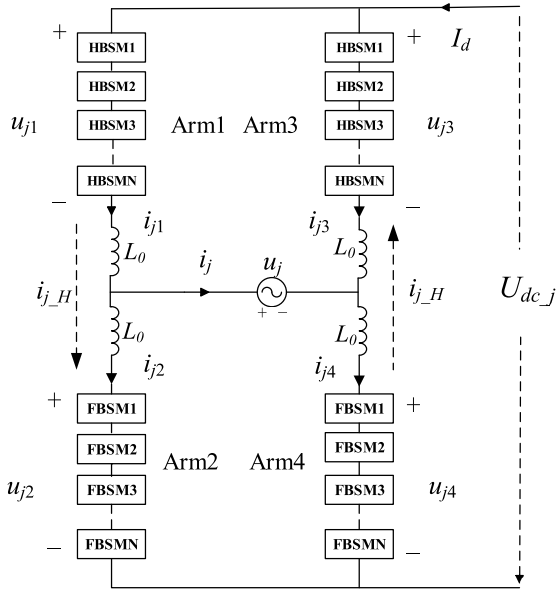


FIGURE 2. Schematic diagram of one phase of SCAH-MMC.

The modulating signal of four arms of one phase are:

$$m_{j\_arm1}(t) = \frac{1}{2} - \frac{u_{ref\_j}}{2U_{dc\_rated\_j}} \quad (5)$$

$$m_{j\_arm2}(t) = \left( \frac{U_{dc\_j}}{U_{dc\_rated\_j}} - \frac{1}{2} \right) + \frac{u_{ref\_j}}{2U_{dc\_rated\_j}} \quad (6)$$

$$m_{j\_arm3}(t) = \frac{1}{2} + \frac{u_{ref\_j}}{2U_{dc\_rated\_j}} \quad (7)$$

$$m_{j\_arm4}(t) = \left( \frac{U_{dc\_j}}{U_{dc\_rated\_j}} - \frac{1}{2} \right) - \frac{u_{ref\_j}}{2U_{dc\_rated\_j}} \quad (8)$$

Assuming the ac current of  $j$ -phase  $i_j$  is:

$$i_j = I_j \cos(\omega t + \varphi_j) \quad (9)$$

where  $I_j$  represents the amplitude of the  $j$ -phase ac current,  $\varphi_j$  is the corresponding phase angle.

The arm currents are:

$$i_{j1} = \frac{I_d}{2} + \frac{i_j}{2} + i_{j\_H} \quad (10)$$

$$i_{j2} = \frac{I_d}{2} - \frac{i_j}{2} + i_{j\_H} \quad (11)$$

$$i_{j3} = \frac{I_d}{2} - \frac{i_j}{2} - i_{j\_H} \quad (12)$$

$$i_{j4} = \frac{I_d}{2} + \frac{i_j}{2} - i_{j\_H} \quad (13)$$

$$i_{j\_H} = i_{j\_2\omega} + i_{j\_3\omega} \quad (14)$$

where  $i_{j\_H}$  represents the harmonic current (neglecting harmonics over 3<sup>rd</sup>-order),  $i_{j\_2\omega}$  and  $i_{j\_3\omega}$  are second and third harmonic current inherent in single-phase SCAH-MMC,  $I_d$  is the dc current.

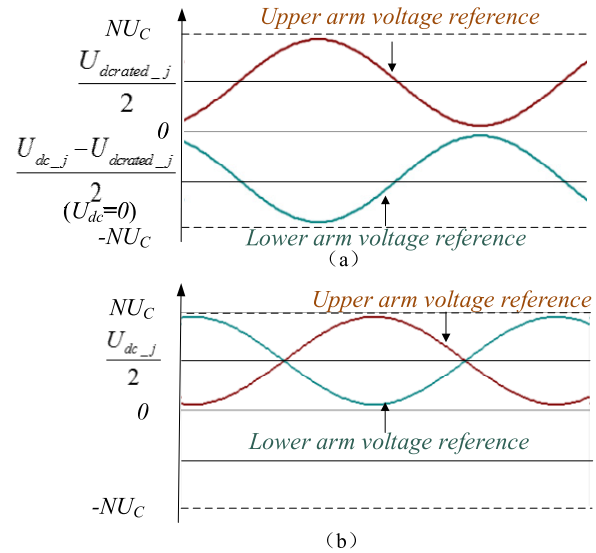


FIGURE 3. (a) Arm voltage references of SCAH-MMC when dc-bus voltage is lower than  $U_{dc\_rated}$  (b) arm voltage references of conventional parallel-connected MMC.

The modulation signal comparison is shown in Fig. 3. Arm voltage references of SCAH-MMC is shown in Fig. 3(a). When dc-bus voltage  $U_{dc}$  is lower than dc rated voltage  $U_{dc\_rated}$  or even reaches to zero, the lower arms would produce a corresponding voltage (could be totally negative). Combining with the upper arm output voltage, the converter can generate a dc voltage to follow the reduced dc-bus voltage  $U_{dc}$ . When dc fault occurs, sub-modules of arms can normally operate and there is no large ac fault currents flowing to the dc fault point. Therefore, the proposed MMC possesses dc fault ride-through capability. In contrast, Fig. 3(b) shows arm voltage references of conventional MMC composed of HBSMs. When dc-bus voltage  $U_{dc}$  is lower than dc rated voltage  $U_{dc\_rated}$ , it is not capable of producing a reduced dc voltage and external actions must be taken to rescue the converter from dc faults.

### C. MODULATION SCHEME

There are several modulation methods that can be applied to SCAH-MMC, for example the nearest level modulation (NLM) and the phase-shifted pulse-width-modulation (PS-PWM). NLM is more suitable for applications with a large number of sub-modules, which can reduce the energy loss significantly. In practical HVDC projects, NLM is applied widely. In this paper, in order to investigate the performance of SCAH-MMC tap, it is connected to  $\pm 350$ kV point-to-point FBSM-MMC based HVDC system (the system is shown in Fig. 12). Therefore, NLM method is applied to SCAH-MMC. For each arm with  $N$  sub-modules, and the number of connected capacitor in  $i$ -arm of  $j$ -phase is:

$$n_{ij\_ref} = \frac{N}{2} \pm \text{round} \left( \frac{u_{ref\_j}}{U_C} \right) \quad (i = 1, 2 \dots 4) \quad (15)$$

### III. SUPPRESSION THE 3<sup>rd</sup> HARMONIC OF SCAH-MMC

#### A. STEADY-STATE ANALYSIS OF INTERACTION BETWEEN HARMONIC COMPONENTS OF ARMS

When SCAH-MMC is in normal operation, dc voltage  $U_{dc_j} = U_{dcrated_j}$ . The reference voltage for the whole single-phase SCAH-MMC can be expressed as:

$$u_{j1\_ref} = \frac{U_{dc\_j}}{2} - \frac{u_{ref\_j}}{2} \quad (16)$$

$$u_{j2\_ref} = \frac{U_{dc\_j}}{2} + \frac{u_{ref\_j}}{2} \quad (17)$$

$$u_{j3\_ref} = \frac{U_{dc\_j}}{2} + \frac{u_{ref\_j}}{2} \quad (18)$$

$$u_{j4\_ref} = \frac{U_{dc\_j}}{2} - \frac{u_{ref\_j}}{2} \quad (19)$$

For upper arm 1 (shown in Fig. 2), the modulating signal is:

$$m_{j\_arm1}(t) = \frac{1}{2} - \frac{U_{ref\_j}}{2U_{dc\_j}} \cos(\omega t + \delta_j) \quad (20)$$

where  $U_{ref\_j}$  and  $\delta_j$  are the amplitude and phase of  $u_{ref\_j}$ .

Modulating signal  $m_{j\_arm1}(t)$  is applied to the arm 1 and the number of connected capacitor in arm 1 is:

$$n_{j\_arm1}(t) = N \left[ \frac{1}{2} - \frac{U_{ref\_j}}{2U_{dc\_j}} \cos(\omega t + \delta_j) \right] \quad (21)$$

The voltage  $u^1(t)$  across a single capacitor is obtained by considering the single capacitor charging current to be  $n(t)i(t)$ .

$$C \frac{du^1(t)}{dt} = n_{j\_arm1}(t) (0.5i_j + i_{j\_H} + 0.5I_d) \quad (22)$$

Substituting (20) and (21) into (22), it becomes:

$$\frac{C}{N} \frac{du_{j\_carm1}}{dt} = m_{j\_arm1}(t) (0.5i_j + i_{j\_H} + 0.5I_d) \quad (23)$$

where  $u_{j\_carm1}(t)$  is the voltage across an equivalent capacitor of constant size  $C/N$ .

It is assumed that second and third harmonic current passing through one arm are:

$$i_{j\_2\omega} = X_2 \cos(2\omega t + \varphi_{j2}) \quad (24)$$

$$i_{j\_3\omega} = X_3 \cos(3\omega t + \varphi_{j3}) \quad (25)$$

Substituting (10), (14), (20), (24) and (25) in (23):

$$\begin{aligned} \frac{C}{N} \frac{du_{j\_carm1}(t)}{dt} = & \left[ \frac{1}{2} - \frac{U_{ref\_j}}{2U_{dca}} \cos(\omega t + \delta_j) \right] \\ & \cdot [0.5i_j + 0.5I_d + X_2 \cos(2\omega t + \varphi_{j2}) \\ & + X_3 \cos(3\omega t + \varphi_{j3})] \end{aligned} \quad (26)$$

For the sake of convenience, the voltage  $u_{j\_carm1}(t)$  is decomposed as:

$$u_{j\_carm1}(t) = 2Q_1 + 2Q_2 + 2Q_3 + 2Q_4 + Q_5 + 2Q_6 + 2Q_7 + 2Q_8 \quad (27)$$

$u_{uj\_arm1}(t)$  is the voltage across arm 1. For the modulating signal of (20),  $n_{uj\_arm1}(t)$  capacitors of (21) are connected in

series as illustrated in Fig. 2. Therefore, the voltage  $u_{uj\_arm1}(t)$  across  $n_{uj\_arm1}(t)$  capacitors is:

$$\begin{aligned} u_{j\_arm1}(t) &= n_{j\_arm1} \frac{u_{j\_carm1}(t)}{N} \\ &= \left[ \frac{1}{2} - \frac{U_{ref\_j}}{2U_{dc\_j}} \cos(\omega t + \delta_j) \right] \\ &\quad \times \left( 2Q_1 + 2Q_2 + 2Q_3 + 2Q_4 \right. \\ &\quad \left. + 2Q_5 + 2Q_6 + 2Q_7 + 2Q_8 \right) \\ &= Q_1 + Q_2 + Q_3 + Q_4 + Q_5 + Q_6 + Q_7 + Q_8 \\ &\quad + Q_9 + Q_{10} + Q_{11} + Q_{12} + Q_{13} + Q_{14} \\ &\quad + Q_{15} + Q_{16} \end{aligned} \quad (28)$$

where

$$Q_{m+8} = -\frac{U_{ref\_j}}{2U_{dc\_j}} \cos(\omega t + \delta_j) 2Q_m \quad (29)$$

for  $m = 1, 2, \dots, 8$ .

The voltage components of arm 1 are deduced and summarized in Table 3 in Appendix A.

For the lower arm 2, the modulating signal is:

$$m_{j\_arm2}(t) = \frac{1}{2} + \frac{U_{ref\_j}}{2U_{dc\_j}} \cos(\omega t + \delta_j) \quad (30)$$

Owing to the reversal in direction of ac current in the lower arm 2 (shown in Fig. 2) and the sign change in the term of  $U_{ref_j}$  in (29), the voltage across the lower arm 2 is:

$$\begin{aligned} u_{j\_arm2}(t) &= Q_1 - Q_2 + Q_3 + Q_4 - Q_5 + Q_6 - Q_7 - Q_8 \\ &\quad - Q_9 + Q_{10} - Q_{11} - Q_{12} + Q_{13} - Q_{14} + Q_{15} + Q_{16} \end{aligned} \quad (31)$$

For the upper arm 3, the modulating signal is:

$$m_{j\_arm3}(t) = \frac{1}{2} + \frac{U_{ref\_j}}{2U_{dc\_j}} \cos(\omega t + \delta_j) \quad (32)$$

Following the same procedure as the analysis of the upper arm 1, the voltage across the upper arm 3 is:

$$\begin{aligned} u_{j\_arm3}(t) &= Q_1 - Q_2 - Q_3 - Q_4 - Q_5 + Q_6 + Q_7 + Q_8 \\ &\quad - Q_9 + Q_{10} + Q_{11} + Q_{12} + Q_{13} - Q_{14} - Q_{15} - Q_{16} \end{aligned} \quad (33)$$

For the lower arm 4, the modulating signal is:

$$m_{j\_arm4}(t) = \frac{1}{2} - \frac{U_{ref\_j}}{2U_{dc\_j}} \cos(\omega t + \delta_j) \quad (34)$$

Following the same procedure as the analysis of the lower arm 2, the voltage of arm 4 is:

$$\begin{aligned} u_{j\_arm4}(t) &= Q_1 + Q_2 - Q_3 - Q_4 + Q_5 + Q_6 - Q_7 - Q_8 \\ &\quad + Q_9 + Q_{10} - Q_{11} - Q_{12} + Q_{13} + Q_{14} - Q_{15} - Q_{16} \end{aligned} \quad (35)$$



**B. DESIGNING FEED-FORWARD CONTROL TO ACCOMPLISH SUPPRESSION OF 3<sup>rd</sup> HARMONICS FROM ANALYTICAL INSIGHTS**

The components of arm voltage show that currents  $i_j, i_d, i_{j_{2\omega}}$  and  $i_{j_{3\omega}}$  lead to voltage terms in dc, fundamental, 2<sup>nd</sup>, 3<sup>rd</sup> and higher harmonics. Fig. 4 shows the equivalent circuit of the 3<sup>rd</sup> harmonic voltages of  $j$ -phase SCAH-MMC. Since the term  $Q_{14_{3\omega}}$  is the only irrelevant to  $i_{j_{3\omega}}$ ,  $Q_{14_{3\omega}}$  is the forcing voltage of the 3<sup>rd</sup> harmonic current (shown in Fig. 4).

$$2Q_{14_{3\omega}} = \frac{NI_j}{32\omega C} \left( \frac{U_{ref\_j}}{U_{dc\_j}} \right)^2 \sin(3\omega t + 2\delta_j + \varphi_j) \quad (36)$$

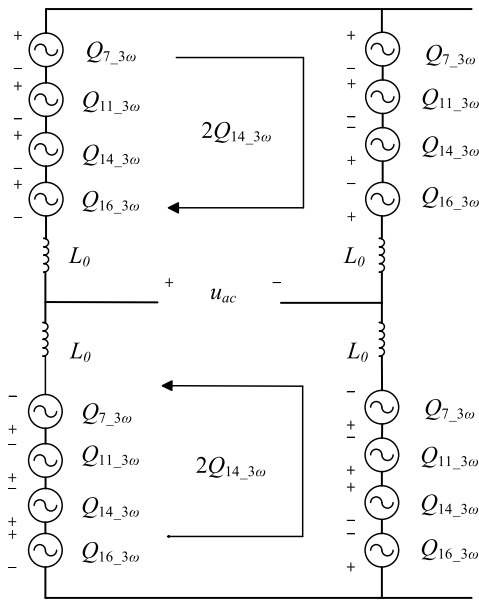


FIGURE 4. Equivalent circuit of the 3<sup>rd</sup> harmonics in each phase.

The 3<sup>rd</sup> harmonic current suppression method is based on inserting a third harmonic voltage  $u_{j\_add}$ , so that:

$$2Q_{14_{3\omega}} + u_{j\_add} = 0 \quad (37)$$

It is accomplished by modifying the modulating signal of arms by adding or subtracting a signal  $u_{j\_add} = Y_j \cos(3\omega t + \gamma_j)$  to modulating signals.  $Y_j$  and  $\gamma_j$  are both the mathematical unknowns to be solved.

Fig. 5. shows the block diagram of the implementation of  $m_{j\_arm1}(t), m_{j\_arm2}(t), m_{j\_arm3}(t)$  and  $m_{j\_arm4}(t)$  ( $j = a, b, c$ ) with 3<sup>rd</sup> harmonic current suppression based on analytical analysis. Appendix B describes the ‘detailed third harmonic suppression’ based on (37).

**C. DESIGNING THE CONTROL TO ACCOMPLISH SUPPRESSION OF 3<sup>rd</sup> HARMONICS BASED ON PR CONTROLLER**

Assuming  $i_j$  consist of fundamental current and third harmonic current. According to Fig. 2, the real output

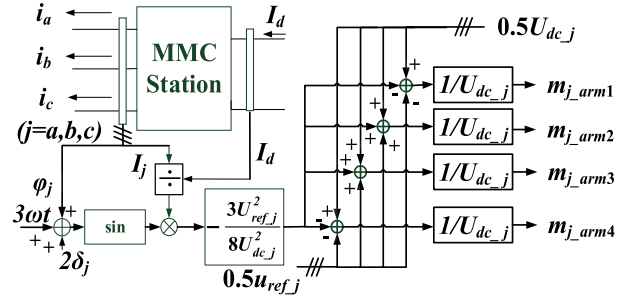


FIGURE 5. Block diagram of modulating signal with feed-forward third harmonic suppression method.

ac voltage of the single- phase SCAH-MMC is:

$$\begin{aligned} u_j &= u_{j3\_ref} + L_0 \frac{di_{j3}}{dt} - u_{j1\_ref} - L_0 \frac{di_{j1}}{dt} \\ &= u_{j\_ref} + \omega L_0 I_j \sin(\omega t + \varphi_j) \\ &\quad + 3\omega L_0 I_{j_{3\omega}} \sin(3\omega t + \varphi_{j_{3\omega}}) \\ &= u_{j\_ref} + u_{jL_0\_ \omega} + u_{jL_0\_3\omega} \end{aligned} \quad (38)$$

It is clear that there would be no third harmonic current if a voltage  $u_{j\_add}$  can be inserted so such that,

$$u_{j\_add} + u_{jL_0\_3\omega} = 0 \quad (39)$$

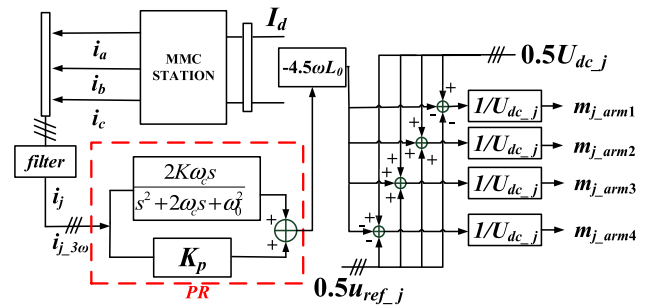


FIGURE 6. Block diagram of modulation signals generation with 3<sup>rd</sup> harmonic current suppression.

Fig. 6 shows the block diagram of the implementation of modulation signals generation with 3<sup>rd</sup> harmonic current suppression based on proportional resonant (PR) controller.

**IV. CONTROL STRATEGY UNDER THE UNBALANCED AC GRID CONDITION**

**A. OPERATION UNDER UNBALANCED GRID CONDITION**

When fault occurs on the ac-side, the converter station should be with the capability to sustain certain power transmission if possible [34]. In the case of SCAH-MMC, the most critical issue is keeping each phase dc voltage balanced under unbalanced grid condition to maintain stable operation of the SCAH-MMC and avoid taking risks of switches breakdown. Therefore,

$$U_{dc\_a} = U_{dc\_b} = U_{dc\_c} = U_{dc}/3 \quad (40)$$

As shown in Fig.1 and Fig.2, the dc current passing through series-connected phases of SCAH-MMC is equal to each other. In order to keep the dc voltage of each phase balanced, the dc power of each phase should be identical. In other word, the averaged active power on the ac-side of each phase should be equal (assuming there is equal power loss of each phase of SCAH-MMC station). Therefore, the averaged active power of each phase should be one-third of total active power  $P$ .

$$P_{ac\_a} = P_{ac\_b} = P_{ac\_c} = P_{ac}/3 \quad (41)$$

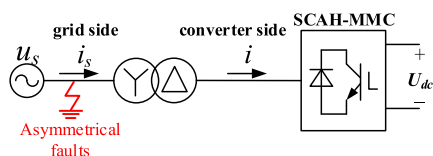


FIGURE 7. Schematic diagram of SCAH-MMC under unbalanced ac fault condition.

As shown in Fig. 7, asymmetrical faults occur at the grid side of transformer in SCAH-MMC system, there will be negative- and zero-sequence components in grid side voltages. In order to maintain the active power balanced, neither negative- nor zero-sequence currents is allowed to flow into converter side through transformer. Thus, the converter transformer is connected in the Y/Δ configuration to exclude the zero-sequence components from the converter. At the converter side of transformer, the zero-sequence component is utilized to realize the power balance of (41). Moreover, a negative-sequence component can be applied to the modulating signal of each arm, which would generate a voltage to offset the negative-sequence voltage at the converter side of the transformer.

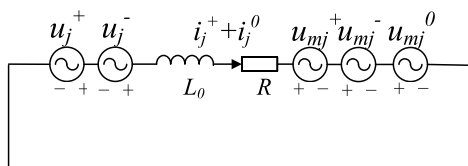


FIGURE 8. Equivalent circuit of  $j$ -phase at the converter side of the transformer with the proposed control scheme.

Fig. 8 shows the equivalent circuit of  $j$ -phase of SCAH-MMC at the converter side of transformer under the unbalanced ac grid condition.  $u_j^+$  and  $u_j^-$  represent the positive-sequence and negative-sequence voltages of

$j$ -phase at the converter side of transformer.  $u_{mj}^+$ ,  $u_{mj}^-$  and  $u_{mj}^0$  represent the positive-sequence, negative-sequence and zero-sequence voltages produced by the  $j$ -phase of SCAH-MMC. To suppress the negative-sequence current,  $u_{mj}^-$  has to be equal to  $u_j^-$ :

$$u_{mj}^- = u_j^- \quad (42)$$

Since the negative-sequence current is assumed to be fully suppressed, the positive-sequence currents and zero-sequence currents have to track their references [20] follows (43), as shown at the bottom of this page, where  $P^*$  and  $Q^*$  represent the reference active power and reactive power, respectively; the matrix  $A$  is composed of sequence voltages. Using equation (43), the references of positive- and zero-sequence currents ( $i_d^{+*}$ ,  $i_q^{+*}$ ,  $i_d^{0*}$  and  $i_q^{0*}$ ) can be derived, which is shown in Fig. 9.

### B. CONTROL SCHEME UNDER UNBALANCED GRID CONDITION

Under unbalanced ac grid conditions (e.g. asymmetrical fault), the unbalanced three-phase voltages and currents at fundamental frequency can be decomposed into positive-, negative-, and zero-sequence components. Formula (1)-(4) can be written as:

$$u_{j1\_ref} = \frac{U_{dcrated\_j}}{2} - \frac{(u_{ref\_j}^+ + u_{ref\_j}^-)}{2} \quad (44)$$

$$u_{j2\_ref} = \left( U_{dc\_j} - \frac{U_{dcrated\_j}}{2} \right) + \frac{u_{ref\_j}^+ + u_{ref\_j}^-}{2} \quad (45)$$

$$u_{j3\_ref} = \frac{U_{dcrated\_j}}{2} + \frac{u_{ref\_j}^+ + u_{ref\_j}^-}{2} \quad (46)$$

$$u_{j4\_ref} = \left( U_{dc\_j} - \frac{U_{dcrated\_j}}{2} \right) - \frac{(u_{ref\_j}^+ + u_{ref\_j}^-)}{2} \quad (47)$$

Fig. 9 shows inner current controller combining positive-, negative-sequence and zero-sequence current control loop. A positive-sequence current controller (PSCC) and a negative-sequence current controller (NSCC) are included, which are the same as the structure used in the two-level VSC. Besides, zero-sequence current controller is the same as the structure used in SC-MMC [20]. The reference of the positive-sequence current  $i_{jd}^+$ ,  $i_{jq}^+$  are derived from (43). The reference of the negative-sequence current  $i_{jd}^-$ ,  $i_{jq}^-$  are always set to zero in order to cancel out the negative-sequence voltage at the converter side of the transformer. The reference

$$\begin{bmatrix} i_d^{+*} & i_q^{+*} & i_d^{0*} & i_q^{0*} \end{bmatrix}^T = A^{-1} [2P^*/3 \ 0]^T + A^{-1} [0 \ 2Q^*/3]^T$$

$$A = \begin{bmatrix} u_d^+ & u_q^+ & 0 & 0 \\ u_q^+ & -u_d^+ & 0 & 0 \\ u_d^- & -u_q^- & u_d^+ + u_d^- & u_q^+ - u_q^- \\ -u_d^- - \sqrt{3} u_q^- & u_q^- - \sqrt{3} u_d^- & (-u_d^+ + \sqrt{3} u_q^- - u_d^- + \sqrt{3} u_q^-) & (-u_q^+ - \sqrt{3} u_d^+ + u_q^- + \sqrt{3} u_d^-) \end{bmatrix} \quad (43)$$

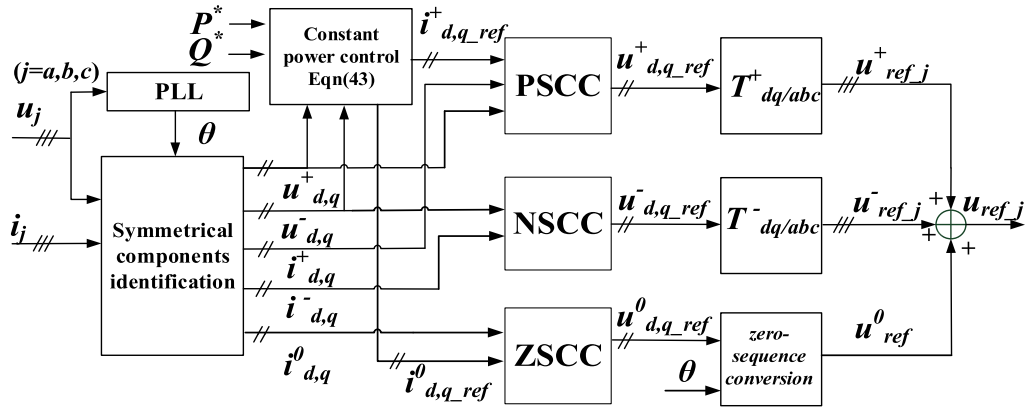


FIGURE 9. Inner current controller combining positive-, negative-sequence and zero-sequence current control loop.

of zero-sequence current controller  $i_{jd}^0, i_{jq}^0$  are also derived from (43), and to maintain the input real power of each phase is equal to each other.

V. SIMULATION RESULTS

A. VALIDATION OF THE THIRD HARMONIC CURRENT SUPPRESSION METHODS

In order to verify the effectiveness of the third harmonic suppression method, in this test, the simulated SCAH-MMC is rated at  $P = 200\text{MW}$  with dc voltage of  $U_{dc} = 165\text{kV}$ . The number of SMs each arm is  $N = 11$  and PS-PWM modulation method is applied, the arm inductance is  $L_0 = 2\text{mH}$  and the value of the SM capacitor is  $C = 4000\mu\text{F}$ .

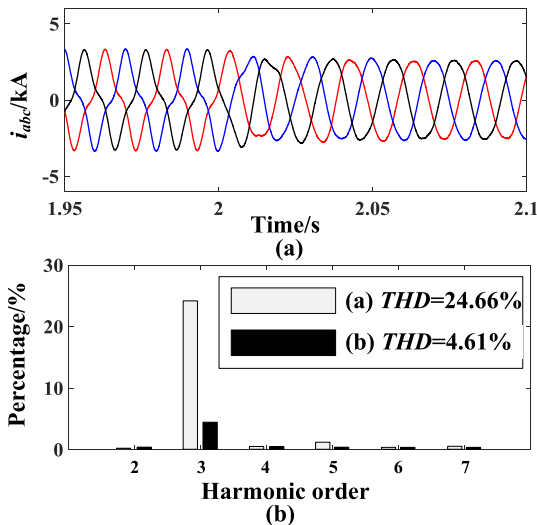


FIGURE 10. Simulation results of the feed-forward third harmonic suppression is on at 2.0 s;(a) transient waveform of ac current; (b) FFT of the ac currents: shaded bars: without the third harmonic suppression; black bars: with the third harmonic suppression.

Fig. 10 shows simulation results before and after the feed-forward third harmonic suppression is applied. Before the suppression method is activated, large amount of 3<sup>rd</sup> harmonic current exists. After the suppression method

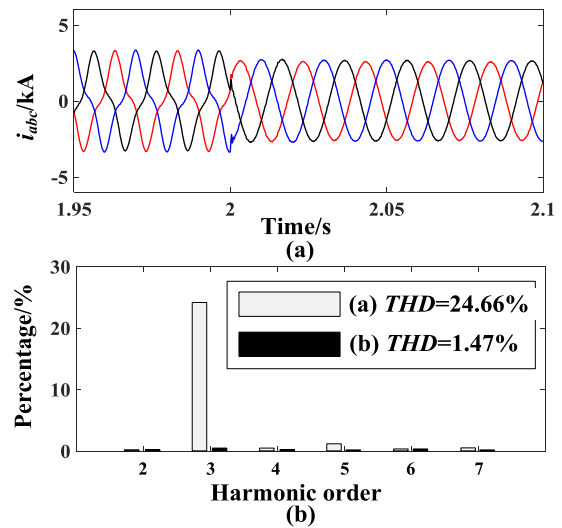


FIGURE 11. Simulation results of the back-forward third harmonic suppression is on at 2.0 s;(a) transient waveform of ac current; (b) FFT of the ac currents: shaded bars: without the third harmonic suppression; black bars: with the third harmonic suppression.

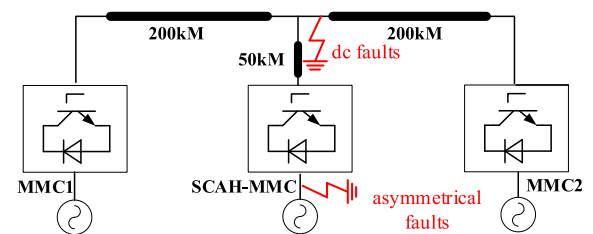


FIGURE 12. Multi-terminal HVDC system with SCAH-MMC tap.

is applied at  $t = 2.0\text{s}$ , the THD of the ac current is significantly reduced, which verifies the validity of the theoretical analysis in Section III.

Fig. 11 shows simulation results before and after the PR controller based third harmonic suppression method is utilized. When activating this method at  $t = 2.0\text{s}$ , the THD of the output current is reduced from 24.66% to 1.47%,

TABLE 1. Main circuit parameters of the simulation system.

| MMC STATION                    | Tap station  | Main station     |                  |
|--------------------------------|--------------|------------------|------------------|
|                                | SCAH-MMC     | MMC1             | MMC2             |
| Rated power $S$                | 200 MVA      | 1000MVA          | 1000MVA          |
| Rated dc voltage $U_{dcrated}$ | $\pm 350$ kV | $\pm 350$ kV     | $\pm 350$ kV     |
| Active power mode              | $P$ control  | $U_{dc}$ control | $P$ control      |
| Reactive power mode            | $Q$ control  | $U_{ac}$ control | $U_{ac}$ control |
| Number of SM per arm $N$       | 60           | 180              | 180              |
| SM capacitance $C$             | 4000 $\mu$ F | 4000 $\mu$ F     | 4000 $\mu$ F     |
| Arm inductance $L_0$           | 40mH         | 50mH             | 50mH             |
| SM capacitor voltage           | 3.9kV        | 3.9kV            | 3.9kV            |
| DC current $I_d$               | 0.286kA      | 1.429kA          | 1.429kA          |
| AC voltage $u_{ac}$            | 135.9kV      | 240.5kV          | 230kV            |
| System frequency               | 50 Hz        | 50 Hz            | 50 Hz            |

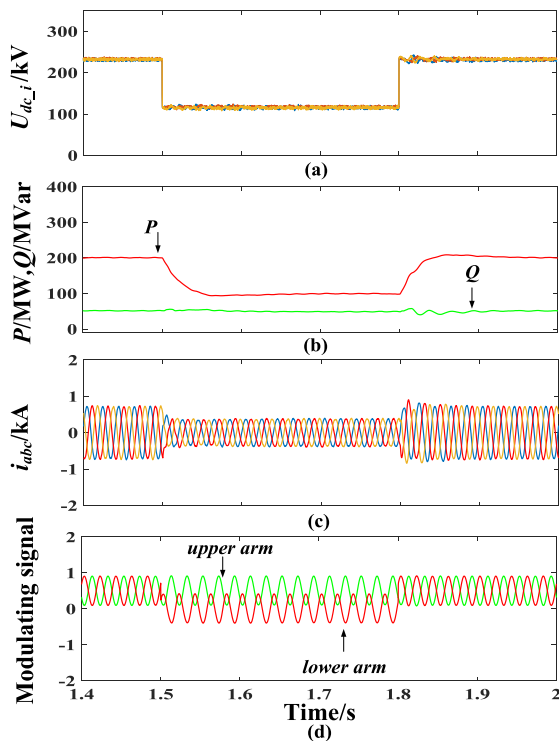


FIGURE 13. Waveforms when dc-bus voltage decreases from 1 to 0.5p.u. (a) dc voltage of each phase; (b) active power and reactive power; (c) ac currents; (d) modulating signal of upper arm and upper arm.

which presents the effectiveness of the proposed 3<sup>rd</sup> harmonic suppression method.

**B. PERFORMANCE OF SCAH-MMC TAP IN A POINT-TO-POINT HVDC SYSTEM UNDER FAULT CONDITIONS**

The objective of this case study is to investigate the behavior of the proposed control strategy for SCAH-MMC tap under dc faults and unbalanced ac grid condition in a multi-terminal HVDC grid, which is shown in Fig.12. MMC1 is working as the main rectifier station (as the voltage regulator), and MMC2 is the inverter station (as the power dispatcher). Both of MMC1 and MMC2 are based on FBSM with dc fault ride-through capability. SCAH-MMC tap is connected in the

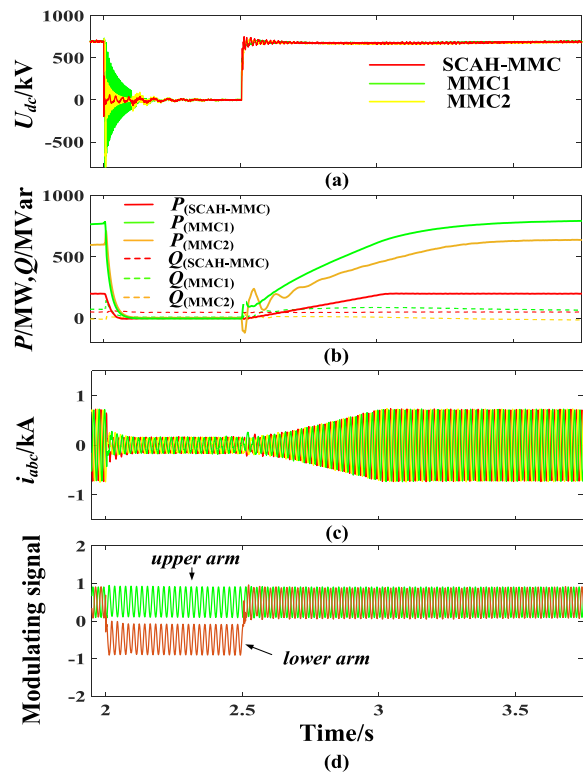
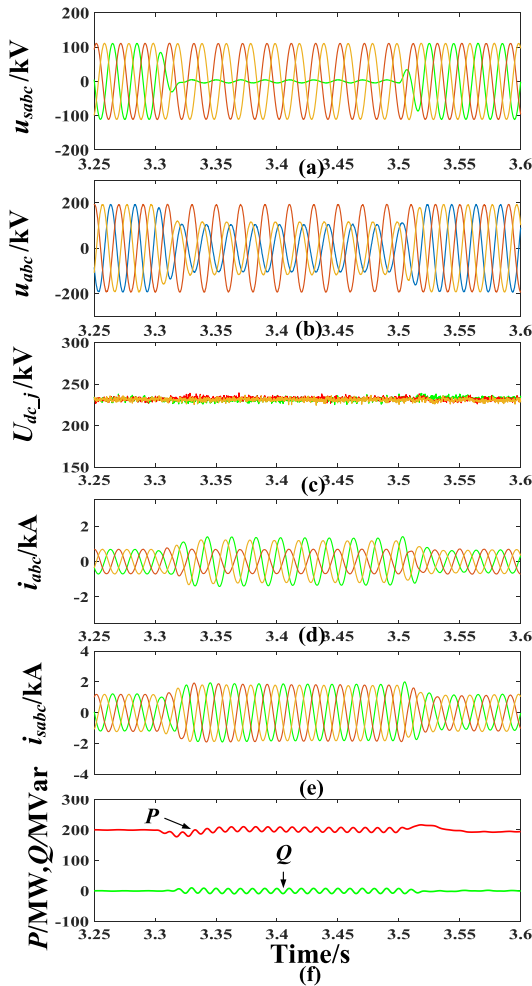


FIGURE 14. Waveforms of the system under dc short-circuit fault condition. (a) dc voltage of each MMC station; (b) active power and reactive power of each MMC station; (c) ac currents of SCAH-MMC tap; (d) modulating signal of upper arm and lower arm of SCAH-MMC tap.

middle of the point-to-point HVDC transmission corridor. Table 1 summaries the parameters and control strategy of the whole simulated system.

The transient behavior of the system under a temporary low dc voltage fault is presented in Fig. 13. The dc-bus voltage is set down to 0.5p.u. at time = 1.5s and it recovers to 1.0 p.u. at time = 1.8s. Fig. 13(a) presents the dc voltage of each phase. During the low dc voltage fault, SCAH-MMC tap still maintains to transfer 0.5p.u. active power and 1p.u. reactive power as shown in Fig. 13(b). Fig. 13(c) presents ac currents of the SCAH-MMC. Fig. 13(d) shows modulating signal of upper arm and upper arm, which confirms the



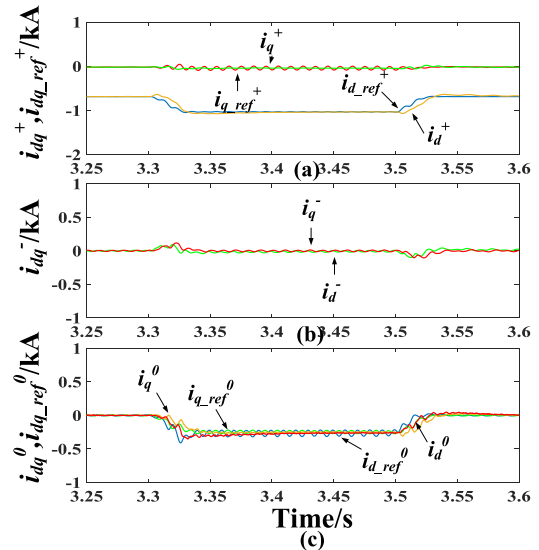
**FIGURE 15.** Simulation waveforms of the studied system under a single-line-to-ground ac fault. (a) three-phase voltage at the grid side of transformers; (b) three-phase voltage at the converter side of transformers; (c) three-phase dc-voltage of SCAH-MMC tap; (d) three-phase current at the converter side of transformers; (e) three-phase current at the grid side of transformers; (f) active power and reactive power.

rationality of the control strategy under low dc voltage fault condition.

Fig. 14 presents the transient behavior of the system under a dc short-circuit fault condition as shown in Fig. 12. At the time  $t = 2.0s$ , a temporary dc short-circuit fault occurs in the middle section of the overhead line (250km from the rectification side), and the fault lasts for 0.1s. The IGBTs of MMC1 and MMC2 block at 2.005s. After the dc short-circuit fault is cleared, the overhead line takes 0.4s for deionization (typical time is 0.2s to 0.5s). SCAH-MMC tap operates normally during the fault and maintains the reactive power  $Q = 50MVar$  as shown in Fig. 14 (b). After 0.5s, MMC1 and MMC2 restart at  $t = 2.5s$ . Fig. 14(c) presents the ac currents of SCAH-MMC tap. Fig. 14(d) presents modulating signal of upper arm and lower arm of SCAH-MMC tap.

The system operates with the command reference of  $P^* = 200MW$  and  $Q^* = 0MVar$ . A temporary single line-to-ground ac fault occurs at 3.3s and lasts for 0.2s. Fig. 15 shows the transient behavior of the system under the

single line-to-ground ac fault condition. Fig. 15(a) and (b) show the three-phase voltages  $u_{sj}$  at the grid side of transformer and voltages  $u_j$  at the converter side of transformer, respectively. Fig. 15(c) shows the dc voltage of each phase, respectively. The dc voltage of each phase is kept to one third of the total dc voltage, which confirms the effectiveness of the control strategy under asymmetrical faults. Fig. 15(d) and (e) show currents  $i_j$  at the converter side of transformer and currents  $i_{sj}$  at the grid side of transformer. Fig. 15(f) shows the total active power and the total reactive power, respectively.



**FIGURE 16.** Simulation waveforms of the studied system under single-line-to-ground fault at grid side: (a) positive-sequence reference currents and positive-sequence currents at converter side; (b) negative-sequence reference currents and negative-sequence currents at converter side; (c) zero-sequence reference currents and zero-sequence currents at converter side.

Fig. 16 shows the currents at the converter side in rotating  $dq$  frame. Fig. 16(a) represents the positive-sequence reference currents  $i_{dq\_ref}^+$  and positive-sequence currents  $i_{dq}^+$  at the converter side, and positive-sequence currents  $i_{dq}^+$  can greatly follow positive-sequence reference currents  $i_{dq\_ref}^+$ . In addition,  $i_q^+$  is also controlled as zero to keep reactive power  $Q = 0$ . Fig. 16(b) represents the negative-sequence reference currents  $i_{dq\_ref}^-$  and negative-sequence currents  $i_{dq}^-$  at the converter side.  $i_{dq\_ref}^- = 0$ , and the  $i_{dq}^-$  can be well controlled to zero through PSSC. Fig. 16(c) represents the zero-sequence reference currents  $i_{dq}^0$  at the converter side.  $i_{dq}^0$  is well regulated to zero-sequence reference currents  $i_{dq\_ref}^0$  to maintain the real power of each phase is equal to each other and the dc voltage of each phase is equal during the single-line-to-ground ac fault.

## VI. CONCLUSIONS

This paper proposes a novel SCAH-MMC which is suitable for the HVDC tapping application. The proposed converter combines the advantages of both SC-MMC and AH-MMC, consequently, it is with low-cost feature and dc



**TABLE 2.** Comparison of several topologies of MMCs.

| Topologies of MMCs                             | parallel-connected MMC |          |                           |             |           |           | series-connected MMC |                 |
|--|------------------------|----------|---------------------------|-------------|-----------|-----------|----------------------|-----------------|
|  | ①                      | ②        | ③                         | ④           | ⑤         | ⑥         | ⑦                    | ⑧               |
|  | HBSM-MMC               | FBSM-MMC | SH-MMC (75%FBSM, 25%HBSM) | AH-MMC [28] | HCMC [23] | AAC [24]  | HBSM-MMC [20]        | Proposed AH-MMC |
| number of SMs                                  | $6N$                   | $6N$     | $6N$                      | $6N$        | $1.5N$    | $3N$      | $4N$                 | $4N$            |
| number of switches in the direct switch        | 0                      | 0        | 0                         | 0           | $6N$      | $12N/\pi$ | 0                    | 0               |
| number of switches                             | $12N$                  | $24N$    | $21N$                     | $18N$       | $12N$     | $15.8N$   | $8N$                 | $12N$           |
| number of conduction switches during operation | $6N$                   | $12N$    | $10.5N$                   | $9N$        | $9N$      | $9.8N$    | $4N$                 | $6N$            |
| control flexibility                            | good                   | good     | good                      | good        | general   | general   | good                 | good            |
| manufacturing difficulty                       | easy                   | easy     | easy                      | easy        | difficult | difficult | easy                 | easy            |
| dc fault ride-through capability               | no                     | yes      | yes                       | yes         | yes       | yes       | no                   | yes             |
| energy loss                                    | low                    | high     | large                     | general     | general   | large     | less                 | less            |
| construction cost                              | low                    | high     | large                     | general     | lower     | general   | low                  | low             |
| THD  | good                   | good     | good                      | good        | fair      | fair      | good                 | good            |

fault ride-through capability. The conclusions are drawn as follows:

1) Compared with other MMC topologies as shown in Table 2, the overall performance of the proposed SCAH-MMC is great. It possesses the dc fault ride-through ability and at the same time reduces the construction cost, which makes it suitable for the HVDC tapping application in the overhead lines transmission system.

2) Simulation results validates that both of the proposed feed-forward 3rd harmonic suppression methods are effective. The suppression of 3rd harmonics eliminates the bad effects inherent in the series-connected AH-MMC. In addition, it makes the reduction of the sub-module capacitor possible and that could further reduce the construction cost.

3) The sequence control strategy guarantees the active power balancing among three phases to maintain the dc voltage of each phase in a balanced condition. Simulation results of a 200MW SCAH-MMC tap validate the feasibility of the sequence control strategy under unbalanced ac grid condition.

## APPENDIX

### A. VOLTAGE COMPONENTS IN ARM 1 OF J-PHASE

TABLE 3 shows all the voltage components in arm 1 of  $j$ -phase.

### B. DETAILED THIRD HARMONIC ELIMINATION BASED ON ANALYTICAL ANALYSIS

For upper arm 1, after adding a signal  $Y_j \cos(3\omega t + \gamma_j)$  to modulating signal,(20) becomes:

$$m_{uj\_arm1}(t) = \frac{1}{2} - \frac{1}{2U_{dc\_j}} [U_{ref\_j} \cos(\omega t + \delta_j) + Y_j \cos(3\omega t + \gamma_j)] \quad (B1)$$

Modulating signal  $m_{uj\_arm1}(t)$  is applied to the arm 1 and the number of connected capacitor in arm 1:

$$n_{uj\_arm1}(t) = N \left[ \frac{1}{2} - \frac{U_{ref\_j}}{2U_{dc\_j}} \cos(\omega t + \delta_j) - \frac{Y_j}{2U_{dc\_j}} \cos(3\omega t + \gamma_j) \right] \quad (B2)$$

It is assumed that third harmonics current is suppressed. So, (26) becomes:

$$\frac{C}{N} \frac{du_{j\_carm1}(t)}{dt} = \left[ \frac{1}{2} - \frac{U_{ref\_j}}{2U_{dc\_j}} \cos(\omega t + \delta_j) - \frac{Y_j}{2U_{dc\_j}} \cos(3\omega t + \gamma_j) \right] \cdot [0.5i_j + 0.5I_d + X_2 \cos(2\omega t + \varphi_{j2})] \quad (B3)$$

TABLE 3. Voltage components of arm1 of j-phase.

| Voltage Terms | Components in different frequencies  |
|---------------|--|
| $Q_1$         | $Q_{1\_dc} = \frac{NI_d t}{8C}$ ; $Q_{1\_w}$ , $Q_{1\_2w}$ , $Q_{1\_3w}$ and $Q_{1\_over3w} = 0$   |
| $Q_2$         | $Q_{2\_w} = \frac{NI_j}{8\omega C} \sin(\omega t + \varphi_j)$ ; $Q_{2\_dc}$ , $Q_{2\_2w}$ , $Q_{2\_3w}$ and $Q_{2\_over3w} = 0$   |
| $Q_3$         | $Q_{3\_2w} = \frac{NX_2}{8\omega C} \sin(2\omega t + \varphi_{j2})$ ; $Q_{3\_dc}$ , $Q_{3\_w}$ , $Q_{3\_3w}$ and $Q_{3\_over3w} = 0$   |
| $Q_4$         | $Q_{4\_3w} = \frac{NX_3}{12\omega C} \sin(3\omega t + \varphi_{j3})$ ; $Q_{4\_dc}$ , $Q_{4\_w}$ , $Q_{4\_2w}$ and $Q_{4\_over3w} = 0$  |
| $Q_5$         | $Q_{5\_w} = -\frac{NI_d U_{ref-j}}{8\omega CU_{dc-j}} \sin(\omega t + \delta_j)$ ; $Q_{5\_dc}$ , $Q_{5\_2w}$ , $Q_{5\_3w}$ and $Q_{5\_over3w} = 0$   |
| $Q_6$         | $Q_{6\_dc} = -\frac{NI_j U_{ref-j} t}{16CU_{dc-j}} \cos(\delta - \varphi_j)$ ; $Q_{6\_2w} = -\frac{NI_d U_{ref-j}}{32\omega CU_{dc-j}} \sin(2\omega t + \varphi_j + \delta_j)$ ; $Q_{6\_2w}$ , $Q_{6\_3w}$ and $Q_{6\_over3w} = 0$   |
| $Q_7$         | $Q_{7\_w} = -\frac{NX_2 U_{ref-j}}{8\omega CU_{dc-j}} \sin(\omega t + \varphi_{j2} - \delta_j)$ ; $Q_{7\_3w} = -\frac{NX_2 U_{ref-j}}{24\omega CU_{dc-j}} \sin(3\omega t + \delta_j + \varphi_{j2})$ ; $Q_{7\_dc}$ , $Q_{7\_2w}$ , and $Q_{7\_over3w} = 0$   |
| $Q_8$         | $Q_{8\_2w} = -\frac{NX_3 U_{ref-j}}{16\omega CU_{dc-j}} \sin(2\omega t + \varphi_{j3} - \delta_j)$ ; $Q_{8\_over3w} = -\frac{NX_3 U_{ref-j}}{32\omega CU_{dc-j}} \sin(4\omega t + \varphi_{j3} + \delta_j)$ ; $Q_{8\_dc}$ , $Q_{8\_w}$ , and $Q_{8\_3w} = 0$   |
| $Q_9$         | $Q_{9\_w} = -\frac{NI_d t U_{ref-j}}{8CU_{dc-j}} \sin(\omega t + \delta_j)$ ; $Q_{9\_dc}$ , $Q_{9\_2w}$ , $Q_{9\_3w}$ and $Q_{9\_over3w} = 0$  |
| $Q_{10}$      | $Q_{10\_dc} = \frac{NI_j U_{ref-j}}{16\omega CU_{dc-j}} \sin(\delta_j - \varphi_j)$ ; $Q_{10\_2w} = -\frac{NI_j U_{ref-j}}{16\omega CU_{dc-j}} \sin(2\omega t + \delta_j + \varphi_j)$ ; $Q_{10\_w}$ , $Q_{10\_3w}$ , and $Q_{10\_over3w} = 0$   |
| $Q_{11}$      | $Q_{11\_w} = -\frac{NX_2 U_{ref-j}}{16\omega CU_{dc-j}} \sin(\omega t + \varphi_{j2} - \delta_j)$ ; $Q_{11\_3w} = -\frac{NX_2 U_{ref-j}}{16\omega CU_{dc-j}} \sin(3\omega t + \varphi_{j2} + \delta_j)$ ; $Q_{11\_dc}$ , $Q_{11\_2w}$ , and $Q_{11\_over3w} = 0$   |
| $Q_{12}$      | $Q_{12\_2w} = -\frac{NX_3 U_{ref-j}}{24\omega CU_{dc-j}} \sin(2\omega t + \varphi_{j3} - \delta_j)$ ; $Q_{12\_over3w} = -\frac{NX_3 U_{ref-j}}{24\omega CU_{dc-j}} \sin(4\omega t + \varphi_{j3} + \delta_j)$ ; $Q_{12\_dc}$ , $Q_{12\_w}$ , and $Q_{12\_3w} = 0$  |
| $Q_{13}$      | $Q_{13\_2w} = \frac{NI_d U_{ref-j}^2}{16\omega CU_{dc-j}^2} \sin(2\omega t + 2\delta_j)$ ; $Q_{13\_dc}$ , $Q_{13\_w}$ , $Q_{13\_3w}$ and $Q_{13\_over3w} = 0$  |
| $Q_{14}$      | $Q_{14\_w} = \frac{NI_j U_{ref-j}^2}{64\omega CU_{dc-j}^2} \sin(\omega t + \varphi_j) + \frac{NI_d t U_{ref-j}^2}{16CU_{dc-j}^2} \cos(\delta_j + \varphi_j) \cos(\omega t + \delta_j)$ ; $Q_{14\_3w} = \frac{NI_j U_{ref-j}^2}{64\omega CU_{dc-j}^2} \sin(3\omega t + 2\delta_j + \varphi_j)$ ; $Q_{14\_dc}$ , $Q_{14\_2w}$ and $Q_{14\_over3w} = 0$   |
| $Q_{15}$      | $Q_{15\_dc} = \frac{NX_2 U_{ref-j}^2}{16\omega CU_{dc-j}^2} \sin(\varphi_2 - 2\delta_j)$ ; $Q_{15\_2w} = \frac{NX_2 U_{ref-j}^2}{12\omega CU_{dc-j}^2} \sin(2\omega t + \varphi_{j2})$ ; $Q_{15\_over3w} = \frac{NX_2 U_{ref-j}^2}{48\omega CU_{dc-j}^2} \sin(4\omega t + \varphi_{j2} + 2\delta_j)$ ; $Q_{15\_w}$ and $Q_{15\_3w} = 0$                |
| $Q_{16}$      | $Q_{16\_w} = \frac{NX_3 U_{ref-j}^2}{32\omega CU_{dc-j}^2} \sin(\omega t + \varphi_{j3} - 2\delta_j)$ ; $Q_{16\_3w} = \frac{3NX_3 U_{ref-j}^2}{64\omega CU_{dc-j}^2} \sin(3\omega t + \varphi_{j3})$ ; $Q_{16\_over3w} = \frac{NX_3 U_{ref-j}^2}{64\omega CU_{dc-j}^2} \sin(5\omega t + \varphi_{j3} + 2\delta_j)$ ; $Q_{16\_dc}$ and $Q_{16\_2w} = 0$ |

Following the same procedure as the analysis of upper arm 1, the voltage across the upper arm1 is:

$$u_{uj\_carm1}(t) = 2Q_1 + 2Q_2 + 2Q_3 + 2Q_5 + 2Q_6 + 2Q_7 + 2Q_A + 2Q_B + 2Q_C \quad (B4)$$

$u_{uj\_arm1}(t)$  is the voltage across arm 1. For the modulating signal of (B1),  $n_{uj\_arm1}(t)$  capacitors of (B2) are connected in series as illustrated in Fig. 2. Therefore the voltage  $u_{uj\_arm1}(t)$  across  $n_{uj\_arm1}(t)$  capacitors is:

$$u_{uj\_arm1}(t) = n_{j\_arm1} \frac{u_{j\_carm1}(t)}{N} = Q_1 + Q_2 + Q_3 + Q_5 + Q_6 + Q_7 + Q_A + Q_B + Q_C$$

$$+ Q_9 + Q_{10} + Q_{11} + Q_{13} + Q_{14} + Q_{15} + Q_D + Q_E + Q_F + Q_G + Q_H + Q_I + Q_J + Q_K + Q_L + Q_M + Q_N + Q_O \quad (B5)$$

where

$$Q_{D,E,F} = -\frac{U_{refj}}{2U_{dcj}} \cos(\omega t + \delta_j) 2Q_{A,B,C} \quad (B6)$$

$$Q_{G,H...O} = -\frac{Y}{2U_{dcj}} \cos(\omega t + \gamma_j) 2Q_{1,2,3,5,6,7,A,B,C} \quad (B7)$$

For arm 2, arm3 and arm 4, following the same procedure as the analysis of upper arm 1, the voltage across the arm 2,

arm 3 and arm 4 are:

$$\begin{aligned}
 u_{uj\_arm2}(t) &= n_{j\_arm2} \frac{u_{j\_carm2}(t)}{N} \\
 &= Q_1 - Q_2 + Q_3 - Q_5 + Q_6 - Q_7 + Q_A - Q_B + Q_C \\
 &\quad - Q_9 + Q_{10} - Q_{11} + Q_{13} - Q_{14} + Q_{15} \\
 &\quad - Q_D + Q_E - Q_F - Q_G + Q_H - Q_I + Q_J - Q_K \\
 &\quad + Q_L - Q_M + Q_N - Q_O \quad (B8)
 \end{aligned}$$

$$\begin{aligned}
 u_{uj\_arm3}(t) &= n_{j\_arm3} \frac{u_{j\_carm3}(t)}{N} \\
 &= Q_1 - Q_2 - Q_3 - Q_5 + Q_6 + Q_7 - Q_A + Q_B + Q_C \\
 &\quad - Q_9 + Q_{10} + Q_{11} + Q_{13} - Q_{14} - Q_{15} + Q_D \\
 &\quad - Q_E - Q_F + Q_G - Q_H - Q_I - Q_J + Q_K + Q_L \\
 &\quad - Q_M + Q_N + Q_O \quad (B9)
 \end{aligned}$$

$$\begin{aligned}
 u_{uj\_arm4}(t) &= n_{j\_arm4} \frac{u_{j\_carm4}(t)}{N} \\
 &= Q_1 + Q_2 - Q_3 + Q_5 + Q_6 - Q_7 - Q_A - Q_B + Q_C \\
 &\quad + Q_9 + Q_{10} - Q_{11} + Q_{13} + Q_{14} - Q_{15} - Q_D \\
 &\quad - Q_E + Q_F - Q_G - Q_H + Q_I - Q_J - Q_K + Q_L \\
 &\quad + Q_M + Q_N - Q_O \quad (B10)
 \end{aligned}$$

Fig.17 shows the equivalent circuit of the 3<sup>rd</sup> harmonics voltage of *j*-phase SCAH-MMC after suppression.

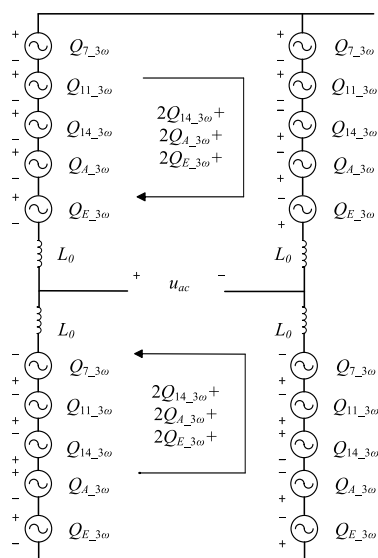


FIGURE 17. Equivalent circuit of the 3<sup>rd</sup> harmonics voltage.

There is no 3<sup>rd</sup> harmonics voltage in equivalent circuit of Fig. 17. Therefore,

$$\begin{aligned}
 &Q_{14\_3\omega} + Q_{A\_3\omega} + Q_{E\_3\omega} \\
 &= -\frac{N I_d Y_j}{24\omega C U_{dc_j}} \sin(3\omega t + \gamma_j) \\
 &\quad + \frac{N I_j U_{ref\_j}}{64\omega C U_{dc_j}^2} \sin(3\omega t + \delta_j + \gamma_j - \phi_j)
 \end{aligned}$$

$$\begin{aligned}
 &+ \frac{N I_j U_{ref\_j}}{128\omega C U_{dc_j}^2} \sin(3\omega t - \delta + \gamma_j + \phi_j) \\
 &+ \frac{N I_j U_{ref\_j}^2}{32\omega C U_{dc_j}^2} \sin(3\omega t + 2\delta + \phi_j) = 0 \quad (B11)
 \end{aligned}$$

Formula (B11) is simplified and  $Y_j \cos(3\omega t + \gamma_j)$  of (26) is with the solution:

$$\begin{aligned}
 Y_j \cos(3\omega t + \gamma_j) &= -\frac{3I_j U_{ref\_j}}{16I_d U_{dc_j}} \sin(3\omega t + \delta_j + \gamma_j - \phi_j) \\
 &\quad - \frac{3I_j U_{ref\_j}^2}{4I_d U_{dc_j}} \sin(3\omega t + 2\delta + \phi_j) \\
 &\approx -\frac{3I_j U_{ref\_j}^2}{4I_d U_{dc_j}} \sin(3\omega t + 2\delta + \phi_j) \quad (B12)
 \end{aligned}$$

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**CAN WANG** (M'15) received the Ph.D. degree in electrical engineering from McGill University, Montreal, Canada, in 2015. In 2016, he was with China Southern Grid (CSG) Electric Power Research Institute (EPRI) as a Research Engineer. In 2017, he joined the Harbin Institute of Technology, Shenzhen, as an Assistant Professor. His research interests include the modeling, control, and simulation of power electronics converters, and power grid integration of renewable energies such as wind and solar.



**YUNMING YANG** was born in 1993. He received the B.Eng. degree from the Harbin University of Science and Technology, Harbin, China, in 2017. He is currently pursuing the M.Eng. degree in electrical engineering with the Harbin Institute of Technology, Shenzhen, China. His research interests include the application of VSC-HVDC and flexible ac transmission systems.



**ZHILI LONG** received the B.S., M.S., and Ph.D. degrees in mechatronics engineering from Central South University, Changsha, China, in 2000, 2002, and 2007, respectively. He is currently an Associate Professor with the Department of Mechanical Engineering, Harbin Institute of Technology, Shenzhen, China. He is also a Co-Researcher at the Guangdong University of Technology, Guangzhou, China. His research interests include the modeling, control, and optimization of ultrasonic systems.



**XUEWEI PAN** (S'12–M'16) received the B.E. degree in electronic engineering from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2011, and the Ph.D. degree in power electronics from the Department of Electrical and Computer Engineering, National University of Singapore, in 2015. He was a Research Fellow with the Energy Research Institute, NTU, Singapore, from 2014 to 2016. He is currently an Associate Professor with the Harbin Institute of Technology (Shenzhen), China. His research interests include distributed generation, renewable integration, micro-grid energy systems, soft-switching methods, and modulation techniques for high-frequency power conversion for renewable energy.

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