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Punch-Through-Stopper Free Nanosheet FETs With Crescent Inner-Spacer and Isolated Source/Drain

JUN-SIK YOON[1], (Member, IEEE), JINSU JEONG[2], SEUNGHWAN LEE[2], AND ROCK-HYUN BAEK[2], (Member, IEEE)

[1]Information Research Laboratories, Pohang University of Science and Technology (POSTECH), Pohang 37673, South Korea
[2]Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang 37673, South Korea

Corresponding author: Rock-Hyun Baek (rh.baek@postech.ac.kr)

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ABSTRACT Structural modifications of 5-nm node nanosheet FETs (NSFETs) were quantitatively analyzed using fully calibrated TCAD. The NSFETs with crescent inner spacer improve the short-channel effects by increasing effective gate lengths but also increase the parasitic capacitances by greater outer fringing electric field. The NSFETs with a crescent inner spacer and slanted source/drain (S/D) increase the physical gate lengths of bottom NS channel, but the anisotropic over-etching of substrate regions induces punchthrough effect at the bottom transistor. Bottom isolation by depositing dielectrics prior to S/D formation is effective to eliminate the punchthrough effect as well as to attain shorter RC delay by better electrostatics and parasitic capacitance reduction. In addition, the isolated S/D NSFETs without punchthrough stopper decrease parasitic and gate capacitances further at the frequency greater than 600 MHz at which the inversion carriers are not formed at the bottom transistor. Thus, although the crescent inner spacer and slanted S/D structure are unintendedly formed under process, these modifications lead to the performance boosting and the process simplicity of the 5-nm node NSFETs.

INDEX TERMS 5-nm node, bottom isolation, bottom transistor, crescent inner-spacer, nanosheet, slanted source/drain.

I. INTRODUCTION

Si fin field-effect transistors (FinFETs) have been scaled down to 10-nm node successfully by narrowing fin with high aspect ratio and optimizing metal-lines (M0) [1]. However, under device scaling, increase of sub-fin leakage and decrease of contact area along with fin depopulation degrade power and performance critically [2]. Gate-all-around FETs improve the short-channel effects (SCEs) by wrapping around the channel, but there are performance bottlenecks by small effective widths (W_{eff}) and AC performance degradation [3].

In the meantime, three-stacked nanosheet FETs (NSFETs) have been introduced to attain greater current drivability and better SCEs [4]. Wider W_{eff} of NSFETs under the same footprint enabled the performance boosting by increasing drive currents and decreasing parasitic capacitances (C_{para}) out of gate capacitances (C_{gg}) [5], [6]. However, structural concerns of the NSFETs that can affect the performance estimation in the following technology node have not been analyzed in detail.

In this work, the 5-nm node NSFETs having different, but realistic structures are investigated using fully-calibrated 3-D TCAD. After evaluating the structural effects of the NSFETs, a promising structure is suggested in the perspective of device performance.

II. DEVICE STRUCTURE AND SIMULATION METHOD

5-nm node NSFETs were simulated using Sentaurus TCAD [7]. Drift-diffusion transport model was calculated with Poisson and carrier continuity equations self-consistently. Density-gradient model was used to consider the

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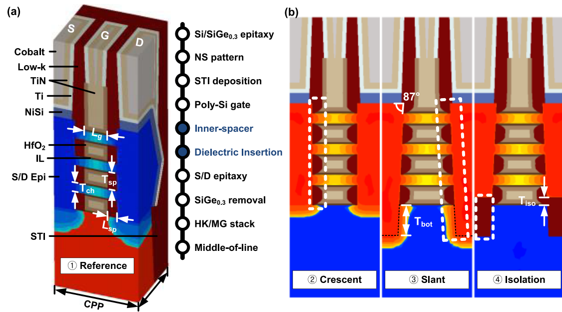

FIGURE 1. (a) Schematic diagram of three-stacked NSFETs and (b) structural modifications as shown in [4]. Four different structures were reference, crescent inner-spacer (IS), slanted source/drain (S/D), and isolated S/D.

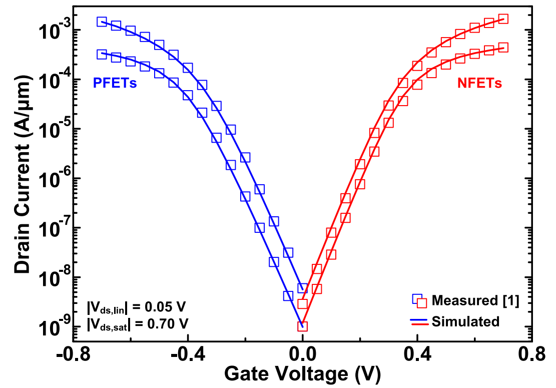

FIGURE 2. TCAD results (lines) calibrated to the experimental data (symbols) of the 10-nm node FinFETs [1].

quantum confinements of the NS channels. Carrier mobility and recombination models used in this work were equivalent to [8]. Deformation potential model was used to consider the changes of energy bandgap, effective mass, and effective density-of-states by the stress.

Fig. 1a shows a schematic diagram of 5-nm node NSFETs. Detailed simulated process flow of NSFETs is specified in [9]. Diamond-shaped source/drain (S/D) epi wrapped with 5-nm-thick NiSi was used. M0 region consisted of Co metal, 2-nm-thick Ti liner (250 $\mu\Omega \cdot$ cm), and 3-nm-thick TiN barrier (350 $\mu\Omega \cdot$ cm) [10]. There were several structural concerns under the NSFET process (Fig. 1b): crescent inner-spacer (IS), slanted S/D, and isolated S/D. Crescent IS is formed because some of Ge atoms diffuse toward Si NS channels under STI annealing and make etching rates of NS spacing different between the middle and the corner [4]. Slanted S/D epi is formed because anisotropic etching is not ideally vertical. Isolated S/D is introduced to remove the bottom leakage current.

Fig. 2 shows the TCAD results calibrated to the 10-nm node FinFETs [1]. Ballistic coefficient and saturation velocity were finely tuned by Monte Carlo simulation. Several mobility parameters related to surface roughness scattering were then tuned to fit the drain currents (I_{ds}) at on-state. Contact resistivity at the NiSi interface was $5 \times 10^{-9} \Omega \cdot \mathrm{cm}^2$. S/D regions were highly doped with phosphorus (boron) at 10^{20} (5×10^{20}) cm^{-3} for NFETs (PFETs), and channel was undoped at 10^{15} cm^{-3}. Table I defines all the geometrical parameters of the NSFETs as in [11].

TABLE 1. Geometrical Parameters For 5-nm node NSFETs.

	Geometrical Parameters	Values (nm)
FP	Fin pitch	56
CPP	Contacted poly-gate pitch	44
$P/N\text{-}SP$	P/N-type separation length	20
L_g	Gate length	12
L_{sp}	Spacer length	5
T_{IL}	Interfacial layer thickness	1
T_{HK}	High-k thickness	2
W_{top}	Top-side NS width	30
W_{bot}	Bottom-side NS width	33
T_{ch}	NS thickness	5
T_{sp}	NS spacing	10
T_{bot}	S/D over-etching depth	15
T_{iso}	Buried oxide depth above PTS	4

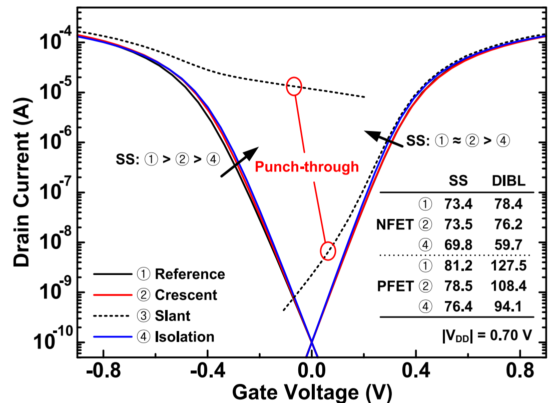

FIGURE 3. Transfer characteristics of 5-nm node NSFETs with four different structures. SS and DIBL are also summarized.

III. RESULTS AND DISCUSSION

Fig. 3 shows the transfer characteristics of the 5-nm node NSFETs having four different structures at the operation voltage (V_{DD}) of 0.7 V. Off-state currents (I_{off}) were fixed to 0.1 nA for standard performance (SP) applications. Slanted S/D NSFETs have high leakage currents due to the punch-through effects at the bottom transistors. Except (3), as the NSFET structure changes from (1) to (4) as shown in Fig. 1, subthreshold swing (SS) and drain-induced barrier lowering (DIBL) are improved. Crescent IS structure increases outer-fringing field at the S/D extension and lengthens the effective gate length (L_{eff}), which is a similar effect as the high-k spacer devices [12]. Slanted S/D structure with bottom isolation (=isolated S/D) increases the L_g of the bottom NS channel and reduces SS and DIBL under the same footprint. Thus, these unintended structural modifications are helpful to improve the SCEs in the 5-nm node.

Fig. 4 shows on-state currents (I_{on}) and stresses along the channel direction (S_{ZZ}). I_{on} and C_{gg} are extracted at the gate (V_{gs}) and drain (V_{ds}) voltages of V_{DD}, and RC delay is calculated as $C_{gg}V_{DD}/I_{on}$. Crescent IS NFETs have smaller I_{on} than do the reference devices, whereas the PFETs are the opposite. Crescent IS NFETs do not improve the

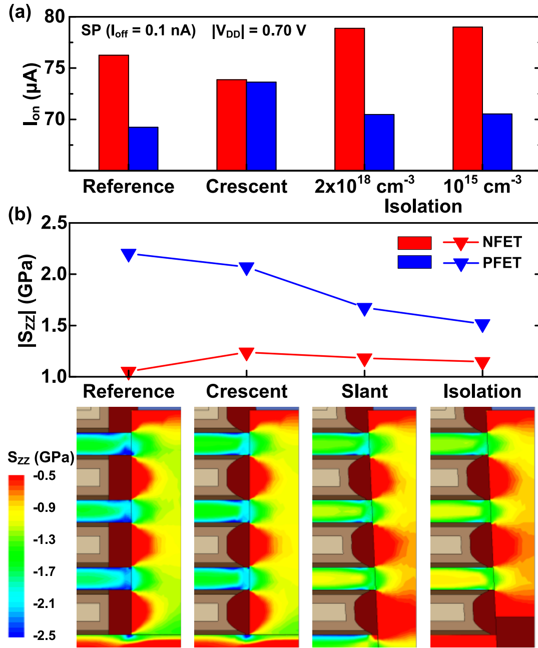

FIGURE 4. (a) On-state currents (I_{on}) for SP applications and (b) stresses along the channel direction (S_{ZZ}) of the NSFETs.

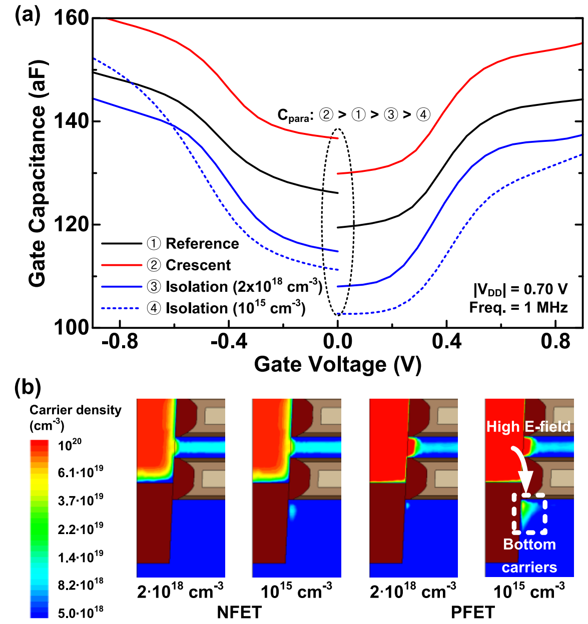

FIGURE 5. (a) Gate capacitances of the NSFETs at 1 MHz and (b) Carrier density of the isolated S/D NSFETs at on-state.

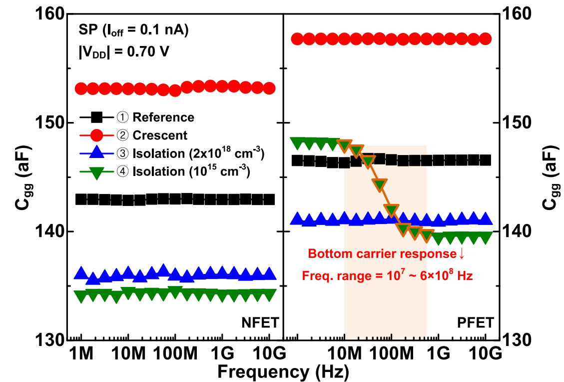

FIGURE 6. C_{gg} of the 5-nm node NSFETs at the frequency from 1 M to 10 GHz.

SCEs because of small S/D doping penetrations into the S/D extensions enough to maintain good SCEs even without crescent IS. On the other hand, the PFETs have larger S/D doping, which penetrates largely into the NS channels and degrades the SCEs. Thus, crescent IS PFETs improve the SCEs greatly, leading to the I_{on} increase.

Isolated S/D NSFETs improve the SCEs much by increasing the L_g, but the I_{on} values of P- and NFETs show different aspects. As the structure changes from the reference to isolated S/D, PFETs decrease the $|S_{ZZ}|$ greatly from 2.20 to 1.52 GPa. The bottom NS has elongated L_g as well as dwindled S/D epi, losing the $|S_{ZZ}|$ critically (Fig. 4b). Isolated S/D NFETs, however, have larger $|S_{ZZ}|$ than do the reference devices because the gate of crescent IS encircles NS channels greatly and increases the S_{ZZ} [10]. By means of improved SCEs and high S_{ZZ}, the NFETs have larger I_{on}. Interestingly, isolated S/D NSFETs with the punch-through stopper (PTS) doping of 2×10^{18} and 10^{15} cm^{-3} have the same I_{on}.

Fig. 5a shows the gate capacitances of reference, crescent IS, and isolated S/D NSFETs at the frequency of 1 MHz. Crescent IS NSFETs increase the C_{para} due to greater outer-fringing field [13], but isolated S/D devices reduce the C_{para} by separating S/D epi from the bottom. Lower PTS doping reduces the C_{para} much, but increases the C_{gg} at high V_{gs} especially for PFETs.

This C_{gg} increase is understood by carrier density profile at on-state in Fig. 5b. The 1-MHz frequency is large enough for minority carriers to follow the response by the V_{gs}. The electron (hole) lifetimes are 9.00 (2.73) μs and 55.6 (17.5) ns at the PTS doping of 10^{15} and 2×10^{18} cm^{-3}, respectively. Carriers are not generated at the bottom transistor having larger threshold voltage than do the NS channels. Instead, the carriers are generated at the bottom corner by high electric field from the S/D epi. As the electric field becomes larger by higher S/D doping or/and lower PTS doping, more carriers are generated and thus larger C_{gg} is obtained.

Although the PFETs with the PTS doping of 10^{15} cm^{-3} have high C_{gg}, substantial decrease of C_{gg} at high frequency alleviates this concern (Fig. 6). The frequency that the holes can not follow the V_{gs} response is about 600 MHz, which is slower than the operation speed of CMOS inverter and SRAM [14]. Therefore, the isolated S/D NSFETs with undoped PTS are advantageous not only to decrease the C_{gg} but also to do the reliable process by eliminating PTS doping process.

Fig. 7 summarizes RC delay of all the NSFETs. Crescent IS NSFETs have larger C_{gg} than any other structures and degrade the RC delay in spite of the improved SCEs. Although bottom isolation decreases the $|S_{ZZ}|$ greatly, better SCEs and smaller C_{gg} reduce the RC delay of both P- and NFETs for all the applications.

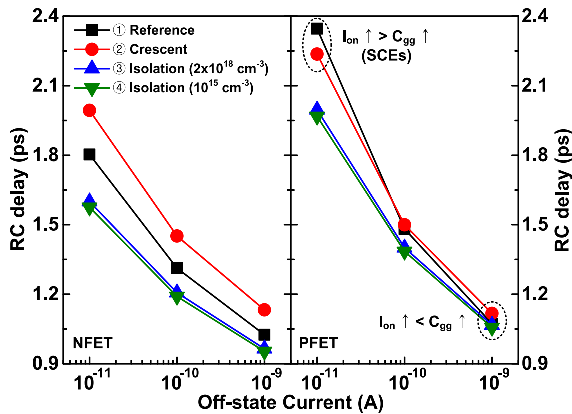

FIGURE 7. RC delay of the 5-nm node NSFETs for LP (I_{off} = 10 pA), SP (I_{off} = 0.1 nA), and HP (I_{off} = 1 nA) applications.

IV. CONCLUSION

Structural effects of 5-nm node NSFETs were analyzed thoroughly using fully-calibrated TCAD simulations. Crescent IS structure decreases SS and DIBL, but also increases the C_{para} by greater outer-fringing field. Slanted S/D structure with bottom isolation increases the L_g of the bottom NS channel, which improves the SCEs further and thus RC delay in spite of $|S_{ZZ}|$ reduction for PFETs within the same footprint. Also, lower PTS doping decreases the C_{para} and C_{gg} at normal CMOS operating frequency greater than 600 MHz. Thus, the unintended structural modifications achieve the decent DC/AC performance and the PTS-free process that prevents the NS surface damage, decreases the fabrication cost, and avoids the variability concerns by PTS.

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JUN-SIK YOON (S'14–M'16) received the B.S. degree in electrical engineering and the Ph.D. degree in creative IT engineering from the Pohang University of Science and Technology (POSTECH), South Korea, in 2012 and 2016, respectively.

He was a Postdoctoral Researcher with the Future IT Innovation Laboratory, POSTECH, from 2016 to 2017, where he has been a Postdoctoral Research Fellow with the Information Research Laboratories (PIRL), since 2018. His research interests include characterization and simulation of advanced nanoscale devices (fin, gate-all-around, tunneling, and nanosheet field-effect transistors (FETs)) and applications (chemical sensor and solar cell).

JINSU JEONG received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), South Korea, in 2017, where he is currently pursuing the M.S. degree in electrical engineering.

His research interests include characterization and simulation of multi-gate field-effect transistors (FETs) (fin FET (FinFETs), nanowire FETs, and nanosheet FETs) and 3-D-stacked CMOS using TSV.

SEUNGHWAN LEE received the B.S. degree in electrical engineering from the Pohang University of Science and Technology (POSTECH), South Korea, in 2018, where he is currently pursuing the M.S. degree in electrical engineering.

His research interests include characterization and compact modeling of multi-gate field-effect transistors (FETs) (fin FETs (FinFETs), nanowire FETs, and nanosheet FETs).

ROCK-HYUN BAEK (S'08–M'11) received the B.S. degree in electrical engineering from Korea University, in 2004, and the M.S. and Ph.D. degrees in electrical engineering from the Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2006 and 2011, respectively.

He was a Postdoctoral Researcher and a Technical Engineer with SEMATECH, Albany, NY, from 2011 to 2015. He was a Senior Device Engineer with the Pathfinding Team, SAMSUNG R&D Center, South Korea, from 2015 to 2017. Since 2017, he has been an Assistant Professor of electrical engineering with POSTECH. His research interests include technology benchmark by characterization, simulation, and modeling of advanced devices and materials (fin, gate-all-around, nanosheet FETs, 3-D-NAND, 3-DIC, SiGe, Ge, and III–V).