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A 24/77 GHz Dual-Band Receiver for Automotive Radar Applications

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ABSTRACT A fully-integrated 24/77 GHz dual-band receiver is presented for automotive radar applications. The proposed receiver consists of a dual-band LNA, a dual-band sub-sampling PLL, and a wideband mixer, operating at 24 and 77 GHz alternatively. Implemented in 65 nm CMOS technology, the receiver achieves 760 and 1800 MHz bandwidth with 52 and 60 mW power consumption in 24 and 77 GHz operation modes, respectively. To the best of authors' knowledge, this is the first fully-integrated CMOS 24/77 GHz dual-band receiver for automotive radar applications.

INDEX TERMS Dual-band, automotive radar, millimeter-wave (mm-wave), integrated circuit (IC), low power, CMOS receiver, sub-sampling, phase-locked loop (PLL),frequency modulated continuous wave (FMCW).

I. INTRODUCTION

Due to the rapid development of CMOS deep-submicron technology, the maximum frequency of current gain f_T and the maximum frequency of power gain f_{max} of CMOS transistors continue to rise, making millimeter-wave (mm-wave) circuits implemented in CMOS technology become a reality. Low cost CMOS mm-wave circuit design is a hot topic in recent years. The applications of mm-wave integrated circuit (IC) include mm-wave active and passive imaging, high data rate communication, and radar, etc. Radar can be used for motion detection, positioning, localization, and imaging applications [1]–[3]. The mm-wave automotive radar is a key technique of the advanced driver assistance systems (ADAS) [4]. An automotive radar operating at both 24 and 77 GHz frequencies helps the driver in terms of safety, convenience, and conform. The low frequency band (24.0-24.25 GHz) radar is usually for short range radar (SRR) applications such as blind-spot detection and collision avoidance [5]–[7]. The high frequency band (76-77 GHz) radar has wider bandwidth, and has been dedicated to long range radar (LRR) applications such as adaptive cruise control (ACC) [5]–[7]. Therefore, an automotive radar that supports both 24 and 77 GHz bands is desired in order to provide a complete solution for both SRR and LRR applications with low cost and compact area [8]–[10].

In recent years, some 24 or 77 GHz band receivers implemented in CMOS technology have been reported. Reference [11] presented a 24 GHz RF front-end including an LNA and a down-conversion mixer. Reference [12] demonstrated the fully-integrated 77 GHz CMOS transceivers for automotive radar applications. In 2009, [8] reported a 24/77 GHz dual-band pulse-based transceiver in BiCMOS technology to achieve low cost, low power, and compact integration. The 24/77 GHz dual-band transceiver implemented in CMOS technology reduces the power consumption and the cost for mass production especially when we integrate the digital circuit together. However, there are some challenges in the

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design of high performance mm-wave circuits in CMOS technology. For example, the low quality factor on-chip inductor and the high flicker noise transistor make the oscillator's phase noise poor, so the signal to noise ratio (SNR) of the demodulated signal becomes worse. Therefore, the proper system architecture and block topologies should be chosen in order to achieve the integration with reasonable performance. However, there is no CMOS 24/77 GHz dual-band frequency modulated continuous wave (FMCW) radar for automotive applications.

In this paper, a low power 24/77 GHz dual-band FMCW receiver is demonstrated in 65 nm CMOS technology. The proposed receiver works at 24 GHz or 77 GHz band alternatively. To the best of authors' knowledge, this is the first fully-integrated CMOS 24/77 GHz dual-band receiver for automotive radar applications. This paper is organized as follows. Section II introduces radar system design consideration. Section III presents the architecture and circuit design of the proposed receiver. In Section IV, the measurement results are shown. Finally, the conclusion is summarized in Section IV.

II. FMCW RADAR SYSTEM DESIGN CONSIDERATION

Due to the relative higher maximum equivalent isotropically radiated power (EIRP) allowed in the standard and the relative narrower bandwidth requirement, compared with the pulse radar, the CMOS FMCW radar is more attractive for 24 GHz SRR and 77 GHz LRR applications respectively [6].

In a conventional FMCW radar [5], the range is $R = cf_b/(2K)$, where c is the speed of light, f_b is the demodulated beat frequency, and K is the ramp slope of the chirp signal. The longer range requires the smaller K for a certain beat frequency f_b. A tunable K provides maximum detectable range. The range resolution is $\Delta R = c/(2BW)$, where BW is the modulation bandwidth. The range resolution is only determined by the modulation bandwidth. For a decent 0.1 meter range resolution, at least 1.5 GHz bandwidth is required. The speed resolution is $\Delta V = c/(2f_cT_m)$, where f_c is the carrier frequency, and T_m is the modulation period. The speed resolution is inversely proportional to the carrier frequency f_c and modulation period T_m. So the 77 GHz radar has better speed resolution, and it can achieve a reasonable 0.1 m/s resolution when $T_m = 20$ ms. The modulation bandwidth BW and modulation period T_m determine the slope K, which affects the beat frequency: $f_b = 2R \cdot BW/(cT_m)$. If the object is 100 meters away from the radar, the beat frequency is about 50 kHz when $BW = 1.5$ GHz, $T_m = 20$ ms. At such low frequency, flicker noise is very serious, making the noise figure of low noise amplifier (LNA) and the phase noise of local oscillator (LO) signal at low offset frequencies become very critical parameters for an RF front end [13].

To generate the mm-wave FMCW signal, typically there are two methods: the fractional-N phase-locked loop (PLL) and the direct digital frequency synthesizer (DDFS) followed by an integer-N PLL or a frequency multiplier chain. The fractional-N PLL solution has lower power consumption and cost, and it becomes more and more popular especially when the new techniques such as digital PLL and two-point modulation were employed to improve the phase noise and linearity [14], [15]. However, its settling time, which is limited by the PLL loop bandwidth, is in the level of microsecond. In contrast, the DDFS solution has merits of better phase noise and more flexible chirp signal period configuration (i.e. both fast chirp and slow chirp) which makes it suitable for the proposed dual-band radar [16]. Usually the phase noise of DDFS solution is determined by the DDFS, or more specifically its high speed reference clock, as long as the loop bandwidth of the integer-N PLL or the locking range of the multipliers is wide enough. The settling time of DDFS is in the level of nanosecond [17], which means the chirp signal period can be ultrashort. Moreover, since the DDFS is essentially a high speed DAC, other special modulations such as the coherent chirp sequence waveform [18] can be performed readily. DDFS followed by an integer-N PLL is preferred at mm-wave frequency compared with that followed by a frequency multiplier chain, because the locking range of a long frequency multiplier chain is narrow. Therefore, the integer-N PLL is integrated in the receiver and the external DDFS is used in the measurement.

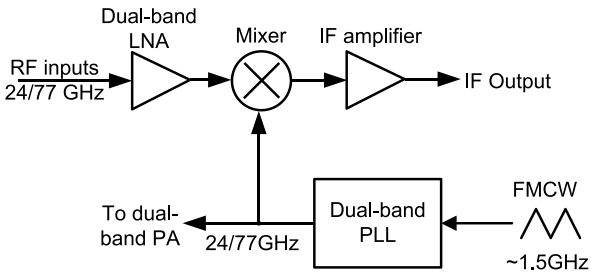


FIGURE 1. Schematic of the proposed dual-band receiver.

III. RECEIVER ARCHITECTURE AND CIRCUIT DESIGN

The proposed receiver consists of a dual-band sub-sampling phase-locked loop (SSPLL) [19], [20], a dual-band LNA [21], a wideband down-conversion mixer [22], and an intermediate frequency (IF) amplifier, as shown in Fig. 1. The dual-band LNA amplifies the 24 or 77 GHz RF signal alternatively. The dual-band SSPLL provides 24 or 77 GHz low phase noise LO signal for both mixer and power amplifier (PA). The wideband down-conversion mixer converts the RF signal to the IF signal which is amplified subsequently by the IF amplifier.

Both the range resolution and the maximum speed of the detected object can be improved by using a larger bandwidth BW in the FMCW radar. In our work, a bandwidth of 760 and 1800 MHz has been demonstrated in 24 and 77 GHz modes, respectively. The external FMCW reference is multiplied by the PLL to generate the 24 or 77 GHz LO signal. The integer-N SSPLL is the best choice to achieve a low in-band phase noise with low power consumption, since its divider noise is eliminated and its PFD and charge pump noise are not multiplied by N^2 [19]. The PLL loop bandwidth

is set to be high enough in order to compatible with both fast chirp and slow chirp inputs.

Fig. 2 shows the schematic of the dual-band SSPLL. A low power dual-band voltage-controlled oscillator (VCO) adopts a passive fourth-order *LC* tank. An injection-locked oscillator (ILO) can work as a buffer in 24 GHz mode or a divide-by-3 divider in 77 GHz mode through slightly tuning its free running frequency. The sub-sampling phase detector is basically a pair of passive NMOS switch with capacitor loads. The reference clock samples the high speed sinusoidal signal from ILO, and the phase difference between them is converted into the voltage difference for the subsequence the transconductance charge pump (TIA-CP) [19]. The pulse generator can control the gain of TIA-CP so as to adjust the loop gain of the PLL. A second order passive *RC* low-pass filter (LPF) converts the current difference into the voltage difference, i.e. the control voltage of VCO. In 24 GHz mode, the proposed SSPLL achieves low in-band phase noise by removing the divider and suppressing the phase noise from the sub-sampling phase detector and the TIA-CP due to the high loop gain. In 77 GHz mode, the situation is similar to that in 24 GHz mode, and the noise contributed by the ILO divider is negligible.

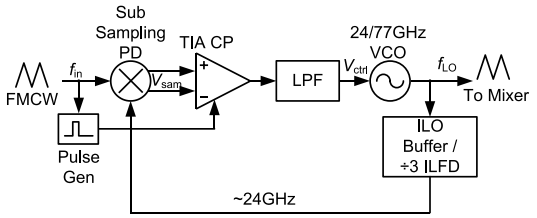
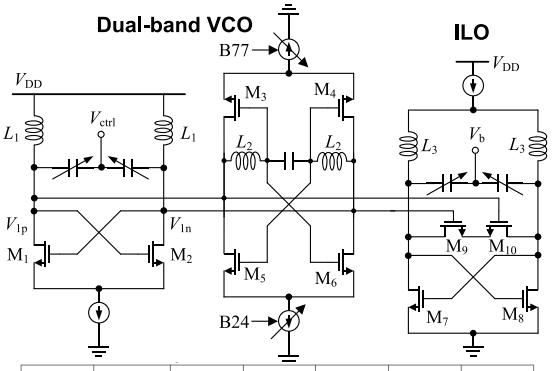


FIGURE 2. Schematic of the dual-band PLL.



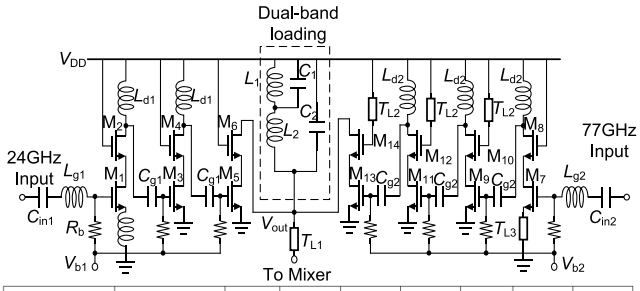
M1,2	M3,4,5,6	M7,8	M9,10	L1	L2	L3
30um	15um	20um	12um	450pH	110pH	184pH

All L=0.06um.

FIGURE 3. Schematic of the dual-band VCO and ILO.

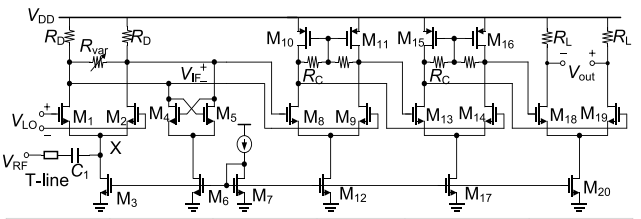
Fig. 3 shows the schematic of the dual-band VCO and ILO. The VCO consists of a fourth-order *LC* tank, a cross-coupled pair, two NMOS amplifier pairs (M3/M4 and M5/M6) for the operation mode switching. By setting only one control signal (B24 or B77) to be active, we can change the phase of the second resonant peak, so as to change the oscillation frequency [23]. The ILO is an *LC* oscillator with a floating-source differential pair as injection devices [24]. When B77 is active, the ILO works as a divide-by-3 injection-locked frequency divider. When B24 is active, the ILO works as an injection-locked buffer. Its free running frequency should be tuned slightly in order to align different input frequencies.

The dual-band LNA consists of a 24 GHz three stages LNA, a 77 GHz four stages LNA, and a shared dual-band loading network at the output, as shown in Fig. 4. Similar to the dual-band VCO, the dual-band loading network is equivalent to a fourth-order impedance peaking at both 24 and 77 GHz [23]. It matches both outputs of 24 and 77 GHz LNAs to the input impedance of mixer through a long transmission line. The LNAs are properly designed so that they can achieve both power matching and noise matching simultaneously across wide frequency ranges by using the source inductive degeneration at the first stage [25]. The biasing voltages V_{b1} or V_{b2} is applied alternatively to get the optimum current density for low power and low noise figure (NF), and the other biasing voltage is set to ground to turn off another LNA.



M1,2	M3-14	Rb	Lg1	Ld1	Lg2	Ld2	L1	L2
32um/0.06um	16um/0.06um	18kΩ	870pH	533pH	265pH	93pH	230pH	128pH
TL1	TL2	TL3	Cin1	Cg1	Cin2	Cg2	C1	C2
490um	180um	20um	924fF	1.4pF	62fF	62fF	117fF	24fF

FIGURE 4. Schematic of the dual-band LNA.



M1,2	M3,6	M4,5	M7	M8,9,13,14,18,19	M10,11,15,16
10um/0.06um	80um/0.2um	12um/0.06um	8um/0.2um	24um/0.06um	162um/0.2um
M12,M17	M20	RD	RC	RL	C1
160um/0.2um	320um/0.2um	4.4kΩ	18kΩ	150Ω	470fF

FIGURE 5. Schematic of the wideband mixer and IF amplifier.

Since the IF frequency is far away from the LO frequency in the FMCW transceiver, the single-balance down-conversion mixer is used to reduce the NF and power consumption, as shown in Fig. 5. Compared with the conventional mixer, this mixer has higher conversion gain at mm-wave frequency since the transmission line can tune out the parasitic capacitance at node X [26]. The cross-coupled

pair (M4 and M5) is used to provide a negative resistance that can compensate the loss between the differential output nodes, so the gain of mixer is improved without increasing much DC power. A variable resistor R_{var} is employed to tune the gain without affecting the output DC. So the viable gain amplifier can be eliminated. The IF amplifier is three-stage differential amplifiers with resistor common mode feedbacks. The last stage is matched to 50 Ohm for measurement.

IV. MEASUREMENT RESULTS

The proposed dual-band receiver is implemented in a bulk 65 nm CMOS technology. The die photograph of the receiver is shown in Fig. 6. Including pads the area of the whole receiver is 1620 μm $\times$ 770 μm. The receiver is measured in 24 or 77 GHz mode alternatively. The power consumption of the whole receiver is 52 and 60 mW for 24 and 77 GHz modes, respectively.

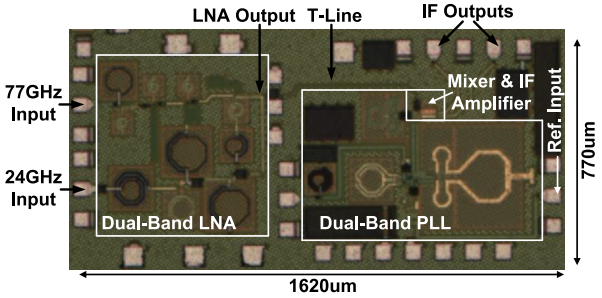


FIGURE 6. Die photograph of the proposed dual-band receiver.

Fig. 7 illustrates the PLL's output spread spectrums in both 24 and 77 GHz modes when the reference input is the FMCW signal from a signal generator. The measured operation range of the dual-band SSPLL is 24 $\sim$ 24.7 and 75 $\sim$ 76.8 GHz. So there are about 760 and 1800 MHz modulation bandwidth for 24 and 77 GHz modes when the input reference bandwidth is 47.5 and 37.5 MHz at around 1.5 GHz, respectively. The latter is corresponding to a theoretical range resolution of 8.3 cm according to equation (2), which is fine enough for most of automotive radar applications. The phase noise of single tone signal is measured by a signal source analyzer. At 1 MHz offset frequency, the phase noise is -120 and -108.5 dBc/Hz in 24 and 77 GHz modes respectively. The in-band phase noise is -103 and -94 dBc/Hz in 24 and 77 GHz modes respectively. The excellent phase noise contributes negligible SNR degradation to the beat signal.

To measure the frequency error of the FMCW output, the high frequency signal is down-converted to the low frequency through an external passive mixer. The output is recorded by a high speed digital oscilloscope and processed by Matlab. Fig. 8 shows the instantaneous frequency of the down-converted output signal. The input chirp signal is sawtooth with idle period, and the bandwidth of chirp is limited by the equipment. In the ramp up period, the linearity is mainly determined by the input source as long as the PLL's bandwidth is wide enough.

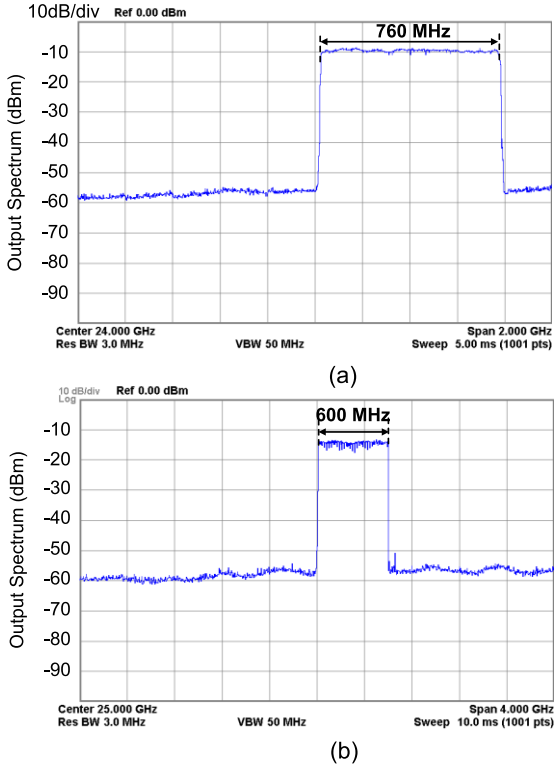


FIGURE 7. Measured output spread spectrums under frequency modulation in (a) 24 and (b) 77 GHz (divide-by-3) modes.

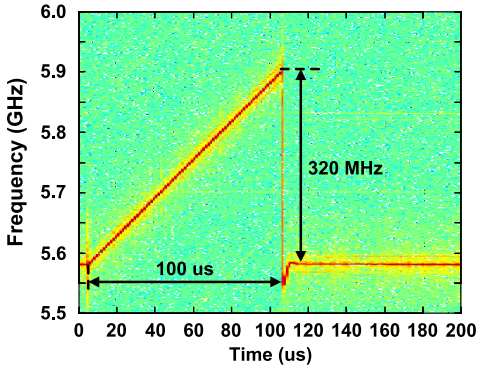


FIGURE 8. Measured instantaneous frequency of the down-converted output signal in 77 GHz mode (divide-by-3).

Fig. 9 shows the measured output frequencies and frequency errors when the modulation period T_m is 10 μs, 100 μs, and 1000 μs in both 24 and 77 GHz modes respectively. The frequency errors of fast chirp modulations are larger compared with the slow chirp ones. In 24 GHz mode, the frequency errors are within 0.7 MHz and the RMS values are within 152 kHz. In 77 GHz mode, the frequency errors are within 0.7 MHz and the RMS values are within 473 kHz. Therefore, the proposed dual-band PLL has good linearity for both fast chirp and slow chirp modulations in both 24 and 77 GHz modes.

The receiver is measured with an mm-wave vector network analyzer. The return loss of the receiver in 24 and 77 GHz

TABLE 1. Comparison of state-of-the-art receivers with frequency synthesizer for automotive radar applications.

Reference	Technology	Supply Voltage (V)	Operation Frequency (GHz)	Phase Noise (dBc/Hz) @ 1 MHz	Conversion Gain (dB)	Noise Figure (dB)	Power Consumption (mW)	Chip Area (mm^2)
[8]	0.18μm BiCMOS	1.8/2.5	22~29	-114	35	4.5	197.5	3.6*
			76~81	-103.5	31	8	282.5	
[17]	90nm CMOS	1.2	78.1~78.8	-85	23.1	15.6	212	4.7*
[5]	65nm CMOS	1.2	75.6~76.3	-85.33	38.7	30	128	0.95*
[27]	65nm CMOS	1.5	75~80	External LO	16	10.5	37.5~57	0.58
[28]	28nm CMOS	N.A.	78~87	-85	45	12	420**	7.9**
[29]	0.13μm BiCMOS	2	77~81	N/A	22.5	18	1000~1200***	31.9***
This Work	65nm CMOS	1.3	24~24.7	-120	36~37	16~16.5	52	1.25
			75~76.8	-108.5	20~24	23~23.5	60	

* Estimated from die photos. ** 2×2 Transceiver. ***16-element phased-array receiver.

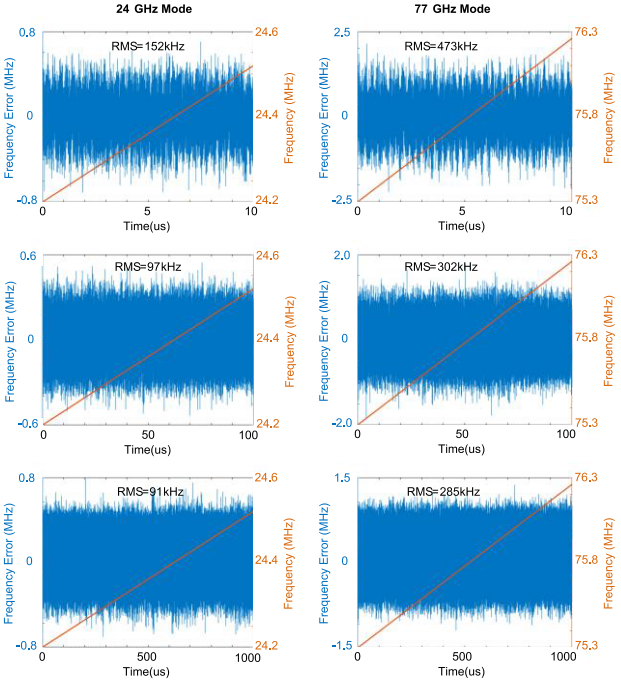


FIGURE 9. Measured output frequencies and frequency errors with 10 μs, 100 μs, and 1000 μs modulation period in both 24 and 77 GHz modes.

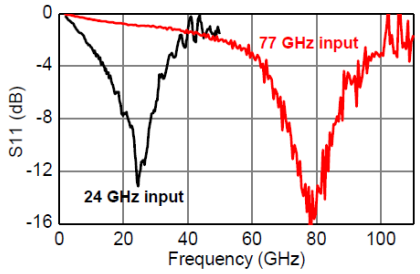


FIGURE 10. Measured return loss of the dual-band receiver in 24 and 77 input ports.

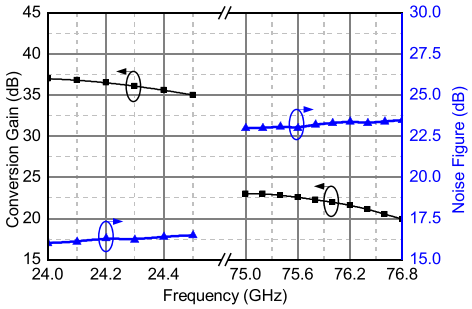


FIGURE 11. Measured conversion gain and noise figure of the dual-band receiver.

input ports are shown in Fig. 10. The conversion gain and the NF of receiver are measured by using the gain method. Single tone signals are fed into the 24 and 77 GHz RF input ports respectively. Fig. 11 shows the measured conversion gain and NF. In 24 GHz mode, the conversion gain of the receiver is 35 $\sim$ 37 dB, and the NF is 16 $\sim$ 16.5 dB. In 77 GHz mode, the conversion gain of the receiver is 20 $\sim$ 24 dB, and the NF is 23 $\sim$ 23.5 dB. The measured performance of the proposed dual-band receiver is summarized and compared with other receivers for automotive radar applications as shown in Table 1.

V. CONCUSION

In conclusion, we firstly proposed and demonstrated a low power 24/77 GHz dual-band receiver in 65 nm CMOS technology. The measured bandwidth of receiver with on-chip LO is 760 and 1800 MHz in 24 and 77 GHz modes respectively. The measured conversion gain is 35 $\sim$ 37 dB and 20 $\sim$ 24 dB, and the measured NF is 16 $\sim$ 16.5 and 23 $\sim$ 23.5 dB, both in 24 and 77 GHz respectively. The proposed work is suitable for both short range and long range automotive radar applications.

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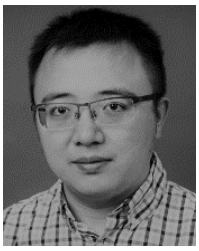

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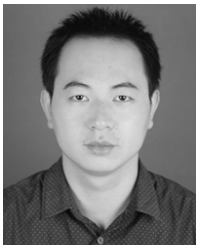

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