Design and Analysis of 0.5-f_T Bandwidth THAs With Resolution Enhancement Techniques in 0.18-μm SiGe Process

YU-AN LIN, (Student Member, IEEE), GUAN-LIN HUANG, YA-CHE YEH, AND HONG-YEH CHANG, (Member, IEEE)

Department of Electrical Engineering, National Central University, Taoyuan 32001, Taiwan

Corresponding author: Hong-Yeh Chang (hychang@ee.ncu.edu.tw)

ABSTRACT This paper presents the design and analysis of microwave and millimeter-wave (MMW) high-linear track-and-hold amplifiers (THAs) for high-speed data conversion systems. The silicon germanium (SiGe) process utilized in the proposed circuits is analyzed in detail and its several merits are demonstrated, including operating speed, linearity, and resolution. Bandwidth extension techniques, such as peaking, Darlington, and distributed topologies, are adopted to further enhance the operating speed of the proposed THAs up to a 0.5-unity current gain frequency (f_T) of the transistor. The switched emitter-follower (SEF) as well as the switched capacitor (SC) track-and-hold (T/H) stages are modified using pedestal error reduction techniques, including a cascode stage and differential cancellation, to further enhance the overall resolution of the THAs. The proposed cascoded SEF-based T/H circuit with a modified Darlington-based input buffer has a track-mode bandwidth of up to 0.5-f_T, a maximum spurious-free dynamic range (SFDR) of 45.1 dBc, and dc power consumption of 94.3 mW. Moreover, the proposed differential cancellation SC-based T/H circuit with an input buffer based on the distributed bandwidth extension technique exhibits an operating speed of up to 0.32-f_T, an SFDR of 47.9 dBc, and dc power consumption of 180.1 mW. Both proposed THAs are suitable for low-power, high-speed MMW conversion systems without incurring a high cost. Moreover, by using the proposed design methodology, a sampling rate up to tens of gigahertz can be easily achieved with time-interleaved architecture.

INDEX TERMS CMOS/SiGe RFIC, microwave integrated circuits (ICs), mixed signal design, high-speed analog IC design, sampling circuits.

I. INTRODUCTION

Due to the tremendous data transmission demands of modern globalized society, next-generation communication systems must be designed that use up to microwave and millimeter-wave (MMW) bands to mitigate modern crowded data traffic. Because of the development of big data in modern information calculation systems, the conversion speed between continuous and discrete signals must be increased considerably to support high-speed supercomputer signal processing. High-resolution analog-to-digital convertors (ADCs) should be designed up to the MMW band to support high-speed data transmission and high-accuracy signal

processing. Successive approximation register (SAR) [1]–[3] and pipeline [4]–[6] ADCs are appropriate candidates for high-resolution calculations of 10–14 bits. However, their sampling speed is restricted because they use digital-to-analog convertors, which are difficult to design up to the MMW band. The flash ADC architecture, which consists of a track-and-hold amplifier (THA), preamplifier, multiple comparators, and a thermometer-to-binary (T2B) convertor, is thus more suitable for an MMW data conversion system in spite of its low resolution [7]–[9]. The sampling speed can currently be up to 10 GS/s or even 24 GS/s [7] because of advanced processes. To mitigate the low resolution of flash ADCs, bubble mitigation techniques, such as bubble error correction circuits [10], bubble tolerant
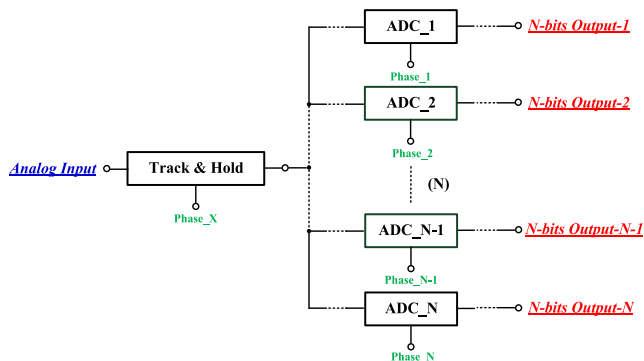
FIGURE 1. Block diagram of the modified time-interleaved ADC with distortion degradation technique.

encoders [11], and fat tree encoders [12], have been proposed. However, the high complexity of the circuit entails complicated layout considerations and costs resulting from high occupation of the circuit area. The operating speed of a T2B convertor also degrades the sampling rate because of its digital circuit block. To further enhance the sampling rate, a time-interleave architecture, which utilizes multiple phases of a sampling clock, has been proposed [13]–[15]. However, the phase noise and phase error of the clock signal substantially affect the accuracy of the ADC. Therefore, to reduce the cost of high scale integration and enhance both the operating speed and resolution, a high-speed, high-linearity, and high-resolution THA must be used to drive several time-interleaving sub-ADCs as shown in Fig. 1.

High-speed and high-dynamic-range THAs have been widely investigated in recent years. THAs have been designed using advanced processes, including the complementary metal oxide semiconductor (CMOS), silicon-on-insulator (SOI) CMOS, silicon germanium (SiGe), indium phosphide (InP), and InP-on-CMOS processes. In 2010, THA sampling speeds of up to 40 GS/s were obtained using a 210 GHz unity current gain frequency (f_T) transistor [16]–[19]. In 2011, a SiGe-based THA had much lower DC power consumption with a total harmonic distortion (THD) of up to −50 dBc [20]. THAs designed in articles published in 2012 [21]–[24] have an input track-mode bandwidth wider than 40 GHz, which is two to three times wider than that of previously reported THAs. In 2013, an advanced 28-nm CMOS process was used to mitigate low-pass response results caused by the parasitic capacitance of devices [25], and in 2014, THAs were widely investigated by using a time-interleaved architecture to enhance the sampling rate [26]–[28]. In 2015, 2016, and 2017, several different THA topologies were summarized and widely employed to simultaneously achieve high speed, high linearity, high resolution, and low DC power consumption [29]–[35]. Although operating speeds of up to 40-GS/s sampling rate [19] and 40-GHz bandwidth [21] are attainable, the cost of the circuits is much higher because of the more advanced process used. Moreover, the operating speed of samplers is still restricted by the unity current gain frequency (f_T) of the device.

Based on the design concept of bandwidth extension technique, we have successfully developed a 27-GHz bandwidth THA in [36] using 0.18-μm SiGe process to significantly improve the operated speed limitation. In this paper, design and analysis of two THAs are presented with approximately 0.5-f_T track-mode bandwidth in the 0.18-μm SiGe process. The conventional switched emitter-follower (SEF) track-and-hold (T/H) stage was modified using a cascode stage to maintain the switching speed between track and hold plateaus. The conventional switched capacitor (SC) T/H stage, which suffers from a large pedestal voltage error, was modified using a resolution enhancement technique. In addition, a few bandwidth-extension techniques, including peaking, Darlington, and distributed techniques, were used to compensate for the low-pass response and insertion loss of the T/H stage. For the proposed THA with a T-coil peaking-based modified Darlington input buffer and cascoded high-linearity SEF T/H stage, the 3-dB bandwidth is wider than 0.5-f_T with a maximum spurious-free dynamic range (SFDR) of 45.1 dBc and a DC power consumption of 94.3 mW. For the proposed THA with a traveling-wave amplifier–based input buffer and cancellation-based SC T/H stage, the 3-dB bandwidth is wider than 0.32-f_T with a maximum SFDR of 47.9 dBc and a DC power consumption of 180.1 mW.

The remainder of this paper is organized as follows: Section II describes the merits of the SiGe process compared with the CMOS process. Section III presents the design methodology of the 0.5-f_T THA using the bandwidth extension techniques. The modified SC T/H circuit using the differential cancellation technique is investigated in Section IV. The circuit implementation of the two THAs is presented in Section V, including schematics and chip photographs. The experimental results and discussions are presented in Section VI, and concluding remarks are given in Section VII.

II. 180-NM SIGE PROCESS FOR THA DESIGN
The proposed THAs are designed using 0.18-μm SiGe process provided by the Taiwan Semiconductor Manufacturing Company (TSMC). The process offers six metal layers and one poly layer for the interconnection. Based on the large-signal model provided by TSMC, the heterojunction bipolar transistor (HBT) exhibits a maximum oscillation frequency (f_{max}) and a unity current gain frequency (f_T) of 100 GHz and 54 GHz, respectively. The n-channel metal oxide transistor (NMOS) exhibits f_{max} and f_T of up to 86 GHz and 54 GHz, respectively. Metal–insulator–metal capacitors, spiral inductors, and poly resistors are also available for the circuit design.

Compared to the CMOS process, a SiGe HBT offers the following advantages:

1) Benefiting from faster electron mobility in the heterojunction, SiGe-based devices have faster switching speeds and higher cutoff frequencies.
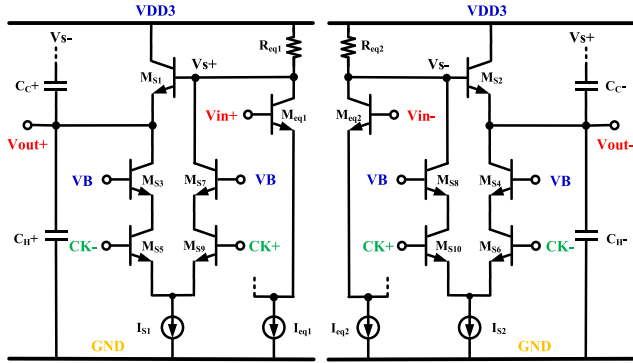2) Because of the semiconductor material employed, the breakdown voltage of the HBT is large and thus the

FIGURE 2. Schematic of the proposed cascoded SEF T/H stage using differential architecture and cancellation technique.

FIGURE 3. Nonlinear and ideal I–V curves obtained for the device.

HBT is highly capable of driving considerable output power.

3) The large concentration at the base of the HBT introduces a higher bias current, enhancing the operating speed of the circuit.

4) Because the HBT has a faster switching speed and higher $f_{\max}$, low distortion can easily be realized using the SiGe process.

5) The HBT produces less noise; therefore, the dynamic range of SiGe circuits is higher compared with that of CMOS circuits.

III. 27-GHZ BANDWIDTH THA

A. CASCODED SEF T/H STAGE

Fig. 2 is the schematic of the proposed cascoded SEF T/H stage. During the track phase with CK− in the high state, $M_{s3,5}$ and $M_{s4,6}$ steer the currents I_{s1} and I_{s2}, respectively. M_{s1} and M_{s2} serve as source followers tracking the input signal. During the hold phase with CK+ in the high state, $M_{s7,9}$ and $M_{s8,10}$ steer the current sources, and the equivalent resistors ($R_{eq1,2}$) of the input buffer acquire an extra voltage drop from $M_{s7,9}$ and $M_{s8,10}$ to turn off M_{s1} and M_{s2}, respectively. Compared with the SC T/H stage, which suffers from heavy dynamic nonlinearity, the SEF T/H stage features lower distortion resulting from different switching times during different sampling periods. Because the general emitter-follower characterizes almost unit gain, the input voltage swing of the T/H stage is approximately equal to the voltage swing at the output node. To switch from track plateaus to hold plateaus, the Vgs of $M_{1,2}$ should be lower than the threshold voltage. Because the amplitude of CK+ stays constant, the constant rise and sink current of $M_{9,10}$, which is dependent on the overdrive voltage (V_{ov}) of the transistor, introduces almost the same switching charging and discharging time during mode transition. As a result, the dynamic nonlinearity is successfully suppressed by the SEF T/H stage.

Although the proposed THA is designed using a low-distortion SiGe process, the base-emitter modulation of the source follower decreases the static linearity. The transistor size and the capacitance of the holding capacitor must
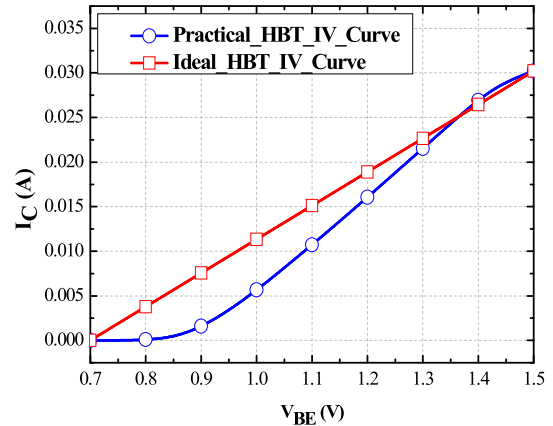
be selected appropriately. By using the Volterra operators, the second (HD_2) and third (HD_3) harmonic can be expressed as [31]

$$HD_2 = \frac{V_T \cdot A}{4} \cdot \left(\frac{2\pi \cdot f \cdot C_H}{I_{SEF}}\right)^2, \tag{1}$$

and

$$HD_3 = \frac{V_T \cdot A^2}{12} \cdot \left(\frac{2\pi \cdot f \cdot C_H}{I_{SEF}}\right)^3. \tag{2}$$

V_T represents the thermal voltage of the HBT, A is the amplitude of the input signal, f is the frequency of the input signal, C_H is the value of holding capacitor, and I_{SEF} is the DC bias current of the SEF-based T/H stage. Because HD_2 can be suppressed using the differential architecture, the HD_3 of the circuit is the most critical factor heavily affecting the static nonlinearity. On the basis of (2), a larger value of the input swing introduces higher distortion. Due to the tunable value of devices' transconductance, which is related to its DC bias condition, the I–V curve of the transistor is nonlinear, with the slope varying as shown in Fig. 3. The larger swing passes through larger nonlinear regions, contributing to heavier distortion. However, to enhance the HD_3, the DC bias current of the T/H stage, which is proportional to the transistor size, should be as large as possible on the basis of (2). As a result, the proposed T/H stage is designed using a 10-μm^2 emitter area HBT, the largest size that the process enables. Fig. 4 plots the simulated bandwidth and the HD_3 calculated using a Volterra operator with an input frequency of 5 GHz, an input amplitude of 0.3 V, a holding capacitance of 0.1 pF, and an emitter area swept from 2 to 10 μm^2. Despite the narrowest bandwidth of the T/H stage, which results from the largest transistor size, the linearity is the most concerning issue; the bandwidth can be compensated using an input buffer (discussed in Section III-B). In addition, to further reduce the static nonlinearity, the holding capacitance should be as small as possible on the basis of (2). Therefore, the input parasitic capacitor of the output buffer serves as a holding capacitor without the need to fabricate another holding capacitor. This not only enhances the linearity but also reduces
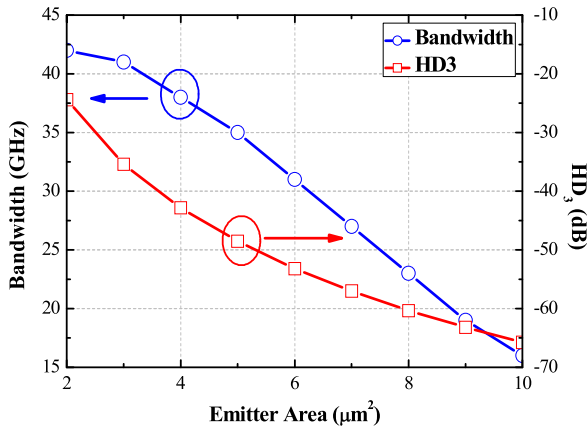
FIGURE 4. Simulated bandwidth and HD$_3$ calculated using the Volterra operator with an input frequency of 5 GHz, input amplitude of 0.3 V, a holding capacitance of 0.1 pF, and an emitter area swept from 2 to 10 μm^2.

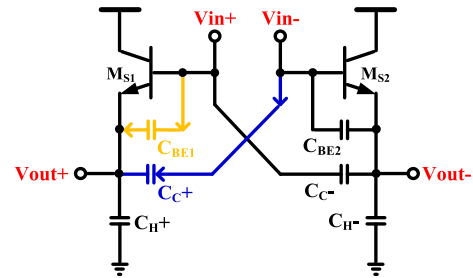**FIGURE 5.** Schematic of the differential cancellation technique used in the T/H stage of the proposed differential cascoded SEF.

the circuit area. Moreover, the differential architecture is utilized to reduce even-mode harmonic distortion, enhancing linearity.

The operating speed of the T/H stage, including track-mode bandwidth and the maximum sampling rate, also matters. According to [7], the relationship among track-mode bandwidth (f_{3dB}), sampling rate (f_S), and resolution (β) can be expressed as

$$f_{3dB} \geq \frac{f_s \cdot \ln(2^{\beta+1})}{\pi}. \quad (3)$$

The sampling rate of the T/H stage is related to the track-mode bandwidth. As a result, by leveraging the 3-dB bandwidth compensation by using the overshoot small-signal gain response of the input buffer, the sampling rate can also be enhanced. To further reduce the settling and acquisition times, the proposed SEF T/H stage is designed using the cascode stages ($M_{S3,7}$ and $M_{S4,8}$) as shown in Fig. 2. The cascoded SEF T/H stage demonstrates a smaller switching time as compared with the conventional topology [31].

On the basis of data conversion design in [37], the resolution of the T/H stage is influenced by operating speed and pedestal error. According to (3), the resolution can be improved by using the previously mentioned operating speed enhancement technique. To further increase the resolution, the pedestal error resulting from clock feedthrough, hold-mode feedthrough, and hold-mode leakage should be manipulated appropriately. Due to the parasitic capacitor between the base and collector (C_{BC}), the clock signal leaks to the holding capacitor through the C_{BC} of M_{s5} and M_{s6} ($C_{BC_S5,6}$) during mode transition, considerably affecting the quantized signal. The voltage error caused by the clock feedthrough without the cascode stage (ΔV_{CH1}) can be expressed as

$$\Delta V_{CH1} = (CK-) \times \frac{C_{BC_S5,6}}{C_{BC_S5,6} + C_H}. \quad (4)$$

To reduce the clock feedthrough effect, $C_{BC_S5,6}$ and the clock amplitude should be as small as possible. Whereas the larger holding capacitor contributes to a smaller clock feedthrough voltage error, the linearity is degraded on the basis of (2). However, according to previously reported THAs, the clock feedthrough voltage errors can serve as offset voltage [37], although the input-dependent parasitic capacitance generates variable offset voltage at different sampling times, introducing dynamic nonlinearity. Moreover, whereas the clock feedthrough effect can be mitigated using differential architecture, it is difficult to achieve high-accuracy cancellation because of the input-dependent parasitic capacitors. As Vin+ swings to the high state, Vin− swings in the opposite direction. On the basis of (4), the differential circuits generate different amounts of offset voltage because of the different values of the parasitic capacitors. Therefore, to mitigate the clock feedthrough, the more effective method is to reduce the parasitic effect. By adopting the cascode stages, (4) can be modified into

$$\Delta V_{CH2} = (CK-) \times \left(\frac{\frac{C_{CE_S3,4} \times C_{BC_S5,6}}{C_{CE_S3,4} + C_{BC_S5,6}}}{\frac{C_{CE_S3,4} \times C_{BC_S5,6}}{C_{CE_S3,4} + C_{BC_S5,6}} + C_H} \right) < \Delta V_{CH1}. \quad (5)$$

ΔV_{CH2} represents the voltage error resulting from the clock feedthrough with cascode stage consideration. $C_{CE_S3,4}$ symbolizes the parasitic capacitance of $M_{S3,4}$ across the collector and emitter. The offset voltage is decreased due to the series parasitic capacitors $M_{s5,6}$ and $M_{s3,4}$. In addition, the value of the equivalent parasitic capacitors is enclosed, mitigating heavy input-dependent parasitic variation. However, the differential cancellation capacitors C_C+ and C_C- are utilized to suppress the hold-mode feedthrough signals. To ensure good cancellation, the value of the cancellators should be equal that of the parasitic capacitor across the base-to-emitter of $M_{S1,2}$ as shown in Fig. 5. To mitigate the hold-mode leakage current, the following stage of the T/H stage is designed using the NMOS instead of the HBT. The HBT has a larger base leakage current than the gate leakage current of the NMOS. Thus, to realize a favorable droop rate, the output buffer must be designed using an NMOS. Moreover, the cascode stages enhance the dynamic range because the breakdown voltage of the system is increased as compared with the conventional emitter-follower design.
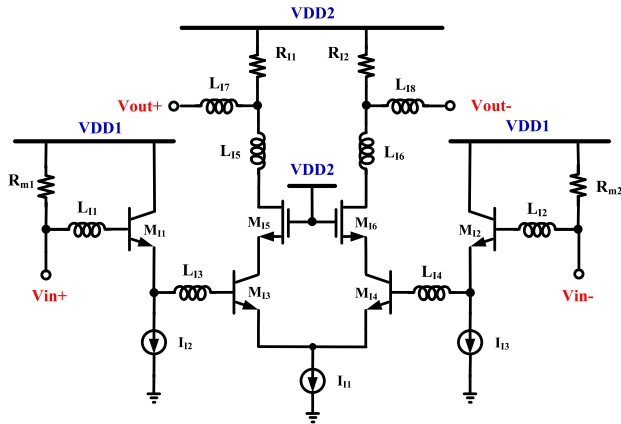
FIGURE 6. Schematic of the proposed Darlington-based input buffer modified by using input series inductors and an output T-coil peaking bandwidth extension technique.

B. MODIFIED DARLINGTON-BASED INPUT BUFFER

To enhance the operating speed of the THAs, the input buffer can be used to peak the roll-off of the T/H stage [38]. Fig. 6 is the schematic of the proposed input buffer. To widen the input bandwidth, the Darlington pair can be adopted for its input parasitic capacitance reduction and double current gain, but the output node is parallel with the two-stage parasitic capacitors. To further enhance the bandwidth, the parallel output of the Darlington pair can be separated to release a low-pass response. Moreover, the output is cascoded to further decrease the output parasitic capacitance due to the series capacitance reduction property. Although the current gain is decreased by separating the two stages, it is enough for the single-stage amplifier to compensate for the insertion loss of the T/H stage. In addition, several inductors (L_{I1-8}) are used to be series or shunt with parasitic capacitances to eliminate parasitic effects and enhance the overall bandwidth. The input inductors (L_{I1-4}) of two stages are used to mitigate the low-pass response at the input node. At the output port, the T-coil peaking network (L_{I5-8}) is utilized to peak the gain response. The simulated small-signal gain of the input buffer is illustrated in Fig. 7. The proposed input buffer demonstrated a DC gain of −2.5 dB and a maximum overshoot frequency of 24 GHz. Because the operating frequency is up to tens of GHz, the input matching circuit is designed using a simple shunt-matching resistance of 50 Ω (R_{m1-2}), which features broadband-matching bandwidth.

C. SOURCE-FOLLOWER-BASED OUTPUT BUFFER

Because of the lower leakage current of the NMOS compared with HBT devices, the output buffer of the proposed THA is designed using source-follower topology in Fig. 8. The source follower features broadband output matching by selecting the appropriate transistor size and dc bias condition. The output impedance of the source follower can be briefly expressed as

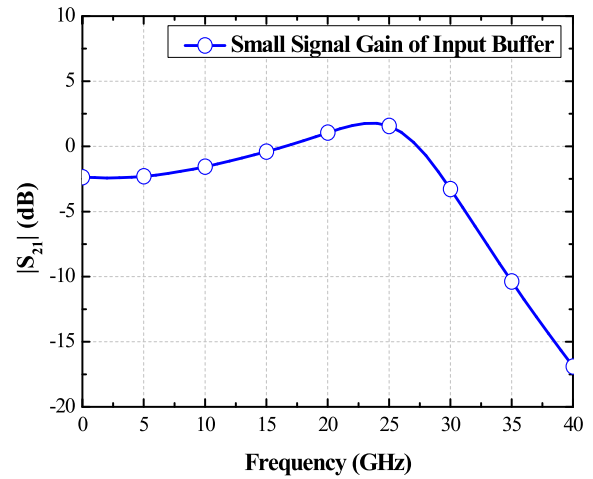$$Z_{OUT} = \frac{1}{gm}. \qquad (6)$$

FIGURE 7. Small-signal gain of the proposed modified Darlington-based input buffer when using input series inductors and an output T-coil peaking bandwidth extension technique.
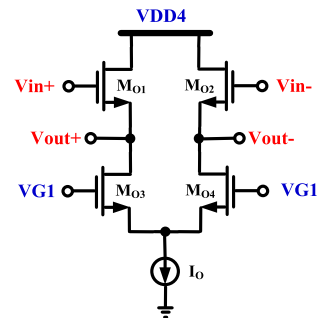

FIGURE 8. Schematic of the proposed differential source follower-based output buffer.

gm represents the transconductance of the device used in the output buffer. To ensure high linearity, the bandwidth consideration of the output buffer is also significant. The output waveform consists of the fundamental frequency with multiple specific harmonics because of the convolution of the sinusoidal and square signals at the output port of the T/H stage. The bandwidth of the output buffer also considerably influences the sampling rate. The simplified relationship between the bandwidth of the output buffer (f_{Output_Buffer}) and the required time duration (t_c) for the holding voltage approximating the deserving voltage can be expressed as [7]

$$t_c \geq \frac{1}{2\pi \cdot f_{OutputBuffer}} \cdot \ln(5 \cdot 2^B \cdot \frac{f_{in}}{f_{OutputBuffer}}), \qquad (7)$$

where f_{in} represents the input frequency. The small-signal gain of the output buffer is shown in Fig. 9. The proposed output buffer demonstrates a 3-dB bandwidth of 62 GHz and an insertion loss of 2 dB. Although the gain of the output buffer is low, the bandwidth of the output buffer is the most pressing issue because the bandwidth of the output buffer substantially affects the overall linearity. The insertion loss can be compensated using the appropriate topology for the input buffer.
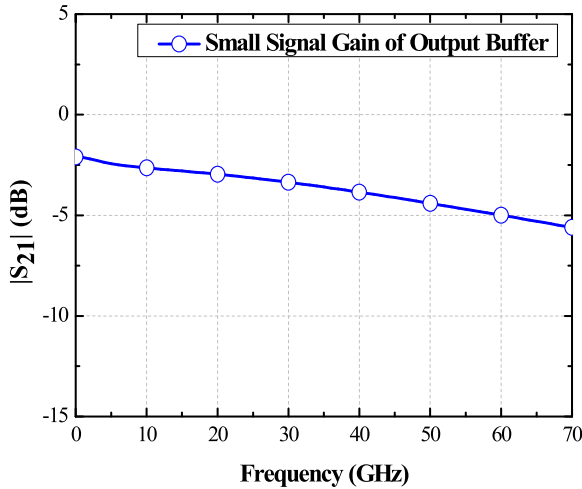
FIGURE 9. Small-signal gain of the proposed source follower-based output buffer.

FIGURE 10. Simulated 3-dB bandwidth and insertion loss of the PMOS SPST switch with a transistor width swept from 20 to 100 μm.

IV. 17-GHz BANDWIDTH THA

A. DIFFERENTIAL CANCELLATION-BASED T/H STAGE

The linearity of a THA is mainly dominated by the T/H stage, which contains a switch and a holding capacitor. Therefore, the topology of the T/H stage should be selected carefully to improve SFDR and the THD. The SC topology is the most basic topology, and it is generally composed of a single-pole single-throw (SPST) switch and a holding capacitor. During the track mode, the input signal passes through the switch and the holding capacitor is charged or discharged by the switch corresponding to the input signal. During the hold mode, the switch is turned off and the input signal is blocked; the holding capacitor maintains the voltage without charging and discharging. The main drawback of the SC topology is the considerable nonlinearity due to both device nonlinearity and the input-dependent timing jitter. If the SPST switch is designed based on a single transistor PMOS (or NMOS), the HD$_3$ can be expressed as [39]

$$HD_3 = \frac{\omega_0 \tau_0}{4} \left(\frac{A}{V_{DD} - V_{SQ} - V_T} \right)^2, \qquad (8)$$

where ω_o is the input angular frequency. τ_o is the transconductance delay of the transistor, which can be obtained based on circuit simulation; the track-mode bandwidth of the switch is $1/\tau_o$. In addition, A is the single-end input swing; V_T is the transistor threshold voltage, whose typical value is 0.3 V; and V_{SQ} is an appropriate DC value of the input signal. From (8), the HD$_3$ worsens as the amplitude of the input signal increases. This result agrees with the analysis presented in Section III. As a result, the turn-on voltage of the SPST switch should be biased as high as possible (but less than the breakdown voltage) to achieve high linearity.

The simulated 3-dB bandwidth and insertion loss of the PMOS SPST switch with various transistor sizes is shown in Fig. 10, where the design tradeoff is between the 3-dB bandwidth and the insertion loss. By considering the available gain from the input buffer, the proposed T/H stage was
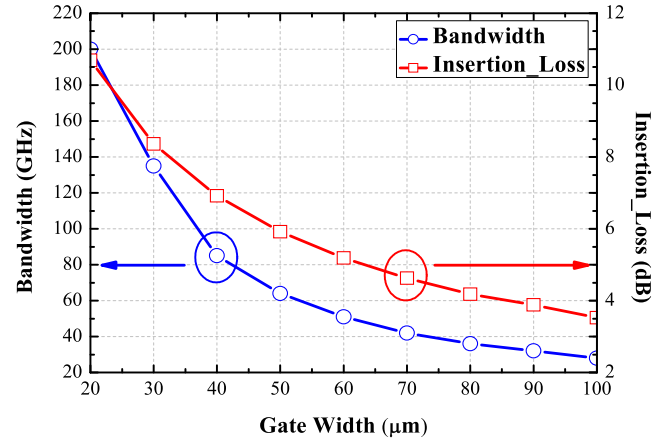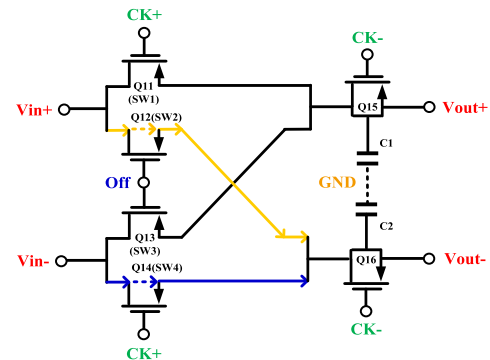

FIGURE 11. Schematic of the modified SC T/H stage with differential cancellation technique and clock-feedthrough mitigation technique.

designed using a total gate width of $2 \times 12 \, \mu$m, and the simulated 3-dB bandwidth can be up to 169 GHz with an insertion loss equal to 8.1 dB. To further enhance the operating speed, the input buffer was adopted to peak the roll-off of the T/H stage; the sampling speed was also enhanced on the basis of the analysis in Section III. In addition, the insertion loss of the T/H stage can be compensated using an appropriate topology for the input buffer.

In practical operation, the input signal may leak to the holding capacitor in the holding period because of the parasitic drain-to-source capacitance (C_{ds}). The hold-mode feedthrough heavily affects the pedestal error and reduces the linearity and dynamic range. Therefore, the differential feedthrough cancellation technique [32], [40] as shown in Fig. 11 is used to improve the feedthrough during the hold mode.

The T/H stage consists of four SPST switches (SW1–4) and two holding capacitors (C1 and C2). In the track mode, SW1 and SW4 are turned on, SW2 and SW3 are turned off, and the differential input signals (Vin+ and Vin−) are routed to C1 and C2 via SW1 and SW4, respectively. The isolation of SW2 and SW3 should be high enough to minimize the insertion loss of the track mode. In the hold mode,
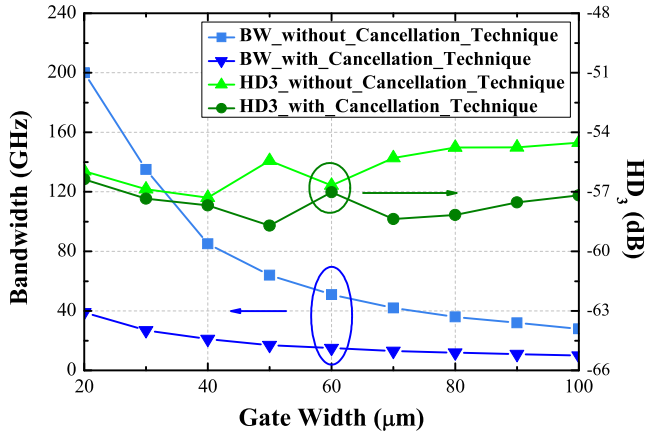
FIGURE 12. Simulated 3 dB bandwidth and HD$_3$ of the proposed T/H stage with and without the differential cancellation technique, where the transistor width is 2 μm and the finger number is swept from 20 to 100; HD$_3$ is simulated with an input peak-to-peak voltage of 0.3 V and an input frequency of 5 GHz.

SW1–4 are all turned off. If SW1–4 are all identical, the input feedthrough is completely cancelled at the output because of the 180° output of phase. In addition, the HD$_3$ of the T/H stage is further enhanced using the proposed differential hold-mode feedthrough cancellation technique, because the HD$_3$ of the tracking path is much better than that of the cancellation path. The third harmonics from the tracking path and the cancellation path are suppressed at the differential outputs due to the 180° output of phase.

The simulated HD$_3$ and 3-dB bandwidth of the T/H stage with and without the cancellation technique are plotted in Fig. 12, where the PMOS gate width is swept from 20 to 100 μm. Although the 3-dB bandwidth decreases as the gate width increases because of the parasitic capacitance of the PMOSs, the low-pass frequency of the T/H stage can be further compensated by the input buffer. Furthermore, the simulated HD$_3$ of the T/H stage with the cancellation technique is superior to that of the T/H stage without the cancellation technique. During the transition from hold to track mode, some acquisition time is required to track the input signal for the holding capacitor. In addition, some settling time is required to maintain the offset voltage for the holding capacitor as the T/H stage shifts from track to hold mode.

Regarding the clock feedthrough, the extent of the voltage error affecting the output signal of the T/H stage during the clock transition can be expressed as

$$\Delta V_{CH1} = (CK+) \times \frac{C_{gs11,14}}{C_{gs11,14} + C_H}, \tag{9}$$

where C$_{gs11,14}$ is the parasitic capacitance between the gate and source of the transistor and C$_H$ is the holding capacitance. The voltage error from the clock feedthrough can be reduced by enlarging C$_H$, but this would decrease the 3-dB bandwidth. This design challenge is overcome in the proposed T/H stage by using a dummy transistor connected to the SPST switch with the inverted clock signal. The schematics of the differential T/H stage with the dummy transistors and cancellation

technique are shown in Fig. 11, with four SPST switches (SW1–4) and two dummy transistors (Q15 and Q16) designed using the PMOS. The source and drain of the dummy transistors Q15 and Q16 are connected to each other. The amount of voltage error contributed by the dummy transistors can be expressed as

$$\Delta V_{CH2} = (CK-) \times \left(\frac{C_{gs15,16}}{C_{gs15,16} + C_H} + \frac{C_{gd15,16}}{C_{gd15,16} + C_H} \right), \tag{10}$$

where C$_{gd15,16}$ and C$_{gs15,16}$ are the parasitic capacitors between the gate and drain and the gate and source of the dummy transistor, respectively. The voltage error of the T/H stage during the clock transition can be rewritten as

$$\Delta V_{CH3} = \Delta V_{CH1} + \Delta V_{CH2}. \tag{11}$$

To thoroughly cancel out the clock feedthrough problem, ΔV$_{CH3}$ should be approximately zero. Therefore, the relationship between the holding capacitance, parasitic capacitors of the switch, and the dummy can be expressed as

$$\frac{C_{gs15,16}}{C_{gs15,16} + C_H} + \frac{C_{gd15,16}}{C_{gd15,16} + C_H} = \frac{C_{gs11,14}}{C_{gs11,14} + C_H}. \tag{12}$$

Because the holding capacitor is much larger than the parasitic capacitors of the T/H stage, (12) can be simplified to

$$\frac{2 \cdot C_{gs15,16}}{C_H} \approx \frac{C_{gs11,14}}{C_H}. \tag{13}$$

From (13), the ratio between the parasitic capacitors of the switch and the dummy is 2. In general, the parasitic capacitance of a transistor is proportional to its size. The optimal gate width of the dummy device should be equal to half gate width of the switch due to the clock feedthrough, charge injection, and DC offset. The SC topology also suffers from some voltage error due to the charge injection. During the track mode, the amount of charge stored in the channel of the MOS transistor can be expressed as [37]

$$Q_{ch} = W \cdot L \cdot C_{ox} \cdot (V_{GS} - V_T), \tag{14}$$

where W and L are the channel width and length, respectively, V$_{GS}$ is the voltage drop across gate and source, V$_T$ is the threshold voltage, and C$_{ox}$ is the parasitic gate capacitance. During the hold mode, some charge leaves the channel for the source and drain terminals, introducing additional voltage errors into the holding capacitor. Although the amount of injected charge is difficult to predict accurately, dummy transistors with an inverted clock signal can be adopted to further reduce the voltage error resulting from the charge injection because the empty channels of the dummy transistors provide extra space in which the injected charge can be stored.

B. MODIFIED DISTRIBUTED-AMPLIFIER-BASED INPUT BUFFER

Unlike parasitic capacitance degradation techniques, the distributed technique takes advantage of parasitic effects as a
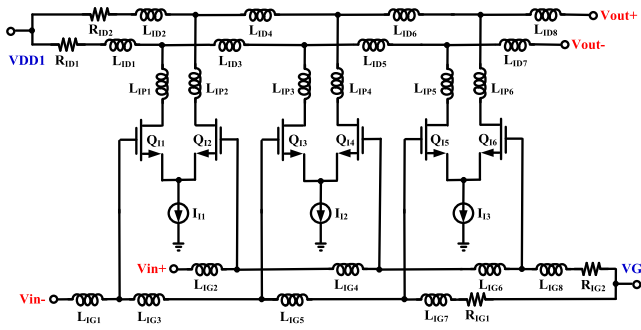
FIGURE 13. Schematic of the modified DA-based input buffer using inductor peaking.

bandwidth extension factor. The distributed technique is intuitively related to the transmission line. The parasitic capacitance of devices can be used to construct the transmission line model with multiple segments of extra series inductors. As the signal enters the artificial transmission line, the input signal is propagated to the load impedance through the constructed model.

The schematic of the proposed distributed-amplifier–(DA-) based input buffer is shown in Fig. 13. The DA was designed using a common-source amplifier as a gain cell. At the input port, multiple segments of the series inductors are connected to multiple shunt C_{gs} to construct the artificial gate transmission line with matching load impedance. At the output port, the artificial drain transmission line is constructed similarly with multiple shunt C_{ds} in use. As the input signal propagates through the gate line, the gain cells generate multiple amplified signals, which then propagate in the drain line. These amplified signals are superpositioned at the output to enhance the high-frequency gain. The proposed DA-based input buffer is designed using three-stage gain cells, which exhibit enough gain to compensate for the insertion loss of the T/H stage. However, because of the multiple segments of the inductors in use, the overshoot response of the input buffer can be easily realized by selecting appropriate drain line inductor values. These drain line inductors serve the peaking technique seen from the output node of a single gain cell to peak the roll-off that results from the T/H stage.

C. CASCODE AND PEAKING-BASED OUTPUT BUFFER

Without complicated bandwidth extension techniques, the conventional common-source amplifier is the basic topology for serving as a buffer. One major advantage is that common-source topology features high DC gain that enables compensation for the insertion loss of the T/H stage. The bandwidth of the output buffer remains a substantial issue; however, the cascode stage is an effective way to mitigate the heavy-output low-pass response. To further enhance the operating speed, inductive peaking is the basic method that does not involve complicated layout considerations that introduce higher costs. According to [41], the bandwidth enhancement ratio (BWER) of peaking technique–based amplifiers has been realized up to 2.8. Fig. 14 presents the schematic of the
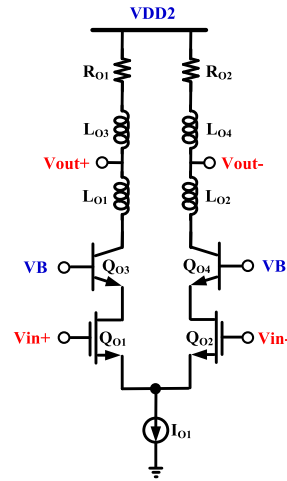

FIGURE 14. Schematic of the proposed cascoded common source amplifier-based output buffer incorporating the output T-coil peaking bandwidth extension technique.
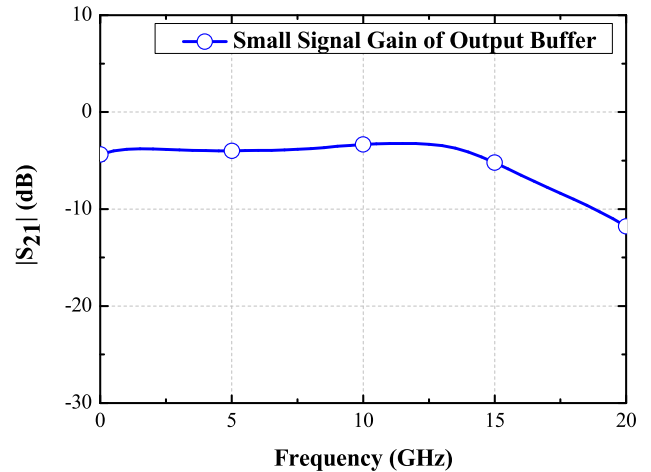

FIGURE 15. Simulated small signal gain of the proposed DA-based input buffer, modified SC-based T/H stage, and cascoded common source amplifier with peaking-based output buffer THA.

proposed output buffer, which consists of a common-source amplifier with a cascode output low-pass mitigation stage and inductive T-coil peaking. The effective parasitic capacitance at the output node with peaking consideration (C_{eff}) can be expressed as

$$C_{eff} = C - \frac{L(\omega)}{[R(\omega)]^2 + [\omega \cdot L(\omega)]^2}, \quad (15)$$

where C is the parasitic capacitor at the output node without active peaking inductor. Compared with the amplifier without the peaking technique, the BWER (β) can be expressed as [27]

$$\beta = \frac{f_{bweff}}{f_{bw}} \approx \frac{1/[2\pi \cdot R(\omega) \cdot C_{eff}]}{1/[2\pi \cdot R_1(\omega) \cdot C]}. \quad (16)$$

$R_1(\omega)$ is the effective resistor at the output node without a peaking inductor. The bandwidth can easily be enhanced 3 to 5 times the original cutoff frequency by selecting the appropriate value of the peaking inductors.
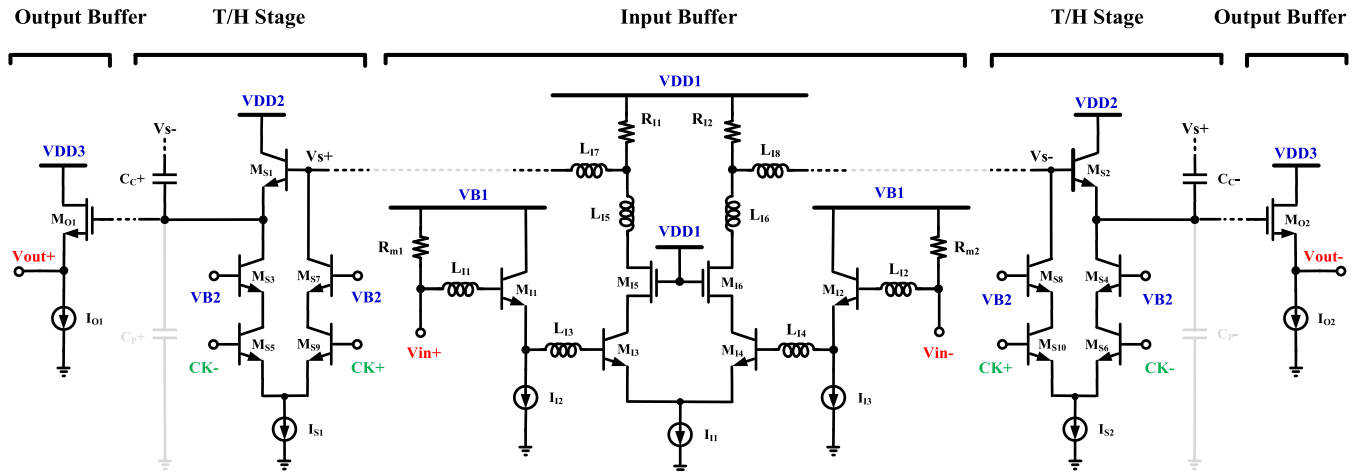
FIGURE 16. Schematic of the proposed modified Darlington-based input buffer, cascoded SEF-based T/H stage, and source follower-based output buffer THA.
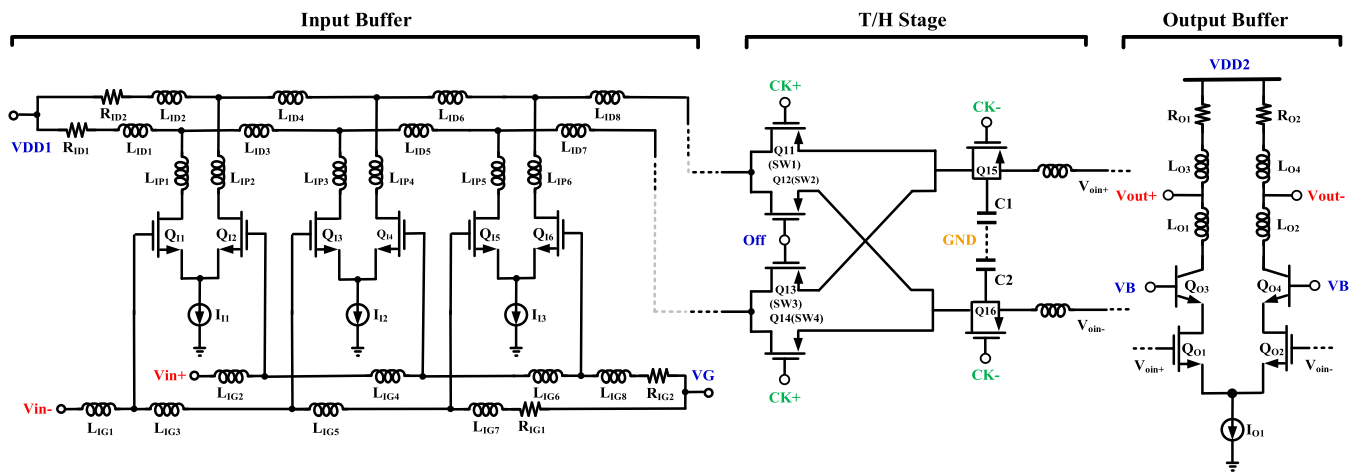

FIGURE 17. Schematic of the proposed DA-based input buffer, modified SC-based T/H stage, and cascoded common source amplifier with peaking-based output buffer THA.

The simulated track-mode bandwidth of the proposed DA and THA based on peaking bandwidth extension techniques is illustrated in Fig. 15, demonstrating a simulated 3-dB bandwidth of 17 GHz with an insertion of 4 dB. The bandwidth-extension techniques used in the proposed design successfully enhance the overall operating speed.

V. CIRCUIT IMPLEMENTATION

A. MODIFIED DARLINGTON AND CASCODED SEF T/H STAGE THA

The schematic of the proposed THA with the modified Darlington-based input buffer and cascoded SEF T/H stage are shown in Fig. 16. A modified Darlington-based amplifier with inductive peaking is used to enhance the 3-dB bandwidth and compensate the insertion loss and low-pass response resulting from the T/H stage. Two resistors R_{m1-2} are employed to improve the input matching and provide a DC bias for the input differential pair M_{I1-2}. The modified cascoded SEF T/H stage incorporating the differential cancellation technique is used to achieve high linearity and high
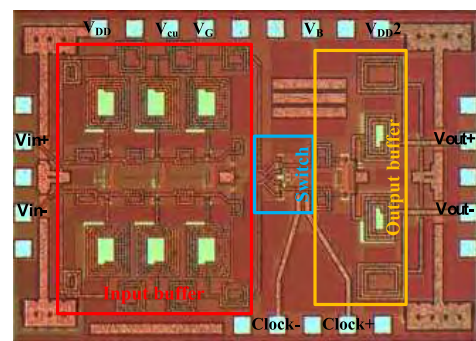
FIGURE 18. Photograph of the chip containing the proposed DA-based input buffer, modified SC-based T/H stage, and cascoded common source amplifier with peaking-based output buffer THA. (Chip size: 1.315 mm × 0.99 mm.)

speed. The voltage error resulting from clock feedthrough is minimized by using the proposed cascoded topology. To achieve good output matching and lower leakage current, the output buffer is designed using source-follower rather than emitter-follower topology, because the HBT has higher

FIGURE 19. Experimental results for the proposed modified Darlington-based input buffer, cascoded SEF-based T/H stage, and source follower-based output buffer THA: (a) simulated and measured S-parameters; (b) measured differential output waveform with a sampling rate of 4 GS/s and an input frequency of 1 GHz; (c) simulated and measured SFDR with a 13.5 GS/s sampling rate and different input frequencies swept from 800 MHz to 6 GHz; and (d) simulated and measured output spectra of differential output with a sampling rate of 13.5 GS/s and an input frequency of 1.2 GHz.

leakage current compared with the NMOS. The output-matching impedance is easy to obtain using source-follower topology. Several current sources are adopted to stabilize the DC biases of the T/H stage, the input buffer, and the output buffer. Some bypass capacitors are included in the DC supply path to suppress the low-frequency noise and the possibility of oscillation due to the DC bias network. The photograph of the chip containing the THA with the modified Darlington-based amplifier input buffer and cascoded SEF T/H stage was shown in [36]. The chip size is 1 mm × 0.73 mm. To enhance its quality, all of the spiral inductors are designed using the coplanar waveguide (CPW) structure. All the passive devices are simulated using an electromagnetic (EM) simulator [42].

B. DA-BASED INPUT BUFFER AND MODIFIED SC T/H STAGE THA

Fig. 17 shows the schematic of the proposed high-linearity high-speed THA with the input buffer based on the distributed bandwidth extension technique and the differential cancellation SC T/H stage. To increase the resolution, the SC T/H

stage with the differential hold-mode feedthrough cancellation technique is used to suppress the hold-mode feedthrough signal. The dummy transistors are adopted to mitigate the large voltage error that results from the clock feedthrough and charge injection. A three-stage DA is designed as an input buffer to compensate the insertion loss of the T/H stage with a small input return loss by designing appropriate inductors of the artificial gate transmission line. To realize favorable output return loss, flat gain, and high isolation from the T/H stage to the following stage, a cascoded common-source amplifier incorporating the inductive peaking technique is adopted as the output buffer. The output-matching impedance is obtained by selecting the appropriate transistor size and bias condition, as discussed in Section V-A. Fig. 18 is the photograph of the chip containing this proposed THA with a chip size of 1.315 mm × 0.99 mm. The thin film microstrip line (TFML) is adopted for the high-frequency interconnection to minimize unwanted coupling and the chip area. Because the pad area is much larger than the THA core, the RF and clock signal lines are designed using CPW to reduce the high attenuation for long signal propagation.

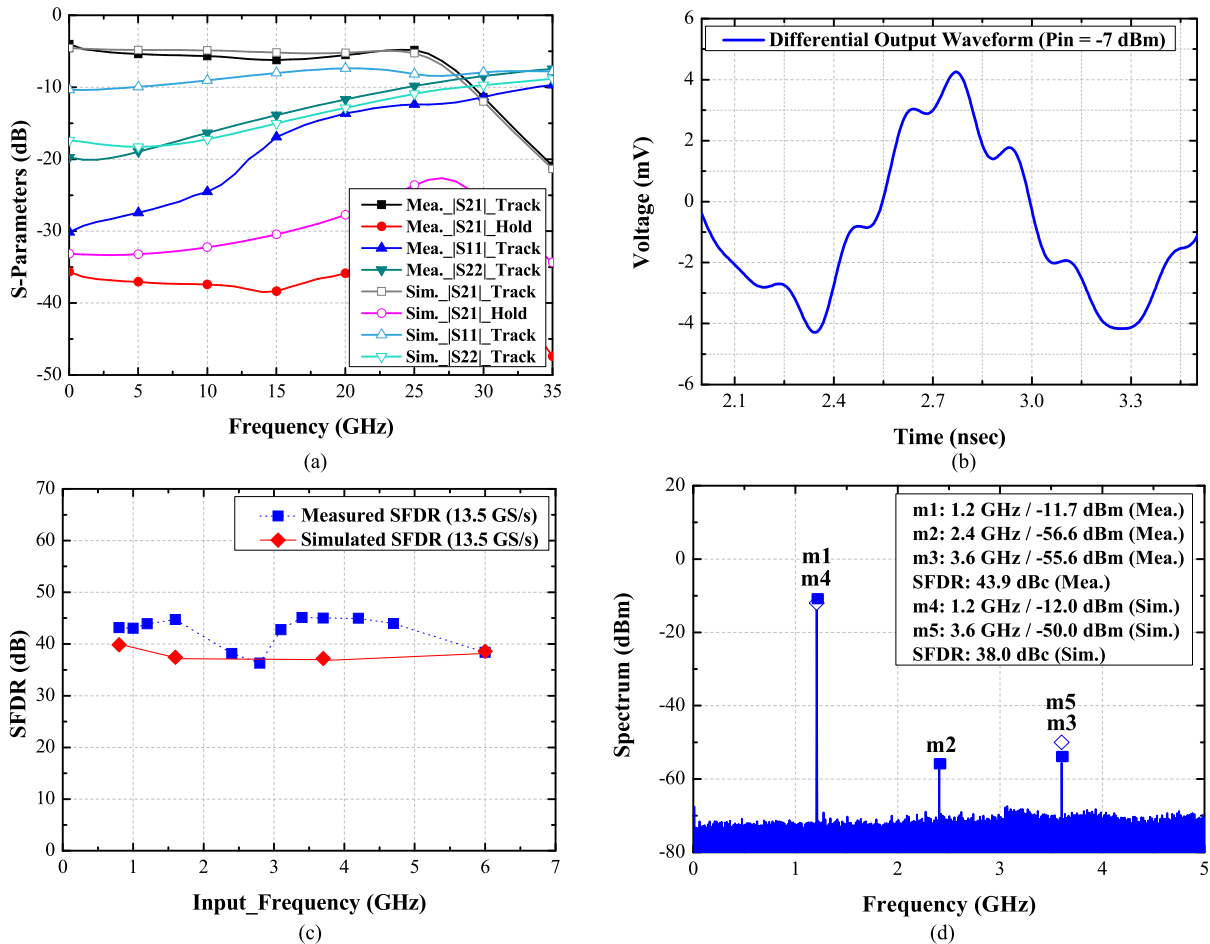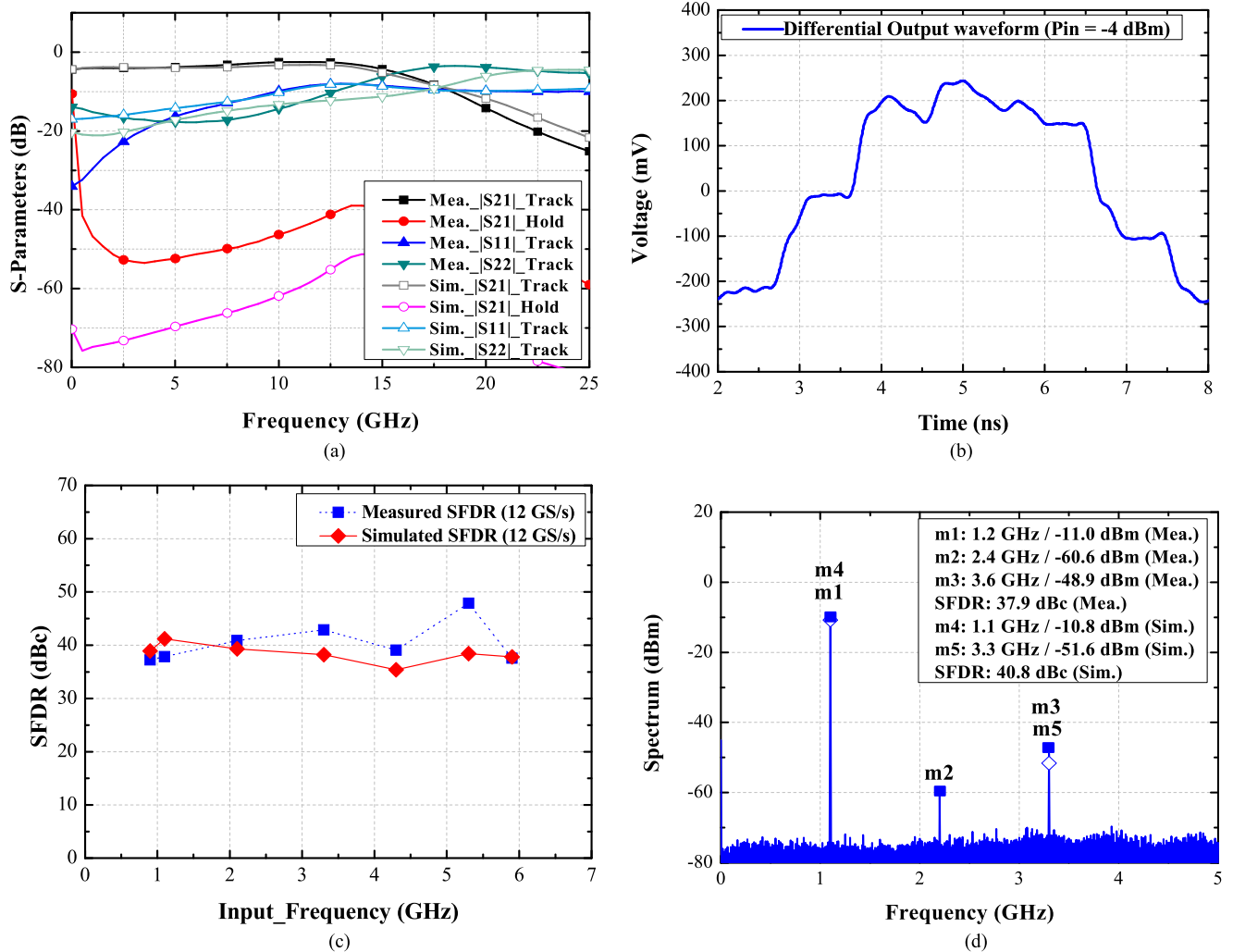**FIGURE 20.** Experimental results of the proposed DA-based input buffer, modified SC-based T/H stage, and cascoded common source amplifier with a peaking-based output buffer THA: (a) simulated and measured S-parameters; (b) measured differential output waveform with a sampling rate of 1 GS/s and an input frequency of 150 MHz; (c) simulated and measured SFDR with a 12 GS/s sampling rate and different input frequencies swept from 900 MHz to 5.9 GHz; and (d) simulated and measured output spectra of differential output with a sampling rate of 12 GS/s and an input frequency of 1.1 GHz.

VI. EXPERIMENTAL RESULTS

A. MEASUREMENT SETUP

The THAs were measured using on-wafer probing with a pitch-to-pitch size of 100 μm. The differential S-parameters were measured using an Agilent N5247A PNA-X four-port vector network analyzer with the differential clock signal replaced by two DC power supplies. For the SFDR measurements, the differential input signal was generated using two Agilent E8257D signal generators with proper calibration and phase synchronization. The signal generators were precisely synchronized using a 10-MHz reference signal with a high-resolution phase shifter in the generator. The two signal generators were calibrated using a three-port calibration kit to ensure the out-of-phase differential pair. During the calibration, the output spectrum of the calibration kit should be approximately zero to avoid phase imbalance between the two signal generators. The differential sampling clock

signals were generated using an Agilent N4903B pulse pattern generator. The output spectrum and waveform were measured using an Agilent E4448A spectrum analyzer and an Agilent 54855A DSO oscilloscope. For the output spectrum measurement, a broadband balun BAL-0026 provided by Mariki Microwave Inc. was employed to combine the differential outputs of the THA to the single-end output, and the insertion loss of the balun is 7 dB with a bandwidth from 300 kHz to 26.5 GHz. The overall insertion loss of the cable and RF probes was approximately 12 dB.

B. 27 GHz BANDWIDTH THA

The experimental results of the proposed THA with the modified Darlington amplifier-based input buffer and cascoded SEF T/H stage are presented in Fig. 19. The simulated and measured S-parameters are plotted in Fig. 19(a). The measured 3-dB bandwidth is 27 GHz with a minimum insertion

TABLE 1. Comparison of the proposed thas with previously reported THAs.

Ref.	Process	BW (GHz)	f_T (GHz)	BW/f_T	f_{sample} (GS/s)	Gain/Iso. (dB)/(dB)	SFDR (dB)	THD (dBc)	V_{DD}/P_{DC} (V/mW)	Input Swing (V)	Chip Area (mm^2)	Topology
[16]	130 nm CMOS	1.8	-	-	20	-/-	30	-29	1.2/71	0.2	0.09	DA + Switched Cascode
[17]	InP	-	175	-	20	-1/-	-	-45	-5.2/735	0.5	2×2	Emitter Deg. + SEF
[18]	90 nm CMOS	-	-	-	0.1	-/-	63	-60	1.2/2.97	0.8	0.18×0.13	P-S T/H Amplifier
[19]	InP	27	210	0.129	40	-/-	43.8	-48	-6/1900	0.5	1.4×1.6	Cherry Hooper + SEF
[20]	130 nm SiGe	-	-	-	10	-/-	-	-50	-/325	1	0.2×0.2	Emitter Deg. + SEF
[21]	InP	40	300	0.133	50	-7.8/-	46.2	-36.5	-6.2/1850	-	1.8	Emitter Deg. + SEF
[22]	65 nm CMOS	2.5	-	-	5	-7/-	46	-	1.2/48.8	0.3	1	Passive Peaking + SC
[23]	130 nm CMOS	3	-	-	2.5	-/-	42.4	-	1.7/	0.285	1.5×2	Common Source + SSF
[24]	InP	16	320	0.050	4	-/-	44	-38.6	-/2100	1.3	1.5×1.8	Data Buffer + SEF
[25]	28 nm CMOS	32	250	0.128	10	1/-	-	-38	1.8/50	0.8	0.89	SCL Buffer + SC
[26]	250 nm InP	27	370	0.073	50	-7/-	55	-29.5	-5/1200	9 dBm	0.675×1.075	Emitter Follower + MS
[27]	65 nm CMOS	19.3	180	0.107	32.5	0/-	37.4	-37	3.3//211	-	0.36	Active Peaking + SSF
[28]	45 nm SOI CMOS	-	-	-	40	-/30	55	-	2.5/415	-	0.85×0.45	Common Source + SC
[29]	90 nm SiGe	18	300	0.060	40	-/-	70	-39	3.9/560	6 dBm	0.7×0.7	Emitter Deg. + SEF
[30]	65 nm CMOS	7	107	0.065	12	0/-	34.2	-32.2	1.8/197	-	0.9×1	Common Source + SC
	90 nm CMOS	19	100	0.190	12	-2.5/-	42	-41.8	2.6/216	-	1×0.64	DA + SC
[31]	250 nm InP on	25	300	0.083	30	-10/35	60	-59	5.5/420	0.6	1.1×0.7	Emitter Deg. + SEF
	90 nm CMOS	19	100	0.190	12	-2.5/-	42	-41.8	2.6/216	-	1×0.64	gm-boost + MS
[32]	0.18 μm SiGe	8	54	0.148	16	-5/>50	48	-45	2.5/132	0.5	1.3×0.89	DA + SC
[33]	28 nm CMOS	55	-	-	25	-2.5/-	35	-28	1.75/73	0.8	0.53	Passive Peaking + SC
[34]	55 nm SiGe	40	330	0.121	108	-5/-	40	-49	2.5/87	-	0.94×0.52	Passive Peaking + SEF
[35]	130 nm SiGe	26	240	0.108	2.5	-1/40	52	-52	4/830	0.5	0.7×0.8	Cascomp + SEF
This	**0.18 μm SiGe**	**27**	**54**	**0.5**	**13.5**	**-4/33**	**45.1**	**-43**	**2.9/94.3**	**0.5**	**1×0.73**	**M. Darlington + SEF**
Work	**0.18 μm SiGe**	**17**	**54**	**0.32**	**13.5**	**-4/40**	**47.9**	**-45**	**2.1/180.1**	**0.5**	**1.315×0.99**	**DA + SC**

*Deg.: Degeneration.   *P-S: Power-Switched.   *SCL: Source Coupled Logic.   *MS: Master-Slave.   *M.: Modified.

loss of 4 dB. The bandwidth is this wide because the proposed SEF T/H stage with the modified Darlington topology and T-coil peaking technique has favorable high-frequency response. During the hold mode, the measured isolation is better than 33 dB over the 3-dB bandwidth. The measured input- and output-returned losses were better than 9 dB over the entire bandwidth. For the hold-mode isolation and the track-mode input return loss, the discrepancies between the simulation and measurement is due to the inaccuracy of the HBT large-signal model under the tracking and holding dc bias conditions. The measured differential output waveform is plotted in Fig. 19(b), where the input frequency is 1 GHz with an input power of −7 dBm, and the sampling rate is 4 GS/s. The THA also features low droop rate during the hold mode. The simulated and measured SFDR versus input frequency is plotted in Fig. 19(c), with an input power of −7 dBm and a sampling rate of 13.5 GS/s. The measured SFDR is better than 38 dBc from 800 MHz to 6 GHz, and the maximum SFDR is up to 45.1 dBc when the input frequency is 3.4 GHz. The measured THD is better than −42.55 dBc when the input frequency is 3.4 GHz. When the input frequency is 1.2 GHz with an input power of −7 dBm and the sampling rate is 13.5 GS/s, the simulated and measured

output spectra of the THA are shown in Fig. 19(d), and it features an measured SFDR of up to 43.9 dBc.

C. 17 GHz BANDWIDTH THA
The experimental results for the THA with the input buffer based on the distributed bandwidth extension technique and the differential cancellation-based SC T/H stage are shown in Fig. 20, including S-parameters, the output waveform and spectrum, and SFDR versus input frequency. The simulated and measured differential S-parameter results are shown in Fig. 20(a); the proposed THA demonstrates a 3-dB track-mode bandwidth of up to 17 GHz, and the smallest insertion loss is 4.4 dB. During the hold mode, the measured isolation is up to 40 dB, which demonstrates that the feedthrough signal is entirely cancelled out. The input and output return losses are better than 8 dB over the entire bandwidth. The proposed THA features good input and output matching because of the appropriate synthesized transmission line design and the proper transistor size selection of the output buffer. The measured differential output waveform is shown in Fig. 20(b), where the input frequency is 150 MHz with an input power of −4 dBm and the sampling rate is 1 GS/s. The proposed THA features low droop rate during

the hold mode. The simulated and measured SFDR versus input frequency is plotted in Fig. 20(c), where the input power is −7 dBm and the sampling rate is 12 GS/s. The measured SFDR is better than 37 dBc from 0.9 to 5.9 GHz, and the maximum SFDR is up to 47.9 dBc when the input frequency is 5.3 GHz. The simulated and measured output spectra of the THA are plotted in Fig. 20(d), where the input frequency is 1.1 GHz with an input power of −7 dBm, and the sampling rate is 12 GS/s; the SFDR is equal to 47.9 dBc. The proposed THA has a broad bandwidth, high speed, and a high dynamic range.

D. PERFORMANCE SUMMARY

Table I compares the proposed THAs with previously reported THAs. The proposed THAs have wide input bandwidth and low DC power consumption. The proposed modified Darlington-based THA using the peaking bandwidth extension technique demonstrates an approximately 0.5-f_T bandwidth, which is wider than any ratio reported in the literature. Moreover, the proposed THA with the distributed technique exhibits a bandwidth close to 0.32-f_T, which is also much larger than that for previously reported THAs. Furthermore, the proposed Darlington-based THA consumes less DC power compared to the DA-based and previously reported circuits. The linearity and dynamic range of the proposed THAs can be compared with those of previously reported advanced THAs. The proposed THAs have the best figure of merit (FOM) among the listed THAs, because the track-mode bandwidth of the proposed THAs with modified circuit topology are nearly half of the HBT's f_T. The proposed THAs are suitable for low-power, high-speed, and wide-input-bandwidth frontends.

VII. CONCLUSION

This paper presents two high-speed, high-linearity, and low-DC-power THAs in 0.18-μm SiGe process. A modified Darlington-based amplifier and a DA with peaking techniques are employed in the input buffers of the proposed two THAs, respectively, to compensate for the low-pass response and insertion loss of the T/H stage with good input matching. In addition, the SC and SEF T/H stages are modified using pedestal error reduction techniques including differential cancellation and cascode stages and investigated to further enhance the overall resolution of the THAs. The two proposed THAs have high dynamic range, low distortion, high sampling rate, wide input bandwidth (approximately 0.5-f_T), and their performance can be compared with that of amplifiers presented in prior papers. Moreover, the proposed design methodology for the THA can potentially support tens of GS/s using time-interleaved architecture in advanced silicon-based technology.

REFERENCES

[1] M. Ding, P. Harpe, Y.-H. Liu, B. Busze, K. Philips, and H. D. Groot, "A 46 μW 13 b 6.4 MS/s SAR ADC with background mismatch and offset calibration," in *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 423–432, Feb. 2017.

[2] M. Krämer, E. Janssen, K. Doris, and B. Murmann, "A 14-bit 30-MS/s 38-mW SAR ADC using noise filter gear shifting," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 64, no. 2, pp. 116–120, Feb. 2017.

[3] C.-C. Liu, M.-C. Huang, and Y.-H. Tu, "A 12 bit 100 MS/s SAR-assisted digital-slope ADC," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 2941–2950, Dec. 2016.

[4] Y. Lim and M. P. Flynn, "A 100 MS/s, 10.5 bit, 2.46 mW comparator-less pipeline ADC using self-biased ring amplifiers," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2331–2341, Oct. 2015.

[5] R. Sehgal, F. van der Goes, and K. Bult, "A 12 b 53 mW 195 MS/s pipeline ADC with 82 dB SFDR using split-ADC calibration," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1592–1603, Jul. 2015.

[6] J. Lin, D. Paik, S. Lee, M. Miyahara, and A. Matsuzawa, "An ultra-low-voltage 160 MS/s 7 bit interpolated pipeline ADC using dynamic amplifiers," in *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1399–1411, Jun. 2015.

[7] G. Tretter, M. M. Khafaji, D. Fritsche, C. Carta, and F. Ellinger, "Design and characterization of a 3-bit 24-GS/s flash ADC in 28-nm low-power digital CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1143–1152, Apr. 2016.

[8] Y. Xu, L. Belostotski, and J. W. Haslett, "A 65-nm CMOS 10-GS/s 4-bit background-calibrated noninterleaved flash ADC for radio astronomy," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 22, no. 11, pp. 2316–2325, Nov. 2014.

[9] P. Ritter, S. L. Tual, B. Allard, and M. Möller, "Design considerations for a 6 bit 20 GS/s SiGe BiCMOS flash ADC without track-and-hold," *IEEE J. Solid-State Circuits*, vol. 49, no. 9, pp. 1886–1894, Sep. 2014.

[10] B. V. Hieu, S. Beak, S. Choi, J. Seon, and T. T. Jeong, "Thermometer-to-binary encoder with bubble error correction (BEC) circuit for flash analog-to-digital converter (FADC)," in *Proc. IEEE Int. Conf. Commun. Electron.* Nha Trang, Vietnam, Aug. 2010, pp. 102–106.

[11] Y.-J. Chuang, H.-H. Ou, and B.-D. Liu, "A novel bubble tolerant thermometer-to-binary encoder for flash A/D converter," in *IEEE VLSI-TSA Int. Symp. VLSI Design, Automat. Test*, Apr. 2005, pp. 315–318.

[12] D. Lee, J. Yoo, K. Choi, and J. Ghaznavi, "Fat tree encoder design for ultra-high speed flash A/D converters," in *Proc. IEEE Midwest Symp. Circuits Syst.*, vol. 2. Tulsa, Oklahoma, Aug. 2002, pp. II-87–II-90.

[13] B. Xu, Y. Zhou, and Y. Chiu, "A 23-mW 24-GS/s 6-bit voltage-time hybrid time-interleaved ADC in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1091–1100, Apr. 2017.

[14] B. T. Reyes, R. M. Sanchez, A. L. Pola, and M. R. Hueda, "Design and experimental evaluation of a time-interleaved ADC calibration algorithm for application in high-speed communication systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 5, pp. 1019–1030, May 2017.

[15] C.-Y. Lin and T.-C. Lee, "A 12-bit 210-MS/s 2-times interleaved pipelined-SAR ADC with a passive residue transfer technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 4, pp. 929–938, Jul. 2016.

[16] H. Orser and A. Gopinath, "A 20 GS/s 1.2 V 0.13μmCMOS switched cascode track-and-hold amplifier," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 57, no. 7, pp. 512–516, Jul. 2010.

[17] S. Yamanaka, K. Sano, and K. Murata, "A 20-Gs/s track-and-hold amplifier in InP HBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 9, pp. 2334–2339, Sep. 2010.

[18] H.-G. Wei, U.-F. Chio, Y. Zhu, S.-W. Sin, S.-P. U, and R. P. Martins, "A rapid power-switchable track-and-hold amplifier in 90-nm CMOS," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 57, no. 1, pp. 16–20, Jan. 2010.

[19] Y. Bouvier, A. Ouslimani, A. Konczykowska, and J. Godin, "A 40 gsamples/s InP-DHBT track-&-hold amplifier," in *Proc. 5th Eur. Microw. Integr. Circuits Conf.*. Paris, France, Sep. 2010, pp. 61–64.

[20] Y. Borokhovych and J. C. Scheytt, "10 GS/s 8-bit bipolar THA in SiGe technology," in *Proc. NORCHIP*. Lund, Sweden, Nov. 2011, pp. 1–4.

[21] J. Deza *et al.*, "A 50-GHz-small-signal-bandwidth 50 GSa/s track&hold amplifier in InP DHBT technology," in *Proc. IEEE/MTT-S Int. Microw. Symp. Digest*, Montreal, QC, Canada, Jun. 2012, pp. 1–3.

[22] H.-L. Chen, S.-C. Cheng, and B.-W. Chen, "A 5-GS/s 46-dBc SFDR track and hold amplifier," in *Proc. Int. Symp. Intell. Signal Process. Commun. Syst.*, pp. 636–639, Nov. 2012.

[23] M. Macedo, G. W. Roberts, and I. Shih, "Track and hold for Giga-sample ADC applications using CMOS technology," in *Proc. IEEE Int. Symp. Circuits Syst.*, Seoul, South Korea, May 2012, pp. 2725–2728.

[24] J. Deza, A. Ouslimani, A. Konczykowska, A. Kasbari, and J. Godin, "A 4 GSa/s, 16-GHz input bandwidth master-slave track-and-hold amplifier in InP DHBT technology," in *Proc. 20th Telecommun. Forum (TELFOR)*, Nov. 2012, pp. 502–505.

[25] G. Tretter, D. Fritsche, C. Carta, and F. Ellinger, "10-GS/s track and hold circuit in 28 nm CMOS," in *Proc. Int. Semiconductor Conf. Dresden Grenoble (ISCDG)*, Dresden, Germany, Sep. 2013, pp. 1–3.

[26] S. Daneshgar, Z. Griffith, M. Seo, and M. J. W. Rodwell, "Low distortion 50 GSamples/s track-hold and sample-hold amplifiers," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2114–2126, Oct. 2014.

[27] S. Ma, H. Yu, and J. Ren, "A 32.5-GS/s sampler with time-interleaved track-and-hold amplifier in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3500–3511, Dec. 2014.

[28] H. Aggrawal and A. Babakhani, "A 40GS/s track-and-hold amplifier with 62dB SFDR3 in 45 nm CMOS SOI," in *Proc. IEEE MTT-S Int. Microw. Symp.*. Tampa Bay, Fl, USA, Jun. 2014, pp. 1–3.

[29] D. Lal, M. Abbasi, and D. S. Ricketts, "A compact, high linearity 40GS/s track-and-hold amplifier in 90 nm SiGe technology," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*. San Jose, CA, USA, Sep. 2015, pp. 1–4.

[30] Y.-C. Liu, H.-Y. Chang, S.-Y. Huang, and K. Chen, "Design and analysis of CMOS high-speed high dynamic-range track-and-hold amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2841–2853, Sep. 2015.

[31] K. N. Madsen, T. D. Gathman, S. Daneshgar, T. C. Oh, J. C. Li, and J. F. Buckwalter, "A high-linearity, 30 GS/s track-and-hold amplifier and time interleaved sample-and-hold in an InP-on-CMOS process," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2692–2702, Nov. 2015.

[32] Y.-A. Lin, Y.-C. Yeh, Y.-C. Liu, and H.-Y. Chang, "A 55-dB SFDR 16-GS/s track-and-hold amplifier in 0.18 μm SiGe using differential feedthrough cancellation technique," in *Proc. IEEE MTT-S Int. Microw. Symp. (IMS)*. San Francisco, CA, USA, May 2016, pp. 1–4.

[33] G. Tretter, D. Fritsche, M. M. Khafaji, C. Carta, and F. Ellinger, "A 55-GHz-bandwidth track-and-hold amplifier in 28-nm low-power CMOS," *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 63, no. 3, pp. 229–233, Mar. 2016.

[34] K. Vasilakopoulos, A. Cathelin, P. Chevalier, T. Nguyen, and S. P. Voinigescu, "A 108GS/s track and hold amplifier with MOS-HBT switch," in *Proc. IEEE MTT-S Int. Microw. Symp. (IMS)*. San Francisco, CA, USA, May 2016, pp. 1–4.

[35] P.-H. Lee, H.-Y. Lee, H.-B. Lee, and Y.-C. Jang, "An on-chip monitoring circuit for signal-integrity analysis of 8-Gb/s chip-to-chip interfaces with source-synchronous clock," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 4, pp. 1386–1396, Apr. 2017.

[36] Y.-A. Lin, Y.-C. Yeh, and H.-Y. Chang, "A 27-GHz 45-dB SFDR track-and-hold amplifier using modified darlington amplifier and cascoded SEF in 0.18-μm SiGe process," in *Proc. IEEE MTT-S Int. Microw. Symp. (IMS)*. Honolulu, HI, USA, Jun. 2017, pp. 1–4.

[37] B. Razavi, *Principles of Data Conversion System Design*. Piscataway, NJ, USA: IEEE Press, 1995.

[38] G. Tretter, D. Fritsche, C. Carta, and F. Ellinger, "Enhancing the input bandwidth of CMOS track and hold amplifiers," in *Proc. 20th Int. Conf. Microw., Radar Wireless Commun. (MIKON)*, Jun. 2014, pp. 1–4.

[39] F. Centurelli, P. Monsurro, and A. Trifiletti, "A model for the distortion due to switch on-resistance in sample-and-hold circuits," in *Proc. IEEE Int. Symp. Circuits Syst.*, Kos, Greece, May 2006, pp. 21–24.

[40] H. Lee, A. Aurangozeb, S. Park, J. Kim, and C. Kim, "A 6-bit 2.5-GS/s time-interleaved analog-to-digital converter using resistor-array sharing digital-to-analog converter," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 23, no. 11, pp. 2371–2383, Nov. 2015.

[41] T. Toifl, M. Kossel, C. Menolfi, T. Morf, and M. Schmatz, "A 23GHz differential amplifier with monolithically integrated T-coils in 0.09/spl mu/m CMOS technology," in *IEEE MTT-S Int. Microw. Symp. Digest*, vol. 1, Philadelphia, PA, USA, Jun. 2003, pp. 239–242.

[42] *Sonnet User's Guide*, 14th ed. North Syracuse, NY, USA: Sonnet Software, 2013.

YU-AN LIN was born in Taipei, Taiwan, in 1992. He received the B.S. and M.S. degrees in electrical engineering from National Central University, Taoyuan, Taiwan, in 2014 and 2017, respectively, where he is currently pursuing the Ph.D. degree in electrical engineering. His research interests include the microwave and millimeter-wave integrated circuits (ICs) and high-speed mixed-signal ICs.
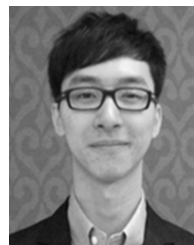
GUAN-LIN HUANG was born in Taoyuan, Taiwan, in 1991. He is currently pursuing the M.S. degree in electrical engineering from National Central University, Taoyuan. His current research interests include the microwave and millimeter-wave integrated circuits, and high-speed mixed-mode circuits.

YA-CHE YEH was born in Nantou, Taiwan, in 1990. He received the M.S. degree in electrical engineering from National Central University, Taoyuan, Taiwan, in 2016. His current research interests include the microwave and millimeter-wave integrated circuits, and high-speed mixed-mode circuits.

HONG-YEH CHANG (S'02–M'05) was born in Kinmen, Taiwan, in 1973. He received the B.S. and M.S. degrees in electrical engineering from National Central University, Taoyuan, Taiwan, in 1996 and 1998, respectively, and the Ph.D. degree from the Graduate Institute of Communication Engineering, National Taiwan University, Taipei, Taiwan, in 2004.

From 1998 to 1999, he was with Chunghwa Telecom Laboratories, Taoyuan, where he was involved in the research and development of code division multiple access cellular phone systems. In 2004, he was a Postdoctoral Research Fellow with the Graduate Institute of Communication Engineering, National Taiwan University, where he was involved in the research on advanced MMW integrated circuits. In 2006, he joined the Department of Electrical Engineering, National Central University, as a Faculty Member, where he is currently a Professor. In 2017, he joined the Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL, USA, as a Visiting Scholar. His research interests include microwave and millimeter-wave circuits, and system designs. His avocations have included amateur radio and high-fidelity audio.

Dr. Chang is a member of the Phi Tau Phi. He was a recipient of the Wu Da-Yu Memorial Award from the National Science Council, in 2013, and the Outstanding Electrical Engineering Professor Award from the Chinese Institute of Electrical Engineering, Taiwan, in 2016. He is currently an Associate Editor of the IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS.

• • •