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Evaluation Method of Flyback Converter Behaviors on Common-Mode Noise

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ABSTRACT Common-mode (CM) conduction electromagnetic interference (EMI) is a challenge for switched-mode power supply (SMPS) designers. A flyback converter is a traditional topology used in low-power isolated applications. The size and cost of EMI filters are important considerations for higher power density and lower cost of SMPS design. In most cases, the CM current is generated by voltage pulsation (*dv/dt*) assigned on the primary winding and the secondary winding. The CM current conduction paths can be mainly categorized into two categories. One is the interwinding parasitic capacitance of the transformer, and the other is the parasitic capacitance between the semiconductor switches and the protective ground. This paper proposed an evaluation method to measure the equivalent CM noise capacitance of the two main CM current conduction paths, respectively. Then, this paper proposed a CM noise cancellation scheme based on the transformer winding design combining the measurement technique and the FEM simulation tool. Planar transformers with PCB windings also have advantages in low profile, good heat dissipation, and good stray parameter consistency. Based on these considerations, an 18-W adapter is designed and tested to verify the effectiveness of the proposed evaluation method and the design scheme.

INDEX TERMS Common-mode (CM), flyback, EMI, planar transformer, equivalent capacitance.

I. INTRODUCTION

Flyback converter is a common topology used in low power applications such as mobile phone chargers, laptop power adapters, and etc. The efficiency, power density, and electromagnetic compatibility (EMC) form the key factors for switched-mode power supply (SMPS). Higher switching frequency can achieve higher power density, but it also needs to meet the electromagnetic interference (EMI) standards. Generally, EMI noise can be decoupled as different-mode (DM) noise and common-mode (CM) noise. Filters are used to suppress EMI noise at the cost of bulky magnetic components and expensive cost. Furthermore, EMI filters are easier to be interfered by electric and magnetic near-field couplings due to the compact space, which will degrade its filtering effect. Besides, the CM noise is usually harder to be attenuated compared to DM noise. Eliminating CM noise can greatly benefit the reduction of CM filter size and cost. For isolated power converters, the characteristics of the transformer will significantly affect the efficiency, power density, and EMI performance, which are the key considerations.

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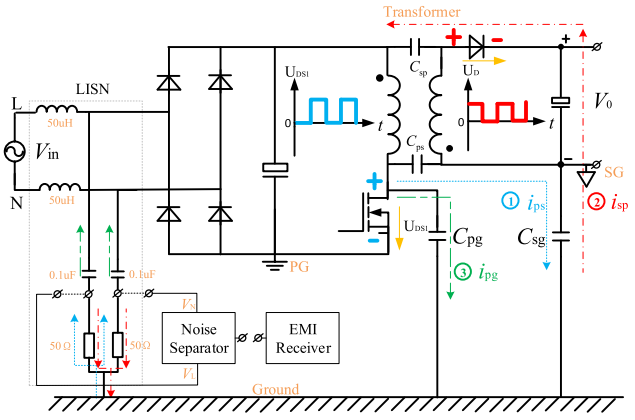


FIGURE 1. CM current conduction path of a flyback converter using secondary diode rectification.

The CM current conduction path in a flyback converter with secondary diode rectification is shown in Fig. 1. The CM current i_{pg} generated by the voltage pulsation (dv/dt) on the primary MOSFET flows into the protective ground through the parasitic capacitance C_{pg} via line impedance stabilization networks (LISNs) at the primary side. Besides, the primary

MOSFET also generates CM current i_{ps} conducting to the secondary side through the equivalent coupling capacitance C_{ps} to the LISN and the secondary diode generates CM current i_{sp} conducting to the primary side through the equivalent coupling capacitance C_{sp} to the LISN, where i_{ps} is determined by $U_{DS1}.C_{ps}$ and i_{sp} by $U_D.C_{sp}$. (C_{ps} is connected between primary voltage hot point and secondary voltage static point. Similarly, C_{sp} is connected between secondary voltage hot point and primary voltage static point.) By balancing the value of i_{ps}, i_{sp}, and i_{pg}, the total CM current is possible to be minimized to zero. The line impedance stabilization network (LISN) provides a specific impedance (50 Ω) for detecting EMI noise. Noise separator is used to decouple the EMI noise as DM noise and CM noise. EMI receiver measures conducted EMI noise spectrums from 150 kHz to 30 MHz according to EN5502 class B.

For reducing CM current in a flyback converter, most of techniques are focused on suppressing either of the CM current i_{pg} caused by the coupling capacitance C_{pg} between the primary switch and the ground or the CM current i_{ps} and i_{sp} by the coupling capacitance between the primary and the secondary winding in the transformer. For instance, in [1]–[3] and in [4]–[12], the reduction of i_{pg} and $i_{ps}-i_{sp}$ are purposed, respectively. Although these techniques may tremendously reduce the total CM current in power converters. However, they can only attenuate either i_{pg} or $i_{ps}-i_{sp}$ not simultaneously. If $i_{ps}-i_{sp}$ is far larger than i_{pg}, the techniques in [1]–[3] will be quite limited. Similarly, if i_{pg} causes large portion in total CM current, the techniques in [4]–[12] are not so effective to suppress.

The transformer coupling path is one of the main paths for CM current conduction, which is very critical for conductive EMI noise, and attract many scholars on how to eliminate the CM noise in view of the transformer winding design. For attenuating CM current in PCB planar transformers, the paired PCB layers concept was proposed and implemented in a flyback planar transformer. Since the adjacent primary and secondary winding layers have the same turns, it can maintain the same voltage potential distribution in the adjacent primary and secondary windings. Hence, their overlapping cannot generate CM displacement current [4]. Because the turns of the primary and secondary windings are different. Usually, the turns of the primary windings are larger than that of the secondary winding for low-voltage output. The remaining primary windings will be placed between the layers of the primary side in order to make them far away the secondary winding. However, the problem in increasing the number of PCB layers and limiting the flexible layout of the PCB winding can also be introduced. In [5], adopting double shielding layers inserted in between the primary and secondary winding layers is purposed to attenuate the CM current. However, the shielding layers cause large power losses, size, and cost. Besides, it is also impractical for fully interleaved transformer structure due to the existence of too many shielding layers. In [6], the partial shielding technique is proposed, only partially shielding the area between the primary and secondary windings is better than the full shielding to cancel the CM noise. To acquire the optimized shielding copper foil structure parameter, such as length, width of partial shielding layer and the distance between the shielding and winding, it can be simulated by FEM simulation tool. For the traditional enameled transformer, there exist inconsistency between the actual transformer and 3D model, since the key structure data is hard to be accurately got, such as the distance between interlayer. In [7], a CM noise shielding-cancellation technique is proposed, which can combine the merit of the shielding technique and noise cancelation method simultaneously. It can also eliminate the displacement current between the shielding and the secondary winding for the same voltage potential distribution. However, this approach also leads to some challenge in occupying more window height and increasing leakage inductance compared with the traditional wiring transformer. In [8], the primary semiconductor device is moved to the middle of the primary winding, unlike traditional flyback topology. This location change can build both positive and negative voltages in the primary winding to achieve CM noise cancellation. However, the challenge in gate driving of the primary switch can also be introduced. The coupling capacitance in the transformer and the voltage potential distribution on windings are the two significant factors and determine the CM current levels of the whole converters. In [13], changing transformer termination and adding an external capacitance are proposed to reduce the CM noise level, which may result in severe high-frequency CM noise due to transformer resonating with the coupling capacitance or termination capacitances of the secondary side semiconductor devices.

In order to achieve full CM noise cancellation, this paper purposed an evaluation method to measure the lumped equivalent CM noise capacitance, which can be further divided into 2 parts. One is the dynamic CM noise capacitance C_Q in transformer coupling path and the other is the external CM noise capacitance C_x between the semiconductor switch and the ground. Hence, C_Q and C_x can reflect the value of the CM current flowing through the transformer coupling path and the other coupling paths for an isolated power converter, respectively. Utilizing the CM current flowing through the transformer coupling path to cancel the CM current flowing through other coupling path in LISN is proposed in this paper. The transformer winding design scheme can be based on the value of C_X and the low-frequency CM noise can be totally canceled in LISN. The corner frequency of a CM filter is determined by low-frequency CM current. The higher the corner frequency the small size and less cost of the filter. The evaluation method proposed in this paper can effectively improve the EMC performance of SMPS. In Section II, the CM current conduction path with synchronous rectification topology is analyzed and the origin of the CM current is analyzed. In Section III, the measurement principle and method for C_Q and C_x are introduced. In Section IV, the transformer winding design principle is proposed based on the proposed evaluation method. Then, some practical CM

noise reduction techniques are introduced in view of the transformer winding design. In Section V, an 18W PCB planar flyback adapter is designed. The relevant tested result can verify the effectiveness of the proposed equivalent CM noise capacitance evaluation method and the transformer winding design scheme. Section VI concludes this paper.

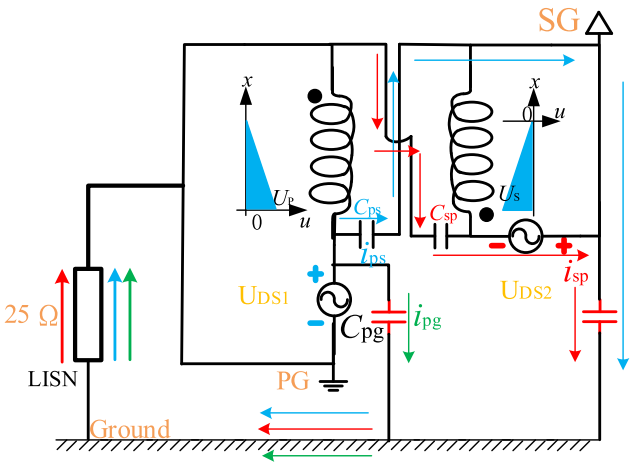


FIGURE 2. CM noise conduction path of a flyback converter using synchronous rectification.

II. ANALYSIS OF CM CURRENT OF A FLYBACK CONVERTER

For reducing the switching power losses caused by the switching on and switching off the secondary diode shown in Fig. 1, the topology of synchronous rectification is applied in secondary side. As shown in Fig. 2, the synchronous MOSFET is used in the secondary side and usually moved from the positive side to negative (ground) for easy gate driving. However, the location change of the synchronous rectification device causes the phase inversion of the secondary CM noise source U_S, resulting in the same phases of the CM current i_{sp} and i_{ps}. The CM current i_{pg} will flow through the coupling capacitance C_{pg} to LISN.

The total CM current flowing through LISN can be expressed as:

$$i_{cm} = i_{pg} + i_{ps} + i_{sp} \tag{1}$$

A. ORIGIN OF CM CURRENT

Moving charges form the displacement current, and then if the displacement current flows through ground line via LISN, called as CM current. Therefore, the total CM current can also be expressed as:

$$i_{cm} = \frac{dQ_{cm}}{dt} = \frac{d(Q_{pg} + Q_{ps} + Q_{sp})}{dt} \tag{2}$$

Q_{cm} is the resultant electric charges moving through ground line caused by voltage pulsation (dv/dt) on primary and secondary semiconductor switches devices. Similarly, Q_{pg}, Q_{ps}, and Q_{sp} are electric charges flowing through equivalent CM coupling capacitance C_{pg}, C_{ps}, and C_{sp}, respectively.

Therefore, for a more clear understanding, the origin of CM noise can be regarded as the resultant electric charges moving through the ground line or LISN.

B. CM ELECTRIC CHARGES MOVING THROUGH THE PARASITIC CAPACITANCE

For flyback topology, the turn ratio of the primary and secondary winding is large for low voltage-output. The voltage pulsation across the primary MOSFET is also far larger than that across the secondary MOSFET. Then, the CM charges caused by secondary MOSFET voltage pulsation moving through the coupling capacitance between the secondary side and the ground can be ignored.

The CM charges Q_{pg} moving through the coupling capacitance C_{pg} can be defined as:

$$Q_{pg} = C_{pg} \cdot V_P \tag{3}$$

where C_{pg} is the equivalent capacitance between the drain of the primary MOSFET and the ground, and V_P is the voltage applied to the primary winding or primary MOSFET.

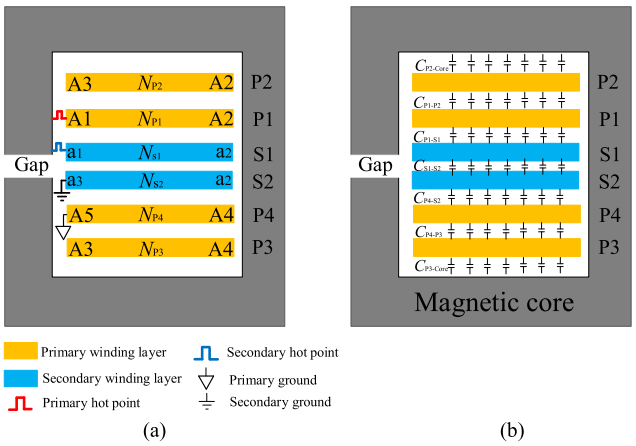


FIGURE 3. Transformer. (a) Transformer structure and connection. (b) Interlayer coupling capacitance.

C. CM ELECTRIC CHARGES MOVING THROUGH THE TRANSFORMER

Fig. 3 (a) shows the winding structure and terminal connection of the PCB planar transformer. There are four layers P1-P4 for primary windings and two layers S1-S2 for secondary windings. The point A1 is connected to primary MOSFET and a1 to secondary diode or MOSFET, then they are considered as voltage hot points. The point A5 is connected to the primary ground and a3 to the secondary ground, so they are both voltage static points. The transformer with interlayer coupling capacitance is shown in Fig. 3(b). The coupling capacitance includes $C_{P2-Core}$ between layer P2 and the magnetic core, C_{P1-P2} between layer P1 and layer P2, C_{P1-S1} between layer P1 and layer S1, C_{S1-S2} between layer S1 and S2, C_{S2-P4} between layer S2 and layer P4, and $C_{P4-Core}$ between layer P4 and the magnetic core.

Then, the electric charges will move through interlayer coupling capacitance to form the displacement current. Only the displacement current flowing through LISN detected by EMI receiver can be called as CM noise. Therefore, the displacement current flowing through C_{P1-P2}, C_{P4-P3}, and C_{S1-S2} just in primary or in secondary winding layers circulating does not cause CM noise. If the magnetic core is connected to the primary ground, the displacement current flowing through $C_{P2-Core}$ or $C_{P3-Core}$ will circulate between the core and the primary winding, which will not flow to LISN. Only the displacement current flowing through coupling capacitance C_{P1-S1} or C_{P4-S2} in the interface of the adjacent primary and secondary winding layers due to the existence of the voltage potential distributions in each turn of the transformer winding layer flows to the LISN via the coupling capacitance between secondary side to ground (for two-wires) or directly to ground (for three-wires).

The wires in a traditional enameled transformer, are always densely wound and the turn numbers are always larger in a layer. Hence, it has a larger trace width and fewer turn numbers in a layer compared with PCB winding. So, for enameled winding, the step of voltage potential distribution in each wire of the layer is very small and it is more reasonable to regard it as a linear distribution in theoretical calculation.

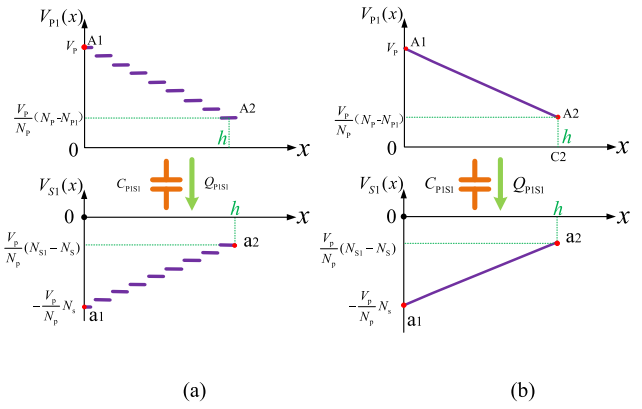


FIGURE 4. Voltage potential distribution of layers P1 and S1. (a) Step voltage potential distribution. (b) Linear voltage potential distribution.

Different with traditional enameled winding transformers, the PCB winding turns usually have larger PCB trace width. Therefore, the voltage potential distribution in a layer is distributed step by step. For the convenience of theoretical calculation, it is reasonable to consider it as evenly continuous linear distribution proximately to get the following expressions of $V_{P1(x)}$, $V_{S1(x)}$, $V_{P4(x)}$, $V_{S2(x)}$. The voltage potential distribution along winding layers P1, S1, P4, S2 are shown in Fig. 4 and Fig. 5. The configuration of secondary sides is synchronous rectification.

$$V_{P1}(x) = -\frac{V_P}{N_P}\left(N_{P1}\frac{x}{h} - N_P\right) \tag{4}$$

$$V_{S1}(x) = \frac{V_P}{N_P}\left(N_{S1}\frac{x}{h} - N_S\right) \tag{5}$$

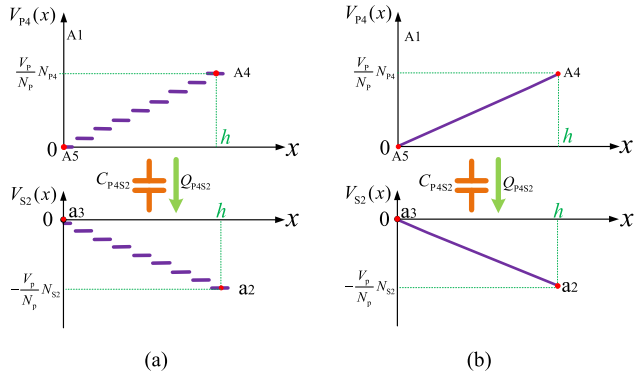


FIGURE 5. Voltage potential distribution of layers P4 and S2. (a) Step voltage potential distribution. (b) Linear voltage potential distribution.

$$V_{P4}(x) = \frac{V_P \cdot N_{P4}}{N_P}\frac{x}{h} \tag{6}$$

$$V_{S2}(x) = -\frac{V_P \cdot N_{S2}}{N_P}\frac{x}{h} \tag{7}$$

where V_P is the voltage across the primary MOSFET or the primary winding and V_S is the voltage across the secondary MOSFET or the secondary winding. h is the width of magnetic core window. N_P and N_S are the total turns of the primary and secondary winding, respectively. Similarly, N_{P1}, N_{P4}, N_{S1}, and N_{S2} are the turn numbers of layers P1, P4, S1 and S2, respectively.

The electric charges Q_{P1-S1} moving from the layer P1 to S1 can be calculated as:

$$Q_{P1-S1} = \frac{C_{P1-S1}}{2}\left(\frac{V_P}{N_P}(-N_{S1} - N_{P1} + 2N_P + 2N_S)\right) \tag{8}$$

Similarly, the electric charges Q_{P4-S2} moving from the layer P4 to S2 can be calculated as:

$$Q_{P4-S2} = \frac{C_{P4-S2}}{2}\left(\frac{V_P}{N_P}(N_{P4} + N_{S2})\right) \tag{9}$$

Then, the total CM charges moving through the transformer by coupling capacitance is

$$Q_{Trans} = Q_{P1-S1} + Q_{P4-S2} \tag{10}$$

The CM charges Q_{Trans} can use a lumped capacitance C_Q to express

$$Q_{Trans} = C_Q \cdot V_P \tag{11}$$

where C_Q is the equivalent CM noise capacitance, which can represent the value of CM charges moving through the transformer coupling path.

D. TOTAL CM CURRENT IN FLYBACK CONVERTER

The total CM charges are the sum of the CM charges moving through coupling capacitance C_{pg} to the ground and the transformer to the secondary side.

$$Q_{CM} = Q_{pg} + Q_{Trans} \tag{12}$$

Based on the equations from (2)-(12), the total CM charges can be expressed as:

$$Q_{CM} = (C_x + C_Q)V_p \tag{13}$$

where

$$C_x = C_{pg} \tag{14}$$

$$C_Q = \frac{C_{P4-S2}}{2}\left(\frac{N_{P4}+N_{S2}}{N_P}\right) + \frac{C_{P1-S1}}{2}\left(\frac{-N_{S1}-N_{P1}+2N_P+2N_S}{N_P}\right) \tag{15}$$

The smaller value of C_x and C_Q, the fewer CM charges will move through LISN.

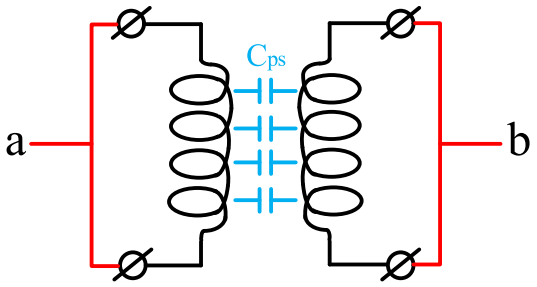


FIGURE 6. Traditional transformer evaluation method by an LCR meter or an impedance analyzer.

III. EVALUATION METHOD

A. TRADITIONAL EVALUATION METHOD

Structure capacitance in a transformer: The traditional evaluation method for EMI characteristics of the transformers is shown in Fig. 6. The two terminals of the primary and secondary winding are connected, respectively. Two ports of the LCR meter or the impedance analyzer connect terminals a and b, respectively. However, this method cannot take the effect of voltage potential distribution along the winding into consideration. In this way, the voltage potential along each turn of the primary and secondary winding is a constant, so the capacitance C_{ps} measured by this method is physical static structure capacitance rather than dynamic CM noise capacitance, which is related with voltage potential distribution. Structure capacitance refers to static capacitance, because its capacitance is only determined by physical structure parameters, such as the cover area, the distance, and the permittivity between the primary and the secondary winding layers. Static capacitance has nothing to do with the transformer EMI noise suppression behaviors in real operating conditions. The dynamic capacitance of transformer depends not only on winding structure parameters but also on potential distribution, and can reflect the transformer behaviors of the CM current suppression.

As aforementioned, the traditional transformer evaluation method cannot reflect the CM current conduction behaviors just because the LCR meter or impedance analyzer cannot impose the voltage potential distribution on the primary and secondary winding.

Based on this consideration, transformer evaluation methods have been proposed in previous papers. Reference [22] proposed that only a signal generator and an oscilloscope can achieve transformer evaluation. However, this method is not accurate enough limited by the accuracy of the test equipment. Reference [21] proposed using EMI receiver with TG option to evaluate the transformer. Hence, the insertion loss is used to calculate the equivalent capacitance but without phase information. The S_{21} parameter obtained by network analyzer have higher accuracy in higher frequency ranges and can reflect phase information. This paper will use network analyzer to evaluate the transformer and the equivalent capacitance is deduced based on S_{21}. Besides, the evaluation method in [21] and [22] both need the prototype to evaluate. S_{21} can not only be measured but also be simulated by FEM simulation tool. Hence, this paper will base on the previous effort [21]–[23] and use FEM full-wave simulation tool to simulate the EMI characteristic of the transformer. Then, the equivalent capacitance C_x between power switch and the ground is measured by the proposed method. The transformer can be designed according the value of C_x with the help of FEM simulation tool. The measuring principle and method of the dynamic CM noise capacitance C_Q and C_x will be discussed in the following.

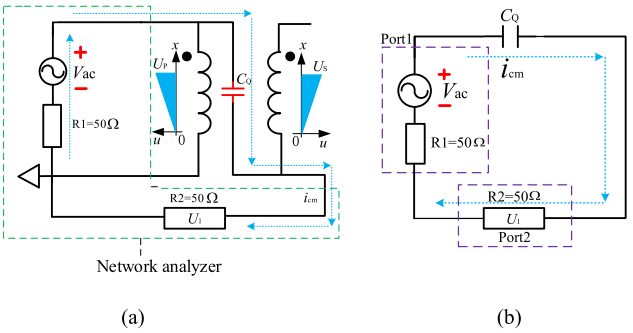


FIGURE 7. C_Q measurement. (a) Proposed evaluation method. (b) Equivalent circuit.

B. C_Q EVALUATION METHOD

Transformer evaluation method: Based on the concept that the transformer can be regarded as a CM filter [21], the insertion loss or S_{21} parameter can be used to evaluate the EMI performance. The S_{21} parameters can be afford not only by Network Analyzer, but also by FEM simulation tool. For the consistency of the test results and the simulation results, the dynamic capacitance of the transformer will be deduced according to the definition of S_{21} in this paper. As shown in Fig. 7 (a), Port 1 of the network analyzer connects voltage hot point of the primary winding and the grounding terminal connects static point of the primary winding. The Port 2 connects to the static point of the secondary winding and the hot point of secondary winding is just open. Port 1 will output excitation and establish voltage potential distributions both in primary and secondary windings, then electric charges will move through equivalent lumped CM noise capacitance C_Q to

form the CM current. Fig. 7 (b) is the test equivalent circuit. The CM displacement current will flow through transformer by the equivalent capacitance C_Q and produce voltage drop U_1 in resistor R2 and the voltage drop U_2 in R2 is with shoring the C_Q. The relationship between S_{21}, U_1, and U_2 can be deduced as in (16) in *dB*, according to the definition of S_{21}.

$$S_{21}(\text{dB}) = 20\lg\left|\frac{U_1}{U_2}\right| \tag{16}$$

where U_1 refers to the voltage drop on resistor R2, when the transformer is regarded as a CM filter, and U_2 refers to the voltage drop on resistor R2 without the transformer or shorting the C_Q. Then (16) can be further deduced by (17) and (18) to (19).

$$U_1 = \frac{50}{100 + \frac{1}{j\omega C_Q}} V_{ac} \tag{17}$$

$$U_2 = \frac{50}{100} V_{ac} \tag{18}$$

$$S_{21}(dB) = 20lg\left|\frac{100}{100 + \frac{1}{j\cdot 2\pi f\cdot C_Q}}\right| \tag{19}$$

In fact, the amplitude of $1/(j2\pi f.C_Q)$ is always much larger than 100 due to tiny capacitance of C_Q and the conductive EMI noise frequency ranges from 150kHz to 30MHz. Hence, if f increases 10 times, and S_{21} (dB) will increase by 20 dB. From the curve slope of the S_{21} traces, it can clearly find that its curve slope is 20 dB/Dec, when frequency axis is represented in logarithmic coordinate. Based on (19), the expression of C_Q can be calculated as in (20).

$$C_Q = \frac{1}{2\pi f\sqrt{10^{\frac{40-S_{21}(\text{dB})}{10}} - 10^4}} \tag{20}$$

where C_Q is the equivalent lumped dynamic capacitance, its amplitude reflects the value of CM current flowing through the transformer. Besides, the direction of CM current flowing through transformer coupling path can also be defined by the sign of C_Q. Then this paper defines that a positive sign of C_Q means that the CM current flows from the primary to the secondary side. Similarly, the negative sign of C_Q means that the CM current flows from the secondary to the primary side.

C. C_X EVALUATION METHOD

Due to the existence of semiconductor switch devices, the primary MOSFET will act as chopped wave and generate voltage pulsation on the primary winding. However, that needs a DC power supply to drive the relevant chips to control the switching on and switching off of the primary MOSFET. Based on these needs, an excitation source in the network analyzer can be assigned on primary winding to generate voltage pulsation. The CM current will be generated by the voltage pulsation. In order to measure the lumped CM noise capacitance in all conduction path, Fig. 8 (a) shows the measurement method.

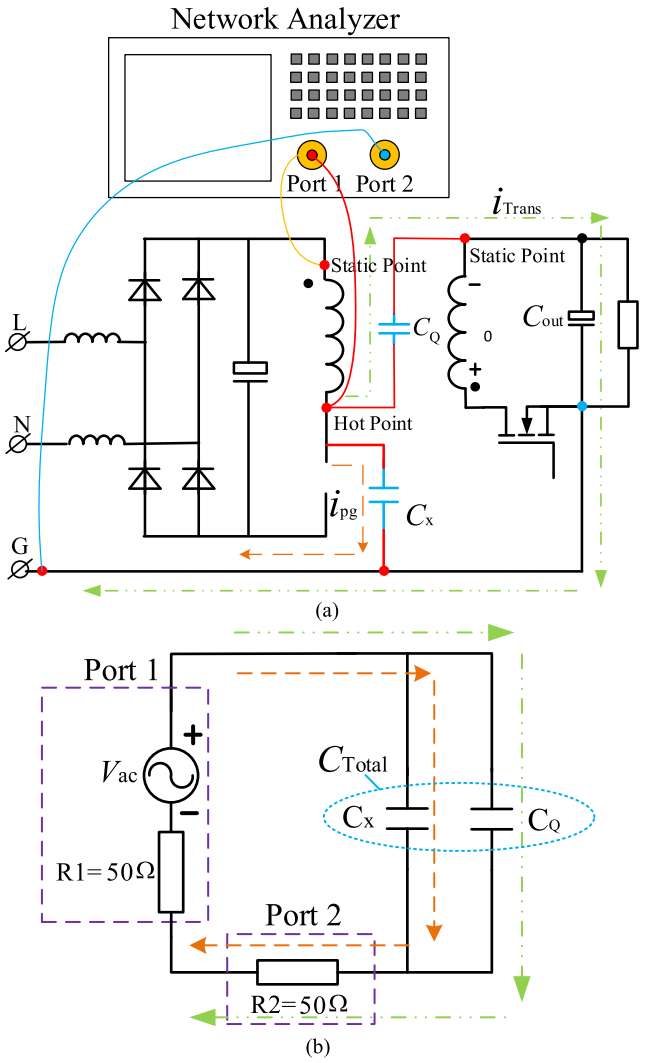


FIGURE 8. C_X measurement with three wires. (a) Proposed evaluation method. (b) Equivalent circuit.

As shown in Fig. 8 (a), Port 1 of network analyzer is connected to primary winding voltage hot point with grounding to the primary winding static point in the whole flyback converter. Due to the existence of a parasitic diode in primary MOSFET, the CM current will flow through the parasitic diode. So the MOSFET should be removed and then the CM current i_{pg} will completely flow through C_x to resistor R2. The ground line of the converter is connected to Port 2. The coupling capacitance C_{sg} between the secondary side and the ground can be omitted, when the converter is with three wires (L, N, and G lines). However, when the converter is with two wires, it needs LCR meter to measure C_{sg}. Besides, the input capacitor C_{in} and output capacitor C_{out} can be treated as short-circuiting in the conducted EMI frequency ranges due to their large capacitance. For the situation that the heat sink is attached to the MOSFET, the heat sink is usually connected to PG (primary ground) and the noise currents flowing to the heat sink from the drain of MOSFET internally return to the

MOSFET and will not flow to the LISN. So there is no need to measure C_x.

Fig. 8 (b) is the test equivalent circuit. Similarly, the total equivalent capacitance C_{Total} can be afforded by (20). Therefore, C_x can be calculated as

$$C_X = C_{Total} - C_Q \tag{21}$$

IV. CM NOISE REDUCTION TECHNIQUE

For the previous CM noise reduction techniques, like shielding technique [6], introducing anti-phases displacement current, and balance winding technique [11] are proposed in view of the transformer design. Then these techniques can only reduce the CM current flowing through the transformer. However, the coupling capacitance in the transformer is not only conduction path for conduction CM noise, but there are also other CM noise conduction paths, just like the parasitic capacitance between the drain of primary MOSFET and ground. Therefore, the following will introduce some CM noise cancellation schemes to attenuate the CM noise flowing through other conduction paths in view of the transformer design.

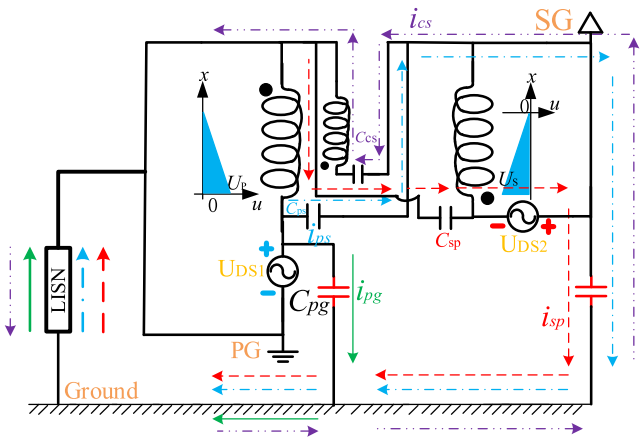


FIGURE 9. CM noise conduction path of a flyback converter with the compensation winding.

As aforementioned in Section II, there does not exist CM noise cancellation mechanism for a flyback converter with secondary synchronous rectification shown in Fig. 2. In order to cancel the CM current i_{ps}, i_{sp}, and i_{pg}, a compensation winding with anti-phase voltage potential is needed to generate anti-phase CM current i_{cs}. As shown in Fig. 9, one terminal of the compensation winding is connected to the primary voltage static point and the other is open. Besides, this compensation winding is inserted in between the adjacent primary and secondary windings. This compensation winding is just used to build electric fields and there is no power current flowing through it. The wiring direction of the compensation winding should be the same as that of the secondary winding. This compensation winding introduces an equivalent coupling capacitance C_{cs} between the adjacent secondary and compensation winding. To better understanding the origin of the CM current previously analyzed in Section II A, the CM current flowing through LISN will be expressed as electric charges.

The total CM charges moving through LISN can be calculated as

$$Q_{CM} = Q_{pg} + (Q_{ps} + Q_{sp} - Q_{cs}) \tag{22}$$

By (22), it can find that the CM charges moving through the transformer are $Q_{ps} + Q_{sp} - Q_{cs}$ determined by $V_P.C_Q$, and C_Q is a lumped CM noise capacitance in transformer coupling path. The CM charges in other conduction path are Q_{pg} determined by $V_P.C_X$.

Based on the above discussion, the total CM charges Q_{CM} in (22) can be further expressed as

$$\begin{aligned} C_X &= \frac{Q_{pg}}{V_P} \\ C_Q &= \frac{Q_{ps} + Q_{sp} - Q_{cs}}{V_P} \end{aligned} \tag{23}$$

According to (13), to achieve zero CM charges Q_{CM}, the value of C_X and C_Q should satisfy

$$C_X = -C_Q \tag{24}$$

where the negative sign means that the moving directions of the CM charges through the equivalent CM capacitance C_x and C_Q to LISN are anti-phase.

A. DESIGN OF COMPENSATION WINDING

The value of anti-phase displacement current i_{cs} varies with the turn numbers of the compensation winding. Then, the value of C_Q can also be changed with different turns of the compensation winding due to the variation of CM current flowing through transformer path. As mentioned in Section III C, the lumped equivalent capacitance C_x can be measured by a network analyzer. For attaining the value of C_Q, which can be afford not only by network analyzer but also by FEM simulation tool. Based on these evaluation methods, the transformer can be designed according to (24). This paper proposed using Ansys HFSS high-frequency full-wave simulation tool to simulate S_{21} parameter to calculate C_Q by (20). S_{21} parameter or C_Q varies with turn numbers of compensation winding. Therefore, if the turns of compensation winding are designed reasonably, then the value of C_Q can satisfy (24) and the CM current in all conduction paths can be completely canceled.

B. DESIGN OF EXTERNAL COMPENSATION CAPACITOR

Another reduction technique is to add an external compensation capacitor to cancel the CM current. Although several papers have purposed some relevant techniques. For example, an external capacitor is paralleled between the gate and drain of the primary MOSFET to change the value of miller capacitance. Then, the value of dV_{DS}/dt can be slower and less EMI noise is generated. But larger switching losses are also introduced with larger switch-on time. Adding Y-cap across the transformer static points of the primary and secondary

windings is very effective to reduce the CM noise flowing through the transformer [20]. However, when the CM current flowing through the other conduction path is larger than that flowing through transformer path. This method may be quite limited. Because Y-cap can only make the CM current circulate in transformer path and that cannot generate anti-phase CM current to cancel the CM current in other conduction paths.

For flyback converter with diode rectification in the secondary side, the CM current conduction paths are shown in Fig. 1. The phases of CM current i_{ps} and i_{sp} are anti-phase and their value can be adjusted by adjusting the value of C_{ps} and C_{sp}. C_{ps} and C_{sp} are equivalent CM capacitance, and paralleling an external capacitor between the primary voltage hot point and the secondary voltage static point can increase the value of C_{ps}. Similarly, the value of C_{sp} can also be adjusted by paralleling an external capacitor. Then, the value of C_Q can vary with that of paralleling external capacitor.

For flyback converter with MOSFET rectification in the secondary side, the CM current conduction paths are shown in Fig. 2. The phases of CM current i_{ps} and i_{sp} are the same. Paralleling a capacitor to change the value of C_{ps} or C_{sp} can only cause larger CM current flowing through the transformer or larger C_Q. But this does not mean that it is impossible to use an external compensation capacitor to reduce the CM current. To solve this problem, an effective solution is purposed. As shown in Fig. 9, anti-phase CM current is generated by compensation winding. However, the compensation winding must be inserted in between the adjacent primary and secondary winding. Because this location can generate equivalent CM capacitance C_{cs} and the CM current will flow through C_{cs} to cancel the CM current i_{ps}, i_{sp} and i_{pg}. Based on this concept, an external winding can be added outside the PCB winding and an external capacitor is added to replace the function of the equivalent parasitic capacitance C_{cs}. Its 3D model is shown in Fig. 10 (a).

Fig. 10 (b) shows the circuit diagram of the proposed noise cancellation. The wiring direction of the additional winding is the same as that of the secondary winding. One terminal of the additional winding is connected to the primary voltage static point with the other terminal connected to the external capacitor. The other terminal of the external capacitor connects to the secondary voltage static point. The CM current i_{cs} varies with the turns of the additional winding and the capacitance of the external capacitor. For easyadjusting i_{cs}, the turns of the additional winding are set as one. Adjusting the capacitance of the external capacitor can change the CM current i_{cs}. The resultant charges induced in the secondary side can be changed due to the different capacitance of the external capacitor. The value of C_Q can also be adjusted.

In a word, an external capacitor is effective to change the value of C_Q to satisfy (24).

V. EXPERIMENTAL RESULTS

To verify the effectiveness of the proposed evaluation method and the CM noise cancellation scheme, a flyback PCB planar

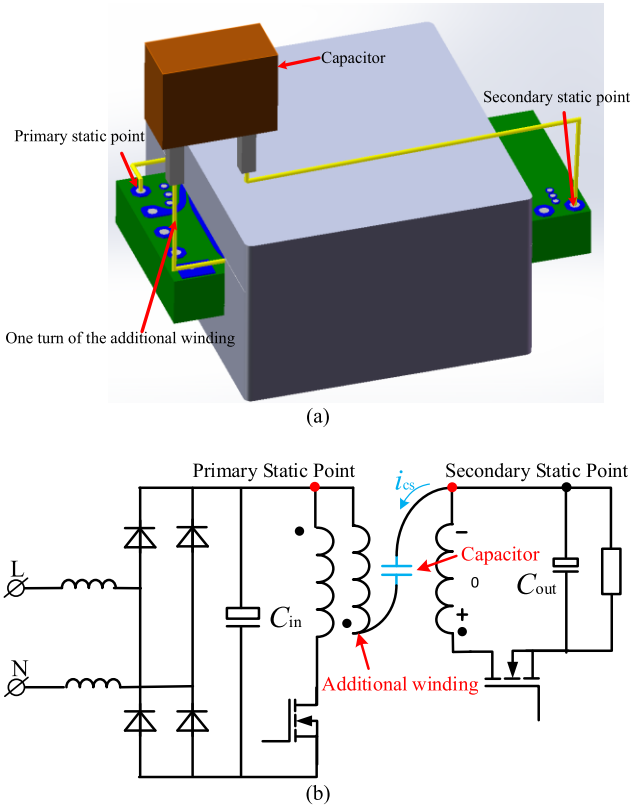


FIGURE 10. Adding external capacitor. (a) 3D model. (b) Circuit diagram.

TABLE 1. Prototype specification.

Input	90-230V
Output	9V/2A
Switching frequency	85kHz
Transformer	EID22.5/12.3, PC95, N_P=20, N_S=2, PSP

transformer is built to verify. The designed flyback converter is with synchronous rectification topology to improve the efficiency and the other detail specification is shown in Table 1. The flyback converter is with three wires.

For canceling CM noise flowing through the transformer path, the compensation winding is added between the adjacent primary and secondary winding to generate the anti-phase displacement current to cancel the CM current. There is a problem in how to afford the optimized turns of the compensation winding. The first step is to simulate the variation tendency trace of C_Q with different turns of the compensation winding and the simulation results are shown in Fig. 11. It can find that there is a minimum value of C_Q with 8 turns of compensation winding. Besides, when the turns of the compensation winding are less than 8 turns, the value of C_Q is positive. That means the direction of CM current flowing through the transformer is from primary to the secondary side. Similarly, when the turns of the compensation winding are larger than 8 turns, the CM current will flow through the transformer from secondary to the primary side with the negative value of C_Q. In Fig. 11, 8 turns of the compensation winding can be chosen as the optimized scheme temporally

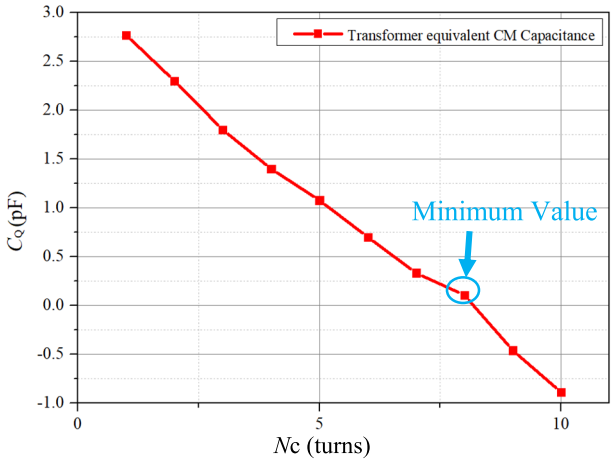


FIGURE 11. Simulation results.

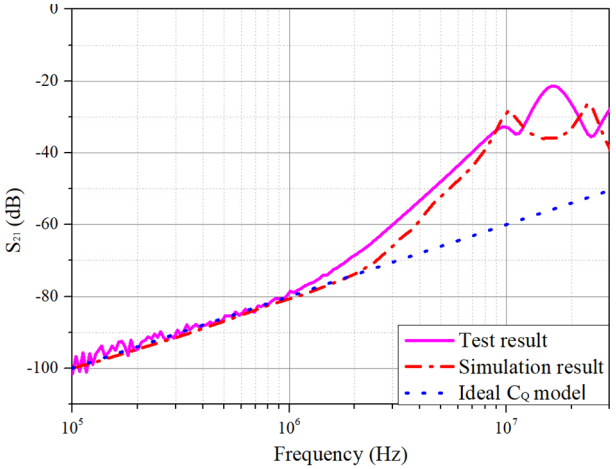


FIGURE 12. Comparison result from simulation, test and ideal C_Q.

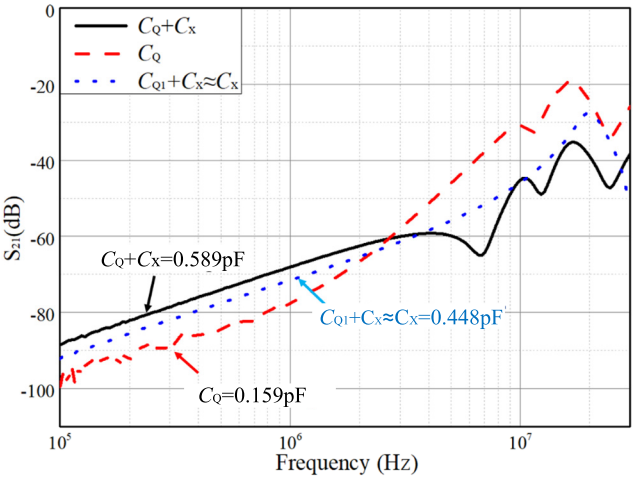


FIGURE 13. Test result.

when the CM current flowing through other conduction path is equal to zero. When the turns of compensation winding increase from 1 to 10, the value of C_Q can be reduced from a certain number to 0 and then the value of C_Q will be increased again from zero. When C_Q is positive, the direction of the total CM current flowing through transformer path is from the primary to the secondary side. When C_Q is zero, there is no CM current flowing through transformer path. When C_Q is negative, the direction of the total CM current flowing through transformer path is from the secondary to the primary side. This process means that the direction of the CM current in transformer path has changed. The second step is to measure the value of C_X and choose proper turns of the compensation winding to satisfy (24). The negative C_Q part here is just to simply express that the direction of the CM current flowing through the transformer is from the secondary to the primary side, corresponding to the positive capacitance in that the CM current flowing from primary to the secondary.

A. C_Q VERIFICATION

Fig. 12 shows the comparisons of the simulation result, test result and ideal C_Q model traces, and the effectiveness of the proposed simulation method can be verified.

For ideal capacitance model of C_Q, the capacitive coupling is only considered in the transformer. Hence, the transformer is just regarded as an equivalent ideal capacitance to conduct the CM noise, and the trace of S_{21} can be calculated by (19) with the slope of 20dB/Dec, when the frequency axis is expressed in logarithmic coordinates.

The simulation and test results of S_{21} is shown in Fig. 12, when the turns of the compensation winding are 8 turns. For the test result trace, there is oscillation on low frequency because the measured S_{21} results are too tiny to be preciously measured. But that can still regard it as a linear trace in low frequency. Based on this assumption, it can find that they conform well below 2MHz, but not well from 2MHz to 30MHz. There are many factors for the discrepancy. One of the most important reasons is that the permeability of the magnetic core varies with the frequencies during so high-frequency ranges, resulting in the variations of magnetizing inductance and leakage inductance. However, the permeability of the core material in the datasheet is usually given only below several MHz. For the core material PC95 used, the permeability below 2MHz is given in datasheet, so that it is difficult to make the simulation and test results have good consistency in high-frequency ranges. Furthermore, the permittivity of FR4 also varies with frequency. The parasitic parameters in transformer including capacitive coupling and inductive coupling, will affect the suppression ability of the CM current in transformer coupling path. Besides, the capacitive coupling play an important role in lower frequency ranges, while the inductive coupling will play a major role in higher frequency ranges. Hence, the transformer cannot be merely regarded as a pure capacitance in all conductive EMI frequency ranges.

B. C_X VERIFICATION

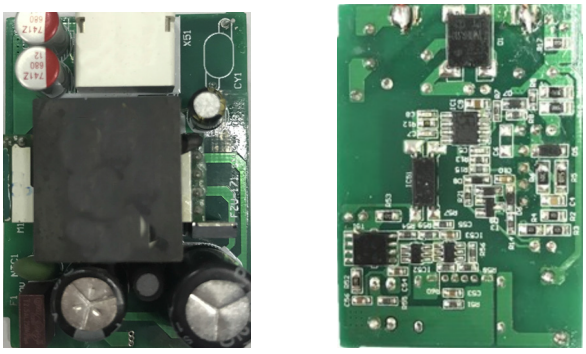
As shown in Fig. 13, the black trace is measured by the designed flyback converter with 8 turns of compensation winding. Using the evaluation method mentioned in

Section III C can get the value of $C_Q + C_x$, which equals to 0.598pF. The red dash trace is measured by the single designed transformer with 8 turns of compensation winding and combining (20) can get the value of C_Q. It equals 0.159pF. Hence, the value of C_x is given according to (21) and it equals 0.439pF.

To verify the effectiveness of C_x, the transformer with 8 turns of the compensation winding is used. Its C_Q is not extremely equal to zero. Then, C_Q can be slightly adjusted to zero by the method mentioned in Section IV B. The value of C_{Q1} is afforded by adjusting the capacitance of the external capacitor (its capacitance is 1.5pF and the turns of the additional winding is one). C_{Q1} will be closer to zero. Then, the adjusted transformer is located in the PCB main board of the flyback converter to measure and calculate the value of $C_{Q1} + C_X$. Due to C_{Q1} close to zero, then the value of $C_{Q1} + C_X$ can be approximated as that of C_X. The measured trace is also shown in Fig. 13 as the blue dot lines. By (20), it can find that the value of $C_{Q1}+C_x$ or C_x is 0.448pF. Because the value of C_{Q1} is hard to completely equal to zero. It can reasonably regard that the measured C_X is right. Although this verification can prove the correctness of C_X, it also needs to be verified by the CM noise test.

As above analysis, the value of the equivalent CM capacitance C_X on other conduction path is 0.439 pF, that means just design the transformer to achieve the minimum value of C_Q can only achieve the zero CM current in transformer path not that in all paths. Therefore, to achieve zero CM current in all paths, the value of C_Q can be determined by (24). According to Fig. 11, it can find that the turns of compensation winding can be designed as 9 turns to completely cancel the CM current in other conduction paths.

The designed flyback adapter picture with the PCB planar transformer is shown in Fig. 14.



(a) (b)

FIGURE 14. Designed flyback adapter. (a) Top view of the prototype. (b) Bottom view of the prototype.

The CM noise spectrum of the designed flyback adapter is measured in the electromagnetic shielding chamber. EMI receiver is R&S ESCI, LISN is R&S ESH2-Z5, and RF current probe R&S EZ-17 is used to measure the CM noise.

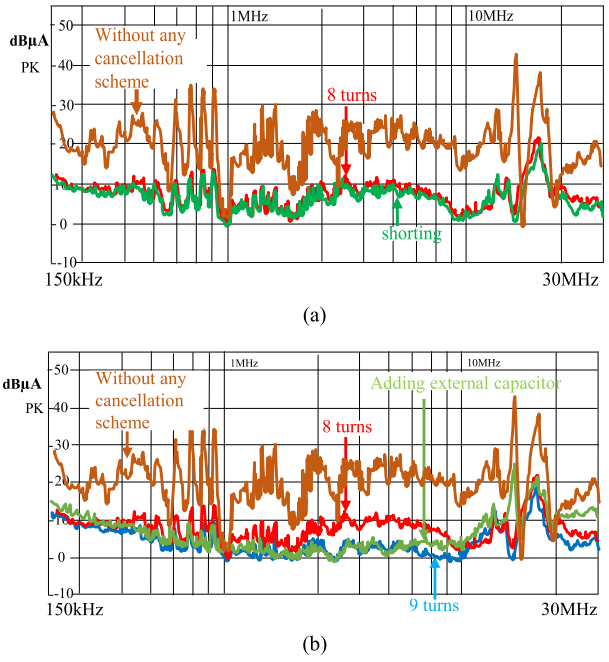


FIGURE 15. Test CM noise spectrum.

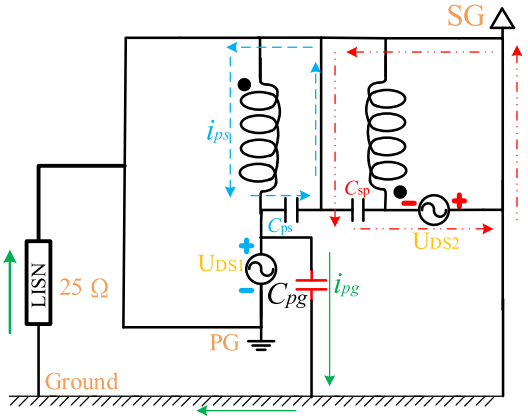


FIGURE 16. Shorting the static points of the primary and secondary windings.

The test CM noise spectrums are shown in Figs. 15 (a) and (b). Fig. 15 (a) is the test CM noise of the designed PCB transformer with 8 turns of compensation winding, shorting the static point of the primary and secondary winding, and the transformer without any noise cancellation scheme. It should be noted this shorting test is just used for verification purpose and not for practice product. This action can make the CM current merely circulate internally in the transformer. There are also some CM current i_{pg} flowing through the capacitance between the primary MOSFET and the ground to LISN. For better understanding, the CM current conduction path with this action is shown in Fig. 16. It can find that both CM noise spectrums are almost the same, which means the CM noise by the transformer path is completely canceled with 8 turns of compensation winding. Besides, the CM noise spectrum

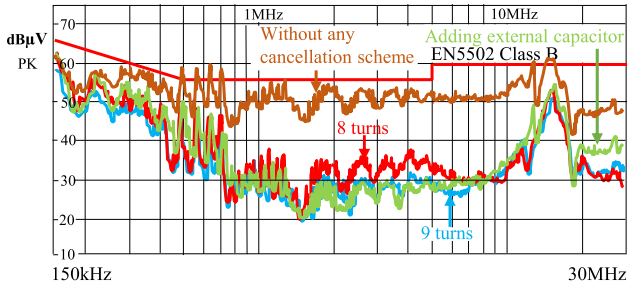


FIGURE 17. Test total noise spectrum.

with the proposed noise cancellation scheme is lower than that without any cancellation scheme.

However, there is also some CM noise via other conduction paths. To further reduce the CM noise, more turns of the compensation winding are needed and the test result is shown in Fig. 15 (b). That shows the measured CM noise spectrum of the designed flyback adapter using two different transformers with 8 or 9 turns of compensation winding. As seen, the peak CM noise of the converter with 9 turns of compensation winding is nearly 7 *dB* lower than that with 8 turns of compensation winding. That means the transformer with 8 turns of the compensation winding can only eliminate the CM current in transformer path but cannot cancel that in other conduction paths. Hence, the transformer with 9 turns of the compensation winding can generate the proper value of anti-phase CM current to cancel CM current in LISN. To verify the effectiveness of the proposed method mentioned in section IV B, Fig. 15 (b) shows the CM noise spectrum, where the turns of the additional winding are one and the capacitance of the external capacitor is 38pF, and the designed transformer without compensation winding was used. It can find that its noise cancelation effect is almost the same as that with 9 turns of compensation winding. But this method may worsen CM noise spectrum in high-frequency range.

But for high-frequency CM noise (above 8 MHz), the reduction effects are discounted. However, for EMI designers, the reduction of the low-frequency CM noise might be more critical. Because EMI filter design is mainly depended on low-frequency EMI noise. The less low-frequency EMI noise, the less cost and size on EMI filter. Then, the high-frequency EMI noise can be filtered by EMI filter. Therefore, the measured results verify the effectiveness of the proposed evaluation method and the simulation method.

Fig. 17 shows the conduction EMI noise spectrums, and the EMI test standard is the EN5502 class B. It can be found that the conduction EMI noise spectrum with 9 turns of the compensation winding and adding an external capacitance both can have good EMI performance, and they are lower than the EMI test standard limit line.

VI. CONCLUSION

1). The CM current conduction path in the transformer is different for secondary side using traditional diode rectification and synchronous rectification. For synchronous rectification, the location change of synchronous devices in the secondary side from positive side to negative (ground) side causes the phase of secondary CM noise source inversion resulting in severe EMI noise.

2). Traditional transformer evaluation method can merely measure the physical structure capacitance instead of the equivalent CM capacitance or the dynamic capacitance. Because the traditional method cannot take the voltage potential distribution along winding into consideration. Based on these demands, a novel EMI noise evaluation method has been proposed to measure the equivalent capacitance C_X in the other conduction path. The experiment can verify the effectiveness of the proposed evaluation method.

3). Based on the proposed evaluation method, two CM noise cancellation schemes is proposed in view of the transformer. Then, the CM current flowing through other conduction paths can be eliminated by optimizing the design of transformer.

4). Entirely eliminating the CM current flowing through the parasitic capacitance in transformer path may not be a best scheme for EMI attenuate. Because there are other CM currents flowing through other conduction paths.

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