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A High Speed On-Chip Soft-Start Technique With High Start-Up Stability for Current-Mode DC-DC Converter

LONG HUANG, PING LUO, CHENYANG WANG, AND XIANLI ZHOU

State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, Chengdu 610054, China

Corresponding author: Ping Luo (pingl@uestc.edu.cn)

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ABSTRACT In high efficiency and high-frequency applications, the soft-start methods for DC-DC converter with fast output voltage settling speed have attracted widespread attention. A novel soft-start circuit with controllable start-up time, high start-up speed, high stability, and no off-chip capacitor for a current mode DC-DC is proposed in this paper. The proposed soft-start circuit introduces a current-limiting feedback technique so that the inductor current during soft-start is controllable. The stability of the soft-start technique is verified theoretically in this paper. A Boost converter using this novel soft-start technique is fabricated in 0.35 μm BCD process. The soft-start time of the Boost converter is only 380 μs at the conditions of 45 V output voltage, 20 μF load capacitance, and 500 mA load current.

INDEX TERMS Current mode DC-DC, soft-start technique, current-limiting feedback technique, output capacitor-less.

I. INTRODUCTION

As a widely used power module for portable electronic devices, the current mode DC-DC converter with its good performance in load capacity, efficiency and transient speed, has been paid much attention in recent years. Especially, higher switching speed between standby state and normal working state of a DC-DC power converter is required to increase system efficiency and extend battery life [1], [2]. Thence, to design a start-up circuit with high-speed and high-reliability for DC-DC converter is of great significance [3]. Meanwhile, current inrush and output voltage overshoot should also be avoided during the start-up period since it could lead to serious consequences [4], [5].

As for current inrush, it could cause serious problems like burning down the circuit or even pulling down the power supply. Furthermore, if the inductor current keeps high and does not fall back before the soft-start is completed, the load capacitor would be overcharged. As a result, the load circuit or components may be damaged due to the output voltage overshoot [6], [7].

In a most common soft-start circuit, the reference input signal V_{ref} of the error amplifier (EA) in DC-DC converter is replaced by a fixed ramp signal, which means the settling time would be limited by the ramp-up speed. This solution is highly reliable without current inrush or voltage overshoot [8]. Charging a capacitor with a fixed current is a viable method to generate the fixed ramp signal. However, limited by process deviations of nanoscale current, a large capacitor is always required to ensure the slow ramp-up speed [9], [10]. In order to remove the off-chip capacitor, a pulse current is used to charge the capacitor and get a ramp signal [11], [12]. Some other start-up schemes in [13] and [14], V_{REF} or the output voltage V_C of EA is replaced by specific waveforms to achieve specific start-up effects. In addition, some digital soft-start circuits are suitable for digital power supplies in [15] and [16]. The above methods have their advantages and limitations. To eliminate the inrush current and overshoot voltage, the performance of start-up speed is always sacrificed. In this paper, a soft-start technique based on current-limiting feedback technique is proposed to against those problems. Under the proposed technique, this soft-start circuit will achieve high-speed start-up and highly stability without off-chip capacitance.

The paper is organized as follows: Section I is the background of soft-start technique; Section II introduces the principle of soft-start circuit with the current-limiting feedback technique; Section III analyzes the stability of soft-start

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circuit based on current-limiting feedback technique in DC-DC application; Section IV gives the experimental results; finally, a summary is given in Section V.

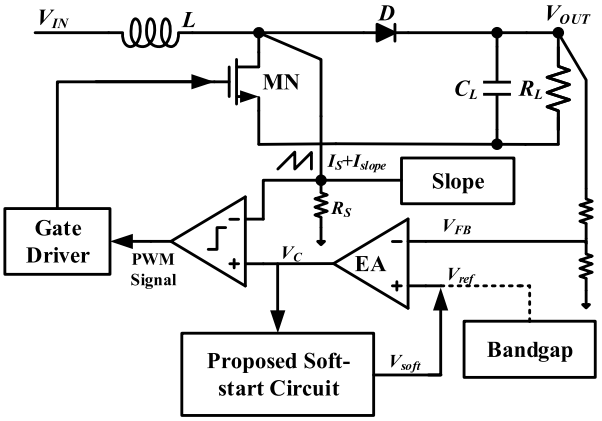

FIGURE 1. Current mode boost converter with proposed soft-start circuit.

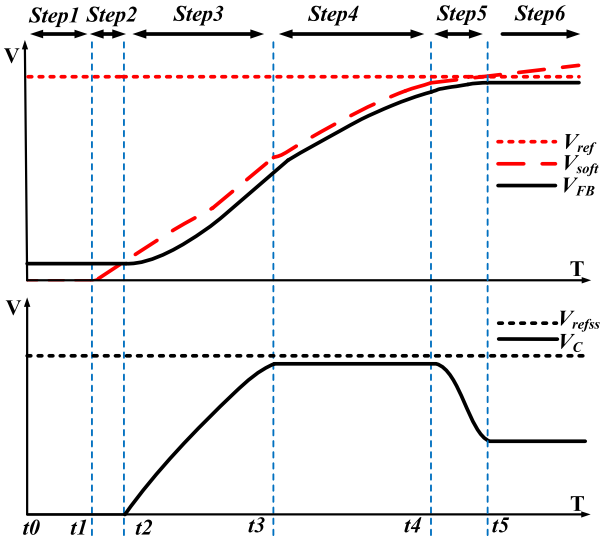

FIGURE 2. Soft-start waveform with proposed soft-start circuit.

II. THE PRINCIPLE OF SOFT-START CIRCUIT WITH THE CURRENT LIMIT FEEDBACK TECHNOLOGY

The current mode Boost converter with proposed soft-start circuit is shown in Fig. 1. The sensing signal of the inductor current I_S is added to the slope compensation current I_{slope}, the sum current of I_S and I_{slope} will converted to voltage signal and then compare with V_C. The result of the comparison will determine the duty cycle of PWM signal, so that the following expression can be introduced.

$$V_S + M_S DTR_S = V_C \tag{1}$$

where V_S, M_S, D, T, and V_C represent the voltage signal carrying the information of I_S, the slope of I_{slope}, the duty cycle, the clock period, and the output voltage of the EA, respectively.

Thus, it is a feature of the peak current mode Boost that the output voltage of EA could not only reflect the information of the inductor current but also limit the peak value of the inductor current.

Under the feature above, this paper proposes a soft-start circuit based on current-limiting feedback technique. Two feedback loops are added to control the output voltage of EA during the soft-start period. This enables the designer to control the inductor current and achieve more controllable start-up. Compare with [13], the proposed current-limiting feedback technique is mainly to control the waveform of the output voltage of EA by negative feedback without cutting the loop, which is benefit for circuit resources saving and system stability. Therefore, how to control the EA waveform to achieve a better soft-start effect is worth discussing.

In order to increase inductor current rapidly during soft-start period and make it under control, a reasonable control method is proposed. Fig 2 shows the waveform diagram of the soft-start control process. This start-up process involves a number of different steps. As shown in Fig. 2, V_C is controlled to reach a preset value V_{refss} at the maximum speed and keep

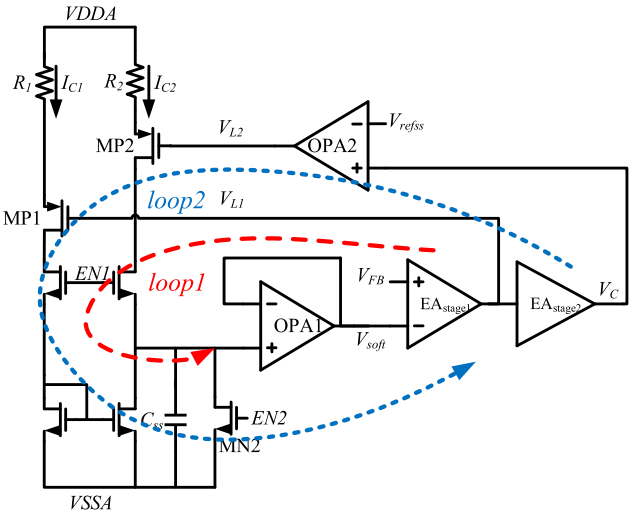

FIGURE 3. The schematic of proposed soft-start circuit with current-limiting feedback technique.

the preset value until the next step. When the Boost output voltage approaches the target value, we release the soft-start control of V_C to make it back to the normal level, which can prevent the overshoot of Boost output voltage. In this case, the preset value mentioned here determines the soft-start speed because it represents the peak level of the inductor current during soft-start.

The schematic of the proposed soft-start circuit shown in Fig. 3 contains two loops to achieve the control of the V_C. EA_{stage1} and EA_{stage2} are the first stage and second stage of the EA in Boost, respectively. The output voltage V_{L1} of the first stage is connected to the gate of MP1 to form the negative feedback loop1. The output voltage V_C of EA is connected to the positive terminal of the amplifier OPA2, and the output voltage V_{L2} of OPA2 is connected to the gate of MP2 to form another negative feedback loop2. The soft-start process is

described in conjunction with the waveform diagram shown in Fig. 2 as follow:

Step1 (t0-t1): During t0-t1, the enable signal *EN1* and the V_{soft} remain zero. Due to the freewheeling diode charging the output capacitor of Boost converter, V_{FB} has an initial value, then $V_{soft} < V_{FB}$. Further, since EA_{stage2} is a reverse amplification, V_C remains zero during Step1.

Step2 (t1-t2): At time t1, *EN1* turns to high level. Since V_C is lower than V_{refss}, V_{L2} still remains zero. A constant current I_{C2_MAX} passes MP2 to charge C_{SS} that makes V_{soft} gradually increases in step2. Here I_{C2_MAX} is defined as the current flowing through MP2 when the output voltage of OP2 is zero. At the same time, since $V_{soft} < V_{FB}$, V_{L1} remains high level, no current flows through MP1. As V_{soft} gradually increases, V_{soft} reaches V_{FB} at time t2.

Step3 (t2-t3): At time t2, $V_{soft} > V_{FB}$, V_{L1} gradually decreases, MP1 turns on and current I_{C1} flowing through it to discharge C_{SS}. When V_{L1} gradually decreases to V_Q, there is $I_{C1} = I_{C2\_MAX}$. Where V_Q is the value of V_{L1} when EA is at the state of maximum slew rate. Therefore, the negative feedback loop maintains V_{L1} at V_Q during Step3, at which the EA is remained at the maximum slew rate rise until V_C approaches the V_{refss}. Since V_{L1} is maintaining close to V_Q, the difference between V_{soft} and V_{FB} is maintained at a suitable value. The function of loop2 is to ensure the rising speed of V_{soft} is limited by the slew rate of EA, thus the soft-start process is controllable during Step3. For further explanation, A deep study for multi-loop negative feedback is described in detail in the next section.

Step4 (t3-t4): At time t3, V_C reaches the set level V_{refss}. At this time, the gain of loop2 becomes far larger than loop1, and the negative feedback operating point is determined by loop2. The inductor current of Boost is held at high level because I_{C2} dominates the charging speed of the capacitor C_{SS} and V_C is clamped to V_{refss} during Step4.

Step5 (t4-t5): To prevent the output voltage V_{OUT} of Boost from overshooting, the control of the V_C is released and return to normal level in advance when the V_{OUT} is close to the target value. At time t4, a fixed soft-start strategy is adopted to replace the previous adaptive soft-start, which uses a pulsed current charging the capacitor to avoid using an excessively large soft-start capacitor.

Step6 (t5-): The start-up is completed. At this time, the positive input of EA is switched from V_{soft} to the reference voltage V_{FB} by a low-voltage select circuit.

Based on current-limiting feedback techniques, some other soft-start effects can be designed. For example, if paying more attention to the start-up speed, the requirement of the V_C waveform is higher that V_C should be raise to the predefined value at the beginning rapidly. However, to break through the limit of the slew rate, an additional charging circuit is required.

A compensation for V_C should be added while considering the effect of slope compensation on the current-limit. V_C can compensate for this effect with a certain slope change to increase the speed of soft-start, but the complexity of the soft-start circuit will increase. This compensation can be calculated by (2) and (3):

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} = \frac{\frac{V_{FB}}{k} - V_{IN}}{\frac{V_{FB}}{k}} = 1 - k\frac{V_{IN}}{V_{FB}} \tag{2}$$

Substituting (2) in (1), it can be obtained:

$$V_C = V_S + M_S T R_S - k\frac{V_{IN}}{V_{FB}} T_S M_S \tag{3}$$

According to (3), it is difficult to design a voltage compensation circuit for V_C in circuit-level. Because a lot of extra circuits will be consumed to achieve the third item in equation (3) while the benefits are not obvious enough.

The scheme and process proposed in this paper is a comprehensive soft-start scheme for current-limiting feedback technique, which achieves a superior trade-off between consumption, performance and stability.

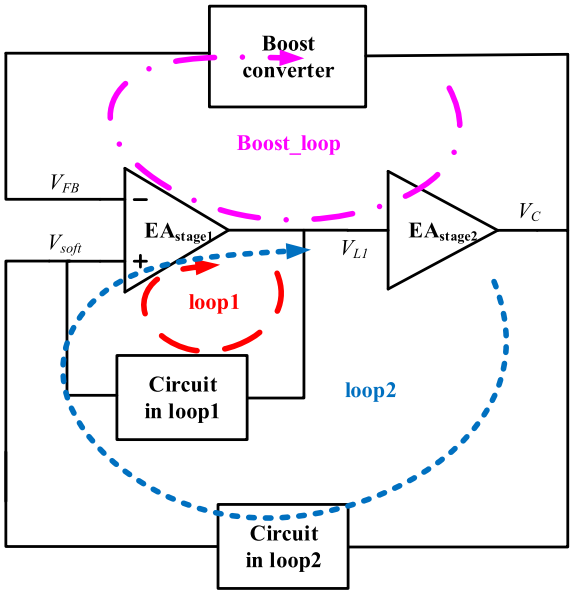

FIGURE 4. Diagram of the loops in the Boost converter with proposed soft-start circuit.

III. THE STABILITY OF THE SOFT-START CIRCUIT BASED ON CURRENT LIMIT FEEDBACK TECHNOLOGY IN DC-DC APPLICATION

A diagram of the loops in the Boost converter with the proposed soft-start circuit is shown in the Fig. 4. There are three negative feedback loops. The preliminary analysis of the loops is given as follow:

Loop1 and loop2 do not have a feedforward path that will not introduce a zero point in Boost_loop. In this application, loop1, loop2 and Boost loop are in turn to be the dominant loop during the start-up period. When a circuit is in multiple negative feedback loops simultaneously, the DC operating point of this circuit, such as V_{soft}, V_{FB}, V_{L1} and V_C is determined by the dominant loop.

In Step3, loop1 is set as the dominant loop to ensure that the rising speed of V_{soft} is limited by the slew rate of EA.

In Step4, loop2 is set as the dominant loop to clamp V_C close to V_{refss}. After start-up, loop1 and loop2 are shielded by the enable signal *EN1*.

A. THE ANALYSIS OF COMMON DOUBLE-LOOP STRUCTURE

It is necessary to analyze the feedback situation and stability of the loops in the key steps, such as Step3 and Step4. In Step3, Boost_loop would influence the performance and stability of loop1, and in Step4, loop1 would influence the performance and stability of loop2.

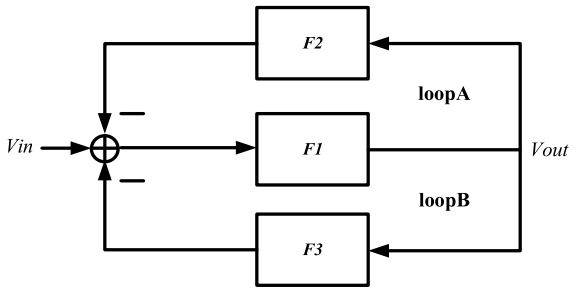

FIGURE 5. Schematic diagram of a double loop negative feedback structure.

To discuss these cases, the double-loop structure with loopA and loopB is taken as an example in Fig. 5. The negative feedback and stability of the double-loop are analyzed here.

$$LG_A = F1 \cdot F2 \tag{4}$$

$$LG_B = F1 \cdot F3 \tag{5}$$

$$\left(\frac{V_{OUT}}{V_{IN}}\right)_{close} = \frac{F1}{1 + LG_A + LG_B} \tag{6}$$

where LG_A and LG_B are the loop gains of loopA and loopB as single loop, respectively. From the closed-loop transfer function of the double-loop, it can be concluded that the negative feedback operating point is dominated by the larger one of the low frequency gain of LG_A and LG_B, and the stability is determined by the larger bandwidth of LG_A and LG_B.

Therefore, the loop gain of the dominant loop is designed larger than the nondominant loop in low frequency gain. For example, if loopB is designed to dominate the negative feedback, LG_B need to be larger than LG_A in low frequency gain. Then, in loopA and loopB:

$$\left(\frac{V_{OUT}}{V_{IN}}\right)_{loopA\_close} = \frac{F1}{1 + LG_A} \tag{7}$$

$$LG_{loopB} = \left(\frac{V_{OUT}}{V_{IN}}\right)_{loopA\_close} \times F3 = \frac{LG_B}{1+LG_A} \tag{8}$$

$$\left(\frac{V_{OUT}}{V_{IN}}\right)_{loopB\_close} = \frac{F1}{1 + LG_B} \tag{9}$$

$$LG_{loopA} = \left(\frac{V_{OUT}}{V_{IN}}\right)_{loopB\_close} \times F2 = \frac{LG_A}{1+LG_B} \tag{10}$$

If assume $GBW_{LGB} >> GBW_{LGA}$ in (8) and (9), loopA is stable since LG_{loopA} is always smaller than 1. Meanwhile, (8) can be simplified as follow:

$$LG_{loopB}\big|_{f \to GBW} \approx LG_B \tag{11}$$

Thus, the stability of loopB can be determined by the GBW of loopB itself.

It can be concluded that loopB should be larger than loopA in both low frequency gain and bandwidth if loopB is designed to dominate negative feedback in the multi-loop structure. This conclusion can be used to analyze the multi-loop problem of the proposed soft-start circuit.

B. LOOP1 AND BOOST_LOOP EXIST AT THE SAME TIME

In Step3, loop2 is deviates from the high gain operating point and there is no small signal path in loop2. During this time, loop2 only provide a quiescent current for loop1. So the multi-loop system can be simplified as a double loop system consists of loop1 and Boost_loop. To ensure loop1 as the dominant loop, the bandwidth and low frequency gain of loop1 is designed much larger than Boost_loop. Thus, the soft-start circuit can be simplified to Fig. 6.

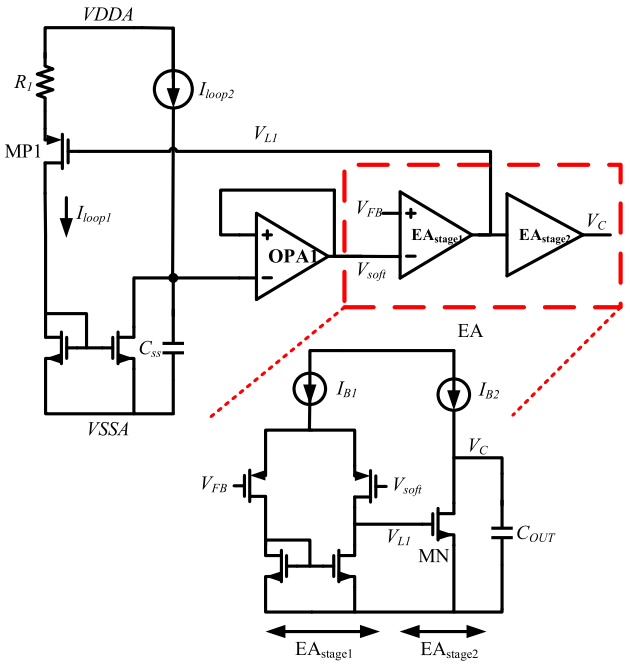

FIGURE 6. The equivalent circuit of soft-start circuit during step3.

In Fig. 6, a simple secondary op amp is used as an example to simplify the problem. EA_{stage1} is a differential amplifier as the first stage of EA, and EA_{stage2} is a common source amplifier as the second stage of EA. When the EA reaches the maximum slew rate, the MN is just turn off. At this time, I_{loop1} can be expressed as:

$$I_{loop1} = \frac{V_{L1} - V_{thp1}}{R_1} \tag{12}$$

$$I_{loop2} = \frac{VDDA - V_{thp2}}{R_2} \tag{13}$$

When the negative feedback is stable, there is

$$I_{loop1} = I_{loop2} \tag{14}$$

By setting the values of R_1 and R_2, V_{L1} equals to V_{thn} can be ensured. Because loop1 dominates the negative feedback, V_C rises according to the maximum slew rate of EA, and V_{soft} is also controlled within the appropriate range in Step3. Here is just a specific solution for the sample of EA, the parameters of loop1 can be designed according to this method when EA is different.

In Step3, the bandwidth and low frequency gain of loop1 is designed to be much larger than Boost_loop. During the start-up period, the loop gain of the Boost_loop is reduced and the *GBW* of it is designed to be around 10kHz. Thus, as shown in Fig. 7, the low frequency gain and the GBW of loop1 is designed as 45dB and 74kHz, respectively.

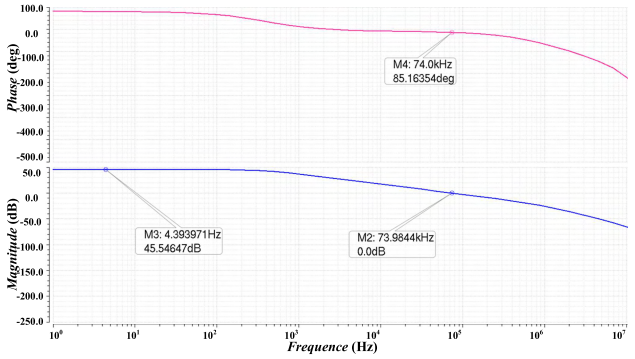

FIGURE 7. The loop response simulation of loop1.

C. LOOP1 AND LOOP2 EXIST AT THE SAME TIME

In Step4, to set loop2 as the dominant loop, the bandwidth and low frequency gain of loop2 is designed to be much larger than that of loop1. When this condition is reached, the bandwidth and low frequency gain of loop2 are also much larger than Boost_loop. Thus, loop2 dominates the negative feedback that the effects of loop1 and Boost_loop can be ignored. Then the circuit can be simplified as Fig. 8.

As shown in Fig. 8 OPA2 amplify the error of V_{refss} and V_C, then output to the gate of MP1 to control the charging speed of the capacitor C_{SS}. When V_C is higher than V_{refss}, the charging current I_2 decreases, the rise speed of V_{soft} becomes slower, and the difference between V_{FB} and V_{soft} becomes smaller, V_C decreases. Similarly, when V_C is lower than V_{refss}, the charging current I_2 increases, V_{soft} rises faster. Further, the difference between V_{FB} and V_{soft} becomes larger, V_C increases. Eventually the negative feedback loop clamps the V_C at a preset level V_{refss}.

In Step4, the bandwidth and low frequency gain of loop2 is required to be much larger than loop1. Since the low frequency gain and *GBW* of loop1 is 45dB and 74KHz, respectively. The low frequency gain of loop2 is designed to 87.7 dB and the *GBW* of loop2 is designed to 406.5kHz as shown in Fig. 9.

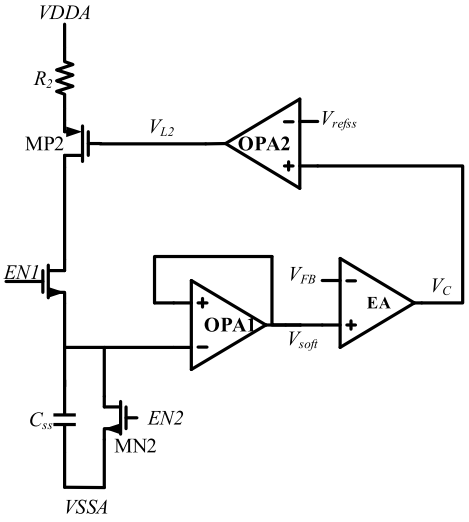

FIGURE 8. The equivalent circuit of soft-start circuit during step4.

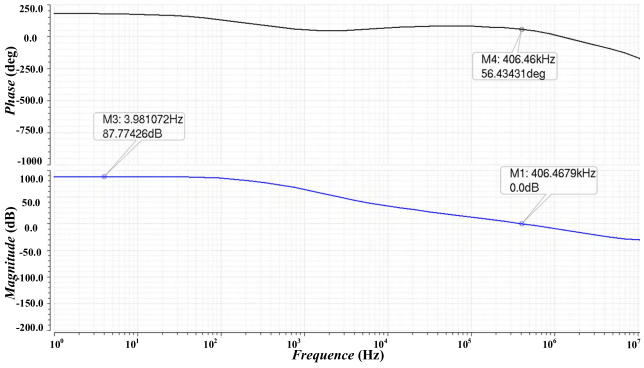

FIGURE 9. The loop response simulation of loop2.

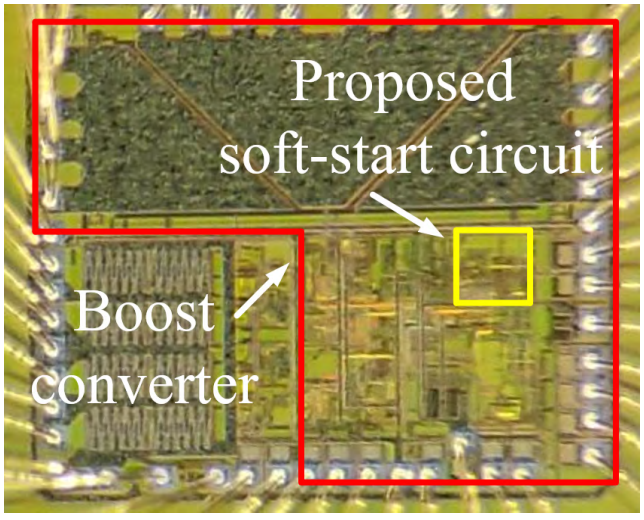

FIGURE 10. Chip micrograph.

IV. EXPERIMENTAL RESULTS

As part of a Boost converter for motor driver applications, the proposed soft-start circuit is fabricated in a 0.35μm 60V BCD process. The micrograph of the Boost converter and is shown in Fig. 10. Including the on-chip capacitance, the soft-start circuit occupies an area of 0.02 mm^2.

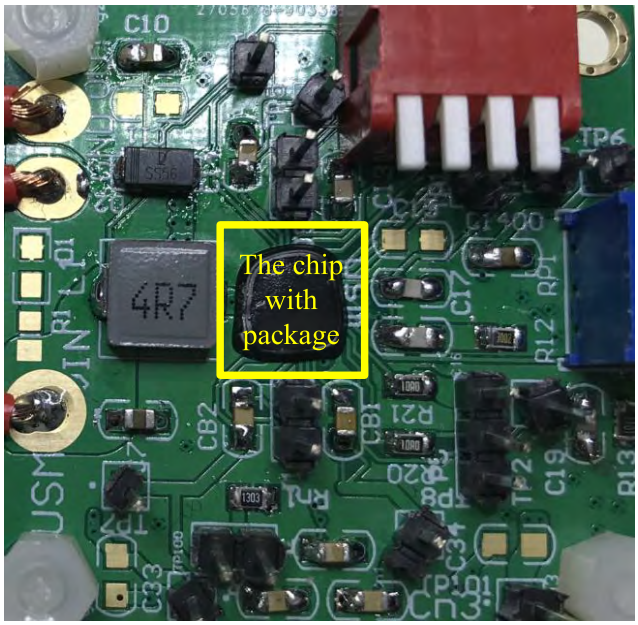

FIGURE 11. Picture of the PCB.

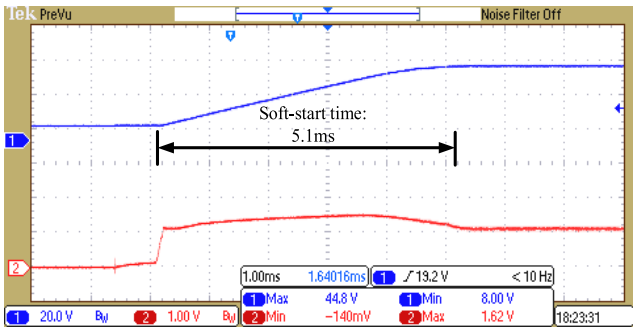

FIGURE 12. Experimental result of start-up with traditional fixed ramp soft-start circuit ($C_O = 20\mu$F, $I_{load} = 50$mA, $V_{OUT} = 45$V).

A test PCB is designed to verify the performance of the proposed soft-start circuit as shown in Fig. 11. In this motor driver application, the input voltage and the output voltage of the Boost converter are 12V and 45V, respectively. The range of the load current is 0-500mA. The capacitor is chosen as 20μF and the inductor is 4.7μH. An off-chip Schottky diode is selected as DO-214AB-SS56. The output voltage of Boost converter reaches 45V. In order to achieve better driving performance, a faster soft-start speed is required. Fig. 12-14 show the experimental results.

With traditional fixed ramp soft-start circuit, the start-up time of Boost is 5.1ms. Compared with traditional fixed ramp soft-start circuit, the start-up with the proposed soft-start circuit lasts only 330μs under the same condition. The experimental results in Fig. 13-14 show that the output waveform of EA meets the theoretical control effect shown in Fig. 2, which allows the inductor current rising quickly to the preset range and remains until the end of the soft-start. As shown in Fig. 14, after the chip is enabled, the output voltage of Boost ramps up to 45 V in 380μs while $I_{load} = 500$mA.

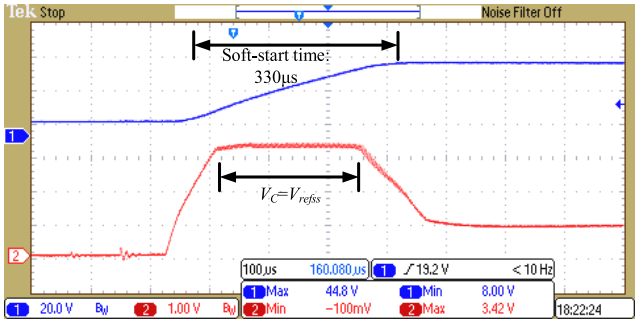

FIGURE 13. Experimental result of start-up with proposed soft-start circuit ($C_O = 20\mu$F, $I_{load} = 50$mA, $V_{OUT} = 45$V).

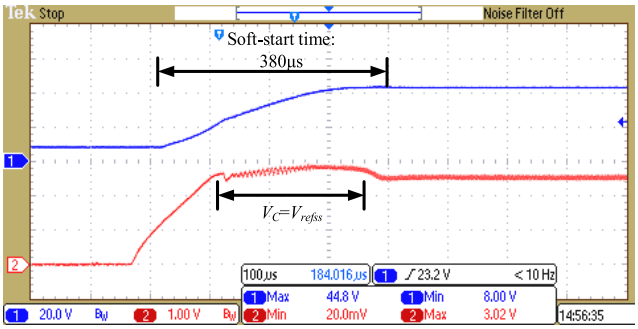

FIGURE 14. Experimental result of start-up with proposed soft-start circuit ($C_O = 20\mu$F, $I_{load} = 500$mA, $V_{OUT} = 45$V).

TABLE 1. Parameters comparison.

parameter	2009'[17] TCAS:II	2013'[18] VLSI	2016'[19] PE	This work
process (µm)	0.35µm CMOS	0.5µm CMOS	Implemented in PCB	0.35µm BCD
Silicon area (mm^2)	0.026	0.042	-	**0.02**
Soft-start time (µs)	600	600	1500	**380**
Soft-start voltage (V)	5	1.8	18	**45**
Load current(mA)	--	2000	120	500
Soft-start capacitor (pF)	5	15	Off-chip	**5**
Output capacitor(µF)	10	10	4.7	**20**

The key parameters in this work and the comparison with prior literatures [17]–[19] are listed in Table 1. Due to the focus on soft-start stability or the avoidance of off-chip capacitors, these literatures cannot achieve the balance between start-up speed and other parameters. In case of higher output voltage and smaller silicon area, the proposed circuit in this paper achieves a faster start-up than that of these papers.

V. SUMMARY

In this paper, a novel soft-start circuit for current mode DC-DC with controllable start-up time, high-speed start-up, high stability, and no off-chip capacitor is proposed. To achieve faster start-up speed, the current-limiting feedback

technique is adopted to ensure the inductor current under control during soft-start period. Meanwhile, the stability of proposed soft-start technique is theoretical proofed in this paper. As a part of a Boost converter for motor driver applications, the proposed soft-start circuit can achieve 380μs start-up time in case of 45V output voltage as shown in experimental results. The proposed soft-start technique is feasible to implement in current mode DC-DC converter and achieves high-speed soft-start with high start-up stability.

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LONG HUANG was born in Guangxi, China, in 1994. He received the B.S. degree from the University of Electronic Science and Technology of China, where he is currently pursuing the M.E. degree in microelectronics and solid-state electronics. His research interests include DC-DC converter, motor driver, and power management unit.

PING LUO was born in Xinjiang, China, in 1968. She received the B.S. and M.S. degrees from Chongqing University, and the Ph.D. degree from the University of Electronic Science and Technology of China, where she is currently a Professor. Her research interests include DC-DC converter, power management unit, energy harvest IC, and energy management strategies.

CHENYANG WANG was born in Hubei, China, in 1995. He received the B.S. degree from the University of Electronic Science and Technology of China, where he is currently pursuing the M.E. degree in microelectronics and solid-state electronics. His research interests include DC-DC converter and power management unit.

XIANLI ZHOU was born in Sichuang, China, in 1996. He received the B.S. degree from the University of Electronic Science and Technology of China, where he is currently pursuing the M.E. degree in microelectronics and solid-state electronics. His research interests include DC-DC converter and power management unit.