IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received November 3, 2018, accepted December 2, 2018, date of publication February 26, 2019, date of current version March 7, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2890872

Optimal Design of a New Cascaded Multilevel Inverter Topology With Reduced Switch Count

MARIF DAULA SIDDIQUE[1], (Student Member, IEEE), SAAD MEKHILEF[1,2], (Senior Member, IEEE), NORAISYAH MOHAMED SHAH[1], AND MUDASIR AHMED MEMON[1]

[1]Power Electronics and Renewable Energy Research Laboratory, Department of Electrical Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia
[2]Center of Research Excellence in Renewable Energy and Power Systems, King Abdulaziz University, Jeddah 21589, Saudi Arabia

Corresponding author: Saad Mekhilef (saad@um.edu.my)

This work was supported in part by the University of Malaya, Malaysia, through FRGS under Grant FRGS/1/2018/TK07/UM/01/3, in part by Frontier Research under Grant FG007-17AFR, in part by BKP under Grant BK052-2016, and in part by Postgraduate Research (PPP) under Grant PG192-2015B.

ABSTRACT Multilevel inverters (MLIs) are a great development for industrial and renewable energy applications due to their dominance over conventional two-level inverter with respect to size, rating of switches, filter requirement, and efficiency. A new single-phase cascaded MLI topology is suggested in this paper. The proposed MLI topology is designed with the aim of reducing the number of switches and the number of dc voltage sources with modularity while having a higher number of levels at the output. For the determination of the magnitude of dc voltage sources and a number of levels in the cascade connection, three different algorithms are proposed. The optimization of the proposed topology is aimed at achieving a higher number of levels while minimizing other parameters. A detailed comparison is made with other comparable MLI topologies to prove the superiority of the proposed structure. A selective harmonic elimination pulse width modulation technique is used to produce the pulses for the switches to achieve high-quality voltage at the output. Finally, the experimental results are provided for the basic unit with 11 levels and for cascading of two such units to achieve 71 levels at the output.

INDEX TERMS Basic unit, cascaded inverter, multilevel inverter (MLI), selective harmonic elimination, SHEPWM, optimization, reduce switch count.

I. INTRODUCTION

Multilevel inverters are among the most used power conversion devices in industrial applications. These applications mostly comprise of the motor drives for the entire voltage and power ratings. Multilevel inverters (MLIs) are also finding their applications in the grid-connected systems, uninterruptible power supply (UPS), electric vehicles and FACTS devices. All these applications are possible due to the ability of the MLI to provide a better output voltage with a more sinusoidal shaped waveform, improved efficiency due to the lower switching frequency operation of switches, lower blocking voltage requirement with reduced *dv/dt* and improved electromagnetic compatibility. Another positive impact of MLI is the reduction of the filter size and cost due to the reduced amount of harmonics at the output [1]–[7].

The conventional multilevel inverter topologies for the industrial application include neutral point clamped (NPC) MLI, flying capacitor (FC) MLI, cascade H-bridge (CHB) MLI, T-type MLI and modular multilevel converters (MMC). These MLI topologies have found their applications with different power and voltage ratings, along with their unique benefits as well as shortcomings. These shortcomings include the higher number of components for a higher number of levels along with capacitor voltage balancing problems. In order to overcome these drawbacks, several new topologies for the multilevel inverter and their control have been introduced in [8]–[10].

The main driving force for the design of new multilevel inverter topologies has been the reduction of the number of switches, number of dc voltage sources, and total standing voltage (TSV) of the topology. Based on these constraints, several topologies with reduced switch count have been proposed in the literature, such as in [11]–[14]. All of them have used H-bridge in order to generate the positive and negative polarities of the output voltage waveform. However, the switches of H-bridge need to block maximum/peak output

voltage, which limits their applications in high voltage. This problem has been solved in E-type [15] and ST-type [16] where the topologies inherently generate both positive and negative levels without using H-bridge. E-type and ST-type topologies use four dc voltage sources to generate 13 and 17 levels at the output by means of 10 and 12 power semiconductor switches respectively. An improved topology has been presented in [17] which generates 25 levels with four dc voltage sources. The main problem with [17] is the use of the diodes, which reduces efficiency.

Several cascaded MLI topologies have been proposed in [18]–[28] based on the basic units. A basic unit developed with the H-bridge has been proposed in [18]. It consists of two dc voltage source with six switches to generate seven levels at the output. A similar topology has been proposed in [19] in which both dc voltage sources in [18] has been replaced by the T-type module having two dc voltage sources and one bidirectional switch. This modification results in 17 levels at the output. In [20], both topologies presented in [18] and [19] has been combined and an improved sub multilevel converter has been proposed. Another topology based on [18] has been proposed in [21] with a reduced number of switches. The basic unit of [21] produces 17 levels with four dc voltage sources and 12 switches. The topologies presented in [18]–[25] can be connected in cascade to achieve a higher number of levels at the output.

The optimal design of cascaded MLI has been another important aspect. The optimal selection of number of cascaded units has been presented in several topologies [19]–[21]. These optimizations of the topology deal with the optimal selection of number of cascaded modules such that higher number of levels are achieved at the output while minimizing the number of switches, driver circuits and dc voltage sources. In this paper, an optimal design cascaded multilevel inverter topology is proposed, which is able to generate a higher number of levels with reduced number of switches. An additional factor has been the variety of dc voltage sources which is reduced in the proposed topology.

The paper is organized as follows: the analysis and description of the proposed basic unit with its generalized structure is presented in Section II. The analysis covers the magnitude selection of dc voltage sources along with total standing voltage (TSV) calculations. Section III elaborates the cascade connection of the proposed topology, and optimization of the cascade connection is given in Section IV. Section V provides a detailed comparison of the proposed topology with existing ones. Section VI deals with the selective harmonic elimination modulation technique. Simulation and experimental results are provided in Section VII followed by the conclusion in Section VIII.

II. ANALYSIS AND DESCRIPTION OF PROPOSED MULTILEVEL TOPOLOGY

A. BASIC UNIT OF PROPOSED TOPOLOGY

Fig. 1 shows the basic unit of the suggested multilevel inverter topology. The assembly consists of three dc voltage sources

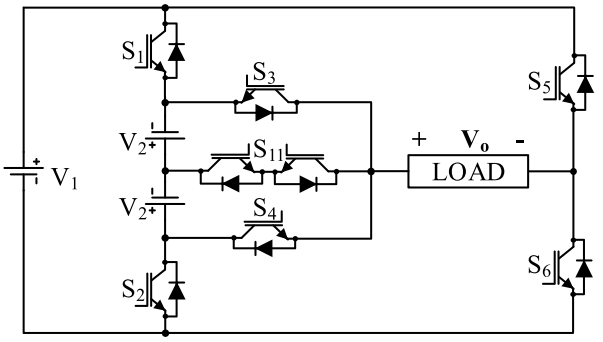

FIGURE 1. Basic unit of the proposed topology.

TABLE 1. Switching table of the proposed basic unit.

S_1	S_2	S_3	S_4	S_5	S_6	S_{11}	V_o
ON	OFF	ON	OFF	ON	OFF	OFF	0
ON	OFF	ON	OFF	OFF	ON	OFF	V_1
ON	OFF	OFF	OFF	ON	OFF	ON	V_2
ON	OFF	OFF	OFF	OFF	ON	ON	V_1+V_2
ON	OFF	OFF	ON	ON	OFF	OFF	$2V_2$
ON	OFF	OFF	ON	OFF	ON	OFF	V_1+2V_2
OFF	ON	OFF	ON	OFF	ON	OFF	0
OFF	ON	OFF	ON	ON	OFF	OFF	$-V_1$
OFF	ON	OFF	OFF	OFF	ON	ON	$-V_2$
OFF	ON	OFF	OFF	ON	OFF	ON	$-(V_1+V_2)$
OFF	ON	ON	OFF	OFF	ON	OFF	$-2V_2$
OFF	ON	ON	OFF	ON	OFF	OFF	$-(V_1+2V_2)$

along with six unidirectional switches and one bidirectional switch. Switch pair (S_1, S_2) and (S_5, S_6) can be termed as outer switches, and only one switch is necessary to be turned ON from each pair. The switches of outer pairs should also operate in a complementary mode to avoid short-circuiting the dc voltage sources. These outer switches are connected across voltage source V_1. The remaining two dc voltage sources with V_2 magnitude are connected in series with additive polarity, along with unidirectional switches S_3, S_4 and bidirectional switch S_{11} forms the inner portion of the proposed basic unit. Only one switch is required to be turned ON in between these three switches. Considering these facts, the switching table for the proposed basic unit is given in Table 1.

B. GENERALIZED STRUCTURE OF PROPOSED TOPOLOGY

The proposed basic unit is able to achieve 11 levels at the output employing three dc voltage sources. In order to generate more number of levels, the basic unit can be extended as shown in Fig. 2. In this extension, the number of dc voltage sources, which is connected to the inner portion of the module, is increased along with bidirectional switches. The switches used in the proposed topology can be grouped into three cells. Cell 1 is made up of switches S_1 and S_2. Switches in cell 1 are operated at fundamental frequency as both have

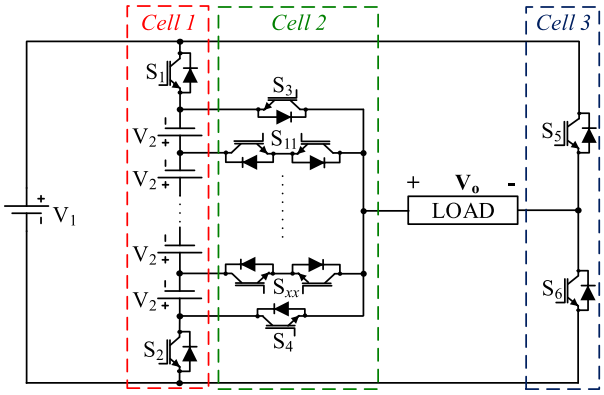

FIGURE 2. Generalized structure of the proposed topology.

to bear maximum voltage stress. Cell 2 consist of all the inner switches and each switch turns ON for any two levels in the one-half cycle. Similarly, cell 3 consist of two switches S_5 and S_6 and both of them operate at a high frequency.

The generalized equations for the proposed topology with k number of dc voltage sources are given as:

$$Maximum\ number\ of\ Levels = N = 4k - 1 \quad (1)$$

$$Number\ of\ Switches = N_{switch} = 2k + 2 \quad (2)$$

$$Number\ of\ Driver\ Circuits = N_{driver} = k + 4 \quad (3)$$

$$Peak\ Output\ Voltage = V_{o,max} = V_1 + (k-1)\,V_2 \quad (4)$$

$$Variety\ of\ dc\ sources = N_{variety} = 2 \quad (5)$$

C. SELECTION OF MAGNITUDE OF DC VOLTAGE SOURCES

The selection of dc voltage sources used in the proposed topology is an important criterion for practical applications. One such benchmark is the variety of dc voltage sources i.e. how many different magnitudes of dc voltage sources are employed in the topology. For the proposed topology, only two different magnitudes of dc voltage sources are required. Another important aspect related to dc voltage sources is their magnitude selection. For the proposed topology, the peak output voltage of the proposed topology is given in (6).

$$V_{o,max} = V_1 + (k-1)\,V_2 = \left(\frac{N-1}{2}\right) \times V_{dc} \quad (6)$$

For the generalized structure, the selection of dc voltage sources can be done in two modes. In MODE I, the magnitude of V_1 is selected as V_{dc}. Then from (1) and (6), the magnitude of V_2 is calculated as

$$V_2 = 2V_{dc} \quad (7)$$

Similarly, in MODE II, the magnitude of V_2 is fixed as V_{dc}. Then the magnitude of V_1 from (1) and (6) is

$$V_1 = \frac{N - 2k + 1}{2} V_{dc} = kV_{dc} \quad (8)$$

The magnitude of dc voltage sources in MODE I is fixed as $V_1 = V_{dc}$ and $V_2 = 2V_{dc}$ irrespective of the number of dc voltage sources, whereas for MODE II, the magnitude of V_1 is depend on k. Therefore, with a higher number of dc voltage sources, the magnitude selection of dc voltage sources in MODE II becomes impractical. Fig. 3 shows all the voltage states in a positive half cycle of the basic unit with voltage sources configured in MODE I.

D. CALCULATION OF TSV

The voltage stress across each switch plays a significant role in determining the cost and efficiency of an MLI. For this purpose, total standing voltage (TSV) is considered as a key parameter [16]. TSV is defined as the sum of maximum voltage stress across each switch considering each level at the output. For the proposed topology, TSV can be expressed as:

$$TSV = TSV_{Cell1} + TSV_{Cell2} + TSV_{Cell3} \quad (9)$$

where TSV_{Cell1}, TSV_{Cell2}, and TSV_{Cell3} are the TSV of cell 1, 2, and 3 respectively. All these values are given as

$$TSV_{Cell1} = 2\,[V_1 + (k-1)\,V_2] \quad (10)$$

$$TSV_{Cell2} = M \times V_2 \quad (11)$$

The value of M can be calculated as follows:

$$\left.\begin{aligned} M &= \frac{3k^2 - 2k - 1}{4} \quad \text{for odd number of } k \\ M &= \frac{3k^2 - 2k}{4} \quad \text{for even number of } k \end{aligned}\right\} \quad (12)$$

Similarly, for cell 3

$$TSV_{Cell3} = 2V_1 \quad (13)$$

Therefore, from (9) – (13)

$$TSV = 4V_1 + (M + 2k - 2)\,V_2 \quad (14)$$

III. CASCADE CONNECTION OF PROPOSED TOPOLOGY

Cascading several modules is another way to increase the number of levels at the output. Fig. 4 shows the cascade connection of the proposed topology with m modules. The output voltage across the load is the sum of all the voltages generated by each module connected in cascade, i.e.,

$$V_o = V_{o1} + V_{o2} + \ldots + V_{om} \quad (15)$$

In order to maintain the modulatory, each module connected in cascade is assumed to be identical i.e. each module has the same number of switches and dc voltage sources. The equations for the proposed topology with m modules in cascade, and with k number of dc voltage sources in each module are given as:

$$N_{switch} = m \times (2k + 2) \quad (16)$$

$$N_{driver} = m \times (k + 4) \quad (17)$$

$$N_{source} = m \times k \quad (18)$$

The number of output levels for the cascade connection depends on the magnitude of dc voltage sources in each module. The magnitude of dc voltage sources of each module can be selected by three different algorithms, described as follows.

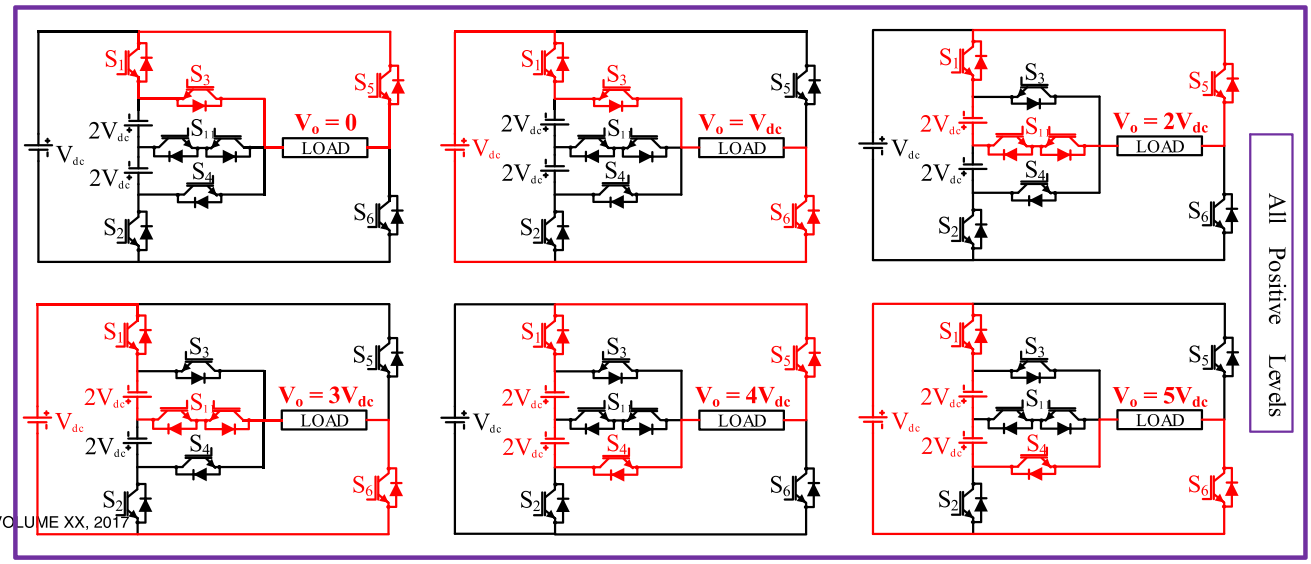

FIGURE 3. Different switching states of the proposed basic unit with MODE I in positive half cycle.

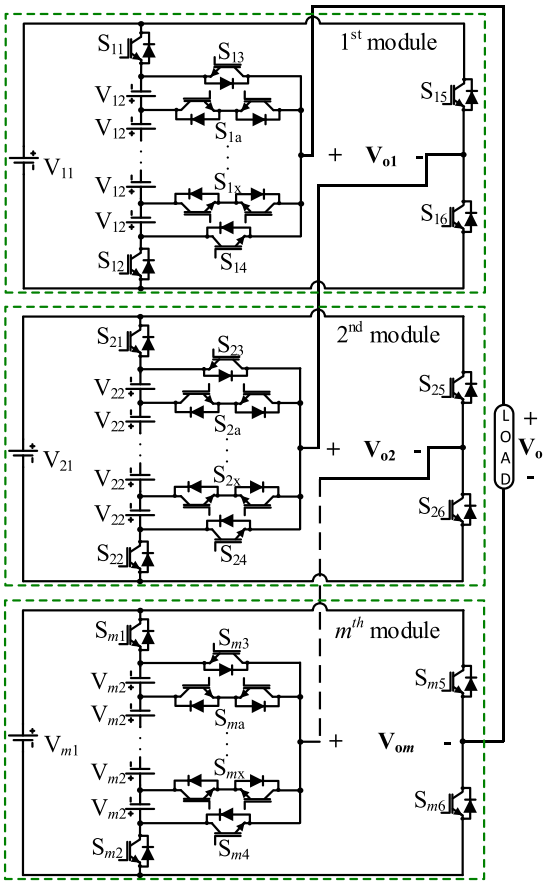

FIGURE 4. Cascade connection of proposed MLI.

A. FIRST ALGORITHM (FA)

In this algorithm, the magnitude of dc voltage sources associated with the individual module is the same. The magnitude selection can be done based on either MODE I or MODE II.

In MODE I,

$$V_{11} = V_{21} = V_{m1} = V_{dc} \tag{19}$$
$$V_{12} = V_{22} = V_{m2} = 2V_{dc} \tag{20}$$

In MODE II,

$$V_{11} = V_{12} = V_{m1} = kV_{dc} \tag{21}$$
$$V_{21} = V_{22} = V_{m2} = V_{dc} \tag{22}$$

In both modes, the number of levels from the first algorithm $N_{level,F}$ at the output is given by:

$$N_{level,F} = [\{m \times (4k-2)\} + 1] \tag{23}$$
$$Variety\ of\ dc\ sources = N_{variety} = 2 \tag{24}$$

B. SECOND ALGORITHM (SA)

In this algorithm, the magnitude of the first module is the same as that of the first algorithm, but for other modules, the selection is made according to the following equations for both modes.

For the 1st module:

In MODE I,

$$V_{11} = V_{dc} \tag{25}$$
$$V_{12} = 2V_{dc} \tag{26}$$

In MODE II,

$$V_{11} = kV_{dc} \tag{27}$$
$$V_{12} = V_{dc} \tag{28}$$

The maximum/peak output voltage of the 1st module is given by:

$$V_{o1,max} = V_{11} + (k-1)\,V_{12} \tag{29}$$

For the 2nd module:

In MODE I,

$$V_{21} = (V_{o1,max} + V_{dc}) \quad (30)$$
$$V_{22} = 2 \times (V_{o1,max} + V_{dc}) \quad (31)$$

In MODE II,

$$V_{21} = k \times (V_{o1,max} + V_{dc}) \quad (32)$$
$$V_{22} = (V_{o1,max} + V_{dc}) \quad (33)$$

The maximum/peak output voltage of the 2nd module is given by:

$$V_{o2,max} = V_{21} + (k-1)\, V_{22} = (2k-1) \times (V_{o1,max} + V_{dc}) \quad (34)$$

Similarly, for the m^{th} module:

In MODE I,

$$V_{m1} = (V_{o(m-1),max} + V_{o(m-2),max} + V_{dc}) \quad (35)$$
$$V_{m2} = 2 \times (V_{o(m-1),max} + V_{o(m-2),max} + V_{dc}) \quad (36)$$

In MODE II,

$$V_{m1} = k \times (V_{o(m-1),max} + V_{o(m-2),max} + V_{dc}) \quad (37)$$
$$V_{m2} = (V_{o(m-1),max} + V_{o(m-2),max} + V_{dc}) \quad (38)$$

The maximum/peak output voltage of the m^{th} module is given by:

$$V_{om,max} = (2k-1) \times (V_{o(m-1),max} + V_{o(m-2),max} + V_{dc}) \quad (39)$$

where $V_{o(m-1),max}$ and $V_{o(m-2),max}$ represent the peak output voltage of $(m\text{-}1)^{th}$ and $(m\text{-}2)^{th}$ modules connected in cascade, respectively. In both modes, the number of levels from the second algorithm $N_{level,S}$ at the output is given by

$$N_{level,S} = \frac{2\left(V_{o1,max} + V_{o2,max} + \ldots + V_{om,max}\right)}{V_{dc}} + 1$$
$$N_{level,S} = 2 \times (2k)^m - 1 \quad (40)$$
$$Variety\ of\ dc\ sources = N_{variety} = 2m \quad (41)$$

C. THIRD ALGORITHM (TA)

In this algorithm, the magnitude of the first module is same as that of the first algorithm but for other modules, the selection is decided according to the following equations in both modes.

For the 1st module:

In MODE I,

$$V_{11} = V_{dc} \quad (42)$$
$$V_{12} = 2V_{dc} \quad (43)$$

In MODE II,

$$V_{11} = kV_{dc} \quad (44)$$
$$V_{12} = V_{dc} \quad (45)$$

The maximum/peak output voltage of the 1st module is given by:

$$V_{o1,max} = V_{11} + (k-1)\, V_{12} \quad (46)$$

For the 2nd module:

In MODE I,

$$V_{21} = (2V_{o1,max} + V_{dc}) \quad (47)$$
$$V_{22} = 2 \times (2V_{o1,max} + V_{dc}) \quad (48)$$

In MODE II,

$$V_{21} = k \times (2V_{o1,max} + V_{dc}) \quad (49)$$
$$V_{22} = (2V_{o1,max} + V_{dc}) \quad (50)$$

The maximum/peak output voltage of the 2nd module is given by:

$$V_{o2,max} = V_{21} + (k-1)\, V_{22} = (2k-1) \times (2V_{o1,max} + V_{dc}) \quad (51)$$

Similarly, for the m^{th} module:

In MODE I,

$$V_{m1} = (2V_{o1,max} + 2V_{o2,max} + \ldots + 2V_{o(m-1),max} + V_{dc}) \quad (52)$$
$$V_{m2} = 2 \times (2V_{o1,max} + 2V_{o2,max} + \ldots + 2V_{o(m-1),max} + V_{dc}) \quad (53)$$

In MODE II,

$$V_{m1} = k \times (2V_{o1,max} + 2V_{o2,max} + \ldots + 2V_{o(m-1),max} + V_{dc}) \quad (54)$$
$$V_{m2} = (2V_{o1,max} + 2V_{o2,max} + \ldots + 2V_{o(m-1),max} + V_{dc}) \quad (55)$$

The maximum/peak output voltage of the m^{th} module is given by:

$$V_{om,max} = (2k-1) \times (2V_{o1,max} + \ldots + 2V_{o(m-1),max} + V_{dc}) \quad (56)$$

where $V_{o(m-1),max}$ represents the peak output voltage of $(m\text{-}1)^{th}$ module connected in cascade. In both mode of operation, the number of levels with the third algorithm $N_{level,T}$ at the output is given by:

$$N_{level,T} = (4k-1)^m \quad (57)$$
$$Variety\ of\ dc\ sources = N_{variety} = 2m \quad (58)$$

IV. OPTIMIZATION OF THE PROPOSED TOPOLOGY IN CASCADE CONNECTION

The optimization analysis of the proposed cascaded MLI in all three algorithms is presented in this section. The optimization of a topology is helpful to minimize the number of switches, number of driver circuit and number of dc voltage sources required in order to generate a higher number of levels at the output. Five different aspects of optimization is considered for the proposed topology and are discussed below.

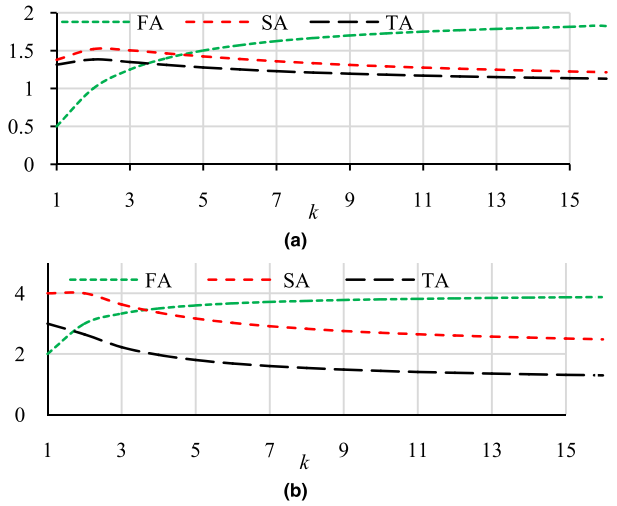

FIGURE 5. Curves related to optimization for (a) constant number of switches and (b) constant number of dc voltage sources for maximum number of level generation.

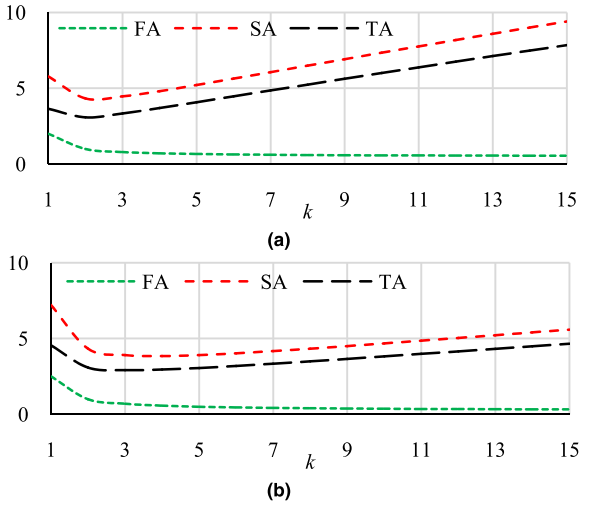

FIGURE 6. Curves related to optimization for (a) minimization of switches and (b) minimization of driver circuit with constant number of levels.

A. OPTIMIZATION OF THE PROPOSED MLI WITH A CONSTANT NUMBER OF SWITCHES FOR A MAXIMUM NUMBER OF LEVELS

In this section, the number of switches is made constant and the number of the dc voltage source in each module is varied in order to generate the maximum number of levels at the output. From (16):

$$m = \frac{N_{switches}}{(2k+2)} \tag{59}$$

From (23), (40), (57), and (59),

$$N_{level,F} = N_{Switches} \times \frac{4k-2}{2k+2} + 1 \tag{60}$$

$$N_{level,S} = 2 \times (2k)^{\left(\frac{N_{Switch}}{2k+2}\right)} - 1 \tag{61}$$

$$N_{level,T} = (4k-1)^{\left(\frac{N_{Switch}}{2k+2}\right)} \tag{62}$$

As $N_{Switches}$ is constant in (60)-(62), the terms $\frac{4k-2}{2k+2}$, $(2k)^{\left(\frac{1}{2k+2}\right)}$, and $(4k-1)^{\left(\frac{1}{2k+2}\right)}$ should be maximum in order to achieve more number of levels at the output with the optimized structure of the proposed topology. Fig. 5 (a) shows the variation of all these terms with respect to the number of dc voltage sources k. As indicated by Fig. 5 (a), the proposed topology is optimized with $k = \infty$ for the first algorithm, with $k = 2$ for the second algorithm and with $k = 3$ for the third algorithm.

B. OPTIMIZATION OF PROPOSED MLI WITH A CONSTANT NUMBER OF DC VOLTAGE SOURCES FOR A MAXIMUM NUMBER OF LEVELS

In this optimization, the number of dc voltage sources is made constant and the variation of k is observed in order to generate the maximum number of levels at the output. This optimization decides the value of k for which the proposed cascade MLI generates a maximum number of levels for all three algorithms. From (20):

$$m = \frac{N_{sources}}{k} \tag{63}$$

From (25), (42), (59), and (63),

$$N_{level,F} = N_{sources} \times \frac{4k-2}{k} + 1 \tag{64}$$

$$N_{level,S} = 2 \times (2k)^{\left(\frac{N_{sources}}{k}\right)} - 1 \tag{65}$$

$$N_{level,T} = (4k-1)^{\left(\frac{N_{sources}}{k}\right)} \tag{66}$$

Fig. 5 (b) shows the variation of the number of levels with k and constant $N_{sources}$. The number of levels is maximized as the terms associated with (64)-(66) i.e. $\frac{4k-2}{k}$, $2\times(2k)^{\left(\frac{1}{k}\right)}$, and $(4k-1)^{\left(\frac{1}{k}\right)}$ attain their maximum value. For FA, the topology is optimized with $k = \infty$. Similarly, from Fig. 5 (b), the proposed structure is optimized in the second and third algorithm with $k = 2$.

C. MINIMIZING THE NUMBER OF SWITCHES WITH CONSTANT NUMBER OF LEVELS

In this section, the topology is optimized with a constant number of levels and a minimum number of switches. Using (60)-(62) the equations for the number of switches with a constant number of levels for the three algorithms are given as:

$$N_{switches,F} = (N_{level,F} - 1) \times \frac{2k+2}{4k-2} \tag{67}$$

$$N_{switches,S} = \ln\left(\frac{N_{level,S}+1}{2}\right) \times \frac{2k+2}{\ln(2k)} \tag{68}$$

$$N_{switches,T} = \ln\left(N_{level,T}\right) \times \frac{2k+2}{\ln(4k-1)} \tag{69}$$

From (67)-(69), the number of switches is minimized as the terms $\frac{2k+2}{4k-2}$, $\frac{2k+2}{ln(2k)}$, and $\frac{2k+2}{ln(4k-1)}$ are minimized while the

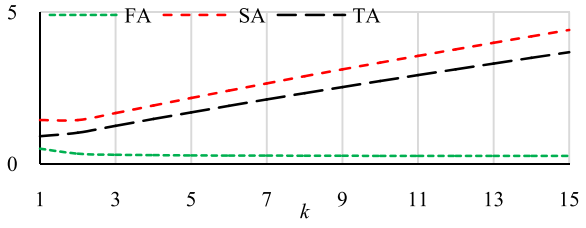

FIGURE 7. Curves related to optimization for minimization of dc voltage sources with constant number of levels.

number of levels are kept constant. Fig. 6 (a) displays the variation of these terms for different algorithms with respect to k. For FA, $k = \infty$ optimizes the proposed topology, while $k = 2$ is optimum for both SA and TA algorithm.

D. MINIMIZING THE NUMBER OF DRIVER CIRCUIT WITH CONSTANT NUMBER OF LEVELS

The optimization of the proposed structure is considered by minimizing the number of driver circuits required with a constant number of levels. (70)-(72) gives the number of driver circuit required with a constant number of levels.

$$N_{driver,F} = (N_{level,F} - 1) \times \frac{k+4}{4k-2} \tag{70}$$

$$N_{driver,S} = \ln\left(\frac{N_{level,S}+1}{2}\right) \times \frac{k+4}{\ln(2k)} \tag{71}$$

$$N_{driver,T} = \ln\left(N_{level,T}\right) \times \frac{k+4}{\ln(4k-1)} \tag{72}$$

From these equations, the terms $\frac{k+4}{4k-2}$, $\frac{k+4}{ln(2k)}$, and $\frac{k+4}{ln(4k-1)}$ should be minimized in order to get the optimized structure. The variation of the number of driver circuit against k with a constant number of levels is illustrated in Fig. 6 (b). With respect to the Fig. 6 (b), the optimal number of driver circuit required for FA is obtained for $k = \infty$. Similarly, for SA and TA, the proposed topology optimizes with $k = 4$ and $k = 3$ respectively.

E. MINIMIZING THE NUMBER OF DC VOLTAGE SOURCES WITH CONSTANT NUMBER OF LEVELS

Rewriting (65)-(67), the equations relating the number of dc voltage sources with respect to k for a constant number of levels are given in (74)-(77).

$$N_{source,F} = (N_{level,F} - 1) \times \frac{k}{4k-2} \tag{73}$$

$$N_{source,S} = \ln\left(\frac{N_{level,S}+1}{2}\right) \times \frac{k}{\ln(2k)} \tag{74}$$

$$N_{source,T} = \ln\left(N_{level,T}\right) \times \frac{k}{\ln(4k-1)} \tag{75}$$

The variation of $\frac{k}{4k-2}$, $\frac{k}{\ln(2k)}$, and $\frac{k}{\ln(4k-1)}$ is shown in Fig 7. For FA, SA and TA, the topology gets optimized with $k = \infty$, $k = 2$, and $k = 2$ repectively.

TABLE 2. Comparison of different basic units for cascade connection.

Topology	N_{switch}	N_{driver}	N_{source}	N_{levels}	TSV×V_{dc}	TSV/N_{levels}
[12]	11	11	4	9	27	3.0
[18]	6	6	2	7	12	1.71
[21]	12	10	4	17	44	2.59
[19]&[20]	10	8	4	17	38	2.24
[22]	10	8	2	9	20	2.22
Proposed	8	7	3	11	22 MODE I 21 MODE II	2.0 1.91

V. COMPARATIVE STUDY

In order to prove the dominance of the proposed basic unit, a comparison is made with other similar basic units and is provided in Table 2. The comparisons are carried out with respect to the number of switches, number of the driver circuit, number of dc voltage sources, number of levels generated across the load and TSV. One important aspect of cascade MLI is that the basic unit must have a lower number of switches and sources. From Table 2, it is clear that the proposed basic unit uses a lower number of switches except [18]. Furthermore, the TSV/N_{levels} is lower compared to other basic units in both modes except [18].

The main intention of proposing the new cascade topology is to reduce the number of switches and dc voltage sources while achieving more number of levels at the output. In order to benchmark the effectiveness of the proposed topology, a comparative study with other comparable MLI topologies is presented in this section. The comparisons are based on the number of switches, number of driver circuit required, number of dc voltage sources, and the total standing voltage against the number of levels. In this comparison, the optimal design is considered for all topologies including the proposed structure. In [19]–[22], two algorithms have been proposed with an optimal design. The best algorithm of all topologies is used for the comparison.

Fig. 8 (a) shows the variation of number of switches against the number of levels at the output. It is clear from the Fig. 8 (a) that the proposed topology uses less number of switches compare to other topologies, thus one of the main objectives of the newly proposed topology have been achieved. Topologies suggested in [19]–[22] and the proposed topology uses bidirectional switches along with unidirectional switches. The use of bidirectional switches reduces the number of driver circuit required if they are configured in common emitter connection. The variation of the number of driver circuit with the number of levels is indicated in Fig. 8 (b). The proposed topology requires a lower number of driver circuit than other topologies except [19], [20].

Reducing the number of dc voltage source has been another important criterion in the selection of an MLI. Fig. 9 (a) compares the number of dc voltage sources required with the number of output levels. The proposed topology requires a lower number of dc voltage sources than other topologies except [22] and [26]. Another crucial feature of an MLI is the

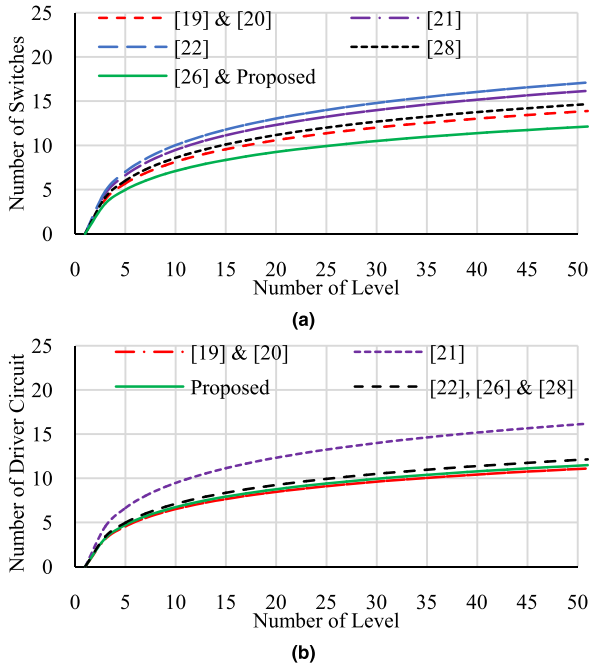

FIGURE 8. Variation of (a) number of switches and (b) number of driver circuit against number of levels.

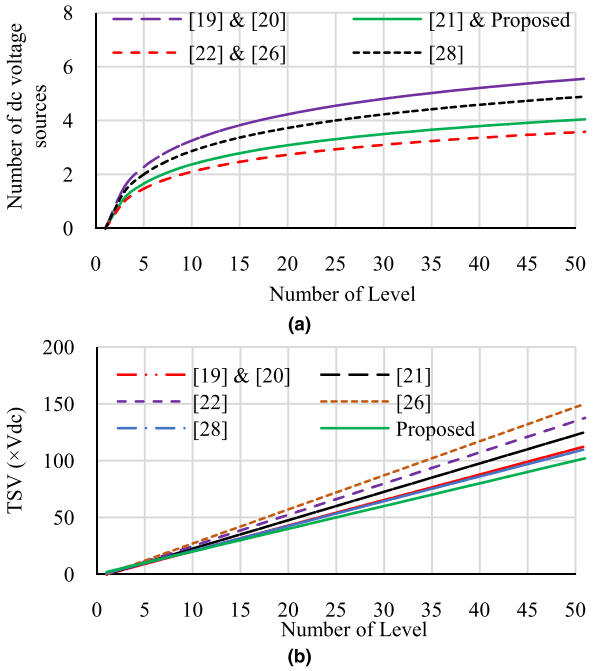

FIGURE 9. Variation of (a) number of dc voltage sources and (b) TSV against number of levels.

lower TSV. Fig. 9 (b) displays the comparison of TSV with the number of levels achieved at the output. The proposed topology has the lowest amount of TSV compare to other MLI structures. Therefore, these comparisons demonstrate the relevance of the proposed cascaded topology in terms of achieving higher number of level generation with a reduction in other parameters.

VI. MODULATION TECHNIQUE

The PWM technique used for the gate pulse generation has been classified into two categories based on the switching frequency namely high switching frequency PWM and fundamental switching frequency PWM techniques. Sinusoidal PWM, space vector PWM and hybrid modulation PWM are some of the examples of high switching frequency techniques. In these PWM techniques, the number of turn ON and turn OFF are high. This results in higher switching losses which reduce the efficiency [9], [30], [31].

Fundamental switching frequency is preferred for multilevel inverters due to reduced switching losses. In this paper, SHEPWM method is used for the computation of switching angles. The Fourier series for the staircase output voltage waveform shown in Fig. 10 is expressed as:

$$v_o(t) = \frac{a_o}{2} + \sum_{i=0}^{n} a_n \cos\left(\frac{2\pi nt}{T}\right) + b_n \sin\left(\frac{2\pi nt}{T}\right) \tag{76}$$

where a_o, a_n, and b_n represents the dc, even harmonic and odd harmonic components of the output voltage respectively, and n is the harmonic order. As the staircase output voltage have quarter wave symmetry, a_o, a_n and sine terms of odd

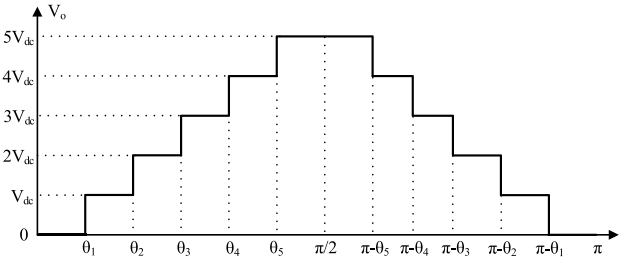

FIGURE 10. 11 level staircase output voltage waveform.

harmonics attain zero value. Therefore, the equation for output voltage modifies to:

$$v_o(t) = \sum_{i=1,3,5,\ldots}^{n} b_n sin(n\alpha_i) \tag{77}$$

For a staircase output voltage, b_n can be expressed as:

$$b_n = \frac{4V_{dc}}{n\pi} \sum_{i=1,3,5,\ldots}^{n} \cos(n\alpha_i) \tag{78}$$

The proposed basic unit generates 11 levels at the output. With 11 levels, four harmonics can be eliminated. Several combinations of these four harmonic orders can be made to be eliminated. Generally, lower order harmonic orders are eliminated. In this paper, 3rd, 5th, 7th, and 9th order harmonics are chosen to eliminate from the output voltage waveform of the proposed MLI. In SHEPWM technique, firing angles $(\theta_1, \theta_2, \ldots, \theta_5)$ are calculated using (79) by maintaining the relationship $(0 < \theta_1 < \theta_2, \ldots, < \theta_5 < \pi/2)$ (79), as shown at the bottom of the next page.

Where $b_1 = V_D$ is the fundamental component and gives the desire output voltage V_D. b_3, b_5, b_7, andb_9 are the

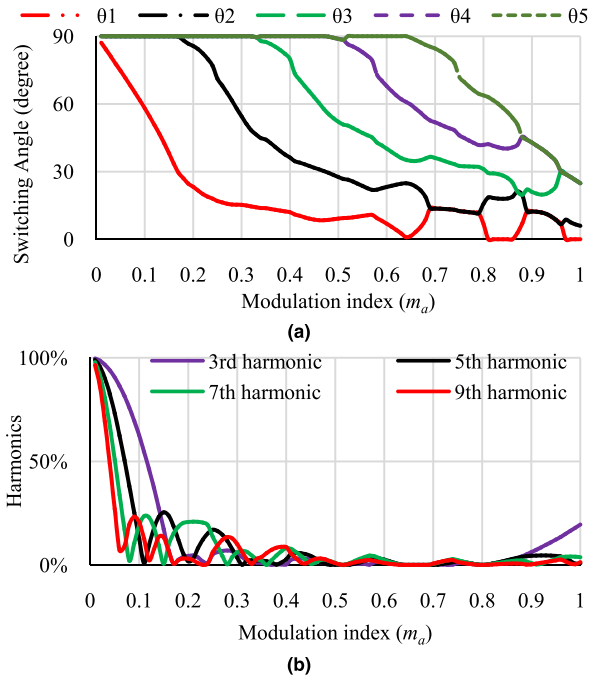

FIGURE 11. Variation of (a) switching angles and (b) harmonics with variation in modulation index.

harmonic orders to be eliminated and made equal to zero. The modulation index is given by,

$$m_a = \frac{\pi \times V_D}{2 \times (N-1) \times V_{dc}} \tag{80}$$

The solution of (79) and (80) gives the switching angle used for the generation of gate pulses. For the proposed inverter, optimized switching angles are calculated using the PSO algorithm described in [9]. Table 3 gives the different switching angles for the 11 level output voltage.

The variation of these switching angles with modulation index m_a is depicted in Fig. 11 (a). Fig. 11 (b) shows the variation of different harmonic orders with modulation index.

On a similar way, for the cascade connection of two modules, SHE is implemented for 71 level. For 71 levels, all the harmonics from 3rd to 69th are considered for the elimination and the switching angles are provided in Table 4.

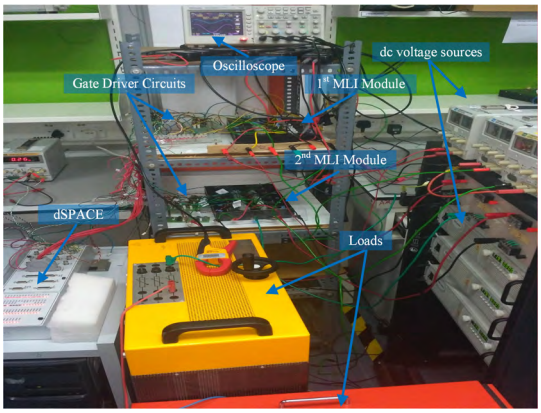

FIGURE 12. Experimental Setup.

TABLE 3. Switching angles for 11 levels ($m_a = 0.8$).

θ_1	θ_2	θ_3	θ_4	θ_5
6.74	15.72	31.06	41.86	63.74

VII. RESULTS AND DISCUSSION

The performance of the proposed multilevel inverter is investigated by designing a prototype experimental setup. The proposed basic unit along with its cascade connection are designed and results for 11 and 71 levels are provided in this manuscript. For the 11 level generation, SHE PWM is used for the gate pulse generation as angles given in Table 3. For the cascade connection with 71 levels, selective harmonic elimination PWM technique is used for gate pulse generation due to its easy implementation and all the switching angles are given in Table 4. All these angles are calculated offline. Fig. 12 shows the hardware setup for the proposed cascade MLI. TOSHIBA IGBT GT50J325 with an antiparallel diode is used for the prototype setup, while dSPACE is used for the gate pulse generation for the switches.

A. EXPERIMENTAL RESULTS FOR THE BASIC UNIT

Basic unit is used for the generation of 11 levels at the output. The selection of the magnitude of dc voltage sources is based

$$\left.\begin{aligned}
b_1 &= \frac{4V_{dc}}{\pi}\left[\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)+\cos(\theta_5)\right] = V_D \\
b_3 &= \frac{4V_{dc}}{3\pi}\left[\cos(3\theta_1)+\cos(3\theta_2)+\cos(3\theta_3)+\cos(3\theta_4)+\cos(3\theta_5)\right] = 0 \\
b_5 &= \frac{4V_{dc}}{5\pi}\left[\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)+cos(5\theta_5)\right] = 0 \\
b_7 &= \frac{4V_{dc}}{7\pi}\left[\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)+cos(7\theta_5)\right] = 0 \\
b_9 &= \frac{4V_{dc}}{9\pi}\left[\cos(9\theta_1)+\cos(9\theta_2)+\cos(9\theta_3)+\cos(9\theta_4)+cos(9\theta_5)\right] = 0
\end{aligned}\right\} \tag{79}$$

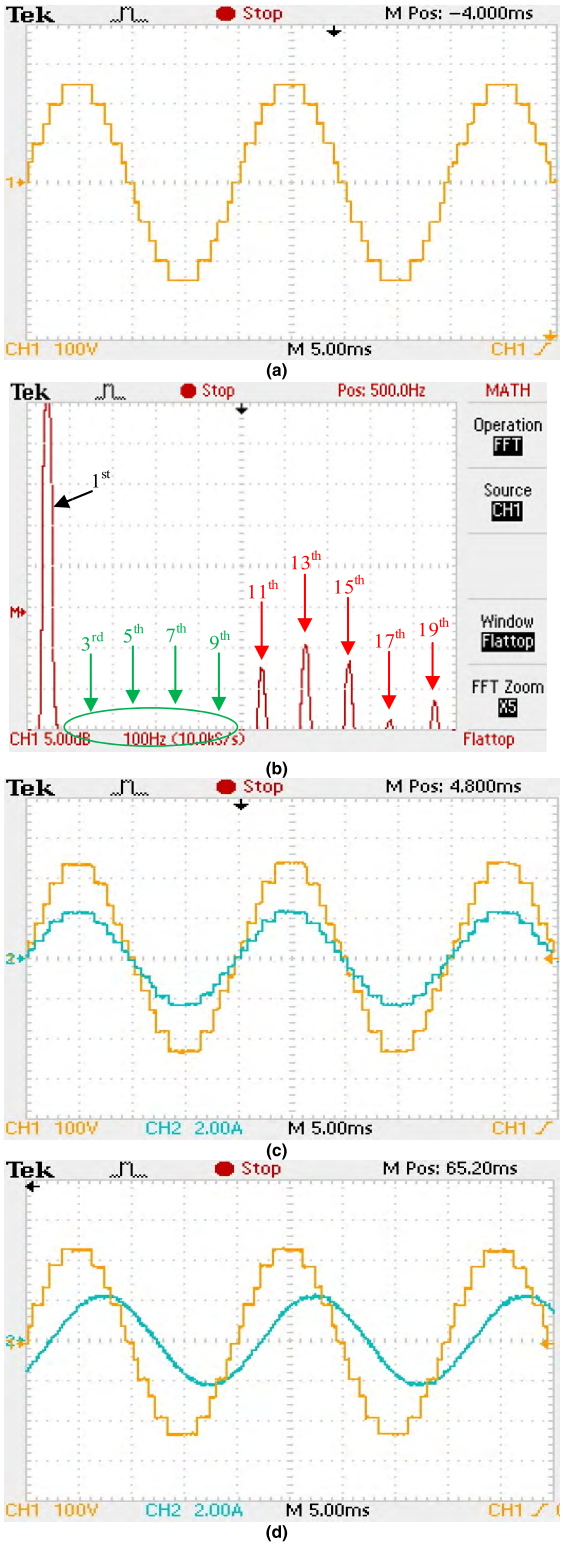

FIGURE 13. Experimental results for basic unit (a) output voltage waveform and (b) FFT of output voltage (c) Output voltage and current waveform with R load and (d) Output voltage and current waveform with RL load.

on MODE I i.e. $V_1 = 50$V and $V_2 = 100$V. The peak voltage generated at the output is 250V, with a voltage step of 50V and 50Hz output frequency. The gate pulses are generated using

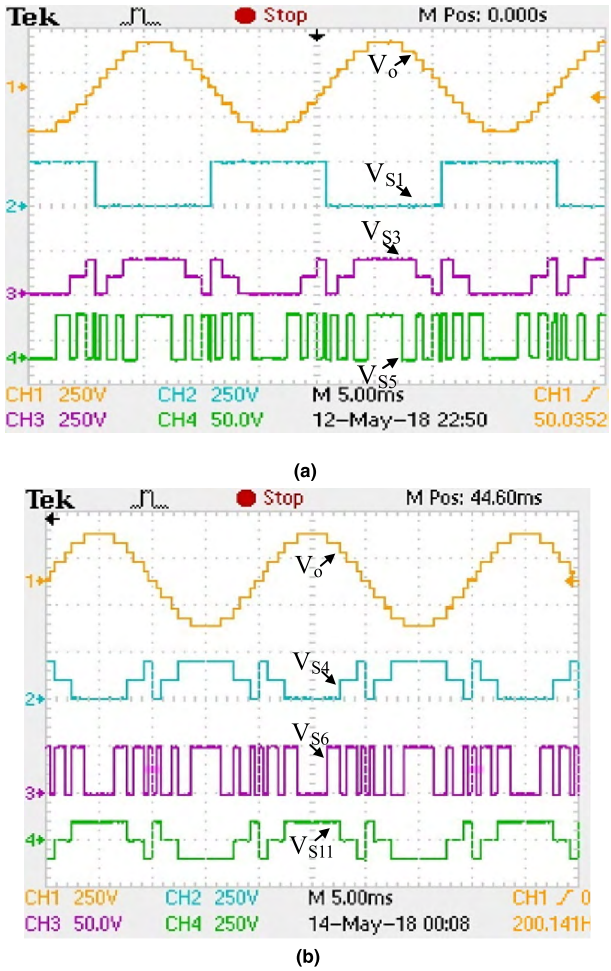

FIGURE 14. Output voltage waveform V_o with voltage stress across switches (a) S_1, S_3, and V_5 (b) S_4, S_6, and V_{11}.

TABLE 4. Switching angles for 71 levels ($m_a = 0.8$).

θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9
1.04	2.33	3.95	5.87	7.18	8.83	10.96	11.80	14.19
θ_{10}	θ_{11}	θ_{12}	θ_{13}	θ_{14}	θ_{15}	θ_{16}	θ_{17}	θ_{18}
15.31	17.58	18.50	21.33	21.82	24.20	26.66	26.84	30.60
θ_{19}	θ_{20}	θ_{21}	θ_{22}	θ_{23}	θ_{24}	θ_{25}	θ_{26}	θ_{27}
30.67	33.43	35.80	36.75	40.28	40.75	44.24	45.66	48.64
θ_{28}	θ_{29}	θ_{30}	θ_{31}	θ_{32}	θ_{33}	θ_{34}	θ_{35}	
50.77	53.64	56.30	59.44	62.67	66.48	70.88	75.90	

SHEPWM at the modulation index of 0.8. The calculated angles are provided in Table 3. Fig. 13 (a) illustrates the output voltage of the basic unit with 11 levels at the output. The 3rd, 5th, 7th, and 9th harmonic orders are selected to be eliminated from the output voltage waveform. Fig. 13 (b) demonstrates the FFT of the output voltage. It is clear from Fig. 13 (b) that all selected harmonic orders are eliminated from the output voltage.

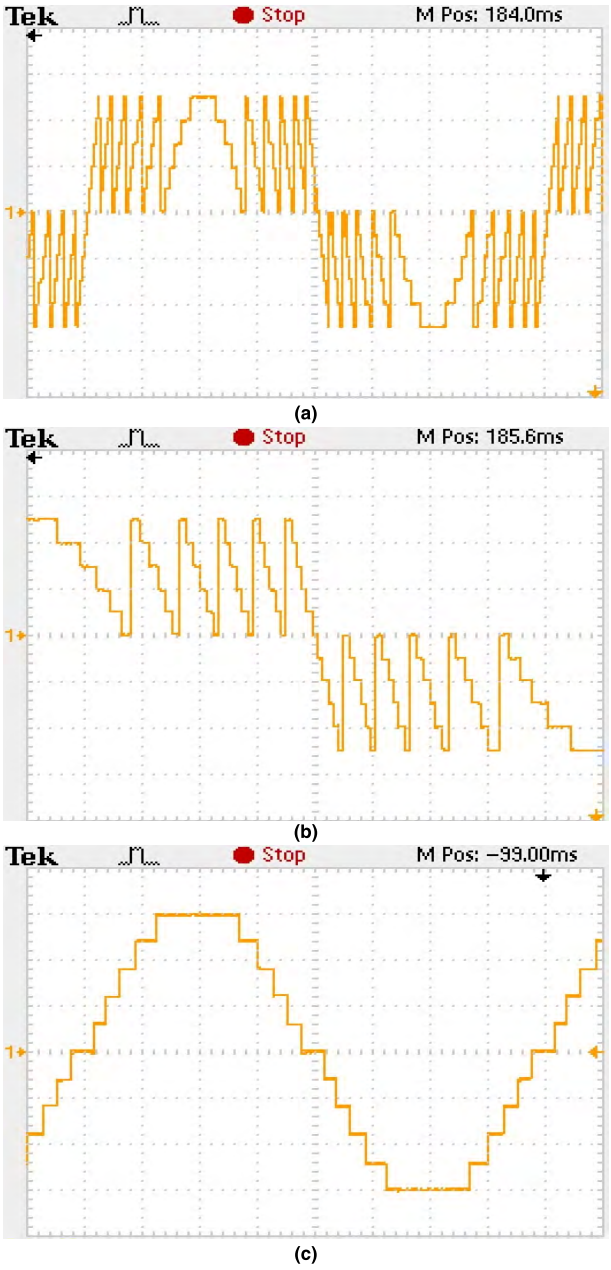

FIGURE 15. (a) Output voltage of first module (20V/div) (b) zoomed voltage view (20V/div) of first module and (c) output voltage of second module with 100V/div.

The performance of the proposed basic unit is checked by connecting different types of load. Fig. 13 (c) shows the output voltage and current waveform for a purely resistive load having a value of 100Ω. Fig. 13 (d) displays the voltage and current waveform with series connected resistive-inductive load with R = 80Ω and L = 200mH. Both output voltage waveforms are of 50Hz with 11 levels at the output.

Fig. 14 (a) – (b) show the voltage stress of different switches of the basic unit. The voltage stress across switch S_1 is the maximum with a value of 250V. The pattern of voltage stress across switch S_2 is the same as that of S_1 with the magnitude of 250V. The voltage stress across switches S_3 and

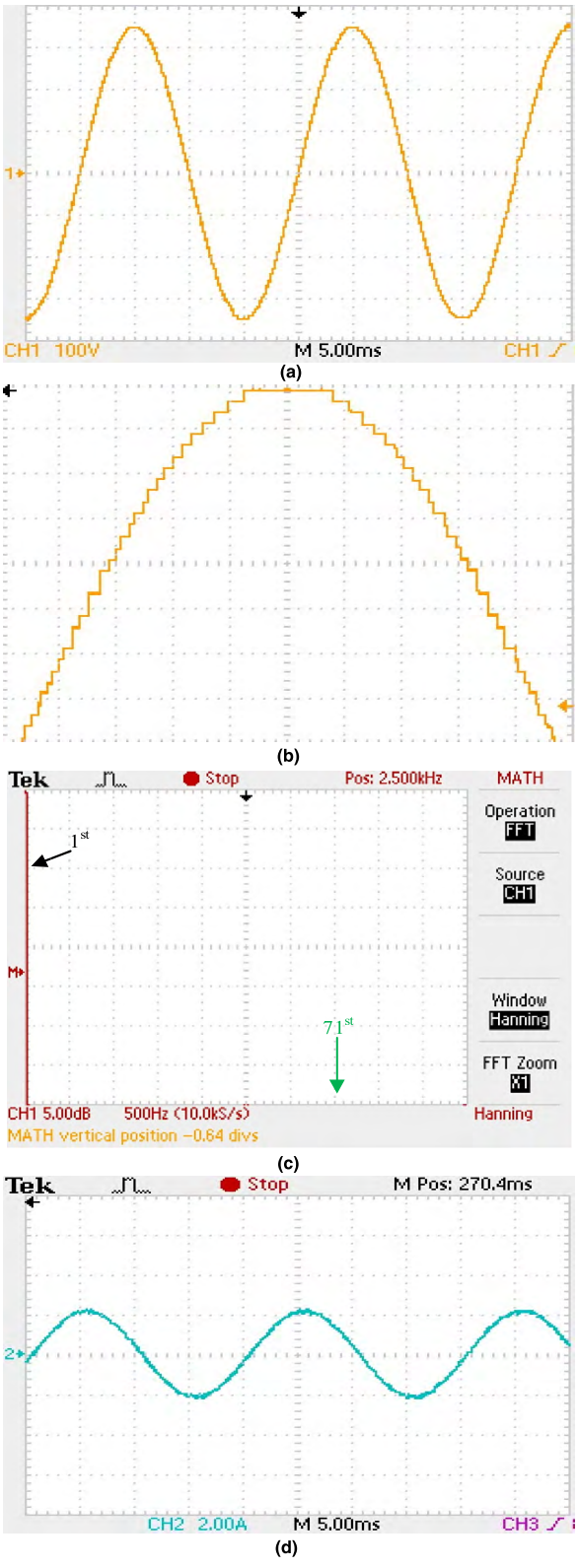

FIGURE 16. (a) Output voltage of two cascaded modules across the load, (b) zoomed view of the output voltage waveform, (c) FFT of the output voltage waveform and (d) load current with RL load.

S_5 is 200V and 50V, respectively, as indicated in Fig. 14 (a). Fig. 14 (b) shows the voltage stress variation of switches S_4, S_6 and bidirectional switch S_{11} with output voltage V_o.

B. EXPERIMENTAL RESULTS FOR CASCADE CONNECTION WITH THE SECOND ALGORITHM

The cascade connection of two basic unit is carried out in order to show the workings of the proposed topology in cascade. Two proposed basic units are connected in cascade using the second algorithm which is able to produce 71 levels at the output. The first module works at low voltage and high frequency operation of the switches. The magnitude of dc voltage sources is calculated from (25)-(26) in MODE I, which comes out to be $V_{11} = 10$V and $V_{12} = 20$V. The output voltage of the first module gives a peak value of 50V with a voltage step of 10V, as shown in Fig 15 (a). Fig. 15 (b) shows the zoomed in view of the output voltage of the first module. From (30) and (31), the magnitude of dc voltage sources for the second module is calculated as $V_{21} = 60$V and $V_{22} = 120$V. The second module generates an output voltage with a peak value of 300V with a voltage step of 60V and is shown in Fig. 15 (c).

The output voltage of the two cascaded modules is illustrated in Fig. 16 (a) with a zoomed view in Fig. 16 (b). The peak voltage of the cascade connection is 350V with 10V voltage step. The FFT of the output voltage waveform is shown in Fig. 16 (c). As illustrated in the FFT, all the lower order harmonics are eliminated from the output voltage. Furthermore, the robustness of the cascade connection is shown by connecting the series connected RL load and the output current waveform is shown in Fig. 16 (d).

VIII. CONCLUSION

A new cascaded multilevel inverter topology has been proposed in this paper with the advantage of having a reduced number of switching devices as well as number of dc voltage sources. The basic unit of the proposed topology generates 11 levels across the load employing eight switches with three dc voltage sources. Two different modes of dc voltage selection have also been presented for the generalized structure of the proposed topology. Both of these modes reduce the need for a variety of dc voltage sources to only two, which makes the proposed topology more practical. To achieve more number of levels at the output, a detailed cascade connection of the proposed topology has been discussed. In a cascade connection, three different algorithms have been formulated in this paper to select the magnitude of the dc voltage sources. Furthermore, the optimization assessments of the cascade connections has been completed using all three algorithms. An in-depth comparison with other recently proposed optimal structure confirms the benefit of the proposed topology. The theoretical explanation of the proposed topology has been verified for the basic unit and cascade connection of two modules in the second algorithm using a laboratory prototype setup.

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MARIF DAULA SIDDIQUE (S'18) was born in Chhapra, India, in 1992. He received the B.Tech. and M.Tech. degrees in electrical engineering from Aligarh Muslim University, in 2014 and 2016, respectively. He is currently pursuing the Ph.D. degree with the Power Electronics and Renewable Energy Research Laboratory, Department of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia. His research interests include step-up power electronics converters (dc/ac and dc/dc), and multilevel inverter topologies and their control.

SAAD MEKHILEF (M'01–SM'12) received the B.Eng. degree in electrical engineering from the University of Setif, Setif, Algeria, in 1995, and the master's degree in engineering science and the Ph.D. degree in electrical engineering from the University of Malaya, Kuala Lumpur, Malaysia, in 1998 and 2003, respectively, where he is currently a Professor and the Director of the Power Electronics and Renewable Energy Research Laboratory, Department of Electrical Engineering. He has authored or co-authored over 400 publications in international journals and conference proceedings. His current research interests include power converter topologies, control of power converters, renewable energy, and energy efficiency.

NORAISYAH MOHAMED SHAH received the B.Eng. degree from the University of Malaya, in 1999, the M.Eng. degree from Oita University, Japan, in 2003, and the Ph.D. degree from George Mason University, Fairfax, VA, USA, in 2014. She is currently a Senior Lecturer with the Department of Electrical Engineering, University of Malaya. Her current research interests include signal processing and renewable energy.

MUDASIR AHMED MEMON received the B.E. degree in electronics engineering and the M.E. degree in electronic systems engineering from the Mehran University of Engineering and Technology, Jamshoro, Pakistan, in 2009 and 2015, respectively. He is currently pursuing the Ph.D. degree in power electronics with the University of Malaya, Malaysia.

From 2009 to 2016, he was a Lecturer and then an Assistant Professor with the Institute of Information and Communication Technology, University of Sindh, Jamshoro. His research interests include multilevel inverters, power quality, and control strategies.