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A Disturbance Rejection Control Strategy for Droop-Controlled Inverter Based on Super-Twisting Algorithm

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ABSTRACT In distributed generation systems, multiple inverters paralleled operation is essential for the power requirement of local loads. To achieve the reasonable power distribution among the inverters, droop control is an effective method for the paralleled operation systems without the control interconnection. In general, the multi-loop control structure is usually utilized to regulate the drooped voltage across local loads. However, by using the traditional multi-loop controller, such as proportional-integral and proportional-resonant controllers, the dynamic process of load variation or mode transfer is slow, even the voltage overshoot or drop may occur. To address the above issues, a compact control structure-based super-twisting algorithm has been proposed in this paper. Benefitting from the designed sliding mode controllers, the dynamic response, the load disturbance rejection, and reference tracking performance can be improved. In addition, the robustness to parameters mismatch can also be achieved by using the proposed control method. The comparative simulation and experimental results validate the correctness and feasibility of the proposed method.

INDEX TERMS Microgird system, voltage-controlled inverter, disturbance rejection, super-twisting algorithm, droop control.

I. INTRODUCTION

Distributed generation (DG) is an ideal method to integrate various renewable resources to provide power for the remote customers [1]. As the power electronic interface, the inverters are one of the most essential components in the microgrid system consisting of DGs. The interface inverters should be performed as a voltage source to adjust their output voltage and frequency [2]. Many control strategies, such as droop control, master-slave control, and average current-sharing control, have been extensively implemented to operate parallel-connected inverters for sharing the powers of the load. Among these methods, the droop control has been widely adopted because of no critical communication links among the parallel-connected inverters. However, the traditional droop control has some drawbacks [3], [4], such as slow transient response and poor disturbance rejection. Recently some modified droop control methods have been proposed to improve the performance of the system. The terms of power derivative-integral are introduced to the droop scheme to obtain a better power controllability of the system [5]. A proportional-derivative (PD) droop control has been proposed to improve steady-state regulation and transient response [6]. The adaptive droop gains have been designed to deal with the low-frequency stability among the paralleled inverters [7]. However, the dynamic of the inner control loop is often neglected in the existing droop control methods due to their traditional multi-loop control structure in [5]–[7].

As for the voltage-controlled inverters, the traditional multi-loop control is usually designed by means of the transfer function model. The proportional-integral (PI) controllers have been employed to attain zero steady-state error under the rotating reference frame (RRF) [8]. Similarly, the proportional-resonant (PR) controllers have been also applied to the stationary reference frame (SRF) [9] or a single-phase inverter [10]. Furthermore, the capacitor current has been also utilized for the inner current loop to enhance the

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robustness of LCL-type grid-connected inverter [11]. Generally, the outer voltage control loop and inner current control loop are used in the nested-loop control structure to guarantee the tracking reference performance and dynamic compensation performance under the system disturbances [12]. However, the transient process of load or reference variation is usually long, and the voltage overshoot or drop may occur [13].

In the light of above problems of the traditional multi-loop control, recently, many advanced control strategies have been proposed in voltage-controlled inverters. The deadbeat control, one of discrete-time linear control laws, can make all the closed-loop poles' place at zero. Thus, the deadbeat controller can force the tracking error to zero within a few sampling steps [14]. A finite control set model predictive strategy has been implemented in the load voltage control, maintaining a good steady-state performance and fast dynamic response [15]. Based on linear matrix inequality (LMI), a state feedback and tracking gains control has been designed for uninterruptible power supply (UPS) applications [16]. However, these methods are all highly sensitive to model uncertainties and parameter perturbations. Therefore, the robustness of system can be maintained usually by a disturbance observer or a state compensator, which will increase system complexity.

Owning to the inherent characteristics of the sliding mode control (SMC), that is, robustness to the system parameter mismatch, overshoot-free, fast dynamic response and the ability to exogenous disturbances rejection, the SMC has been applied in voltage-controlled inverter. A sliding mode control based on three-level hysteresis sliding function has been proposed in a single-phase UPS inverter [17]. A mixed H_2/H_∞-based voltage control and a sliding mode control are applied to acquire a good dynamic response [18]. However, the MATLAB toolbox is needed to obtain the voltage control gains, which is not beneficial to practical application. In addition, the integral sliding mode surfaces are used to design the current control loop. Therefore, the potential chattering around the sliding manifold still exists although the switching frequency is fixed. The chattering phenomenon can be avoided by using high-order sliding mode (HOSM) method [19]. The super-twisting algorithm (STA), one of the HOSMs, which does not need any information about the derivative of the sliding variable, has been adopted in various areas [20]–[22]. Considering the external disturbances and inertia uncertainties, a novel adaptive-gain STA has been proposed to achieve the finite-time attitude tracking control in rigid spacecraft [20]. Based on STA for brushless doubly fed induction generator (BDFIG), a direct power control strategy has been designed to maintain both transient and steady-state performance [21]. A single voltage loop based on STA and PI controller has been proposed to achieve small steady state error in a voltage-controlled inverter, however, the experimental results are not provided [22]. To take full excellent properties of the STA introduced in aforementioned applications, a STA-based control structure in the single-phase

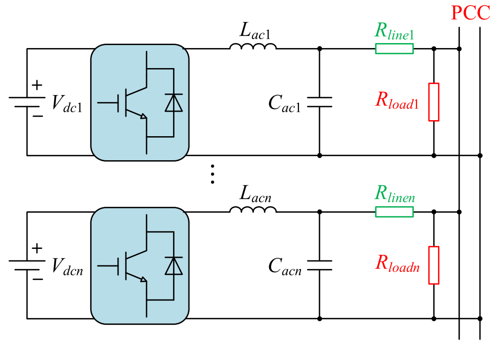


FIGURE 1. Structure of multiple paralleled systems.

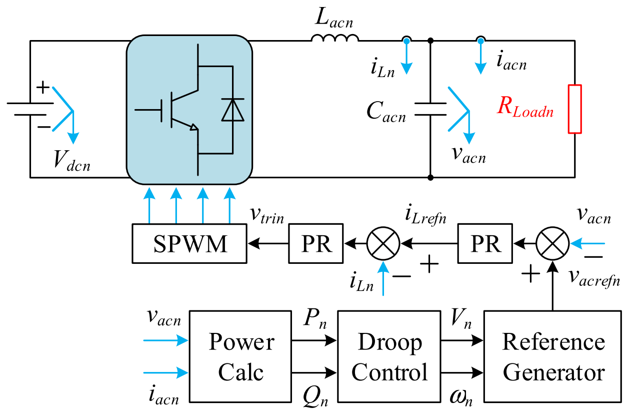


FIGURE 2. PR-based traditional multi-loop control structure of a voltage-controlled inverter.

voltage-controlled inverter has been investigated and firstly applied in the droop-controlled paralleled inverters system. The feedforward terms are contained benefitting from the designed STA controllers and the dynamic process of load variation or mode transfer for droop-controlled inverter has been improved. The paper is organized as follows: a disturbance rejection control strategy is proposed in Section II for droop-controlled paralleled inverters based on STA; discussion of simulation and experimental results are shown in Sections III and IV respectively; then the conclusion is drawn in Section V.

II. DISTURBANCE REJECTION CONTROL STRATEGY BASED ON STA

A. TRADITIONAL CONTROL OF A DROOP-CONTROLLED INVERTER

The structure of the paralleled inverter systems is shown in Fig. 1. The system is composed of two single-stage full-bridge inverters in parallel, where L_{acn} are the filter inductors; C_{acn} are the filter capacitors; R_{linen} are the line impendences; R_{loadn} are the local loads connected with the point of common coupling (PCC).

Fig. 2 shows the traditional multi-loop control of a voltage-controlled inverter based on PR controller, and the zero steady-state error can be achieved. The scheme in Fig. 2 will therefore operates well, but its performance may sometimes be compromised to the following drawbacks.

1) The reference current i_{Lrefn} and the modulation wave v_{trin} are totally determined by the outer voltage controller and the inner current controller, respectively. The voltage overshoot may occur when the voltage reference or load varies dramatically.
2) Due to the lack of feedforward, the transient changes of voltage or current cannot be reflected to the modulation signal in time, which may cause the long transient process.

B. SUPER-TWISTING ALGORITHM

Consider an uncertain nonlinear system,

$$\begin{aligned} \dot{x} &= f(t,x) + b(t,x)u \\ y &= s(t,x) \end{aligned} \tag{1}$$

where $x \in \mathbb{R}^n$, $u \in \mathbb{R}$ represent a stage vector and a control function, respectively; $f(t,x) \in \mathbb{R}^n$ represents a differentiable vector-field; $s(t,x)$ represents a sliding variable.

The input-output dynamics of system (1) can be expressed as

$$\dot{s}(t,x) = \frac{\partial}{\partial t}s(t,x) + \frac{\partial}{\partial x}s(t,x)\left[f(t,x) + b(t,x)u\right] \tag{2}$$

$$\begin{aligned} \ddot{s}(t,x) &= \frac{\partial}{\partial t}\dot{s}(t,x,u) + \frac{\partial}{\partial x}\dot{s}(t,x,u)\left[f(t,x) + b(t,x)u\right] \\ &\quad + \frac{\partial}{\partial u}\dot{s}(t,x,u)\dot{u} \\ &= \chi(t,x,u) + \varphi(t,x,u)\dot{u} \end{aligned} \tag{3}$$

where $\chi(t,x,u)$ and $\varphi(t,x,u)$ are bounded but unknown, i.e., there are positive constant values X, $\Phi_{\min}$ and $\Phi_{\max}$,

$$\begin{aligned} 0 < \Phi_{\min} < \varphi(t,x,u) < \Phi_{\max} \\ -\mathrm{X} < \chi(t,x,u) < \mathrm{X} \end{aligned} \tag{4}$$

Then, a differential inclusion can be obtained as

$$\ddot{s} \in [-\mathrm{X}, \mathrm{X}] + [\Phi_{\min}, \Phi_{\max}]\dot{u} \tag{5}$$

Thus, a control law based on Super-Twisting algorithm (STA) can be designed as follows [23]

$$\begin{aligned} u &= -\lambda|s|^{\frac{1}{2}} sign(s) + v \\ \dot{v} &= -\alpha sign(s) \end{aligned} \tag{6}$$

where λ and α are the designed positive parameters determined by the boundary conditions (4).

The sliding variable s can converge to the sliding manifold $s = \dot{s} = 0$ in the finite time, under the sufficient conditions, that is [23]:

$$\alpha > \frac{\mathrm{X}}{\Phi_{\min}}, \quad \lambda^2 \geq \frac{4\mathrm{X}}{\Phi_{\min}^2}\frac{\Phi_{\max}}{\Phi_{\min}}\frac{\alpha + \mathrm{X}}{\alpha - \mathrm{X}} \tag{7}$$

C. DISTURBANCE REJECTION CONTROL SCHEME BASED ON STA

The typical *R*/*X* ratio of a low voltage (LV) line has been given as 7.7, as compared to 0.85 of a medium voltage (MV) line and 0.31 of a high voltage (HV) line [2]. Obviously, for a LV distribution network, the line impedance is mainly resistive. Considering the line impendence, the resistive *P*-*V* and *Q*-ω droop expressions are given in

$$\begin{aligned} V_n &= V_{0n} - k_{pn}(P_n - P_{0n}) \\ \omega_n &= \omega_{0n} + k_{qn}(Q_n - Q_{0n}) \end{aligned} \tag{8}$$

where ω_{0n} and V_{0n} are the rated angular frequency and output voltage amplitude of converter "n", P_{0n} and Q_{0n} are its rated active and reactive powers, and k_{pn} and k_{qn} are its active and reactive power droop coefficients, respectively.

1) OUTPUT VOLTAGE LOOP DESIGN

As shown in Fig. 2, the dynamics of a single system can be described by

$$\begin{aligned} L_{acn}\dot{i}_{Ln} &= u_n V_{dcn} - v_{acn} \\ C_{acn}\dot{v}_{acn} &= i_{Ln} - i_{acn} \end{aligned} \tag{9}$$

The dynamic of the current loop should be faster than the voltage loop in general, therefore, the voltage and current loop can be designed independently. Thus, the dynamic of output voltage can be rewritten as

$$C_{acn}\dot{v}_{acn} = i_{Lrefn} - i_{acn} \tag{10}$$

The sliding mode variable for voltage control is defined as

$$s_{vn} = v_{acrefn} - v_{acn} \tag{11}$$

Then the first-time derivative of s_{vn} can be derived

$$C_{acn}\dot{s}_{vn} = C_{acn}\dot{v}_{acrefn} - \left(i_{Lrefn} - i_{acn}\right) \tag{12}$$

The first-time derivative of s_{vn} contains the control input $u(i_{Lrefn})$. Hence, the inverter system, as shown in Fig. 2, is of relative degree one and a traditional first-order sliding mode can be applied. Motivated by the chattering elimination aim, a super-twisting-based control is employed, which can keep the control signal u continuous and chattering avoided. The proposed STA controller for voltage loop is given by

$$i_{Lrefn} = \mu_{vn}(s_{vn}) + i_{acn} + C_{ac0n}\dot{v}_{acrefn} \tag{13}$$

where C_{ac0n} is the rated value of C_{acn}, and $\mu_{vn}(s_{vn})$ takes the following form

$$\mu_{vn}(s_{vn}) = \lambda_{vn}|s_{vn}|^{\frac{1}{2}} sign(s_{vn}) + \alpha_{vn}\int_0^t sign(s_{vn})d\tau \tag{14}$$

where λ_{vn} and α_{vn} are the designed positive parameters.

From (13) and (14), the dynamic of s_{vn} can be obtained

$$C_{acn}\dot{s}_{vn} = -\mu_{vn}(s_{vn}) + \Delta C_{acn}\dot{v}_{acrefn} \tag{15}$$

where ΔC_{acn} is the parametric uncertainties.

It can be easily obtained that there is a positive constant C_{vn} satisfying,

$$\left\| d\Delta C_{acn}\dot{v}_{acn}/dt \right\| \leq C_{vn} \tag{16}$$

The sliding variable s_{vn} can converge to the sliding manifold $s_{vn} = \dot{s}_{vn} = 0$ in the finite time, under the sufficient conditions, that is [23]:

$$\alpha_{vn} > C_{acn}C_{vn}, \quad \lambda_{vn}^2 \geq 4C_{acn}^2 C_{vn}\frac{\alpha_{vn}+C_{vn}}{\alpha_{vn}-C_{vn}} \tag{17}$$

Therefore, control block diagram for voltage is shown in Fig. 3(b).

2) INDUCTOR CURRENT LOOP DESIGN

The control objective of the inductor current loop is to track the reference current i_{Lrefn} computed from the output voltage loop. Similarly, the sliding mode variable for inductor current control is defined as

$$s_{in} = i_{Lrefn} - i_{Ln} \tag{18}$$

Then the control law u_n can be obtained as

$$u_n = \left(\mu_{in}(s_{in}) + v_{acn} + L_{ac0n}\dot{i}_{Lrefn}\right)/V_{dcn} \tag{19}$$

The dynamic of s_{in} can be obtained as

$$L_{acn}\dot{s}_{in} = -\mu_{in}(s_{vn}) + \Delta L_{acn}\dot{i}_{Lrefn} \tag{20}$$

where ΔL_{acn} is the parametric uncertainties, and $\mu_{in}(s_{in})$ takes the following form

$$\mu_{in}(s_{in}) = \lambda_{in}|s_{in}|^{\frac{1}{2}}\, sign(s_{in}) + \alpha_{in}\int_0^t sign(s_{in})d\tau \tag{21}$$

where λ_{in} and α_{in} are the designed positive parameters. It can also be easily obtained that there is a positive constant L_{in} satisfying

$$\left\| d\Delta L_{acn}\dot{i}_{Lrefn}/dt \right\| \leq L_{in} \tag{22}$$

The sliding variable s_{in} can converge to the sliding manifold $s_{in} = \dot{s}_{in} = 0$ in the finite time, under the sufficient conditions, that is [23]:

$$\alpha_{in} > L_{acn}L_{in}, \quad \lambda_{in}^2 \geq 4L_{acn}^2 L_{in}\frac{\alpha_{in}+L_{in}}{\alpha_{in}-L_{in}} \tag{23}$$

It should be noted that the designed output voltage loop controller contains the output current i_{acn} and the designed current loop controller contains the output voltage v_{acn} according to (13) and (19). The term i_{acn} can be regard as a feedforward, which can improve the dynamic performance and reduce the disturbance effect of load variation. Similarly, the term v_{acn} can be regard as a feedforward too, which can improve the effect of reference variation. It is a natural advantage to utilize the STA. Although, the gains of STA controllers $\mu_{vn}(s_{vn})$ and $\mu_{in}(s_{in})$ will be reduced accordingly, the settling time are not decreased. The overall control structure is shown in Fig. 3.

The proposed disturbance rejection scheme is shown in Fig. 3. The ac output voltage v_{acn} and output current

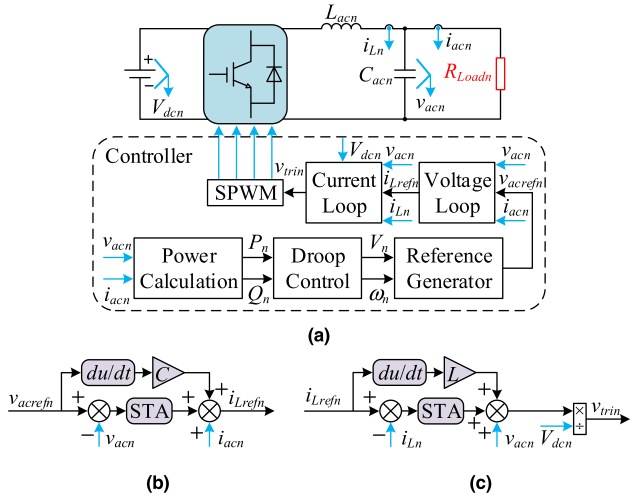


FIGURE 3. Illustration of (a) proposed disturbance rejection control scheme, (b) control block diagram for voltage loop, (c) control block diagram for current loop.

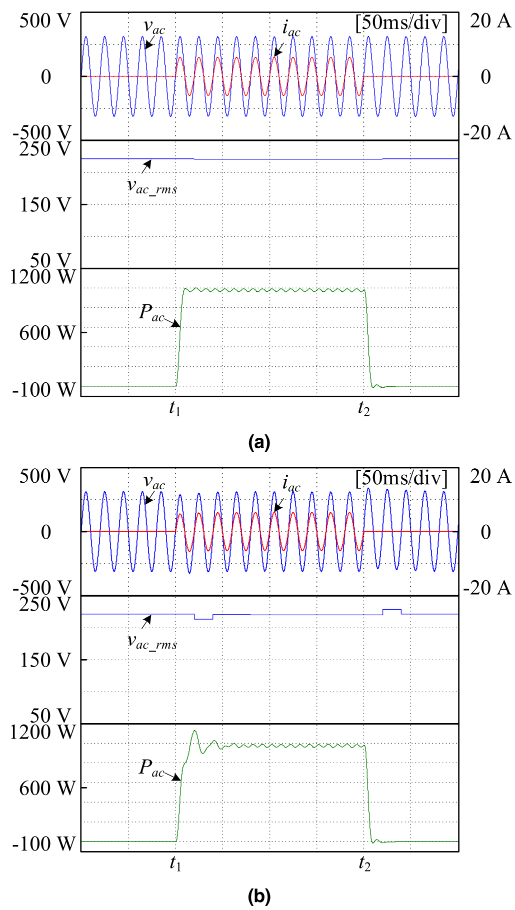


FIGURE 4. Simulation results of load variation, (a) the proposed control, (b) the traditional multi-loop control.

i_{acn} should be measured in order to obtain the active power P_n and reactive power Q_n, then the output voltage amplitude V_n and angular frequency ω_n can be obtained from the droop expression in (8). Thus, the generated output reference

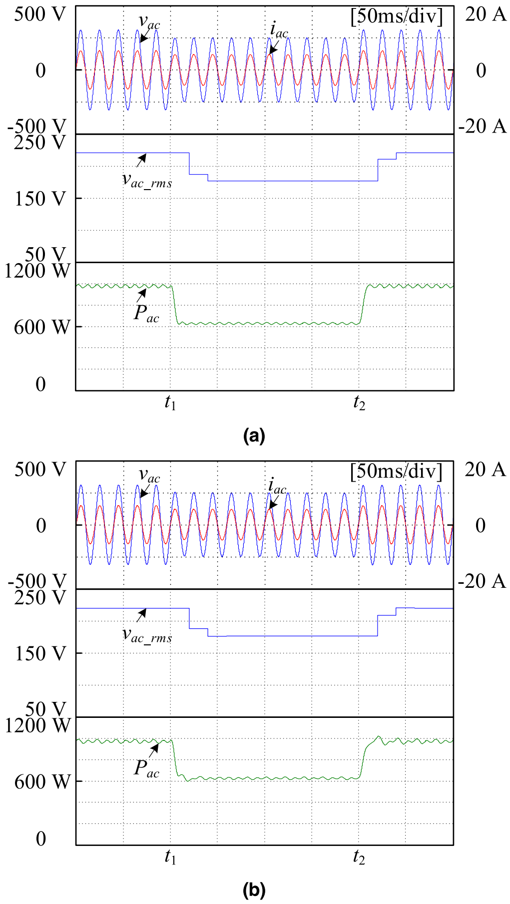


FIGURE 5. **Simulation results of the reference voltage variation, (a) the proposed control, (b) the traditional multi-loop control.**

voltage V_{acrefn} can be tracked by the voltage-current loop based on STA.

D. PROOF OF THE STABILITY

To prove the stability of the proposed controllers, a candidate Lyapunov function for voltage loop is introduced:

$$V_v = \frac{1}{2} C_{acn} s_{vn}^2 \geq 0 \tag{24}$$

The time derivative of V_v can be obtained as

$$\dot{V}_v = -s_{vn} \left(\lambda_{vn} \left| s_{vn} \right|^{\frac{1}{2}} sign\left(s_{vn}\right) + \alpha_{vn} \int_0^t sign\left(s_{vn}\right) d\tau \right) \tag{25}$$

If $s_{vn} > 0$, $sign(s_{vn}) = 1$, thus, $\dot{V}_v < 0$; if $s_{vn} < 0$, $sign(s_{vn}) = -1$, thus $\dot{V}_v < 0$. Since V_v is a positive-definite function and its first-time derivative ($\dot{V}_v$) is a negative-definite function, the sliding surface s_{vn} converges to zero asymptotically and the proposed voltage controller becomes asymptotically stable. The stability proof of current loop can refer to the above process.

Even though the designed STA controllers can guarantee fast dynamic response and good disturbance rejection, the switching function "*sign*(*s*)" of the switching control input may bring instability problems to the system. To solve this issue, a boundary layer around the sliding surface is adapted in the switching function as follows

$$sign\left(s\right) = \begin{cases} 1, & \text{if } s > \beta \\ s/\beta & \text{if } |s| \leq \beta \\ -1 & \text{if } s < \beta \end{cases} \tag{26}$$

where, β is the width of boundary layer.

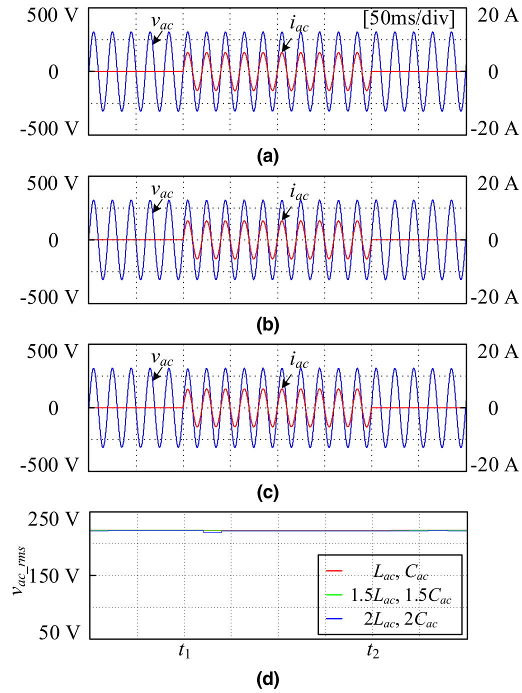


FIGURE 6. **Simulation results of system parameters variation for the proposed control, (a) L_{ac} = 5mH and C_{ac} = 5 μF, (b) 1.5 L_{ac} and 1.5 C_{ac}, (c) 2 L_{ac} and 2 C_{ac}.**

E. PROOF OF THE ROBUSTNESS

The performance of the control system may be affected by system disturbances in practical application conditions, such as parameter variations, measurement noises, analogue-digital sample errors, thus, (15) can be rewritten as

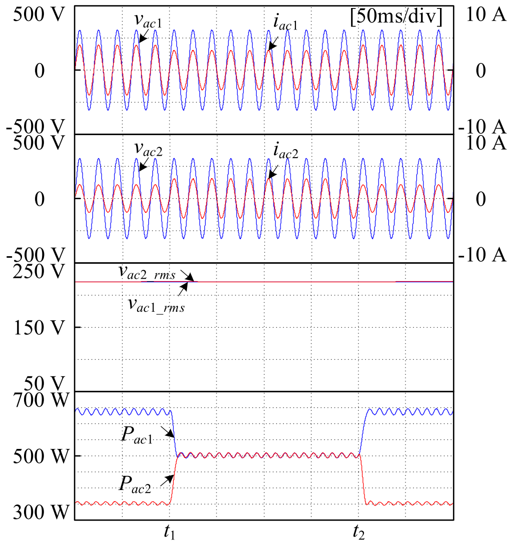
$$C_{acn}\dot{s}_{vn} = -\mu_{vn}\left(s_{vn}\right) + F_v \tag{27}$$

where F_v is the overall internal and external disturbances.

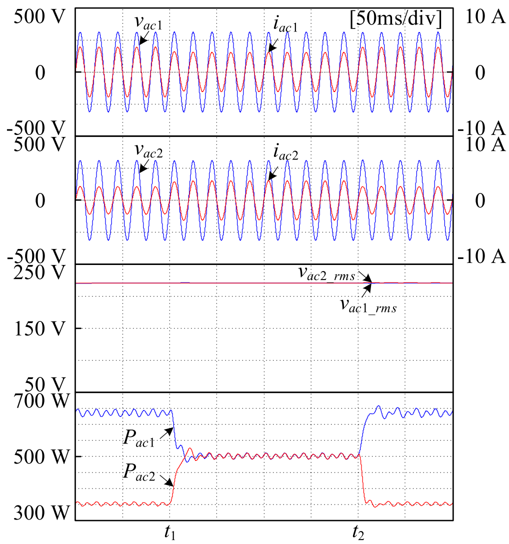
Thus, (25) can be rewritten as

$$\dot{V}_v = -s_{vn} \left(\lambda_{vn} \left| s_{vn} \right|^{\frac{1}{2}} sign\left(s_{vn}\right) + \alpha_{vn} \int_0^t sign\left(s_{vn}\right) d\tau - F_v \right) \tag{28}$$

If the positive control gains λ_{vn} and $\alpha_{vn}$are set large enough to fulfill (28), $\dot{V}_v$ is still definitely negative. According to Lyapunov stability theorem, the proposed controller features strong robustness, if the control gains are selected properly.



(a)



(b)

FIGURE 7. Simulation results of inverters paralleled operation, (a) the proposed control, (b) the traditional multi-loop control.

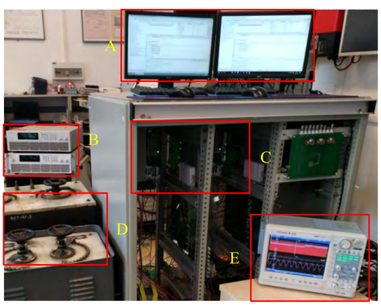
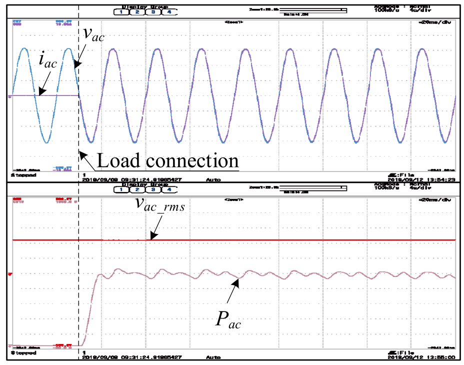


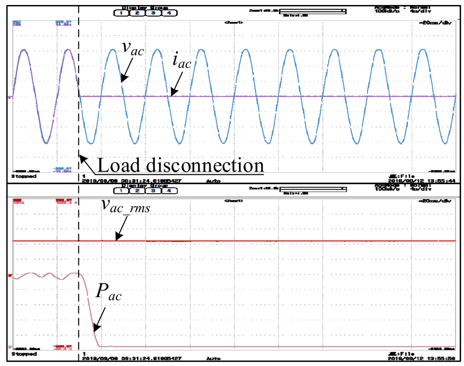
FIGURE 8. Illustration of laboratory setup: A — computers, B — dc sources, C — inverters, D — loads, and E — YOKOGAWA DL850.

III. SIMULATION RESULTS

Simulations have been performed with two 1-kW rated inverter systems in PLECS to validate the proposed method. The utilized parameters are listed in Table 1 for each system,



(a)



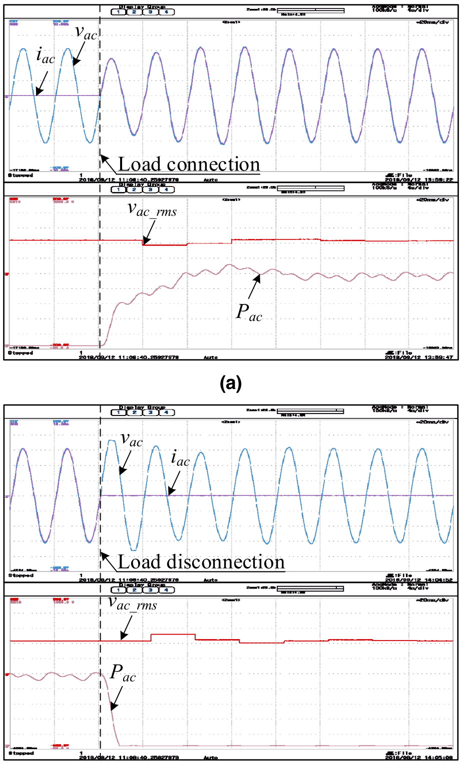
(b)

FIGURE 9. Experimental results of the proposed control for load variation, (a) load connection (b) load disconnection.

TABLE 1. Parameters used for testing.

Symbol	Quantity	Values
V_{dcn}	DC-link voltage amplitude	400 V
V_{0n}	Rated output voltage amplitude	311 V
f_{0n}	Rated frequency of the PV inverter	50 Hz
L_{acn}	Output filter inductance	5 mH
C_{acn}	Output filter capacitance	5 μF
f_{sn}	Inverter switching frequency	10 kHz
k_{pn}	Active droop coefficient	0.001 rad/(s•W)
k_{qn}	Reactive droop coefficient	0.001 V/Var

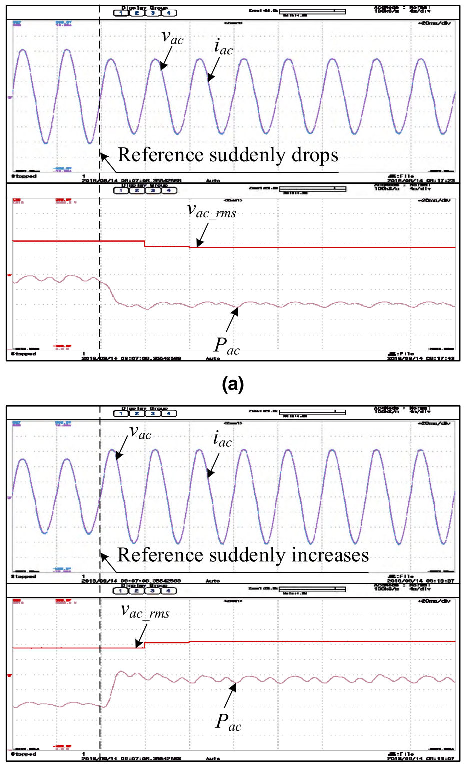
which are also the values used in the experimental results. The main purpose of the simulations is to verify the disturbance rejection and fast response to the load variation. In addition, the traditional multi-loop control and the proposed method have all been performed comparatively to verify the superiority of the proposed one. First, a 1-kW resistance load is used to verify the dynamic performance of the load variation. The load is connected to the inverter at t_1 and disconnected at t_2. The simulation results of the proposed method and the traditional multi-loop control method are shown in Fig. 4. Fig. 4(a) shows that the root-mean-square (rms) value v_{ac_rms} of the output voltage v_{ac} can change precisely according to the Eq. (8) by the proposed method and has only a voltage drop about 0.6 V (rms) when the load is connected. The output current i_{ac} and active power P_{ac} can be returned to



(a)

(b)

FIGURE 10. Experimental results of the traditional multi-loop control for load variation, (a) load connection (b) load disconnection.



(a)

(b)

FIGURE 11. Experimental results of the proposed control for reference voltage variation, (a) the reference voltage drops, (b) the reference voltage increases.

the steady state within 5 ms. The dynamic process of the load disturbance can almost be eliminated. However, v_{ac_rms} has dropped obviously (about 7 V (rms)) by the traditional multi-loop control when the load is connected as shown in Fig. 4 (b). The dynamic process of the output current i_{ac} and active power P_{ac} returned to the steady state can last more than 40 ms. Therefore, it can be inferred that the proposed control method has a better dynamic performance under load variation.

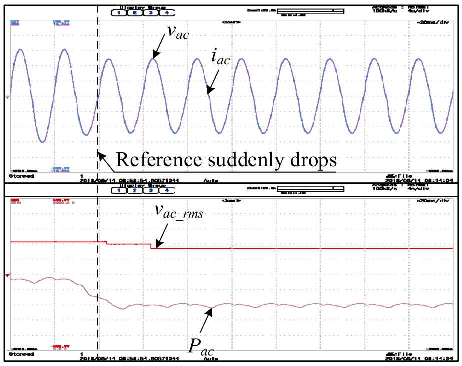
Second, Fig. 5 shows the simulation results of the two methods when the reference voltage varies. The amplitude of the reference voltage steps from 1 pu (311 V) to 0.8 pu at t_1 and steps from 0.8 pu to 1 pu at t_2. The reference voltage can still be tracked precisely by the proposed method as shown in Fig. 5(a), and i_{ac} and P_{ac} regain a steady state within 5 ms. Comparatively, the reference voltage also can be tracked by the traditional multi-loop control shown in Fig. 5(b), but the fluctuation of i_{ac} and P_{ac} will last about 20 ms. The greater the voltage reference is changed, the worse the fluctuation of i_{ac} and P_{ac} will be. Therefore, the proposed control method has a better performance of reference tracking.

To verify the robustness of the proposed control method, Fig. 6 shows the simulation results of the load variation for the proposed method with different system parameters (L_{acn} and C_{acn}). The performance of the system will not be affected when the parameters mismatch does not exceed 50%. When the parameters mismatch reaches 100% ($2L_{acn}$ and $2C_{acn}$), only the dynamic process will be affected slightly while the steady state won't be affected. The simulation results have demonstrated the proposed control method owns a strong robustness to the parameter uncertainties.

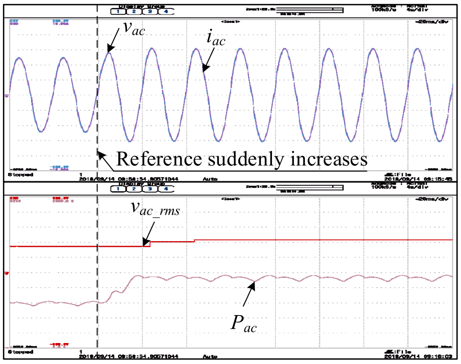
To verify the power sharing performance of the two control methods, Fig. 7 shows the simulation results of two inverters paralleled operation. The proposed control method can realize precisely the load power sharing within 5 ms without any fluctuation when the two inverters are connected or disconnected as shown in Fig. 7(a). However, for the traditional multi-loop control, the dynamic process of mode transfer will last about 30 ms with a power fluctuation shown in Fig. 7(b). The simulation results demonstrate that the proposed control method can improve the dynamic performance of paralleled inverters based on droop control.

IV. EXPERIMENT RESULTS

With the use of two 32-bit floating-point TMS320F28335 digital signal processors, two paralleled 1 kW inverter systems have been tested to verify the proposed disturbance rejection and dynamic process improvement with a STA control core. The sources for the two systems are from two Chroma 62150H-600S dc supplies. Fig. 8 shows the platform of the experiment, and its parameters are given in Table 1.

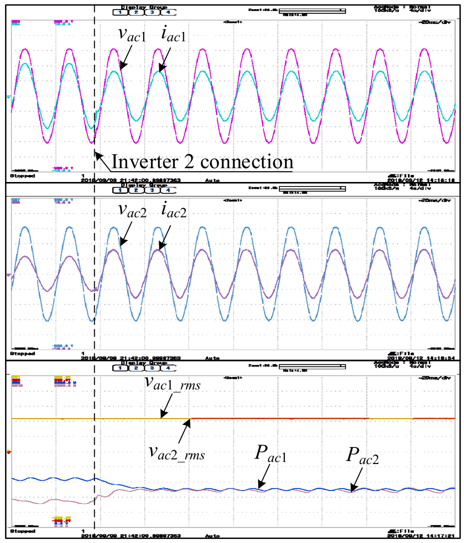


(a)

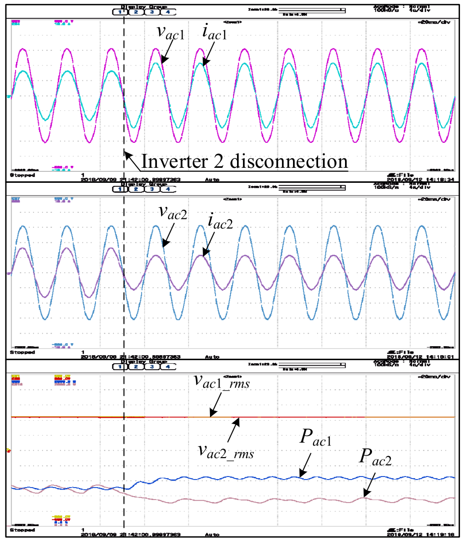


(b)

FIGURE 12. Experimental results of the traditional multi-loop control for reference voltage variation, (a) the reference voltage drops, (b) the reference voltage increases.



(a)



(b)

FIGURE 13. Experimental results of the proposed control for inverters paralleled operation, (a) connection (b) disconnection.

To verify the disturbance rejection and dynamic response of the proposed control method, a full power load is suddenly connected and disconnected to the inverter, respectively. Fig. 9 shows the experimental results of the proposed control for load variation. When the load is connected, the output voltage varies according to the droop line (peak voltage has decreased from $v_{ac} = 312.3$ V to 310.5 V), and the output current and the output power has both increased ($i_{ac} = 0$ A to 6.2 A and $P_{ac} = 0$ W to 963 W) within 10 ms. The dynamic process of output voltage can be improved effectively whenever the load is connected or disconnected. However, for the traditional multi-loop control shown in Fig. 10, the dynamic process of output voltage is longer (about 50 ms) and the voltage drop is much bigger at the instant of the load connection (peak voltage has decreased from $v_{ac} = 312.5$ V to 248 V). In addition, a big voltage overshoot has occurred when the load is disconnected, which may bring catastrophic results if there is not a limiter. Therefore, the proposed control method performs an excellent dynamic voltage quality with minor voltage drop and short transient time when the load varies.

It is important for a voltage-controlled inverter to track the reference. Therefore, the voltage reference can vary to adjust the power flow between the inverters. Figs. 11 and 12 show the experimental results of reference variation with the proposed control and the traditional multi-loop control. The dynamic process of output voltage is reduced significantly (about 10 ms) by the proposed method when the reference varies as shown in Fig. 11. Although the traditional multi-loop control can track the reference variation shown in Fig. 12, the dynamic process (about 30 ms) is long and tracking error still exists.

Figs. 13 and 14 show the experimental results of inverters mode transfer with the two control methods. The inverters supply power separately ($P_{ac1} = 669$ W and $P_{ac2} = 358$ W) before the inverter 2 connected. When the inverter 2 is connected, the output current i_{ac1} decreases from $i_{ac1} = 4.3$ A to 3.27 A, and the output current i_{ac2} increases from $i_{ac2} =$ 2.3A to 3.23 A. The inverters can share power faster (the dynamic process of load power sharing lasts about 20 ms) by the proposed control shown in Fig. 13(a) compared to the traditional multi-loop control (the dynamic process of load power sharing lasts about 40 ms) shown in Fig. 14(a)

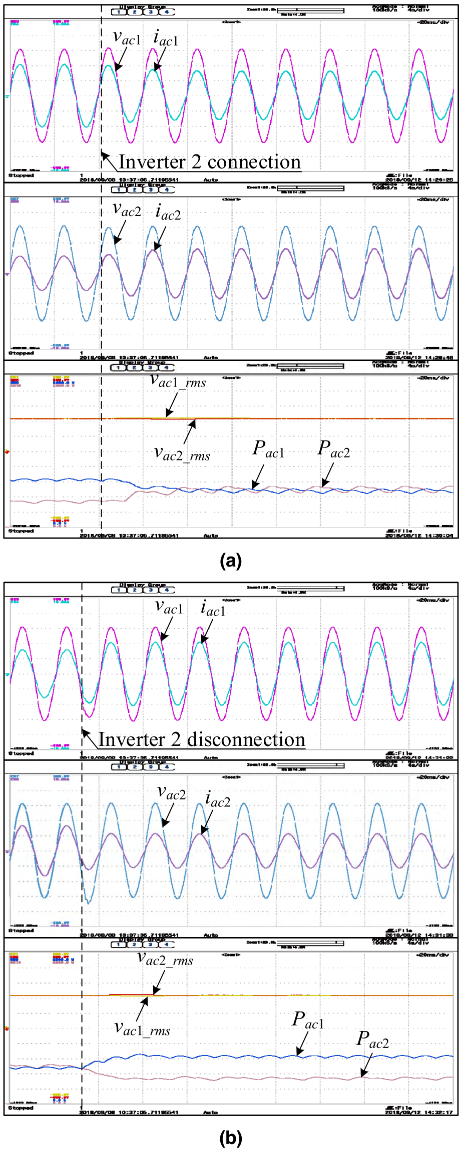


FIGURE 14. Experimental results of the traditional multi-loop control for inverters paralleled operation, (a) connection (b) disconnection.

when mode transfer from alone to parallel mode. Likewise, the same mode transfer has been observed in Figs. 13(b) and 14(b), during the return from parallel to alone mode. Upon being completed, the return causes the active powers to vary from power sharing (P_{ac1} = 508 W and P_{ac2} = 502 W) to their initial values (P_{ac1} = 667 W and P_{ac2} = 360 W). Conversely, the voltage overshoot (for v_{ac1}) or drop (for v_{ac2}) has occurred in the dynamic process shown in Fig. 14(b), but it cannot be seen in Fig. 13(b). Hence, the experimental results shown in Fig. 13 prove that the dynamic performance of paralleled inverters system based on droop control can be improved by the proposed control method.

A performance comparison between proposed and traditional control can be observed in Table 2. It should be mentioned that the proposed control method has a better performance of dynamic response and disturbance rejection.

TABLE 2. Performance comparison between proposed and traditional control.

Method	case	Features		
		dynamic process (ms)	voltage overshoot	voltage drop
proposed control	load variation	10	×	×
	reference variation	10	×	×
	parallel operation	20	×	×
traditional control	load variation	50	√	√
	reference variation	30	×	×
	parallel operation	40	√	√

V. CONCLUSION

Based on STA, a disturbance rejection control for droop-controlled paralleled inverters system has been proposed in this paper. Although the gains of the STA controllers are reduced, the control performances are not deteriorated. The designed STA-based voltage controller and current controller contain output current and output voltage terms, respectively, which can all be regard as the feedforward, to improve the transient process under load variation, voltage reference change and mode transfer. Moreover, the proposed controller is robust and insensitive to the parameters mismatch. The effectiveness of the proposed control method has been demonstrated by extensive simulations and experiments.

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