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Real-Time Response-Based Fault Analysis and Prognostics Techniques of Nonisolated DC–DC Converters

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ABSTRACT DC–dc converters have been extensively used in industrial systems and their failure may cause the systems to work abnormally and even accidents. Current research on circuit fault analysis is mainly based on a model or complex signal processing. In order to avoid modeling difficulties and complex selection of signal processing methods, a fault analysis method based on circuit output signal is proposed in this paper, which can judge the circuit health status by directly monitoring the circuit response. This method of monitoring output signal also avoids the problem of inconvenient access to internal nodes of the converter circuit. By continuously monitoring the output voltage, two advantages are simultaneously achieved: 1) the fault components range of an abnormal circuit is located and 2) its remaining useful performance (RUP) can be predicted. The particle filter algorithm commonly used to predict RUP often encounters the problem of particle degeneracy, which leads to the decrease of particle diversity and makes the final RUP prediction accuracy lower. In view of this problem, the developed novel way of RUP prediction by monitoring the circuit output voltage is based on a newly developed conditional particle filter, which tracks the degradation process of the circuit according to collected historical degeneration data. The case studies of two dc–dc converter circuits show that the developed fault analysis method can easily analyze the fault condition of the converter circuits and the improved particle filter algorithm achieves excellent prediction accuracy.

INDEX TERMS DC-DC converter, fault analysis, fault identification, failure prognosis, exemplar-based conditional particle filter.

I. INTRODUCTION

Power electronic converters for energy conversion have been applied not only in the entire electrical field but also widely used in other related fields due to its high efficiency, control flexibility, and easy implementation [1]. As a common type of power electronic converter, DC-DC converters are prone to suffer from critical failures mainly because of different operational and environmental conditions (such as strong-vibration environments, high-temperature), frequently changing component values in tolerance, and complicated failure mechanisms (such as soldering joint problems).

Effective fault diagnostics of converter circuit is the basic requirement to ensure the safe operation of the system. The research in converter diagnostics can be classified into three types. The first one is aiming at independent component in converter circuits. Several statistical studies show that capacitors, semiconductor power switches are the main components for critical failures [2]. Several studies on fault diagnosis or identification of capacitors in converters have been developed in [3]–[5]. Moreover, semiconductor power switches like transistors are analyzed separately. For example, a fault diagnosis method for power transistors in power converters and a precursor parameter identification method for insulated gate bipolar transistor were developed in [6] and [7], respectively. The second type features the open- and short-circuits. Open-circuit fault detection and tolerant operation for a parallel-connected single active bridge DC-DC converter were conducted in [8]. An open- and short-circuit switch fault diagnosis method for nonisolated DC-DC

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converters using field programmable gate array was developed in [9]. A DC short fault of Modular DC-DC Converter is analyzed by employing a new submodule with damping-resistor in [10]. In addition to the above two types of fault diagnosis methods for specific devices and specific fault types, some studies focus on the fault diagnosis of converter circuits from the perspectives of signal analysis [11], data processing [12]–[14], and model building [15]. Among them, the methods based on signal analysis and model building require expert knowledge of circuit principles, while the methods based on data processing have high dependence on algorithm selection. Therefore, this paper proposes a brand new method to judge the health status of a DC-DC converter circuit by monitoring its output signals.

In this paper, we mainly consider the degradation failure of the circuit components, a new fault analysis method is proposed for DC-DC converter circuits. Degradation failure refers to the failure caused by the degradation or aging of components in system. It is also be called soft fault failure or parametric failure. This failure mode makes the converter mainly show phenomena of function degradation, i.e., decay of life. Unlike a large number of existing complex fault diagnosis methods based on data processing, in this work, only the responses of DC-DC converter circuits are measured in real time, and internal testing nodes of circuits are not required so that this method can analyze the fault condition of complicated converter circuits. Meanwhile, a fault-indicating curve that does not require feature normalization or scaling is introduced.

Besides fault diagnosis, another effective way for system safety is fault prognosis which provides early warning of failure and enables forecasting of system maintenance. Prognostics for a circuit refer to a prediction of the time when the circuit will no longer be capable of performing its intended function [16]. This lack of performance is often a failure beyond which the circuits can no longer be used to meet desired performance such as filtering [17]. The predicted time then becomes the remaining useful performance (RUP) guaranteeing system operation in the case of analog circuits. There are several works on prognostics techniques for individual components such as capacitor in a filter circuit, aiming at predicting the future performance of a component by assessing the extent of deviation or degradation of a whole circuit from its expected normal operating conditions. But it is technically inaccessible to set a uniform failure threshold or fault indicator for all the critical components in a circuit to predict the RUP of the whole circuit because each component serves a totally different role in the whole circuit.

In recent years, there are seldom works for prognostics of converter circuits. Generally, the performance degradation model is established by assuming that the components drift gradually over time to simulate the operating conditions. Specifically, a general nonlinear stochastic process with a time-dependent drift coefficient is adopted to characterize the dynamics and nonlinearity of the degradation process. The particle filter (PF) is often employed to predict the RUP of systems because of its strong ability to deal with non-linear problems [18], [19], whose state-space model has unknown parameters. However, particle degeneracy is a common phenomenon for the PF-based methods, where most particles will have negligible weights after a few iterations [20]. Resampling methods are frequently adopted to avoid particle degeneracy, but suffer from particle impoverishment [21], since resampling schemes reduce the diversity of the particles. These drawbacks may result in inaccurate RUP estimation for DC-DC converter circuits. Moreover, most existing PF-based methods can only process a fixed number of samples during the entire filtering time. Therefore, PF needs to bear a large computational load, and the computation efficiency will be reduced, which is not conducive to the real-time system.

This paper developed a novel framework based on particle learning (PL) to update the prediction model for RUP prediction of DC-DC converter circuits. The PL framework adopts a resampling-propagation strategy that inverts the PF procedure. With effective use of the current measurement information, particle decay is avoided, and consequently, the error of RUP estimation is reduced. The PL framework can adaptively and dynamically adjust the number of particles to reduce the running time of the algorithm and increase online efficiency. In the PL framework, the parameters of the prediction model are regarded as a part of the joint state. They can be propagated together with the true state. Accordingly, it is suitable for online applications. The flowchart of the proposed methods is shown in Fig. 1. The work is composed of two processes: one runs offline for constructing a fault-indicating curve by inputting a 12V DC power and the other is to monitor circuit outputs online during field operation.

In summary, the contributions of our approach are summarized below:

1) Sensitive components are screened from the circuit with reference to the converter circuit output. A feature that directly reflects the health of the converter circuit is extracted from the circuit response as a basis for fault analysis. The fault components range of the circuit can be located by directly monitoring the response of the circuit.
2) A failure prognostics method is proposed in which historical degradation data is considered to be a prior exemplar. This prognostics method achieves accurate tracking of performance degradation trends and accurate RUP prediction.

This paper is organized as follows. Section II introduces Voa (output average voltage) based fault identification. Section III describes how to realize failure prognostics. Case studies and experimental results are shown in Section IV. Section V concludes the whole work.

II. VOA-BASED FAULT ANALYSIS

A. SENSITIVE COMPONENTS DETERMINATION

DC-DC converter achieves switching mode power suppling by turning on and off power semiconductor device periodically. Fig. 2 gives the basic DC-DC buck converter circuit

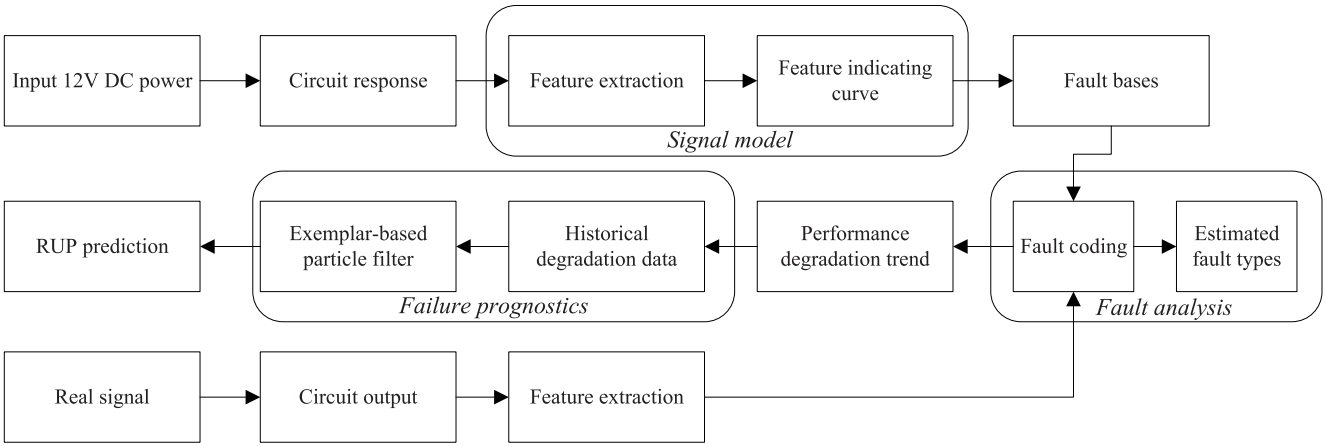

FIGURE 1. Overview of the proposed fault analysis and prognostics method for DC-DC converter circuits.

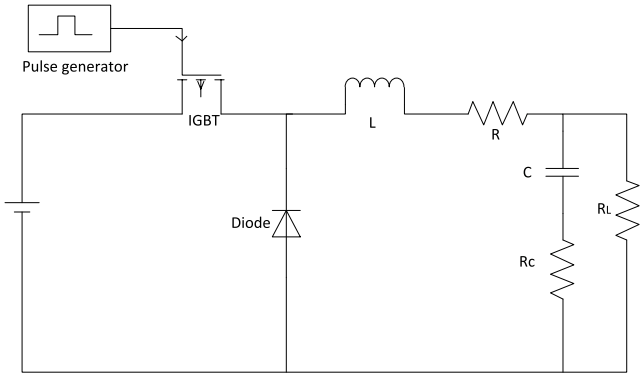

FIGURE 2. Basic DC-DC buck converter circuit schematic diagram.

schematic diagram. DC-DC converters contain three modules usually: i) switching device, IGBT and BJT etc., turning on and off persistently; ii) diode for rectifying; iii) inductor and capacitor for filtering. Typically, the output DC voltage is doped with a minor ripple voltage. Every component in the circuit plays its specific role in converter's operation. Therefore, fault or failure of any one component can affect the function of the converter. However, not all components are equally critical to the circuit output that is most concerned. Some components are more sensitive to the circuit output, which means that small changes in the parameter value of these components will result in larger changes in the circuit output than those of others. These components are called sensitive components in DC-DC converter circuit. The selection of sensitive components is conducted by simulation and theoretical analysis of the converter circuit. Through the analysis of the working principle of the circuit, we can roughly screen out the devices which have great influence on the circuit function in theory, and then lock the sensitive devices in combination with the ''analysis'' function of the software. For instance, components L and C are confirmed as sensitive components in Fig. 2 since the output voltage (V_O) is obviously affected when the device parameter value changes.

B. THEORETICAL BACKGROUND OF VOA CURVE

Operating principle of converters are based on the periodic switching of the power semiconductor device, which results from periodicity of driving signal. The period T of driving signal is

$$T = \frac{1}{f_s} \tag{1}$$

where f_s is the frequency of on-off, which directly determined by the frequency of driving signal. PWM wave is chosen to be the driving signal in the basic DC-DC converter circuit in Fig. 2 while pulse-width-modulation control circuit chips, like TL494 developed by TI, are usually employed to produce driving signal in converters in practical application. The impedance of capacitor C are named R_C, which is calculated by the following equation:

$$R_C = \frac{V_O}{di_L} = \frac{V_{pp}}{0.2I_N} \tag{2}$$

where V_O is output average voltage when the output of circuit is stable, di_L is variation of inductor L in an operating period, V_{pp} is peak to peak ripple value of output voltage and I_N is output current value. The product of C and R_C is decided when a DC-DC converter is designing. Therefore C is attained for the determination of R_C. When power semiconductor device is on the state of switch-on. The following equation is true:

$$V_{IN} - V_O - V_L - V_{ON} = \frac{L \cdot di_L}{T_{ON}} \tag{3}$$

where V_L is resistance voltage dropping in inductor L, V_{ON} is forward voltage of power semiconductor device and T_{ON} is switch-on time in a period of power semiconductor device, which adds T_{OFF} equals T. Similarly, when power semiconductor device is on the state of switch-off, the following equation is attained:

$$V_O + V_L + V_D = \frac{L \cdot di_L}{T_{OFF}} \tag{4}$$

where V_D is forward voltage of diode for rectification. Inductance of L for filtering can be expressed as the following equation according to Eqs.3 and 4:

$$L = T_{ON} \frac{V_{IN} - V_O - V_L - V_D}{di_L} \tag{5}$$

Herein, all components' parameter values are got. It is reasonable that the Voa will not agree with the Voa designed. The Voa will be larger than 5V if inductance value of L decreases in 12-5V DC-DC converter circuit. The circuit will be faulty when Voa beyond 5% larger than 5V and the inductance value of L is faulty value at this time. Required filtering effect will not be reached if inductance value of L decreases from principle of operation perspective.

C. FAULT ANALYSIS BASED ON VOA

The function of a DC-DC converter circuit is to output a specific voltage value, so the output voltage value directly reflects the health of the DC-DC converter circuit. In this paper, by directly monitoring the response of the circuit, namely the output voltage, fault analysis is conducted, which avoids the inconvenience of deploying test nodes in the circuit. Here we only extract the circuit output average voltage (Voa) as the only feature of circuit's performance. The circuit output average voltage is measured and characterized as meaningful feature, which forms a fault-indicating curve in the feature plane during changing the deviations from the nominal value of each sensitive component gradually and continuously. The process runs in the case wherein the values of other components stay nominal. The extracted feature and fault-indicating curve only depends on outputs of the test signal. Feature points on the fault-indicating curve are considered as over-complete fault bases. In each fault case, a corresponding fault-indicating curve is generated in turn for fault analysis.

The output voltage wave changes when a fault occurs in the DC-DC converter circuit under test, and the change is related to sensitive components and the level of degradation. For instance, when the parameter of the sensitive component L in the basic DC-DC buck converter circuit is changed, the difference of the output voltage waveform is as shown in Fig. 3, the blue line corresponds to the case where the inductance value of the device L is normal, and the green line and the red line correspond to the inductance value of the device L deviates from normal condition. For different sensitive components in a DC-DC buck converter, the effect on the output voltage of the circuit is different, which provides the basis for analyzing the fault class according to the circuit output voltage.

The real-time circuit output fault analysis in field operation is realized by a series of fault-indicating curves which are pre-constructed and stored in the factory setting. Each curve is related to a critical component, and different curve segments indicate its fault levels including normal condition, faulty condition, and failure condition. After fault-indicating curves of all the sensitive components in a circuit are built,

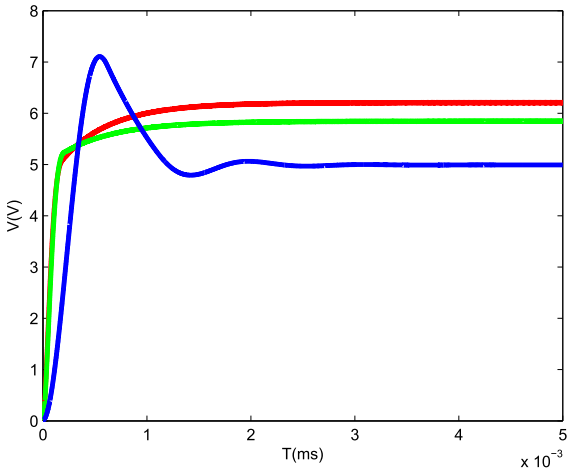

FIGURE 3. Different output voltage waveforms corresponding to different L fault levels.

the response of the circuit is monitored during field operation. The new feature Voa is extracted in real time by sampling output signals with a high sampling rate. Comparing the collected Voa with the rated output voltage value and then all possible fault classes can be analyzed by comparison with all fault-indicating curves established in advance. The severity of the fault component can be inferred based on the extent to which Voa deviates from the rated output voltage value.

III. FAILURE PROGNOSTICS

For the degradation failure studied in this paper, the fault and failure of a component is an accumulated result. That is to say, before a component fails, the circuit has shown corresponding symptoms, which can be reflected in the response of the circuit. Continuous monitoring of the key feature of the circuit response, i.e., Voa, can constitute a fault-indicating curve to measure system degradation during field operation after the module of failure prognostics is triggered. The performance degradation trend is tracked to predict the RUP. During prediction, historical degradation experience collected previously are also considered for improving robustness and accuracy, and the proposed exemplar-based conditional particle filter can handle these data and take full consideration of converting these past data to valuable information.

A. PERFORMANCE DEGRADATION TRENDS

The fault feature Voa can capture the variation of component value and fault level dynamically. When the fault level reveals serious status, the Voa value changes largely from an initial code near the nominal value of the component. Furthermore, when the value of a critical component rises or drops from the initial spot in the Voa curves, the fault feature value moves along special direction of its fault-indicating curve. This result reflects the degradation (up or down) of the analyzed component in a qualitative way. The fault indicator deviates from 5V to a threshold when the fault level of the DC-DC converter circuit increases from normal status to

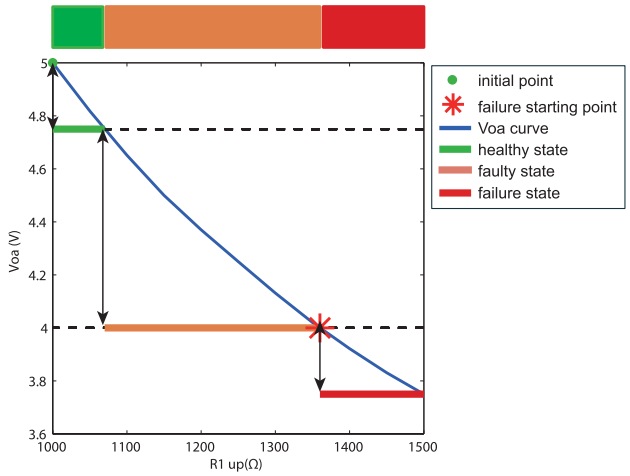

FIGURE 4. The performance degradation trend of basic DC-DC buck converter circuit.

complete failure. Fig. 4 shows the performance degradation trend represented by the fault indicator, where the value of one component deviates from its nominal value gradually. The component value deviates up from its nominal value, and rises with a specific step in each cycle, which is considered as a time index here. Hence, continuous variations in the fault indicator are realized with time. Each variation simulates a hypothetical degradation process in which one component fails gradually, resulting from exterior environmental influences, but practical degradation during field operation may be more complicated than anticipated.

B. PERFORMANCE PROGNOSTICS

By the circuit designer's definition, RUP refers to useful performance from the current time to the end of performance. When the circuit does not contribute to the overall system it means that the circuit life will be terminated, (e.g., output voltage value too low lead to the termination of system operation). Consequently, prediction of RUP is more meaningful for DC-DC converter circuits.

The performance of the converter circuit degrades gradually with its continuous operation. RUP can be estimated by measuring performance degradation trend and converting it into observations and updates. Generally, statistical prognostic approaches are used to estimate RUP. Some non-linear and non-Gaussian methods have been developed to solve the problem of real-time estimation of RUP for a given performance degradation trend. For example, sequential importance sampling, a Monte Carlo method, can used to calculate the probability density function (PDF) of parameters in nonlinear models. Particle filter (PF) is seen as a Monte Carlo approximation to Bayesian estimation, so it has become a popular method. Since the concept of resampling emerged, it has overcome the problem of particle degradation. This Monte Carlo method (PF) has been widely used to make the estimation for nonlinear and non-Gaussian systems. In this paper, a RUP prognostics method is proposed based on the theory of particle filter, which is described as follows.

1) OPTIMAL BAYESIAN ESTIMATION

The state model of dynamic system can be represented by the following two equations:

$$x_k = f_k(x_{k-1}, u_{k-1}) \tag{6}$$

$$y_k = h_k(x_k, w_k) \tag{7}$$

$x_k \in \mathbf{R^{n_x}}$ is the state at k-th time with n_x dimensions. f_k: the nonlinear state equation. $y_k \in \mathbf{R^{n_y}}$ is the k-th time (cycle) step observation and it has n_y dimensions. h_k is the measurement equation at k-th time (cycle) step, u_{k-1} and w_k are the independent and identically distributed (i.i.d.) process noise sequence and measurement noise sequence, respectively.

We assume that the state x_k is the first-order Markov process, and the initial state x_0 follows the prior distribution $p(x_0 \mid y_0) = p(x_0)$. In the predicting phase, we assume that the posterior probability density function (PDF) $p(x_{k-1} \mid y_{1:k-1})$ at time (cycle) $k-1$ has been known. The prior PDF $p(x_k \mid y_{1:k-1})$ without the observation at cycle k can be calculated as the following equation.

$$p(x_k \mid y_{1:k-1}) = \int p(x_k \mid x_{k-1}) p(x_{k-1} \mid y_{1:k-1}) dx_{k-1} \tag{8}$$

In the update phase, when the measurement y_k can be obtained at time (cycle) k, the posterior PDF can be calculated as follows.

$$p(x_k \mid y_{1:k}) = \frac{p(y_k \mid x_k) p(x_k \mid y_{1:k-1})}{\int p(y_k \mid x_k) p(x_k \mid y_{1:k-1}) dx_k} \tag{9}$$

The iteration between Eqs. 8 and 9 forms the optimal Bayesian estimation. However, it is difficult to get analytic solutions for the complex integration in the state space, especially for non-gaussian and nonlinear systems.

2) PARTICLE FILTER

Particle filter is commonly used to approximate nonlinear filters in PHM field. A set of i.i.d. state samples $\{x_{0:k}^1, x_{0:k}^2, x_{0:k}^3, \ldots, x_{0:k}^N\}$ from $p(x_{0:k} \mid y_{1:k})$ can represent the posterior PDF.

$$p(x_{0:k} \mid y_{1:k}) \approx \frac{1}{N} \sum_{i=1}^{N} \delta(x_{0:k} - x_{0:k}^i) \tag{10}$$

where $\delta(\cdot)$ is the Dirac function. However, it is general to sample from an easily implemented distribution $q(x_{0:k} \mid y_{1:k})$ (also known as the proposal distribution) rather than from the posterior PDF, so that a posterior PDF can be estimated from the sample.

$$p(x_{0:k} \mid y_{1:k}) \approx \sum_{i=1}^{N} \overline{w}_k^i \delta(x_{0:k} - x_{0:k}^i) \tag{11}$$

As N approaches infinity both sides of this equation are equal.

$$\begin{aligned} \overline{w}_k^i &= \frac{w_k^i}{\sum_{j=1}^{N} w_k^j} \\ w_k^i &= \frac{p(y_{1:k} \mid x_{0:k}^i) p(x_{0:k}^i)}{q(x_{0:k}^i \mid y_{1:k})} \end{aligned} \tag{12}$$

Eq. 12 can be further written as

$$w_k^i = w_{k-1}^i \frac{p(y_k \mid x_k^i)p(x_k^i \mid x_{k-1}^i)}{q(x_k^i \mid x_{k-1}^i, y_{1:k})} \tag{13}$$

The estimated state $\overline{x}_k$ at time (cycle) k can be calculated by the equation.

$$\overline{x}_k = \sum_{i=1}^{N} \overline{w}_k^i x_k^i \tag{14}$$

3) EXEMPLAR-BASED CONDITIONAL PARTICLE FILTER

Based on the particle filter, the proposed prognostic algorithm takes into account historical degradation data possibly suffering from various disturbances (such as environmental temperature, system noise, working current, and vibration). The simulation of disturbance in a probabilistic way is realized by changing component values in tolerance, and obtaining a certain amount of historical degradation data as exemplars. Estimation effects can be improved by particle filter working conditionally under the supervision of these exemplars. Hence, the developed exemplar-based conditional particle filter calculates the weight of particles by combining historical degradation data of the same component with filtering stage. The details of the proposed method are as follows.

The state model of the system is given by Eqs. 6 and 7. According to the Monte Carlo method, the posterior distribution is approximated by a weighted sum of N samples drawn from the posterior distribution, where

$$p(x_k \mid y_{1:k}, Y_{exem1:k}) \approx \frac{1}{N} \sum_{i=1}^{N} \delta(x_{0:k} - x_{0:k}^i) \tag{15}$$

where Y_{exem} is the mean of multiple curves formed by sampled historical data under different operating conditions, which are simulated by changing component values randomly within their tolerances. $Y_{exem1:k}$ denote known example values on the mean curve from 1 to k. It is worth noting that these samples are different from real-time running data $y_{1:k}$. The posterior distribution can be estimated by the following equation when the samples are drawn from the proposal distribution.

$$p(x_{0:k} \mid y_{1:k}, Y_{exem1:k}) \approx \sum_{i=1}^{N} \overline{w}_k^i \delta(x_{0:k} - x_{0:k}^i), \tag{16}$$

$$\overline{w}_k^i = \frac{w_k^i}{\sum_{j=1}^{N} w_k^j}$$

$$w_k = \frac{p(y_{1:k} \mid x_{0:k}, Y_{exem1:k})p(x_{0:k} \mid Y_{exem1:k})}{q(x_{0:k} \mid y_{1:k}, Y_{exem1:k})} \tag{17}$$

Eq. 17 can be rewritten as follows according to the Bayesian rules

$$w_k = w_{k-1} \frac{p(y_k \mid x_k, Y_{exem1:k})p(x_k \mid x_{k-1}, Y_{exem1:k})}{q(x_k \mid x_{0:k-1}, y_{1:k}, Y_{exem1:k})} \tag{18}$$

The weight with respect to every particle is

$$w_k^i = w_{k-1}^i \frac{p(y_k \mid x_k^i, Y_{exem1:k})p(x_k^i \mid x_{k-1}^i, Y_{exem1:k})}{q(x_k^i \mid x_{0:k-1}^i, y_{1:k}, Y_{exem1:k})} \tag{19}$$

For Eq. 19, we have the following assumption:

$$p(x_k^i \mid x_{k-1}^i, Y_{exem1:k}) = p(x_k^i \mid x_{k-1}^i) \tag{20}$$

$$q(x_k^i \mid x_{0:k-1}^i, y_{1:k}, Y_{exem1:k}) = p(x_k^i \mid x_{k-1}^i) \tag{21}$$

Eq. 21 is the so-called proposal distribution. We join Eqs. 20 and 21 into Eq. 19.

$$w_k^i = w_{k-1}^i p(y_k \mid x_k^i, Y_{exem1:k}) \tag{22}$$

Eq. 22 indicates that when calculating the weight in the update phase, not only the filtered data of current degradation, should be considered, but also the historical degradation data of the same component under different experiment conditions (such as environmental temperature, system noise, working current, and vibration) should be taken into consideration. These variable conditions are eventually reflected by random changes in the range of component tolerance. Specifically, there are three steps performed. To compute y_k using x_k^i according to the measurement function is the first step. Then the best observation y', which is closest to y_k, is selected among the observation which belongs to the data of current degradation at cycle$k$ and Y_k from $Y_{exem1:k}$ at cycle k. y_k and y' are put into inputs to compute the weight with respect to the particle finally.

Therefore, the state can be estimated as Eq. 23

$$\overline{x}_k = \sum_{i=1}^{N} \overline{w}_k^i x_k^i \tag{23}$$

IV. IMPLEMENTATION RESULTS AND DISCUSSION

Case studies on two DC-DC converter circuits demonstrating the proposed fault analysis and RUP prognostics method are presented. The tested circuits include a DC-DC converter based on MC34063a and a DC-DC converter based on TL494, where both SPICE models and real circuits are established. These two circuit diagrams are shown in Fig. 5 and 6, where the nominal values of circuit components are marked. Fig. 7 is the experimental environment built for the real circuits.

Tolerance, Fault, and Failure: This experiment ran in the presence of component tolerances. The definitions of tolerances and faults are not unique, but they need to be defined before specific experiments. One viewpoint is that a circuit element with 50% deviation from its nominal value should be considered to be faulty, regardless of its tolerance range. Another viewpoint is that a circuit is faulty when its critical elements deviate beyond their tolerance range, which includes three cases: a tolerance of 1% for all the components, 5% for resistors, and 10% for capacitors adopted in previous works, or 10% for both resistors and capacitors. This paper does not adopt any viewpoint referred above, but considers this problem from a new aspect of the Voa when the circuit

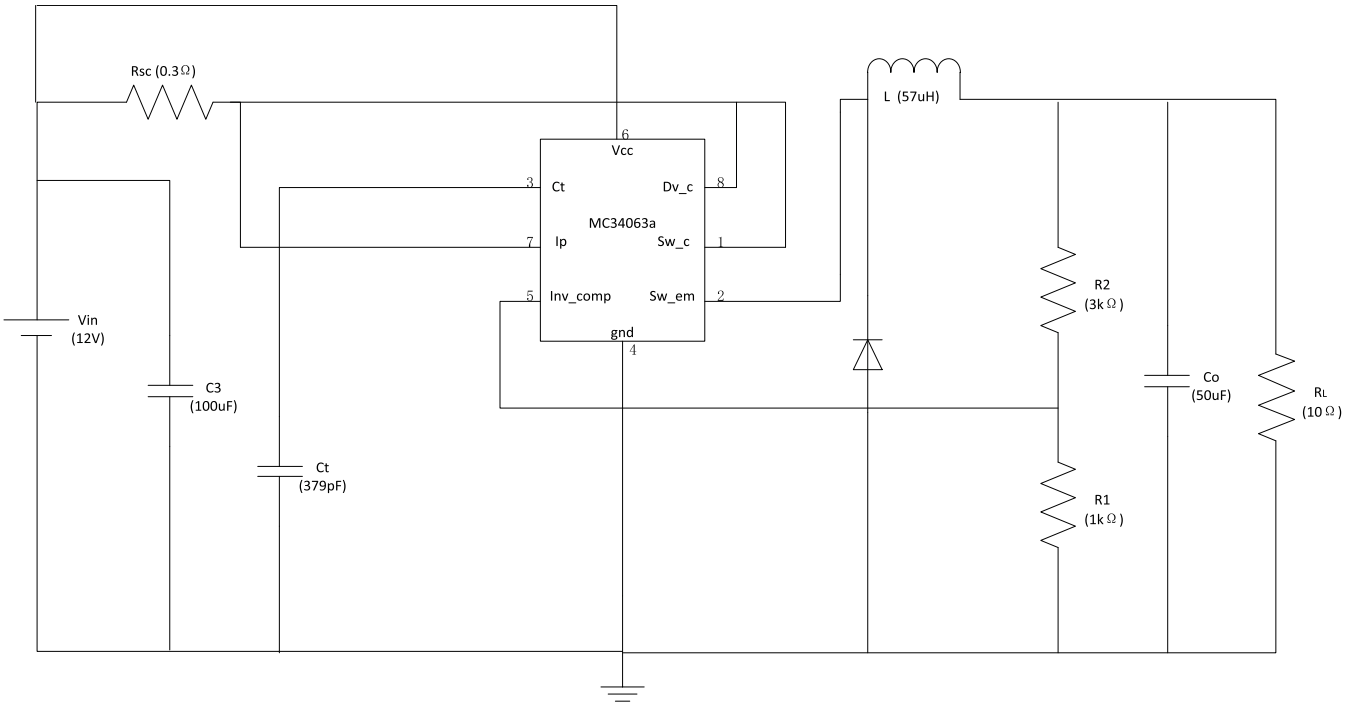

FIGURE 5. DC-DC converter based on MC34063a.

works stably. The DC-DC converter circuits are aiming to provide constant output voltage, so the Voa of this type of circuit is the most concerned issue for users or customers. The criterion about the converters of 5V output voltage is that the tolerance of output voltage is 5%. Therefore, we define that a converter circuit is considered to be faulty if the Voa has deviated beyond the tolerance range of 5%, and the converter circuit reaches complete failure if the Voa has exceeded a predefined failure threshold (e.g., 20% deviation from its nominal value). The threshold is defined according to function loss of converters.

Experimental Setup: The experimental equipment is demonstrated in Fig. 7, which consists of power supply, a digital oscilloscope, a DC-DC converter based on MC34063a or a DC-DC converter based on TL494 as the testing sample circuit, a data acquisition board of National Instruments for AD conversion, and Labview software for recording the acquired data. The input is a DC 12V supply power. For each circuit, some sensitive components are chosen to demonstrate the proposed approach. In the DC-DC converter based on MC34063a, R1, R2, Ct and Rsc are chosen as sensitive components, and L1, R11, R12 and R13 are selected in the DC-DC converter based on TL494.

A. TWO IMPLEMENTED DC-DC CONVERTER CIRCUITS

1) CASE 1. DC-DC CONVERTER BASED ON MC34063A

A DC-DC converter based on MC34063a shown in Fig. 5 aims to converter DC 12V into DC 5V. MC34063a is a DC to DC converter control circuit, which takes the place of PWM generator in the basic DC-DC converter. Although both of these two circuits are converting DC 12V to DC 5V essentially, the constituent parts of modules are different to an extent. For example, the most obvious is that, MC34063a chip contains a switch inside already, correspondingly, electronic semiconductor device like IGBT is not contained in its external circuit, resulting in the DC-DC converter based on MC34063a simply constructed. It should be noted that Co is the output filtering capacitor of the DC-DC circuit, while R1 and R2 are two dividing feedback resistors. i.e., R1 and R2 will influence the magnitude of the output voltage, and Co will affect the size of the output voltage ripple.

2) CASE 2. DC-DC CONVERTER BASED ON TL494

As shown in Fig. 6, the circuit is also a switching circuit of DC 12V to DC 5V but more complex than DC-DC converter based on MC34063a superficially. The input side of the circuit is 12V DC input voltage supply, and the voltage across the resistor load is DC 5V. TL494 chip is essentially a pulse-width-modulation control circuit. It achieves voltage reduce by controlling a P channel MOSFET on and off periodically, then the gotten voltage will be rectified by a high-frequency rectifier, i.e., Schottky diode D. Finally the output voltage ripple will be reduced by an output filtering capacitor Co and the filtering inductor L. It should be noted that, R6 is a resistor for protecting the switch transistor Q2, R14 is a compensation resistor to help control and adjust the output voltage. R11 is a resistor for current sampling. There are two error amplifiers in the TL494 chip. The node between R12 and R13 is connected with pin 15, and its voltage is the reference voltage for current feedback.

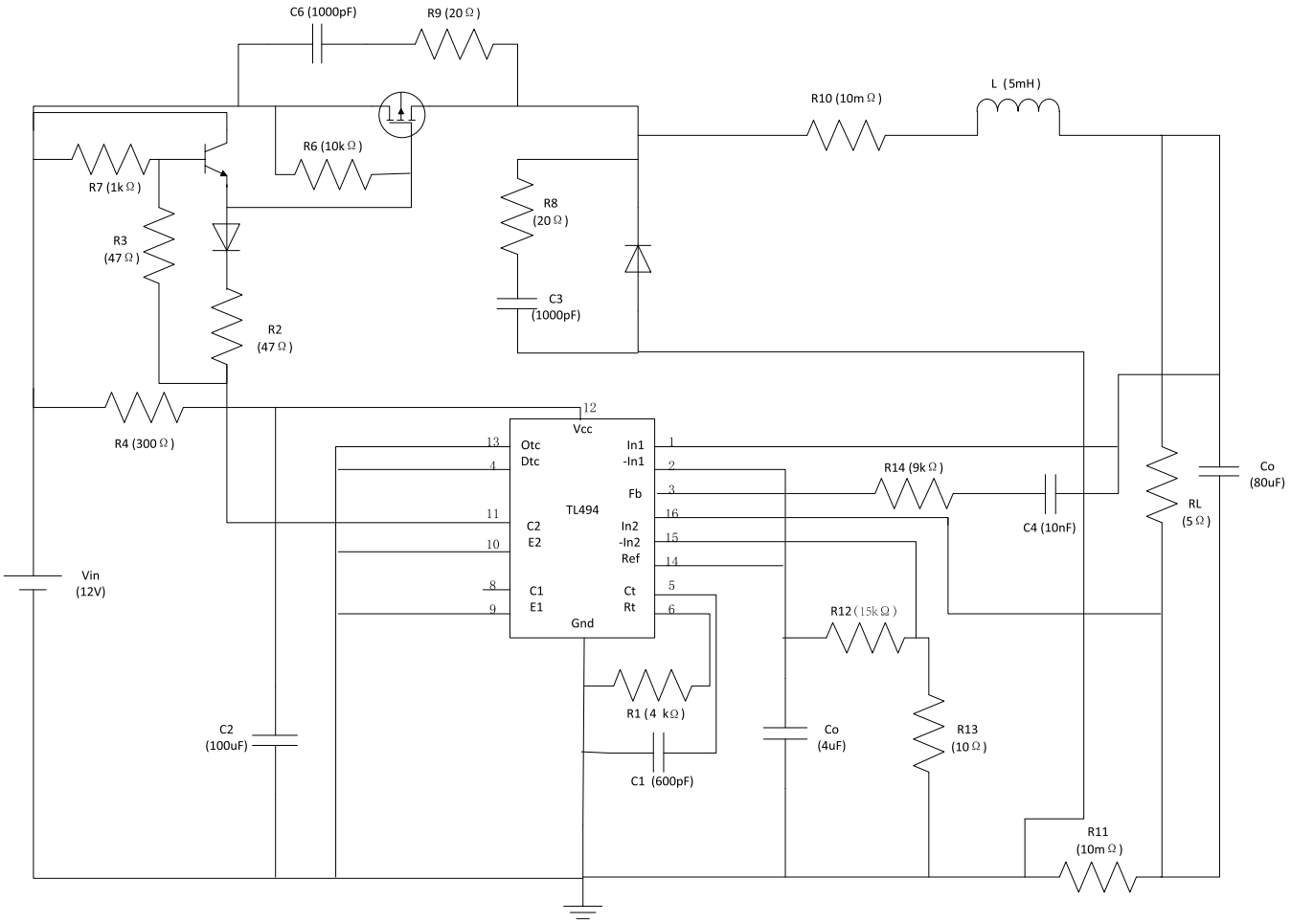

FIGURE 6. DC-DC converter based on TL494.

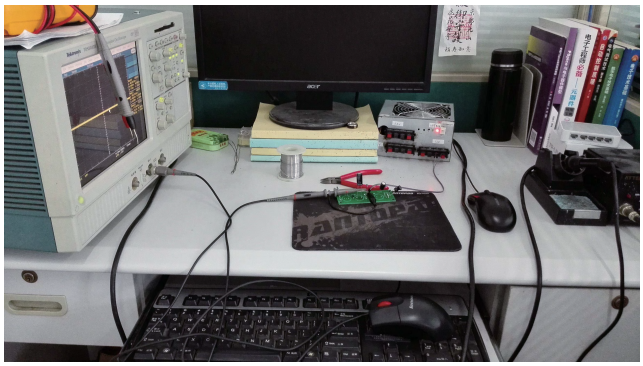

FIGURE 7. Experiment setup.

B. SENSITIVE COMPONENTS DETERMINATION

1) DC-DC CONVERTER BASED ON MC34063A

R1 and R2 in DC-DC converter based on MC34063a are voltage feedback resistors which are monitoring the output voltage at every moment to deliver the output signal to the MC34063a chip for the following actions of the DC-DC converter, and the node between R1 and R2 is connected with inverter-comparator pin of the MC34063a chip. Therefore, the output voltage will change once resistor value of R1 and R2 deviates from their nominal value respectively. As for Ct, the timing capacitor in this converter circuit, which connects with ct pin of the MC34063a chip, it is closely relevant to the operation frequency of the chip and then the whole converter. Rsc, connecting with ipk pin of the MC34063a chip, decides the permitted current value between pin 6 and pin 7. The chip will start up protection function once the voltage between pin 6 and pin 7 goes beyond 300 millivolts. The only diode D1 in the circuit is for rectifying and capacitor C1 and Co are both for filtering of voltage, which will reduce the size of voltage ripple wave. Inductor L also manages the output voltage for the last step. A resistor RL is chosen to be the load of this converter, whose value is 5Ω, for the designed output current is 1A.

2) DC-DC CONVERTER BASED ON TL494

Appropriate inductance of L in this converter will help to embellish Voa for the last step, which denotes the Voa will be stable and balanced. Inductor should reset successfully in every period in the cycle of switch on and off. Therefore, the schematic will not be an effective topology if the

inductance of L is too little. R11 in this circuit is a current sampling resistor as referred above. Actually R1 and RL separate the voltage of negative side of L. So it's reasonable that Voa will decrease when R11 increases. What's more, node voltage between R12 and R13 is the reference voltage for current feedback, so there is the same effect either R12 increase or R13 decreases. For instance, if resistance value of R13 reduces, voltage in pin 15 drawn in will decreases as a result. Voltage of pin 16 of the TL494 chip, which is called inverter-comparator 2, will required decrease by external adjustments in the chip and then the converter circuit to make the difference of pin 15 and 16 tends to a smaller value. Qualitative analysis of all components is not abundant for the determination of sensitive components, the final determination will be more reasonable if practical experiments are added. Simulation is a good way for it's convenient, fast and cost-effective. R2, R2, Ct and Rsc are selected as sensitive components in the DC-DC converter based on MC34063a ultimately, meanwhile, L, R11, R12 and R13 are selected as sensitive components in the DC-DC converter based on TL494.

C. THEORETICAL BACKGROUND

1) DC-DC CONVERTER BASED ON MC34063A

The output voltage Voa in DC-DC converter based on MC34063a is calculated by the following equation:

$$V_{oa} = (1 + \frac{R_2}{R_1}) * 1.25 \tag{24}$$

where R_1 and R_2 denotes the resistor value of R_1 and R_2 respectively. Because the comparison voltage is 1.25V in the pin 5 of MC34063a chip, namely upper, positive side of R_1 not ground is 1.25V and upper, positive side of R_2 is computed by Eq.24 based on the principle of voltage is decomposed according to the resistor value. Therefore, Voa will increases if the R_1 value decreases or R_2 value increases only then the circuit can re-operates stably. On the contrary, the R_1 value increases or R_2 value decreases will result in decrease of Voa correspondingly. R_{sc} decides the current value from when the chip starts-up over current protection actions which is reflected in the following equation.

$$R_{sc} = \frac{0.3}{I_{PK}} \tag{25}$$

where I_{PK} is peak current of resistor load, which is taken sample in pin 7. Over current protection actions are activated when voltage between pin 6 and pin 7 exceeds 300 millivolts. Faulty value of R_{sc} is beyond its nominal value, which means the start over current value will decrease for the constant 300 millivolts between pin 6 and pin 7. The pulse wave export to Q terminal of R-S trigger will be influenced. The output current flow through resistor load will reduce to cooperate with the start over current. As a result, the output voltage is adjusted lower than 5V, which is the reason for the decrease of Voa along with the increase of R_{sc}. Pin 3 is connected with C_t, the timing capacitor of the oscillator, which decides the frequency is high or low of the oscillator, as well as the switch on-off time. Duty cycle D of DC-DC converter based on MC34063a is:

$$D = \frac{T_{ON}}{T_{OFF}} = \frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}} \tag{26}$$

where T_{ON} is switch-on time in a period of chip operation and T_{OFF} is switch-off time accordingly. $V_{in(min)}$denotes the minimum input voltage which is constant DC 12V in this paper and V_{out} is designed as DC 5V. A period time T is composed of T_{ON} and T_{OFF}, whose relation with frequency f_s is shown in Eq.(1) above. What's more, C_t, the timing capacitor of the oscillator is computed as follows:

$$C_t = 4.010^{-5} T_{ON} \tag{27}$$

from where we find T_{ON} directly bounds up with C_t. If C_t increases, T_{ON} ascends in a certain proportion, resulting in the rise of duty cycle D of DC-DC converter and increase of Voa finally.

2) DC-DC CONVERTER BASED ON TL494

The selected sensitive components in DC-DC converter based on TL494 are L, R11, R12 and R13. Voltage of pin 15 inverter-comparator is calculated by the equation:

$$V_{15} = \frac{R_{13}}{R_{12}} * 5 \tag{28}$$

where V_{15} is the voltage of pin 15 and R_{13}, R_{12} denotes resistor values of R_{13} and R_{12} respectively. This formula abides by separate voltage principle in circuit theory. The voltage on the upper and positive pole of R_{12} is 5V equals to pin 14, the reference voltage of TL494 chip. If resistor value of R_{12} goes up, or resistor value of R_{13} drops, voltage on pin 15 V_{15} will descends as a result according to Eq. 28. Output difference of IN2 in the chip will rises up, which can result in width reduce of PWM waves. IGBT in the converter circuit switch-on for less time in a period eventually and Voa decreases finally. The maximum current value through resistor load and the allowed minimum resistor load are computed as follows:

$$\begin{aligned} I_{max} &= \frac{V_{15}}{R_{11}} \\ RL_{min} &= \frac{5}{I_{max}} - R_{11} \end{aligned} \tag{29}$$

Similarly, Voa will increase when resistor value of R_{12} goes down, for voltage of pin 15 will increase from the initial value which leads to larger difference between $IN2$ and $-IN2$ pins of the TL494 chip. The width of PWM waves will narrow down for the rise of control signal, then Voa goes down ultimately.

D. FAULT ANALYSIS

1) FAULT CLASSES

One or two fault classes for each sensitive component are defined. The faulty values in tolerance are defined based on the deviation of Voa, increasing Voa amplitude higher than the tolerance limit of 5%, or decreasing Voa amplitude lower than the tolerance limit of 5%. There are 6 faulty classes and 1 fault-free class for the DC-DC converter circuit based on MC34063a while 5 faulty classes and 1 fault-free class for the DC-DC converter circuit based on TL494. For validation of the proposed fault diagnosis and identification method, in each class, the value of sensitive component was set manually in an uncertain interval based on simulation results on Saber software. For example, the nominal value of R_{sc} was 0.3Ω, and the value increased by 0.024Ω or 0.018 in each step. Faulty values are attained once the Voa changes 5% to 25% by the step of 5% meanwhile the failure threshold is corresponds to 20% deviation of nominal Voa. Hence, the amount of steps was 6 from 5V to 3.75V or from 5V to 6.25V and 6 component values were obtained in total. The corresponding value of R_{sc} is shown in Table 1. The other components are operated in the same way.

TABLE 1. Fault classes for DC-DC converter on MC34063a.

Fault Class	Fault Code	Nominal Value	Faulty Value
NF	F0	-	-
R1↑	F1	1kΩ	1.07,1.15,1.25,1.36,1.5kΩ
R1↓	F2	1kΩ	0.75,0.79,0.83k,0.882,0.937kΩ
R2↑	F3	3kΩ	3.2,3.4,3.6,3.8,4kΩ
R2↓	F4	3kΩ	2,2.2,2.4,2.6,2.8kΩ
Rsc↑	F5	0.3Ω	0.324,0.342,0.358,0.392,0.416Ω
Ct↑	F6	379pF	9.94,16.92,21.97,30.82,34.2nF

TABLE 2. Fault classes for DC-DC converter on TL494.

Fault Class	Fault Code	Nominal Value	Faulty Value
NF	F7	-	-
L↓	F8	5mH	0.186,0.082,0.057,0.029,0.018mH
R11↑	F9	10mΩ	38,275,414,417,418mΩ
R12↑	F10	15kΩ	20.13,20.35,20.88,20.96,21.33kΩ
R12↓	F11	15kΩ	0.31,0.38,0.4,0.45,0.49kΩ
R13↓	F12	10Ω	7.03,7.19,7.24,7.37,7.43Ω

Tables 1 and 2 show these values of the two converter circuits respectively. Fault class denotes the predefined fault class according to sensitive components and their deviations. Fault code is a number differentiating these fault classes. Nominal value of sensitive component is set by circuit designers, assuming that it works under normal condition. Tolerance range is limited to 5% deviation from its nominal value of 5V Voa. Failure threshold means that when exceeding this value the component reaches failure, which is set to 20% deviation from the nominal Voa value. The reason for setting a failure threshold lies in determining when the prognostics stage starts. Variation limitation is possible maximum deviation that this paper considers in practice. The variation step is set according to 1% Voa nominal value.

2) FAULT-INDICATING CURVES

Voa curves or called fault-indicating curves were first created for sensitive components to generate fault-free and fault bases representing different circuit status. One Voa curve was built for each critical component and was composed of the following three segments: a normal segment within tolerance, an increasing segment within the failure threshold, an increasing segment beyond the failure threshold, or a normal segment within tolerance, a decreasing segment within the failure threshold, and a decreasing segment beyond the failure threshold. There are the sampled 6 bases on total segments, which were acquired from the monitored converter circuit output. Fig. 8 (a)-(f) shows Voa curves of four critical components in the DC-DC converter circuit based on MC34063a in both simulation and experiment. The 6 different fault classes are shown respectively. Simultaneously, Fig. 9 (a)-(e) show various Voa curves of four critical components in the DC-DC converter circuit based on TL494 in both simulation and experiment, and five diverse fault classes are illustrated detailed. The normal segment within tolerance is green, the segment within failure threshold is blue, and the segment beyond failure threshold is red. The Voa curve was used to code faults occurring in the corresponding circuit, while other components changed in their tolerance range randomly.

Voa curves for different components are all about the Voa value changes with the variation of sensitive component's value, which actually can be seen as function f(x), which implies the transform character from parameter value of sensitive component to the output Voa of converter, among which, the independent variable is parameter value of a sensitive components while the dependent variable is Voa for each of all Voa curves. However, it is infeasible or particularly difficult to derive the corresponding detailed and accurate formula about the relation for the complex operation principles of DC-DC converters.

3) FAULT ANALYSIS BASED ON VOA

The proposed Voa curves were used to recognize system faults and isolate different components. Test data was generated by randomly changing/sampling component values for both circuits, including 6 faulty responses within its variation limitation for each sensitive component, while all other components kept varying randomly within their tolerance range. Fault-free data was also sampled 6 times when all the components randomly varied in their tolerance range. It should be noted that this method does not require a training process and much training data. Fault diagnosis results for two filter circuits are summarized. Table 3 shows the results of possible faulty components analysis based on real-time acquired Voa signals from DC-DC converter based on MC34063a and DC-DC converter based on TL494.

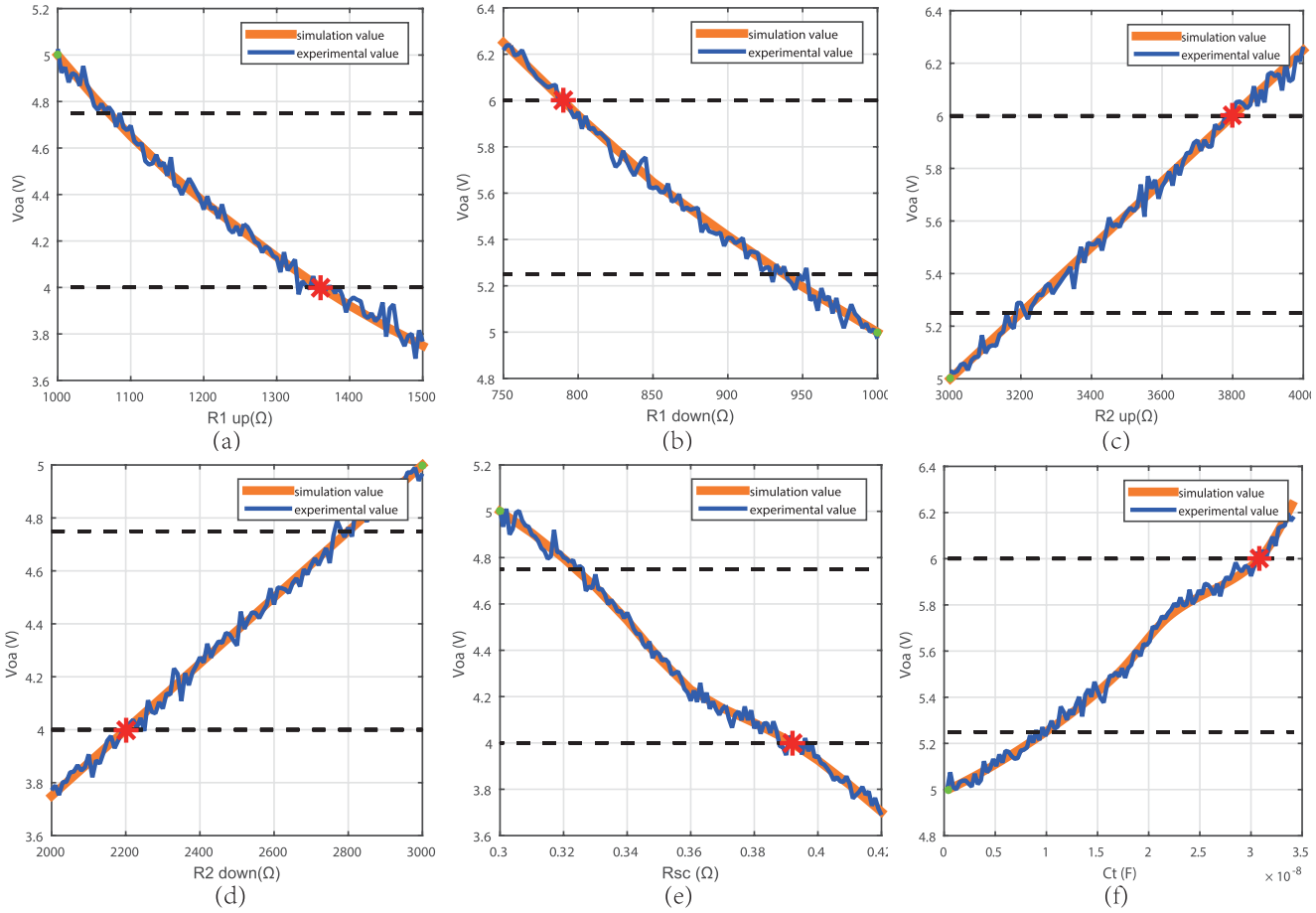

FIGURE 8. Fault-indicating curves corresponding to different fault classes in DC-DC converter based on MC34063a in both simulation and experiment. (a) F1: R1 up, (b) F2: R1 down, (c) F3: R2 up, (d) F4: R2 down, (e) F5: Rsc, and (f) F6: Ct.

TABLE 3. Fault analysis result for DC-DC converters based on MC34063a and TL494.

Measured Voa	DC-DC Converter	Fault Classes Analysis Results
<5V	MC34063a	F1 F4 F5
<5V	TL494	F9 F10 F11 F12
=5V	MC34063a	F0
=5V	TL494	F8
>5V	MC34063a	F2 F3 F6
>5V	TL494	F7

E. FAILURE PROGNOSIS

During the use of components, their values typically deviate from their nominal values, causing the output voltage of the circuit to deviate from the nominal output. This phenomenon directly affects the performance that the circuit should perform and may cause unforeseen system failure. Timely failure prognosis is necessary for avoiding abrupt system disaster from converter circuits. Fault indicator (FI) is used to describe the performance degradation trend, as illustrated in Fig. 4. Assume that the fault level for each component is gradually increased (or decreased) gradually with respect to time. It is assumed that, when Voa crossed around 20%, namely the 4V or 6V, component reached its end of performance (EOP) and became complete failure. Accordingly, the FI value gradually approaches the prior value set as FI threshold. For example, for component R13 in DC-DC converter based on TL494, when its FI value crosses its FI threshold 4V, it means that the circuit begins to fail. The FI threshold is set relevant to each individual component. For the two converter circuits in the experiment, two FI thresholds 4V and 6V correspond to different sensitive component in the circuit respectively.

RUP refers to the remaining cycles from the cycle of starting prognosis module to the cycle of EOP. The prognosis module is immediately triggered when an anomaly is encountered a fault is detected. The predicted RUP by the proposed filter method is compared to the actual RUP during prognosis to show the prognosis capability of the developed prognosis method. Obviously, the error in prediction is desired to be zero.

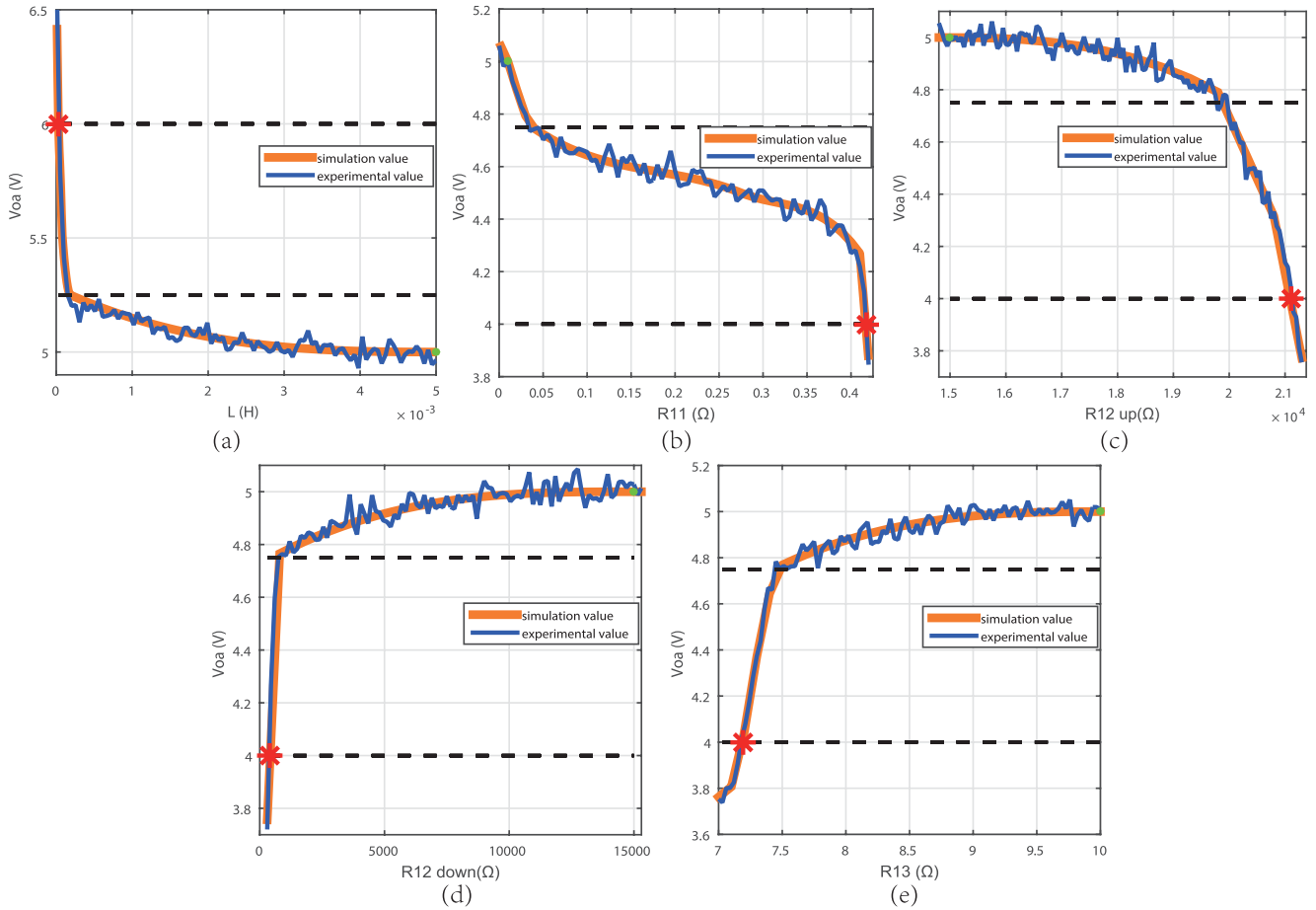

FIGURE 9. Fault-indicating curves corresponding to different fault classes in DC-DC converter based on TL494 in both simulation and experiment. (a) F8: L, (b) F9: R11, (c) F10: R12 up, (d) F11: R12 down, and (e) F12: R13.

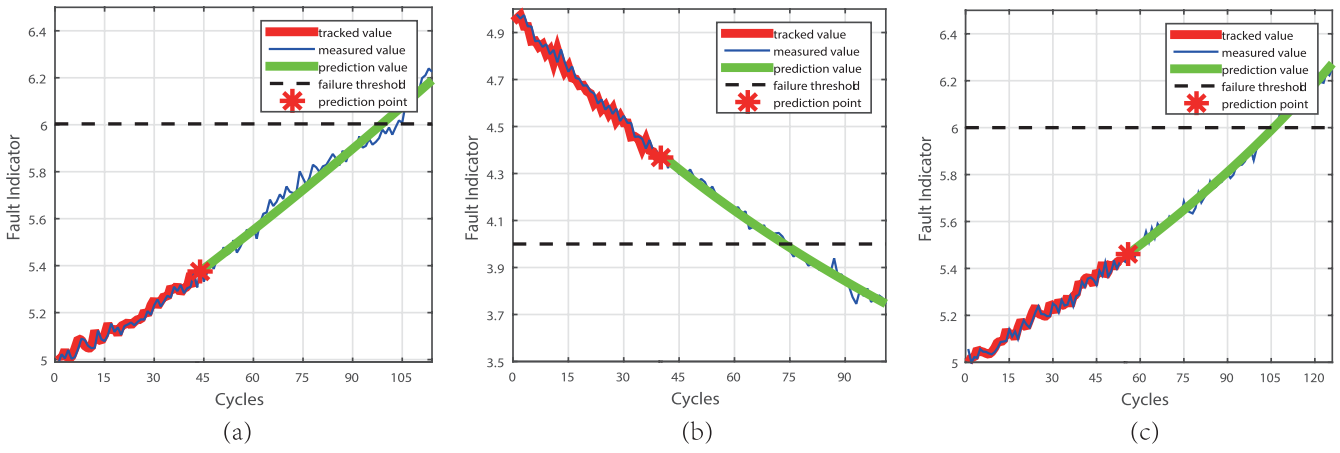

FIGURE 10. RUP estimation for (a) Ct, (b) R1up, and (c) R1down in DC-DC converter based on MC34063a.

1) TREND MODEL

Through curve fitting on the performance degradation trend, the performance degradation trend can be described well by the following trend model:

$$FI_k = a_k * exp(b_k * k) + c_k * exp(d_k * k) \quad (30)$$

where FI is the fault indicator, k is the time index, and a_k, b_k, c_k and d_k are the parameters of this model. Due to system noise and environment influence, the parameters of this model are assumed to be subject to Gaussian distribution, and a random walk model is adopted to estimate these parameters

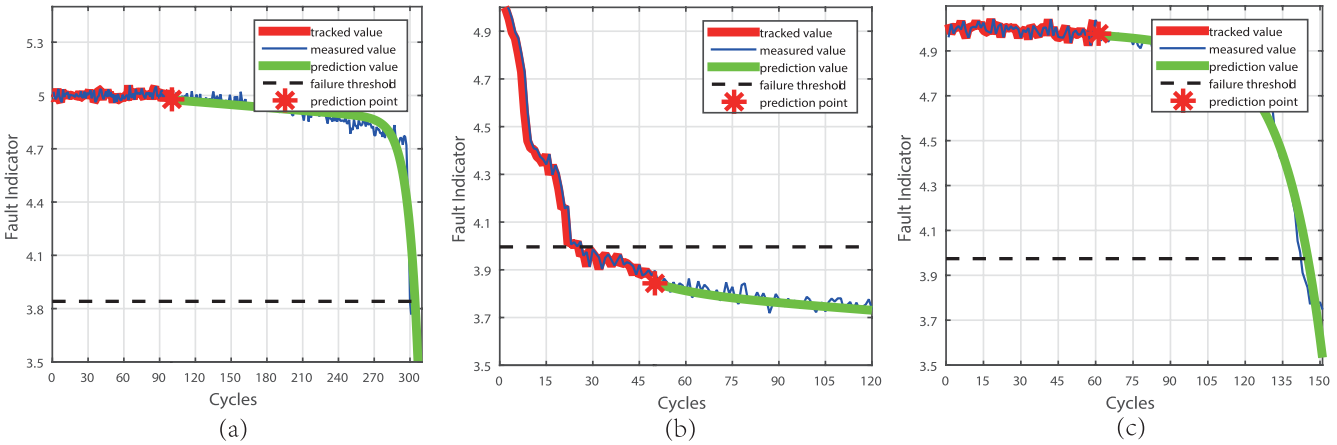

FIGURE 11. RUP estimation for (a) R12down, (b) R12up, and (c) R13 in DC-DC converter based on TL494.

as follows:

$$\begin{cases} a_k = a_{k-1} + w_a; & w_a \sim N(0, \sigma_1) \\ b_k = b_{k-1} + w_b; & w_b \sim N(0, \sigma_2) \\ c_k = c_{k-1} + w_c; & w_c \sim N(0, \sigma_3) \\ d_k = d_{k-1} + w_d; & w_d \sim N(0, \sigma_4) \end{cases} \tag{31}$$

$$x_k = (a_k, b_k, c_k, d_k) \tag{32}$$

where x_k is the state at cycle k.

2) PROGNOSIS RESULTS

From the time the prognosis module is triggered, the fault indicator value is monitored in real time and tracked at any cycle to predict RUP. Fig. 10 and 11 show the prognosis results for six components, Ct, R1 and R2 in DC-DC converter on MC34063a, and R12, R13 and R11 in DC-DC converter on TL494 respectively. It is seen that tracking and predicted trend follow closely along with the true values until it reaches the failure threshold. The error between the actual failure cycle and predicted EOP is small. In Figs. 10 and 11, the maximum error occurs in Fig. 10 (a) with an error of only 4 cycles. The RUP of circuits can be accurately estimated. The predicted curve accords well with the actual curve, which further validates the accuracy of prognosis. The relative smoothing of the estimated curve proves that the proposed prognostic method is robust regardless of when the prediction module begins.

V. CONCLUSION

A novel fault analysis method and a improved prognosis method for DC-DC converter circuits are proposed in this paper, aiming at providing early fault analysis and isolation, and failure prognosis to avoid catastrophic system failure in safety-critical electronic systems during field operation. The developed fault analysis method avoids the difficulties of modeling and the complexity of choosing signal processing algorithms in traditional methods, and realizes efficient and effective real-time analysis, which is suitable for detecting complicated converter circuits. Compared with testing methods based on circuit nodal equations which require access to the internal nodes of circuits, the proposed method only monitors the response of stimulated circuits at the output node, which makes it possible to provide highly efficient fault analysis for converter circuits. The developed failure prognosis approach based on fault indicator and performance degradation trend takes full consideration of historical degradation data as a prior exemplar for more accurate prediction of RUP. Two case studies validate the effectiveness of the proposed fault analysis method. show that RUP estimates at different times are close to linearity, achieving relatively accurate predictions. The proposed approach can assist in preventative maintenance for avoiding unscheduled system shut-down.

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