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Open-Circuit Fault Diagnosis of Dual Active Bridge DC-DC Converter With Extended-Phase-Shift Control

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ABSTRACT This paper proposes a simple and fast fault diagnosis strategy for bidirectional isolated dual-active-bridge dc–dc converter with the extended-phase-shift control to improve reliability. The fault diagnosis strategy utilizes the average values of the voltage to quickly identify failures position and devices in either transistors or diodes without adding any hardware cost. First, two conditions are classified according to the direction of the inductor current on the primary side. Then, a comprehensive operation analysis during normal and faulty conditions is presented. Based on the characterization of open-circuit faults in diodes and transistors, open circuit faults diagnose strategy is derived and validated through both simulation and experimental test for different fault conditions.

INDEX TERMS Bidirectional DC-DC converter, extended-phase shift control, fault diagnosis, reliability.

I. INTRODUCTION

Bidirectional isolated dc-dc converters are becoming more and more important for the applications in the Electric Vehicles [1], energy storage system [2], distributed energy generating [3], and solid-state transformer [4]. Among different circuit topologies for the bidirectional isolated dc-dc converters, dual-active-bridge (DAB) dc-dc converter shows obvious advantages in terms of power density, modular design, and easy-to-control [5]–[10].

The circuit diagram of DAB converter is shown in Fig. 1 and the conventional phase shift (CPS) is used due to its control simplicity. However, the energy conversion efficiency with the CPS is limited due to high circulating current and narrow soft-switching range [11]. Thus, a great deal of advanced phase-shift strategies have been proposed in [12]–[17], which present the operation principle of multiple phase shift control by adding additional control dimensions for achieving optimal control scheme. Among them, the extended-phase-shift (EPS) is regarded as one promising strategy for achieving the efficiency improvement in [18]. Furthermore, the EPS control only has one additional control dimension, which achieves the balance in the efficiency improvement and the implementation complexity [19].

The reliability of power electronics converters such as the DAB converter is essential especially for some critical applications such as electric vehicles, aerospace, and medical industry [20]. A survey about the reliability of the power electronic converters indicates that the most vulnerable component for failure is the power electronics devices including MOSFETs or diodes [21]. The consequences of the faults in power electronics devices include high repair cost, device replacement, and usually stoppage of whole system [22]. Thus, different failure mechanism for power electronics devices under different conditions should be analyzed intensively and fault diagnosis strategies must be utilized

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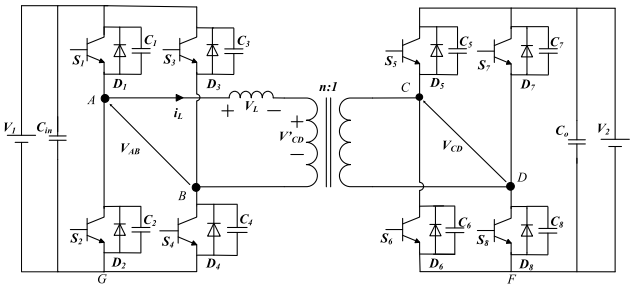

FIGURE 1. Circuit diagram of the DAB converter.

in order to improve the reliability of power electronics converters.

Although there are different causes for failures in power devices, one consensus is clear that all these failures such as the open-circuit and short-circuit faults are closely linked with the operation conditions and circuit parameters. For the short-circuit faults, hardware protection has been integrated into the gate driving circuit as a standard design. However, considering that no standard design is used for the open-circuit faults, this paper will mainly focus on the open-circuit fault diagnosis for power devices in DAB converter. Especially with the EPS control, more control variables result in complicated operation modes and faulty conditions. Thus, main symptoms of DAB converters during faulty conditions must be deeply investigated.

When open-circuit faults (OCFs) in power devices occur, the stoppage of the system may not happen immediately, the resulted overstress may damage some healthy components if the faults cannot be detected as early as possible. Thus, many methods have been used to address the problem. For instance, conventional methods such as conservative design with overlarge power rating and devices or circuits parallel are not cost effective [23]. Also, the additional parallel circuit deteriorates the power density of power converters. In [24], an OCF diagnosis method was proposed according to the faulty operation analysis. Additional components are required and the circuit reconfiguration should be made under an open-circuit power device fault. In [25], the dc-link current derivative sign was adopted to detect the OCFs in interleaved dc-dc converter. Both healthy and faulty operations are studies to derive the dc-link current. In [26] and [27], the magnetic near field by using a loop near field probe was utilized to detect the OCFs for the dc-dc converter. However, the accuracy of near field probe is highly relied on the detection position, which may cause the detection error issue. In [28], the change of the inductor current with the time was used to detect the OCFs. Field Programmable Gate Array (FPGA) and high bandwidth current sensor were used to implement the complicated algorithm and ensure its performance. However, it may increase the cost of fault detection method. In [29], a printed circuit board Rogowski coil was placed on the capacitor terminals and the derivative of the capacitor current was captured to detect the OCFs. In [30], the diode voltage was used as the detection signature and a logic circuit was designed to indicate the failed devices. In [31], additional hardware circuit was designed by measuring the submodule output voltage to locate the OCFs. These methods shows limitation of increased cost, system reconfiguration, or relatively slow response time. Besides, software-based algorithms are proposed for the fault diagnosis. In [32], the input and output voltage of the rectifier were used and a proper calculation strategy is implemented for the fault detection combined with additional sensors. In [33], the decomposing circuit model was used to locate the fault position of OCFs. In [34], the converter average phase currents and the absolute currents are used to formulate the OCF diagnosis. In [35], a mixed logical dynamic model of the converter was built for the grid current estimation and the error was used to allocate different open-circuit faults. In [36], the spectrum analysis of the voltage and current was utilized for the OCF detection. Besides, complicated algorithm are used for the OCF diagnosis. For instance, a Luenberger observer and on an adaptive threshold was adopted for the OCFs diagnosis in wind power system [37]. In [38] and [39], model predictive control was adopted for the OCFs in modular multilevel converters. These algorithms are effectives for specific applications. However, the computational burden is heavy. In [40], the circuit-analysis based diagnosis method was proposed for the OCFs. The failure position in different stage such as rectifier or inverter can be specified. However, this method is unable to identify the failed power device. Other methods such as the multivariate statistical process monitoring (MSPM) method can be used for the fault diagnosis [41].

The above-mentioned analysis shows that an ideal OCF diagnosis algorithm should have the features of low-complexity, fast speed, accuracy device allocation, and compatible with existed hardware. Regarding the OCF diagnosis for the DAB converter, the voltage drop of all power semiconductors were measured and properly modified in order to generate the OCF signal [42]. Although no additional sensors are used with this method, the accurate measure of the devices' voltage drop in real time is difficult. Besides, the analysis of the open circuit fault is only focused on the CPS control, which limits the scope of application. In [43], the distortion of voltage waveform on the primary winding by using the active-phase-shifted control was proposed. Nevertheless, this method is expensive due to the required additional auxiliary winding and magnetic probes. Besides, the fault tolerant topology for full bridge converter is shown in [44]. It can diagnose and isolate fault semiconductor component while maintain normally power transmission ability through the fault tolerant topology. The input-parallel-output-series (IPOS) converter for wind farm application is discussed, which can ensure uninterrupted operation of system when it occurs tolerable fault [45]. Although the literatures [43]–[45] present detailed analytical methodology on investigating the distortion of bridge AC output voltage and inductor current under various open-circuit fault conditions, it is only focused on traditional unidirectional full bridge converter. In [46],

the average value of the voltage on the primary winding was analyzed for the OCFs. However, it can merely distinguish the faulty leg of the bridge instead of precisely locating the faulty transistor. So it can't accurately locate certain fault devices. In [47], a faulty diagnose method was discussed and the middle point voltage of the phase leg in the primary winding was analyzed to precisely locate the faulty transistor and anti-parallel diode [48]. However, none of them have studied the faulty diagnosis of DAB converters under EPS control considering eight power devices in DAB converters and multiple operation modes with the EPS control.

In order to address the concerns, this paper proposes a simple and fast fault diagnosis strategy for DAB dc-dc converter with the EPS control. The fault diagnosis strategy utilizes the average values of the voltage to quickly identify failures position and devices in either transistors or diodes without adding any hardware cost. The remainder of this paper is organized as follows. A comprehensive operation analysis during normal and faulty conditions is presented in Section II and III. Then, an open circuit faults diagnose strategy is derived and presented in Section IV. Main simulation and experimental evaluations are illustrated in Section V and VI. Finally, conclusions are drawn in Section VII.

II. OPERATION PRINCIPLE OF DAB CONVERTER WITH EPS CONTROL

A typical DAB topology is presented in Fig. 1, which is comprised of 4 switches on either the primary or secondary side. Each switch has antiparallel diode $D_1 \sim D_8$ and parasitic capacitor $C_1 \sim C_8$. Both sides are isolated by a high frequency transformer that is providing current and voltage isolation. A coupling inductor is inserted on the primary side, which can be integrated as the leakage inductance of the high-frequency transformer. Each power switch is usually composed of a power transistor, a parasitic capacitor and an antiparallel diode. The symmetric structure of the DAB converter can ensure bidirectional power flow and flexible power regulation.

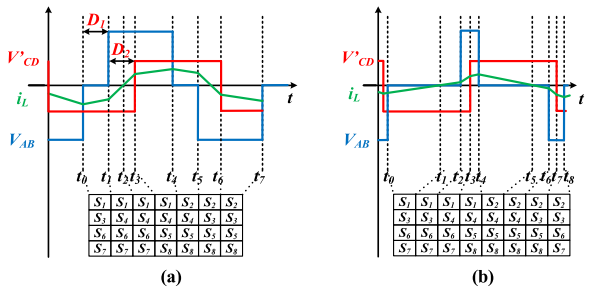

FIGURE 2. Definition of control variables and typical waveforms of DAB converters with EPS control under normal operation: (a) Condition 1; (b) Conditions 2.

Fig. 2 illustrates the definition of control variables and typical waveforms of DAB converters with EPS control under normal operation. With EPS control, two control variables such as D_1 and D_2 are used. Specified conducting devices under two conditions for different instants from t_0 to t_8 are illustrated in Fig. 2. In this paper, the operation analysis of DAB converter with EPS under the circumstance of "$D_2 > 0$", namely S_4 is leading S_5 as the diagram demonstrate in Fig. 2 (a), is presented. Similar analysis can be made for the circumstance of "$D_2 < 0$", namely S_4 is lagging S_5. By analyzing different circumstances that the open circuit fault happens to transistors, it was observed that both duty cycles D_1 and D_2 could affect the value of i_L at a specific instant. Therefore, when an open-circuit fault happens to the transistor at or before the specific instant, the of the waveforms' distortion shows different features. Thus, it is necessary to classify different conditions so that the open circuit faults on each transistor under different conditions will be analyzed in details. In this paper, two conditions are classified according to the direction of the inductor current on the primary side. Thus, two conditions at the instant t1 are defined. Specifically, condition 1 and condition 2 are defined as $i_L(t_1) < 0$ and $i_L(t_1) > 0$ respectively. When an open-circuit fault happens to transistors, a transient state will appear, which usually consists of 4 snubber capacitors on that bridge. Thus, detailed transient analysis during different operation modes must be analyzed. Furthermore, considering the deadtime for DAB converters is usually set longer than the time for capacitors to charge and discharge, the effect of deadtime has been analyzed in [45] and will not be considered in the operation modes analysis.

III. OPEN CIRCUIT FAULT ANALYSIS

A. CONDITION 1 OF THE PRIMARY SIDE: $i_L(t_1) < 0$

Main waveforms of the DAB converter, including "V_{AB}", "V'_{CD}", and "i_L", during one period when open-circuit faults happen to different transistors are demonstrated in Fig. 1. The symmetry property of the DAB converter can be applied under this condition and the corresponding waveforms when open-circuit faults happen to device S_1 and S_4 are regarded as the same. Thus, only open-circuit faults on S_1 and S_2 will be presented in this work. The voltage of the inductor and the inductor current during different modes are summarized in Table 1 and Table 2 corresponding to the fault on S_1 and S_2 respectively, which are deduced based on (1) and (2).

$$V_L = V_{AB} - V'_{CD} \tag{1}$$

$$di/dt = V_L/L \tag{2}$$

1) ANALYSIS OF THE OPEN CIRCUIT FAULT ON S_1

Mode 1 [t_0,t_1]: as shown in Fig. 3 (a), when S_2 is switched off, snubber capacitor C_2 will be charged by i_L and the snubber capacitor C_1 will be discharged. When they are fully charged and discharged to V_1 and 0, the parasitic diode D_1 will be conducted. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Consequently, i_L is negative and its magnitude is decreasing.

Mode 2 [t_1,t_2]: at the instant $t = t_1$, S_4 and S_3 will be switched on and off respectively. Thus, their corresponding snubber capacitors C_4 and C_3 will be discharged and charged

TABLE 1. Inductor voltage and the slope of the inductor current when the open-circuit faults happen to S1.

Mode	Inductor voltage	Slope of the inductor current
Mode 1	nV_2	nV_2/L
Mode 2	V_1+nV_2	$(V_1+nV_2)/L$
Mode 3	nV_2	nV_2/L
Mode 4	$-nV_2$	$-nV_2/L$
Mode 5	-	-
Mode 6	$-nV_2$	$-nV_2/L$
Mode 7	$-V_1-nV_2$	$(-V_1-nV_2)/L$
Mode 8	$-V_1+nV_2$	$(-V_1+nV_2)/L$

TABLE 2. Inductor voltage and the slope of the inductor current after the fault happens to S2.

Mode	Inductor voltage	Slope of the inductor current
Mode 1	nV_2	nV_2/L
Mode 2	V_1+nV_2	$(V_1+nV_2)/L$
Mode 3	V_1+nV_2	$(V_1+nV_2)/L$
Mode 4	V_1-nV_2	$(V_1-nV_2)/L$
Mode 5	$-nV_2$	$-nV_2/L$
Mode 6	$-V_1-nV_2$	$(-V_1-nV_2)/L$
Mode 7	$-nV_2$	$-nV_2/L$
Mode 8	nV_2	nV_2/L
Mode 9	-	-

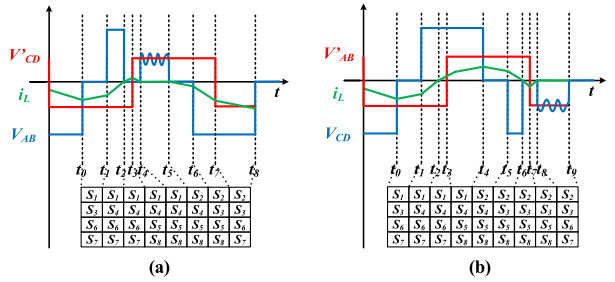

FIGURE 3. Typical waveforms of the DAB converter when open-circuit faults happen on different transistors of the primary side under condition 1. (a) Open circuit fault on S_1 or S_4. (b) Open circuit fault on S_2 or S_3.

simultaneously. When C_4 and C_3 are fully discharged and charged to 0 and V_1 respectively, D_4 will be conducted. As a consequence, i_L will continue to decrease with a larger slope, and the inductor is charging V_1 and V_2.

Mode 3 [t_2,t_3]: since the magnitude of i_L decreases, at the instant $t = t_2$, its direction will be reversed. However, since the fault has happened to S_1, i_L will charge C_1 and discharge C_2. When the voltage potential on C_1 and C_2 are equal to V_1 and 0, D_2 will be conducted and i_L will flow in the positive direction. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Therefore, the voltage across the inductor is "nV_2".

Mode 4 [t_3,t_4]: at the instant $t = t_3$, S_6 and S_7 are switched off, which will result in charging C_6, C_7 and discharging C_5, C_8. When C_6, C_7 are fully charged to V_2 and C_5, C_8 are discharged to 0, D_5, D_8 will be conducted. Although S_5, S_8 are switched on at t_3, the current on the secondary side will flow through D_5, D_8 instead of them. During this period, $V_{AB} = 0$, $V'_{CD} = nV_2$. Thus, i_L will decrease since the inductor voltage changes from "nV_2" to "$-nV_2$".

Mode 5 [t_4,t_5]: since the magnitude of i_L decreases, the value of i_L equals to 0 with a tendency to flow in the opposite direction at the instant $t = t_4$. Nevertheless, since the open circuit fault has happened to S_1, i_L cannot flow through S_1, which results in a resonant mode that involves the inductor, C_1 and C_2. During this mode, the inductor current is so small that its value is regarded as zero.

Mode 6 [t_5,t_6]: the resonant state will be terminated as S_1 is switched off at the instant that $t = t_5$. When S_1 is switched off, C_1 will be charged and C_2 will be discharged. When they are fully charged and discharged to V_1 and 0 respectively, D_2 will be conducted. However, since i_L is flowing in the opposite direction and S_2 is switched on, i_L will flow through S_2 instead of D_2. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. Therefore, i_L starts to increase in the opposite direction, and the inductor will be charged by V_2.

Mode 7 [t_6,t_7]: at the instant t_6, S_4 is switched off, C_4 is charged and C_3 is discharged. When they are fully charged and discharged to V_1 and 0, D_4 will be conducted. Because the i_L is flowing in the opposite direction, it will flow through S_4 directly instead of flowing through D_4. Within this interval, $V_{AB} = -V_1$, $V'_{CD} = nV_2$. Therefore, the inductor is charged by both V_1 and V_2, and its value is increasing in the opposite direction with a larger slope.

Mode 8 [t_7,t_8]: as shown in Fig. 3 (a), at the instant t_7, S_5 and S_8 are switched off, which leads to the charging operation of C_5, C_8 and the discharge of C_6, C_7. When they are fully charged and discharged to V_2 and 0 respectively, D_6, D_7 will be conducted, which enables the soft-switching of S_6 and S_7. Within this interval, $V_{AB} = -V_1$, $V'_{CD} = -nV_2$. Moreover, V_1 supplies power to the inductor and V_2, and the magnitude of i_L continues to increase in the opposite direction with a smaller slope.

2) ANALYSIS OF THE OPEN CIRCUIT FAULT ON S_2

Mode 1 [t_0,t_1]: as shown in Fig. 3 (b), when S_2 is switched off, its corresponding snubber capacitor C_2 will be charged, and C_1 will be discharged. When they are fully charged and discharged to V_1 and 0 respectively, D_1 will be conducted, which enables the soft-switching operation of S_1. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Therefore, the inductor

releases power the V_2, and the magnitude of i_L continues to decrease in the opposite direction.

Mode 2 [t_1,t_2]: at the instant t_1, S_3 is switched off. As a consequence, C_3 will be charged, and C_4 will be discharged by i_L. When they are fully charged and discharged to V_1 and 0, D_4 will be conducted. Within this interval, $V_{AB} = V_1$, $V'_{CD} = -nV_2$. Thus, the inductor supplies power V_1 and V_2, and the magnitude of i_L is decreasing in the opposite direction with a larger slope.

Mode 3 [t_2,t_3]: As the magnitude of i_L continues to decrease, the direction of it will reverse at t_2. Consequently, the parasitic diodes D_1, D_4, D_6 and D_7 will be disconnected. Within this interval, $V_{AB} = V_1$, $V'_{CD} = -nV_2$. As a consequence, the inductor is charged by V_1 and V_2, and the magnitude of i_L starts to increase in the positive direction.

Mode 4 [t_3,t_4]: at the instant t_3, S_6 and S_7 are switched off, which results in charging C_6, C_7 and discharging C_5, C_8. When they are fully charged and discharged to V_2 and 0 respectively, D_5, D_8 will be conducted, which enables the soft switches of S_5 and S_8. Within this interval, $V_{AB} = V_1$, $V'_{CD} = nV_2$. Consequently, V_1 supplies power to charge the inductor and V_2, and the magnitude of i_L is increasing with a smaller slope in the positive direction.

Mode 5 [t_4,t_5]: at the instant t_4, S_1 will be switched off, which results in the charging operation of C_1 and the discharging operation of C_2. When they are charged and discharged to V_1 and 0 respectively, D_2 will be conducted. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. Therefore, the inductor supplies power to V_2, and i_L stops to decrease.

Mode 6 [t_5,t_6]: at the instant t_5, S_4 is switched off, which results in charging C_4 and discharging C_3. When they are fully charged and discharged to V_1 and 0 respectively, D_3 will be conducted, which ensures the soft-switching of S_3. Within this interval, $V_{AB} = -V_1$, $V'_{CD} = nV_2$. Thus, the inductor supplies power to V_1 and V_2, and the magnitude of i_L stops to decrease.

Mode 7 [t_6,t_7]: since the magnitude of i_L continues to decrease, the direction of it will be reversed when its value equals to 0 at the instant t_6. However, given that the open circuit fault has happened to S_2, C_2 will be charged to V_1, and C_1 will be discharged to 0. Therefore, when the charging and discharging process is complete, D_1 will be conducted. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. As a consequence, V_2 supplies power to the inductor, and the magnitude of i_L starts to increase in the opposite direction.

Mode 8 [t_7,t_8]: at the instant t_7, S_5 and S_8 are switched off, which results in charging C_5, C_8 and discharging C_6, C_7. When they are fully charged and discharged to V_2 and 0 respectively, D_6 and D_7 will be conducted, which enables the soft switch of S_6 and S_7. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Consequently, the inductor supplies power to V_2, and the magnitude of i_L stops to decrease in the opposite direction.

Mode 9 [t_8,t_9]: as shown in Fig. 3 (b), as the magnitude of i_L continues to decrease, its value equals to 0 with a tendency to flow in the positive direction at the instant t_8. However, since the open circuit fault has happened to S_2, i_L cannot flow through it, which leads to the resonant state that involves in C_1, C_2 and the inductor.

B. CONDITION 2 OF THE PRIMARY SIDE: $i_L(t_1) \geq 0$

Similarly, main waveforms of the DAB converter during one period when the open-circuit faults happen to different transistors are demonstrated in Fig. 4. However, the property of symmetry of DAB converter cannot be applied under this condition. For instance, the circuit appears resonant after the fault happens to transistor S_1, but it is absent after the fault happens to transistor S_4 as the diagram demonstrated in Fig. 4 (a) and Fig. 4 (d), respectively. Similarly, based on the equation (1), the expressions of the voltage divided on the inductor are summarized in Table 3.

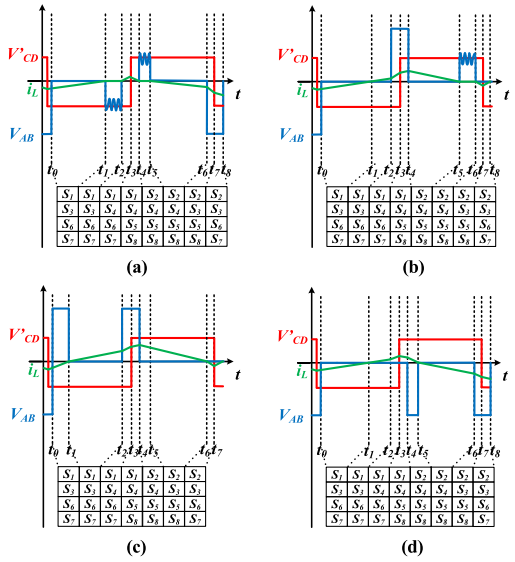

FIGURE 4. Typical waveforms of the DAB converter when faults happen on different transistors of the primary side under condition 2. (a) Open circuit fault on S_1. (b) Open circuit fault on S_2. (c) Open circuit fault on S_3. (d) Open circuit fault on S_4.

1) ANALYSIS OF THE OPEN CIRCUIT FAULT ON S_1

Mode 1 [t_0,t_1]: as shown in Fig. 4 (a), when S_2 is switched off at the instant t_0, the snubber capacitors C_2 and C_1 will be charged and discharged to V_1 and 0 respectively. When the charging process is complete, the parasitic diode D_1 will be conducted, which enables the soft-switching operation of S_1. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Consequently, the inductor supplies power to V_2, and the magnitude of i_L starts to decrease in the opposite direction.

Mode 2 [t_1,t_2]: since the magnitude of i_L continues to decreasing, its value equals to 0 with a tendency to flow in the positive direction at the instant t_1. However, because the open circuit fault has happened to S_1, i_L cannot flow through S_1, and the circuit starts to be stuck in the resonant state as the circuit diagram illustrated in Fig. 4, which involves in C_1, C_2 and the inductor. In addition, with i_L flows in the positive direction, D_6 and D_7 on the secondary side are disconnected.

TABLE 3. Inductor voltage when faults happens under condition 2.

Mode	Inductor voltage			
	S_1	S_2	S_3	S_4
Mode 1	nV_2	$-nV_2$	V_1+nV_2	nV_2
Mode 2	-	nV_2	nV_2	nV_2
Mode 3	nV_2	V_1+nV_2	V_1+nV_2	nV_2
Mode 4	$-nV_2$	V_1-nV_2	V_1-nV_2	$-nV_2$
Mode 5	-	$-nV_2$	$-nV_2$	$-V_1-nV_2$
Mode 6	$-nV_2$	-	$-nV_2$	$-nV_2$
Mode 7	$-V_1-nV_2$	$-nV_2$	nV_2	$-V_1-nV_2$
Mode 8	$-V_1-nV_2$	nV_2		$-V_1-nV_2$

Mode 3 [t_2,t_3]: at the instant t_2, S_3 is switched off, which results in charging C_3 and discharging C_4. When they are fully charged and discharged to V_1 and 0, D_4 will be conducted. However, since i_L attempts to flow in the positive direction after S_4 is switched on, it will flow through S_4 directly. Therefore, the conduction of S_4 provides a path for i_L to flow, and the resonant state is terminated. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Therefore, V_2 supplies power to the inductor, and the magnitude of i_L starts to flow in the positive direction.

Mode 4 [t_3,t_4]: at the instant t_3, S_6 and S_7 are switched off, which leads to charging C_6, C_7 and discharging C_5, C_8. When they are fully charged and discharged to V_2 and 0 respectively, D_5 and D_8 will be conducted, which enables the soft-switching operation of S_5 and S_8. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. Thus, V_2 supplies power to the inductor, and the magnitude of i_L starts to decrease in the positive direction.

Mode 5 [t_4,t_5]: at the instant that S_1 is still switched on, the magnitude of i_L equals to 0, and i_L tends to flow in the opposite direction. However, since the open circuit fault has happened to S_1, i_L cannot flow through it, and the circuit starts to be stuck in the resonant state, which involves in C_1, C_2 and the inductor. Additionally, due to the direction change of i_L, D_5 and D_8 are disconnected.

Mode 6 [t_5,t_6]: when S_2 is switched on at $t = t_5$, it provides an avenue for i_L to flow in the opposite direction. Therefore, the resonant state is terminated. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. Thus, V_2 supplies power to the inductor, and the magnitude of i_L starts to increase in the opposite direction.

Mode 7 [t_6,t_7]: at the instant t_6, S_4 is switched off, which results in charging C_4 and discharging C_3. When they are fully charged and discharged to V_1 and 0, D_3 will be conducted. However, since i_L flows in the opposite direction, i_L will not flow through it. Within this interval, $V_{AB} = -V_1$, $V'_{CD} = nV_2$. Consequently, V_2 supplies power to the inductor, and the magnitude of i_L continues to increase with a larger slope in the opposite direction.

Mode 8 [t_7,t_8]: at the instant t_7, S_5 and S_8 are switched off, which leads to charging C_5, C_8 and discharging C_6, C_7. When they are fully charged and discharged to V_2 and 0 respectively, D_6, D_7 will be conducted, which enables the soft switch of S_6 and S_7. Within this interval, $V_{AB} = -V_1$, $V'_{CD} = -nV_2$. As a consequence, V_1 supplies power to the inductor and V_2, and the magnitude of i_L continues to increase in the opposite direction with a smaller slope.

2) ANALYSIS OF THE OPEN CIRCUIT FAULT ON S2

Mode 1 [t_0,t_1]: as shown in Fig. 4 (b), when S_2 is switched off at the instant t_0, the snubber capacitors C_2 and C_1 will be charged and discharged to V_1 and 0 respectively. When the charging process is completed, parasitic diode D_1 will be conducted, which enables the soft switch of S_1. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Consequently, the inductor supplies power to V_2, and the magnitude of i_L decreases in the opposite direction.

Mode 2 [t_1,t_2]: as the magnitude of i_L continues to decrease in the opposite direction, when its value equals to 0 at instant t_1, D_3 will be conducted to provide another avenue for i_L to flow through. Moreover, due to the direction change in i_L, the current on the secondary side will flow through S_6 and S_7 instead of D_6 and D_7. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Therefore, V_2 supplies power to the inductor, and the magnitude of i_L starts to increase in the positive direction.

Mode 3 [t_2,t_3]: at the instant t_2, S_3 is switched off, which results in C_3 and C_4 being charged and discharged to V_1 and 0 respectively. After this process is complete, D_4 will be conducted, which enables the soft switch of S_4. After S_4 is switched on, i_L will flow through it directly. Within this interval, $V_{AB} = V_1$, $V'_{CD} = -nV_2$. Therefore, V_1, V_2 supply power to the inductor, and the magnitude of i_L starts to increase in the positive direction.

Mode 4 [t_3,t_4]: at the instant t_3, S_6 and S_7 are switched off, which leads to charging C_6, C_7 and discharging C_5, C_8. When they are fully charged and discharged to V_2 and 0 respectively, D_5, D_8 will be conducted, which enables the soft switch of S_5 and S_8. Within this interval, $V_{AB} = V_1$, $V'_{CD} = nV_2$. Therefore, V_1 supplies power to the inductor and V_2, and the magnitude of i_L continues to increase in the positive direction with a smaller slope.

Mode 5 [t_4,t_5]: at the instant t_4, S_1 is switched off, which results in charging C_1 and discharging C_2. When they are fully charged and discharged to V_1 and 0, D_2 will be conducted, which ensures the soft switch of S_2. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. Thus, the inductor supplies power to V_2, and the magnitude of i_L stops to decrease in the positive direction.

Mode 6 [t_5,t_6]: since i_L continues to decrease, its magnitude equals to 0 with a tendency to flow in the opposite direction at t_3. However, because the open circuit fault has happened to S_2, i_L cannot flow through it, which leads circuit

to the resonant state. In addition, with i_L flows in the positive direction, D_5 and D_8 on the secondary side are disconnected.

Mode 7 [t_6,t_7]: at the instant t_6, S_4 is switched off, which results in charging C_4 and discharging C_3. When they are fully charged and discharged to V_1 and 0 respectively, D_3 will be conducted, which provides an avenue for i_L to flow in the opposite direction. Moreover, C_2 and C_1 will be fully charged and discharged to V_1 and 0 as well. Therefore, the resonant state is terminated. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. As a consequence, V_2 supplies power to the inductor, and the magnitude of i_L proceeds to increasing in the opposite direction.

Mode 8 [t_7,t_8]: at the instant t_7, S_5 and S_8 are switched off, which leads to charging C_5, C_8 and discharging C_6, C_7. When they are fully charged and discharged to V_2 and 0 respectively, D_6, D_7 will be conducted, which enables the soft switch of S_6 and S_7. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Consequently, the inductor supplies power to V_2, and the magnitude of i_L stops to decrease in the opposite direction.

3) ANALYSIS OF THE OPEN CIRCUIT FAULT ON S_3

Mode 1 [t_0,t_1]: as shown in Fig. 4 (c), when S_2 is switched off, the snubber capacitors C_2 and C_1 will be charged and discharged to V_1 and 0 respectively. When the charging process is complete, parasitic diode D_1 will be conducted, which enables the soft switch of S_1. When the open circuit fault happens to S_3 after S_1 is switched on, D_4 will be conducted to allow i_L flow through. Within this interval, $V_{AB} = V_1$, $V'_{CD} = -nV_2$. Therefore, the inductor supplies power to V_2, and the magnitude of i_L starts to decrease in the opposite direction.

Mode 2 [t_1,t_2]: The magnitude of i_L continues to decrease. When its value equals to 0 with a tendency to flow in the positive direction at t_1, C_4 and C_3 will be charged and discharged to V_1 and 0 respectively. When this process is completed, D_4 will be conducted, and D_1, D_6 and D_7 will be disconnected. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Consequently, V_2 supplies power to the inductor, and the magnitude of i_L starts to increase in the positive direction.

Mode 3 [t_2,t_3]: at the instant t_2, S_3 is switched off, and S_4 is switched on. Since D_3 conducts in the last interval, the circuit connection will not be influenced when S_3 is switched off. Within this interval, $V_{AB} = V_1$, $V'_{CD} = -nV_2$. Thus, the inductor is charged by V_1 andV_2, and the magnitude of i_L starts to increase in the positive direction with a larger slope.

Mode 4 [t_3,t_4]: at the instant t_3, S_6 and S_7 are switched off, which leads to charging C_6, C_7 and discharging C_5, C_8. When they are fully charged and discharged to V_2 and 0 respectively, D_5, D_8 will be conducted, which enables the soft switch of S_5 and S_8. Within this interval, $V_{AB} = V_1$, $V'_{CD} = nV_2$. As a consequence, V_1 supplies power to the inductor and V_2, and the magnitude of i_L continues to increase in the positive direction with a smaller slope.

Mode 5 [t_4,t_5]: at the instant t_4, S_1 is switched off, which results in charging C_1 and discharging C_2. When they are fully charged and discharged to V_1 and 0 respectively, D_2 will be conducted. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. Therefore, the inductor supplies power to V_2, and the magnitude of i_L starts to decrease in the positive direction.

Mode 6 [t_5,t_6]: Since the magnitude of i_L continues to decrease, its value equals to 0 with a tendency to flow in the opposite direction at the instant t_5. Furthermore, when S_4 is switched off, and S_3 is switched on, it cannot provide an avenue for i_L to flow through because of the open circuit fault on S_3. Consequently, D_4 will be conducted and i_L will flow through it. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. Therefore, V_2 supplies power to the inductor, and the magnitude of i_L starts to increase in the opposite direction.

Mode 7 [t_6,t_7]: as shown in Fig. 4 (c), at the instant t_6, S_5 and S_8 are switched off, which leads to charging C_5, C_8 and discharging C_6, C_7. When they are fully charged and discharged to V_2 and 0 respectively, D_6, D_7 will be conducted, which enables the soft switch of S_5 and S_8. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Thus, the inductor supplies power to V_2, and the magnitude of i_L starts to decrease in the opposite direction.

4) ANALYSIS OF THE OPEN CIRCUIT FAULT ON S_4

Mode 1 [t_0,t_1]: as shown in Fig. 4 (d), when S_2 is switched off, C_2 and C_1 will be charged and discharged to V_1 and 0 respectively. When this process is complete, D_1 will be conducted, which enables the soft switch of S_1. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Consequently, the inductor supplies power to V_2, and the magnitude of i_L starts to decrease in the opposite direction.

Mode 2 [t_1,t_2]: as the magnitude of i_L continues to decrease in the opposite direction, when its value equals to 0 at instant t_1, D_3 will be conducted to provide another avenue for i_L to flow through. Moreover, due to the direction reversion of i_L, the current on the secondary side will flow through S_6 and S_7 instead of D_6 and D_7. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. As a consequence, V_2 supplies power to the inductor, and the magnitude of i_L starts to increase in the positive direction.

Mode 3 [t_2,t_3]: at the instant t_2, S_3 is switched off. Nevertheless, it will not affect the circuit connection because of the conduction of D_3. Within this interval, $V_{AB} = 0$, $V'_{CD} = -nV_2$. Therefore, V_2 supplies power to the inductor, and the magnitude of i_L starts to increase in the positive direction with the same slope.

Mode 4 [t_3,t_4]: at the instant t_3, S_6 and S_7 are switched off, which leads to charging C_6, C_7 and discharging C_5, C_8. When they are fully charged and discharged to V_2 and 0 respectively, D_5, D_8 will be conducted, which enables the soft switch of S_5 and S_8. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. Thus, V_2 supplies power to the inductor, and the magnitude of i_L starts to decrease in the positive direction.

Mode 5 [t_4,t_5]: at the instant t_4, S_1 is switched off, which results in charging C_1 and discharging C_2 to V_1 and 0 respectively. When this process is completed, D_2 will be conducted, which ensures the soft switch of S_2. Within this interval,

$V_{AB} = -V_1$, $V'_{CD} = nV_2$. Consequently, the inductor supplies power to V_1 and V_2, and the magnitude of i_L continues to decrease in the positive direction with a larger slope.

Mode 6 [t_5,t_6]: as the magnitude of i_L continues to decrease, its value equals to 0 with a tendency to flow in the opposite direction at the instant t_5. Because of the open circuit fault happened on S_4, the reversion of the direction of i_L will result in charging C_4 and discharging C_3. When they are fully charged and discharged to V_1 and 0, D_4 will be conducted. Additionally, D_5 and D_8 will be disconnected because of the reversion of the direction of i_L. Within this interval, $V_{AB} = 0$, $V'_{CD} = nV_2$. Therefore, the inductor supplies power to V_1 and V_2, and the magnitude of i_L starts to increase in the opposite direction.

Mode 7 [t_6,t_7]: at the instant t_6, S_4 is switched off, which results in charging C_4 and discharging C_3 to V_1 and 0. When this process is complete, D_3 will be conducted, which ensures the soft switch of S_3. However, because of the direction of i_L, when S_3 is switched on, it will flow through it directly. Within this interval, $V_{AB} = -V_1$, $V'_{CD} = nV_2$. Thus, the inductor is charged by V_1 andV_2, and the magnitude of i_L continues to increase in the opposite direction with a larger slope.

Mode 8 [t_7,t_8]: at the instant t_7, S_5 and S_8 are switched off, which leads to charging C_5, C_8 and discharging C_6, C_7. When they are fully charged and discharged to V_2 and 0 respectively, D_6, D_7 will be conducted, which enables the soft switch of S_6 and S_7. Within this interval, $V_{AB} = -V_1$, $V'_{CD} = -nV_2$. As a consequence, the inductor is charged by V_1 and V_2, and the magnitude of i_L continues to increase in the positive direction with a smaller slope.

C. THE TRANSISTORS OPEN CIRCUIT FAULT ON THE SECONDARY BRIDGE

When the open circuit faults occur to the transistors of the secondary side, the distortion severity of main waveforms depends 2 conditions, which are the time instant that the direction of i_L reverses. However, the EPS control only has inner phase shift on primary side while the secondary bridge voltage has no inner phase shift. Thus, the corresponding open-circuit fault analysis for DAB converter with EPS is regarded as the same as the SPS control.

Fig. 5(a) illustrates the open circuit fault on switches S_5 or S_8, which cause the amplitude of V'_{CD} is dropping from positive to zero when inductor current is decreasing from positive to negative during t_6 and t_7. The typical waveforms when the open circuit faults occur on S_6 or S_7 are illustrated in Fig. 5(b). The fault condition is similar like S_5 and S_8, but the problem is happed on moment of inductor current from negative to positive. Due to the space constraints, the detailed analysis for the open-circuit faults on the secondary devices will not present here.

IV. FAULT DIAGNOSIS STRATEGY

The previous theoretical analysis on the behavior of the typical waveforms when open circuit faults occur to transistors is used for the design of the fault diagnose strategy.

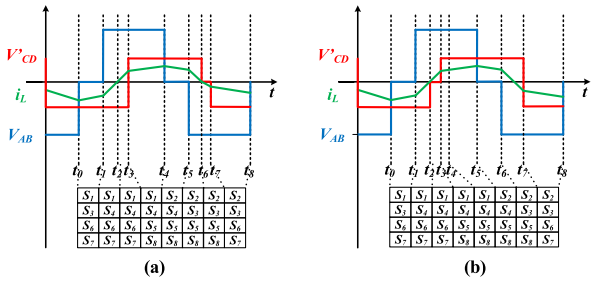

FIGURE 5. Typical waveforms of the DAB converter when faults happen on different transistors of the secondary side under condition 2. (a) Open circuit fault on S_5 or S_8. (b) Open circuit fault on S_6 or S_7.

By analyzing these waveforms of transistors under faulty conditions, it is noticed that the distortion of key waveforms are mainly caused by the parasitic resonant states and the conduction of the freewheeling diodes. Therefore, it will inevitably change the average mean value of the voltage potential at the middle position on the corresponding faulty leg.

However, if the fault diagnose method is merely based on the distortion of V_{AB} and V_{CD}, it will lead to two major problems. Firstly, since both V_{AB} and V_{CD} are AC voltage whose amplitude is much larger than the limitation of ADC port in microcontroller like DSP, the changing voltage polarity and larger amplitude may cause the voltage sensor essential to measured result of the V_{AB} and V_{CD}. It will increase the cost of entire fault detection system. Secondly, the single distortion phenomenon of V_{AB} and V_{CD} can be related to multiple open-circuit fault conditions. For example, the open circuit fault on S_1 and the open circuit fault on S_4 under condition1 may cause same distortion on V_{AB} and i_L in Fig. 3(a). So it is impossible to accurately identify the open circuit fault actually located on S_1 or S_4 with those variables.

In order to solve above two problems, the mid-point voltage of each switches pairs is used to replace AC voltage V_{AB} and V_{CD} as the voltage signal in fault diagnose method. In Fig.1, it can be seen that A, B, C and D are the midpoint of each switches pairs. V_A represents the voltage different between midpoint A and the ground point G. Similar, V_B, V_C and V_D can be measured through the switches arm midpoint B, C and D with corresponding ground, respectively. In Fig. 6(a), the distortion of primary AC output can be divided as midpoint voltage V_A and V_B. According to the operation principle of DAB converter, the midpoint voltage is 50% duty cycle square wave and the amplitude is equal to V_1 or V_2 under normal operation condition and the average value of each square wave can be calculated as:

$$Avg\,(V_A) = Avg\,(V_B) = \frac{V_1}{2}, \quad Avg\,(V_C) = Avg\,(V_D) = \frac{V_2}{2} \tag{3}$$

where the $Avg(V_A)$, $Avg(V_B)$, $Avg\ (V_C)$ and $Avg(V_D)$ are the average value of V_A, V_B, V_C and V_D under normal operation condition. According to the previous analysis in section III and Fig. 6(a), during moment from t_2 to t_4, the positive

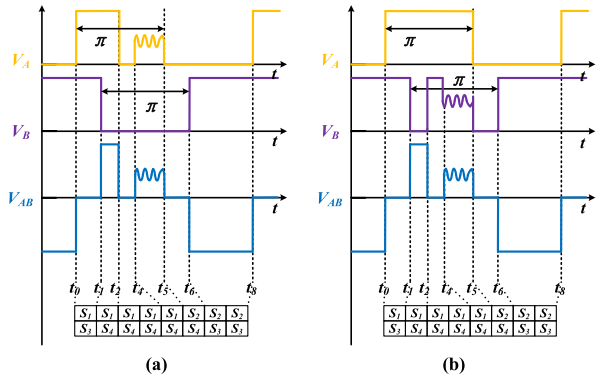

FIGURE 6. Typical waveforms of the DAB converter when the open-circuit fault happen on S_1 or S_4 under condition 1. (a) Fault on S_1. (b) Fault on S_4.

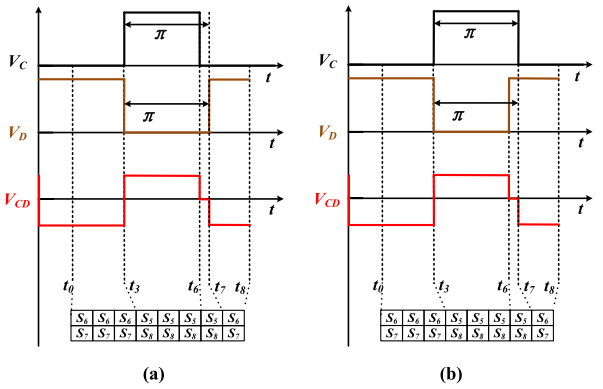

FIGURE 7. Typical waveforms of the DAB converter when open-circuit faults happen on S_5 or S_8 under condition 1. (a) Fault on S_5. (b) Fault on S_8.

inductor current i_L is flowing through S_4 and D_2 on S_1 open fault condition instead of flowing through S_1 and S_4 under normal condition. So the amplitude of V_A is decreasing to zero during this moment. Similar, the oscillation of V_{AB} during the time interval from t_4 to t_5 is also shown in V_A. Due to the amplitude of V_A is equaled to zero during time interval from t_2 to t_4 and suffered oscillation during time interval from t_4 to t_5, the average value of V_A will be obvious less than $V_1/2$. In the same time, the inductor current i_L is always flowing the S_4 or D_4, which is same as the normal operation condition. So the midpoint voltage V_B maintains as 0 during moment from t_1 to t_6, which is same as normal operation condition. In Fig. 6(b), the open circuit fault on S_4 under condition 1, the inductor current i_L is always flowing S_1 and D_1, which can ensure the V_A maintain amplitude as V_1. However, the conduction path of the inductor current i_L is changing from S_4 or D_4 to S_3 or D_3 during moment from t_2 to t_6. It cause the distortion of the midpoint voltage V_B and the average of V_B is larger than $V_1/2$. According to previous analysis and Fig.6, it is clearly that midpoint voltage V_A and V_B can not only represent the distortion of V_{AB}, but also has ability to locate certain fault component. So the midpoint voltage is selected as the proper diagnostic criterion in proposed fault diagnose method.

Open circuit faults on S_5 and S_8 are shown in Fig. 7. It can be seen that the fault on S_5 only cause the average of V_C become less than $V_2/2$, and the fault on S_8 only cause the average of V_D becoming larger than $V_2/2$. It proves V_C and V_D can perfectly represent the distortion of V_{CD}, which can actually be used to locate fault component.

Based on previous analysis, midpoint voltages V_A, V_B, V_C, and V_D are chosen as diagnostic criterion in design of fault detection scheme In Fig, 8. By comparing the average value of those midpoint with standard average value $V_1/2$ or $V_2/2$, the fault can be detected and located. The threshold voltage Δ is designed to adjust the sensitivity of the proposed fault diagnose method for avoiding false operation or malfunction. It should be smaller enough for just ensuring normal operation with noise condition, which eliminate the influence of noise

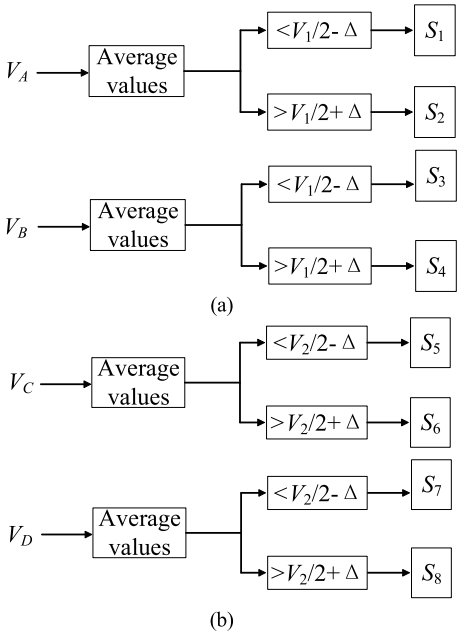

FIGURE 8. Block diagram of the open circuit faults diagnose strategy (a) for the primary side (b) for the secondary side.

and ensure sensitivity to fault operation condition. However, the value of threshold voltage Δ is highly dependent on the noise degree of normal operation, which is different on various DAB hardware. So the value of threshold voltage Δ need to be determined through experiments. In literature [47], it set threshold voltage as 7V for determining properly operation condition. After repeatedly testing and adjusting the Δ with experimental hardware platform in this paper, 5V is considered as a proper value for ensuring stability and the effectiveness of proposed detection method.

V. SIMULATION RESULTS

The simulation results by using the proposed open-circuit fault detection algorithm are presented in this section. Since the algorithm is designed based on the typical waveforms such as V_{AB} and V_{CD} as shown in Fig. 2, the fault diagnosis

results should be similar under condition 1 and condition 2 except the fault trigger moment. Therefore, this paper adopts open-circuit faults on transistors under condition 2 to verify the proposed fault detection algorithm. Table 4 summarizes main parameters for the DAB converter.

TABLE 4. Parameters for the DAB converter.

Parameter	Value
V_1	100 V
V_2	75 V
L	40 μH
$C_{1\sim8}$	50 pF
Transformer turns ratio	2
Switching frequency	20 kHz

Fig. 9(a) illustrates the simulated waveforms of the DAB converter when an open circuit fault occurs on S_1. In this figure, main waveforms such as the primary voltage "V_{AB}", the secondary voltage "V'_{CD}", and the inductor current "i_L" are depicted in the upper subfigure, while the fault trigger signal is depicted in the lower subfigure. The DAB converter works normally until t = 17 μs, when the transistor S_1 experiences an open-circuit fault. "V_{AB}" shows obvious oscillations due to the resonance. The current "i_L" is negatively biased. With the proposed fault detection algorithm, the open-circuit fault at transistor S_1 is correctly detected, as illustrated in Fig. 9(a). Similar results are presented for the open-circuit faults happen on other devices. The simulation results meet the theoretical results in Fig. 4 well, which verifies the correctness of the operation modes analysis under faulty conditions for the DAB converter with the EPS control.

VI. EXPERIMENTAL RESULTS

To validate the analysis and simulation results, experimental results were presented in this section. The DAB experimental platform was built and shown in Fig. 10 and the control system was implemented by using a DSP28335 board. During the test, the DAB was controlled to work under various voltage and current levels. Main parameters for the DAB converter are shown in Table 5.

TABLE 5. Parameters of the DAB converter prototype.

Item	Parameter
Transformer turns ratio N	2
Inductance L_s	60 µH
Switching frequency f	20kHz
Maximum input voltage V_1	100V
Maximum output voltage V_2	100V

The experimental results under condition 1 are demonstrated in Fig. 11. DAB converter works normally until an open-circuit fault occur on S_1. Main waveforms when the fault happens to S_1 are illustrated in Fig. 11 (a), which shows that the measured inductor current is negatively biased and the circuit experienced a period of resonant state, which

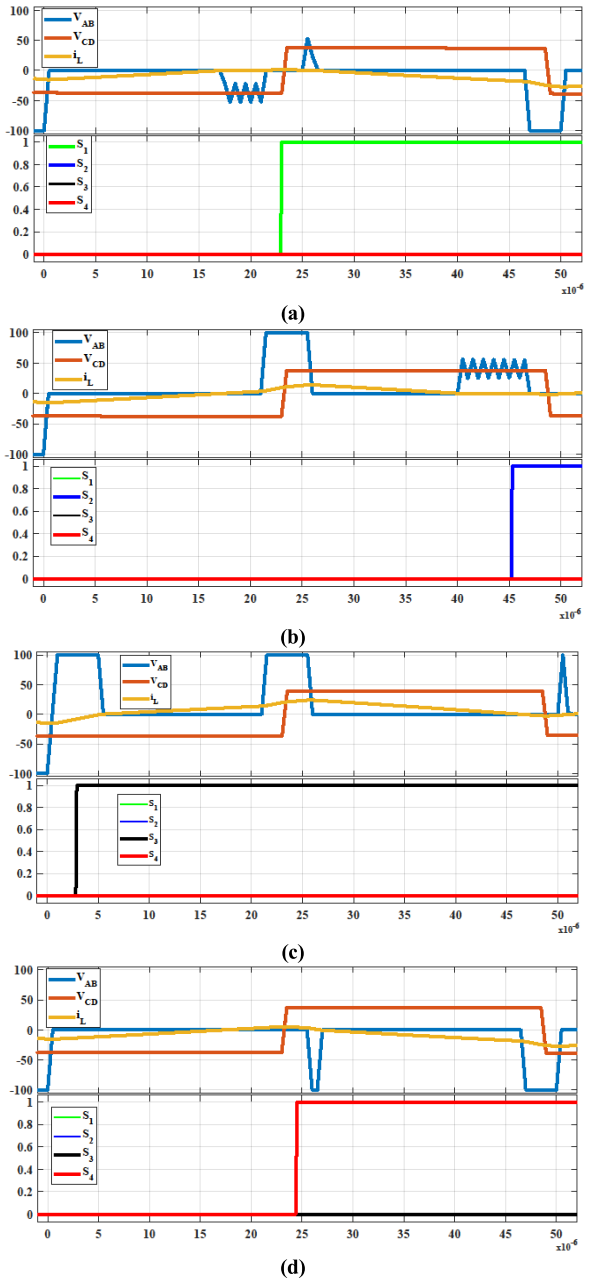

FIGURE 9. Simulation result of the DAB converter when open-circuit faults happen on different transistors on the primary side under condition 2. (a) Open circuit fault on S_1. (b) Open circuit fault on S_2. (c) Open circuit fault on S_3. (d) Open circuit fault on S_4.

matches the theoretical and simulation results well. Main waveforms when the open-circuit fault happens to S_2 are presented in Fig. 11 (b). It shows that the "i_L" is positively biased and "V_{AB}" appears resonant in a short period. For the test, the resonant distortion is observed from the waveform of "V_{AB}" because the measured primary side voltage is toggled from the maximum point to a negative one. In Fig. 11 (c) and (d), the waveforms when the open-circuit faults happen to the transistor on the secondary winding are presented. It could be observed that the distortions on V_{CD}

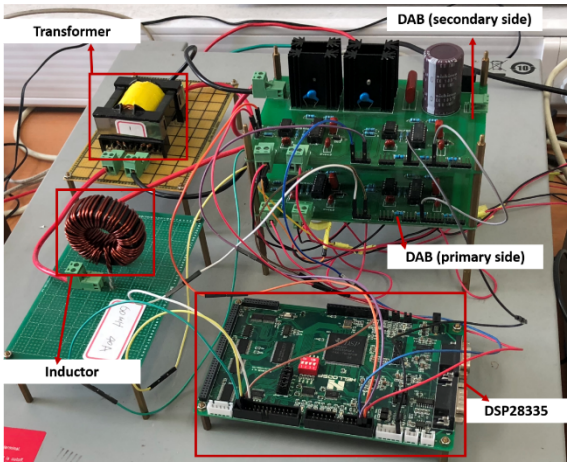

FIGURE 10. Experimental platform.

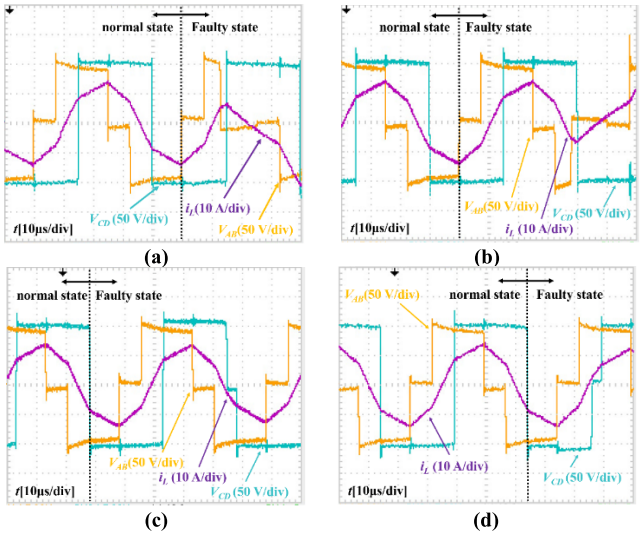

FIGURE 11. Experimental results when faults happen on different transistors of the primary side under condition 1. (a) Open circuit fault on S_1 or S_4. (b) Open circuit fault on S_2 or S_3. (c) Open circuit fault on S_5 or S_8. (d) Open circuit fault on S_6 or S_7.

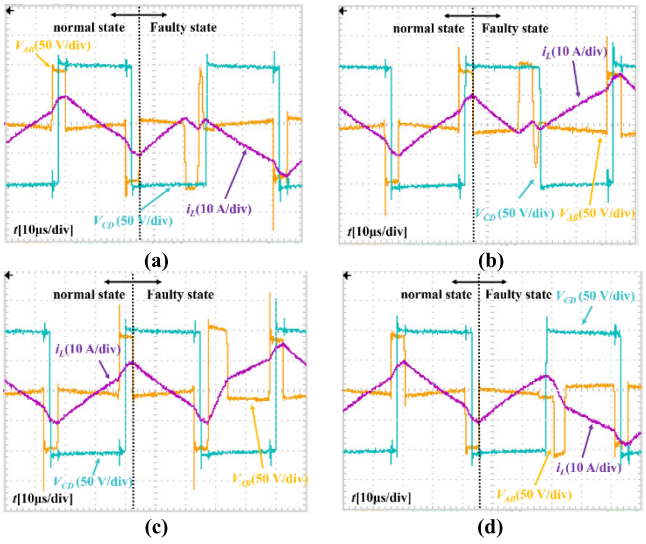

FIGURE 12. Experimental results when faults happen on different transistors of the primary side under condition 2. (a) Open circuit fault on S_1. (b) Open circuit fault on S_2. (c) Open circuit fault on S_3. (d) Open circuit fault on S_4.

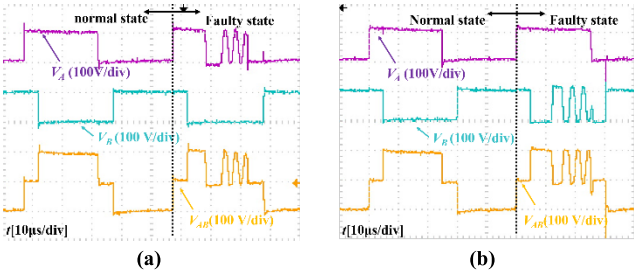

FIGURE 13. Experimental results when faults happen on different transistors of the primary side under condition 1. (a) Open circuit fault on S_1. (b) Open circuit fault on S_4.

have less impact on the bias of i_L, compared to the distortion on V_{AB}.

Fig. 12 (a), (b), (c) and (d) present the measured results when the open-circuit faults happen to S_1, S_2, S_3 and S_4 respectively under condition 2. In Fig. 12(a), two continuous negative pulses are observed due to the faulty state when the DAB converter is controlled by EPS, as indicated by the region of ''faulty state''. Furthermore, a positive peak is observed just after the negative pulse. The measured inductor current ''i_L'' is negatively biased, which is the same as the fault under the condition 2. However, the current ''i_L'' shows more oscillations after the faults.

Fig. 13(a) shows the distortion of AC input voltage on V_{AC}, midpoint voltage V_A and midpoint voltage V_B when open circuit fault happed on S_1 under condition 1. In normal state, both V_A and V_B are square wave with 50% duty cycle and 100V peak value. So the average vault should be equal to 50V, which is same as half of input voltage V_1. In fault state, it is clearly that the distortion of fault transient moment on V_A can represent the distortion of V_{AB}, while the V_B maintains same as normal operation condition. The experimental results prove the previous theoretical analysis in Fig. 6(a) that V_A and V_B can be used to identify fault component. Fig. 13(b) shows the experimental results when fault happens on switch S_4. Although the distortions of fault V_{AB} are similar as the fault on S_1 condition, the fault transient moment has the effect on V_B instead of V_A under S_1 fault condition. Thus, the open circuit fault on S_1 and S_4 can be detected and located by measuring and processing the midpoint voltage V_A and V_B. It verify the previous theoretical analysis. The secondary side AC voltage V_{CD} has similar relationship with midpoint V_C and V_D.

Fig. 14 (a) and (b) illustrates the measured fault trigger signals, which correspond to the fault on S_1 and S_2 respectively. The measured open-circuit fault detection performance among different devices shows some kind of difference by observing the two figures. Specifically, after the distortions of key waveforms occurs, the time required to detect the fault on

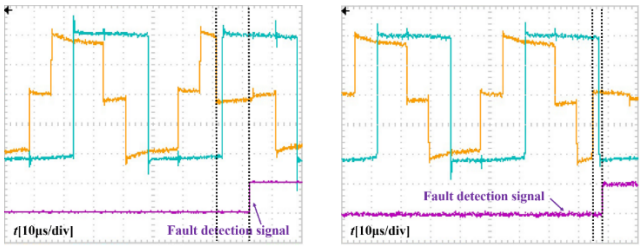

FIGURE 14. Experimental results of fault detection control. (a) Open circuit fault on S_1. (b) Open circuit fault on S_2.

S_1 and S_2 is approximately 10 μs and 3 μs, respectively. The results validate the advantage of the proposed algorithm in terms of the fault detection accuracy and fast detection merit.

VII. CONCLUSION

Reliability is essential for the power converters such as the bidirectional isolated dual-active-bridge (DAB) dc-dc converter. With the advanced control such as extended-phase-shift control (EPS), the open-circuit diagnosis for power devices in DAB converter becomes more challenging due to more operation modes and faulty conditions. This paper proposes a simple and fast fault diagnosis strategy for DAB converters with the EPS control to improve the reliability. Different operation conditions are classified according to the direction of the inductor current on the primary side. A comprehensive operation analysis during normal and faulty conditions is presented. Then, the fault diagnosis criteria are determined according to the average mean values of the primary or secondary side voltage. Consequently, an open circuit faults diagnose strategy is derived to quickly identify failures position and devices in either transistors or diodes without adding any hardware cost. The research shows that an open-circuit fault in a transistor will produce the oscillations in the middle-point voltage due to the parasitic resonance. Furthermore, a positive or negative bias is observed for the inductor current for the leg containing the faulty device. Considering the middle-voltage difference for various legs, the method of determining all transistors in both primary and secondary sides are derived and the threshold is tuned considering the tradeoff between the fault detection speed and accuracy. Main simulation and experimental results show that the fault conditions are the same as the previous analysis. The proposed fault diagnose strategy can quickly detect the faulty devices. It is also worth noting that the oscillations and distortions of waveforms affect the average value of their bridge arm.

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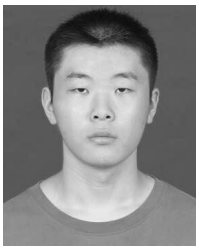

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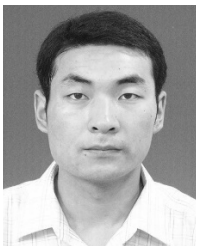

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