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98-dB Gain Class-AB OTA With 100 pF Load Capacitor in 180-nm Digital CMOS Process

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ABSTRACT In this paper, a new two-stage class-AB operational trans-conductance amplifier (OTA) is proposed. Using active loads in the first stage and improved recycling structure, the effective trans-conductance of the first stage is increased. The nonlinear current mirrors boost the current of the second stage in the slewing mode, leading to the increase of the slew rate (SR). Exploiting the multi-path scheme and increasing the effective trans-conductance cause the OTA DC-gain to be enhanced. The proposed OTA has been fabricated using 1P6M 180-nm CMOS technology under 1.8 V supply voltage. The OTA exhibits 98 dB DC-gain and 21 MHz unity-gain bandwidth with a 100 pF capacitive load, consuming 3 mW from 1.8 V supply voltage.

INDEX TERMS Class-AB OTA, trans-conductance, nonlinear current mirror, multi-path scheme, DC-gain.

I. INTRODUCTION

Operational trans-conductance amplifiers (OTAs) are a basic building block of various analog and mixed signal circuits. They are widely used in continuous-time Gm-C filters, switched-capacitor circuits, data converters, and low-dropout (LDO) voltage regulators [1]–[7]. In applications such as very high-resolution delta-sigma modulators and LDO voltage regulators, the OTA should drive large capacitive loads (even 200pF [7]) and meanwhile keep high enough the DC-gain, unity-gain bandwidth (UGBW), and slew rates (SR), while working under low voltage supply and low static power [5]–[7]. These features cannot easily be achieved using conventional class-A OTAs since enhancing SR and UGBW are obtained at the cost of increased power dissipation. However, some class-A OTAs, mostly relying on the sub-threshold and body driven techniques, have been reported in the literature to alleviate the above mentioned problem [8]–[11].

When driving large capacitive loads aimed, the ultimate solution is to employ class-AB OTA [7], [12]–[16]. In [7], a fully differential class-AB OTA capable of driving 200pF load capacitance is presented, which is based on the single-stage structure with nonlinear current amplifier. In [12], adaptive biasing circuit (ABC) [17]–[25] is applied in the tail of the input differential pair, leading to very high SR. This circuit is improved in [13] by utilizing nonlinear current mirrors at the output stage. The main goal in [12] and [13] is to achieve high SR while driving 80pF load capacitance. In contrast, DC-gain and UGBW are not taken into account satisfactorily in these works. The main concentration of [14] is to design an ultra-low voltage, ultra-low power class-AB OTA with 10pF load capacitance by utilizing ABC technique. DC-gain, SR, and UGBW are not remarkable enough in [14]. In [15], in addition to SR, DC-gain is also taken into account. For this purpose, both the recycling folded cascade (RFC) OTA [26] and ABC are combined to drive 70pF load capacitance. The RFC amplifier have better UGBW and SR compared to the conventional folded-cascade (FC) amplifier for the same area, power budgets, and capacitive load [26]. Although the disadvantages of the above mentioned works are explained here, they are all admirable works and provide variety of solutions for the designer on the table. A designer considering his/her own required specifications could select the appropriate one.

In this paper, a two-stage class-AB OTA is presented, capable of driving 100 pF load capacitance. The first stage is a folded cascade amplifier, in which the improved recycling

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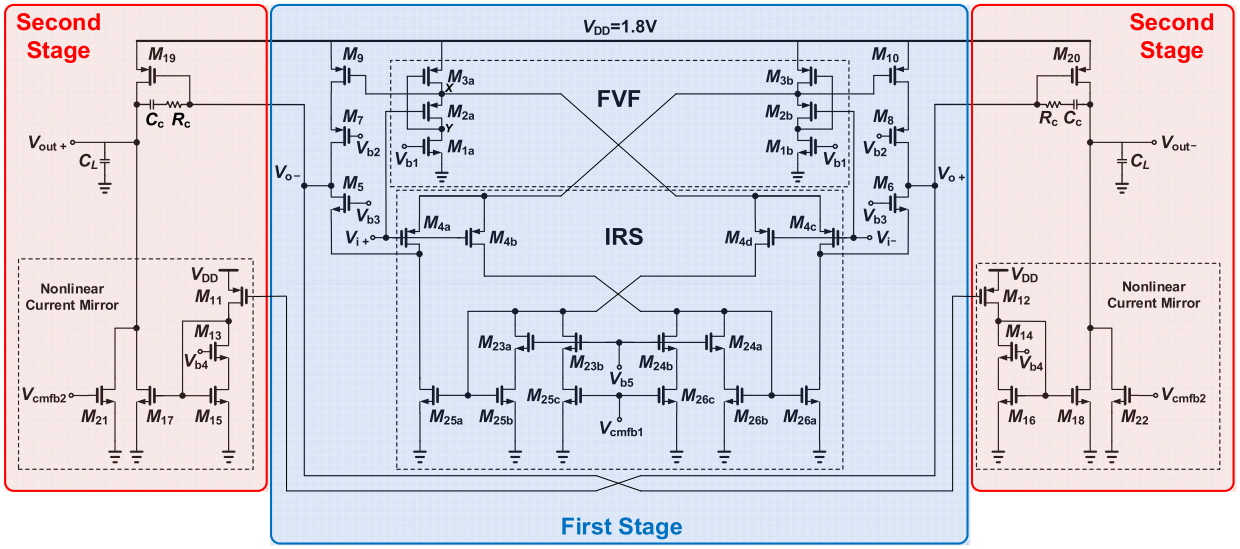

FIGURE 1. The proposed class-AB OTA.

structure (IRS) [27] is utilized to increase the effective trans-conductance. The high DC-gain is achieved by increasing the trans-conductance and using the multi-path scheme. In order to improve slew rate, both ABC in the first stage and nonlinear current mirrors in the output stage are utilized.

The rest of the paper is organized as follows. In Section II, the proposed class-AB OTA is described. The performance evaluations of the OTA and comparison results are illustrated in Section III. Finally, the conclusions are given in Section IV.

II. PROPOSED CLASS-AB OTA

The proposed two-stage class-AB OTA, utilizing a folded cascade amplifier in the first stage and the common-source amplifier in the second stage, is shown in Fig. 1. In fact, the first stage is inspired from [27], realizing IRS. In the tail of the input differential pairs, a flipped voltage follower (FVF) [28] consisting of a set of transistors (M_{1a}, M_{1b}, M_{2a}, M_{2b}, M_{3a}, M_{3b}) is used as an ABC, which help increase the SR. In Fig. 1, V_o and V_{out} signals are the output voltages of the first and second stages, respectively. By applying a large differential input signal, the FVF delivers more current compared to the quiescent current, and hence operates in class-AB. Input signals are applied to the split transistor sets with identical aspect ratio, (M_{4a}, M_{4b}) and (M_{4c}, M_{4d}). The IRS technique provides different paths for DC and AC currents, enhancing the trans-conductance. Source terminals of transistors (M_{4a}, M_{4b}) are connected to the drain of M_{3b} and to the gate of M_{10}.

Similarly, source terminals of transistors (M_{4c}, M_{4d}) are connected to the drain of M_{3a} and to the gate of M_9. Therefore, the input signal appears at the gates of active load transistors M_9 and M_{10}, enhancing the trans-conductance of the OTA. In addition, nonlinear current mirrors are utilized at the output stage, improving the SR.

A. DC ANALYSIS

When the OTA operates in the quiescent mode ($V_{i+} = V_{i-} = V_{cmi}$; V_{cmi} denotes the input common mode voltage), transistors M2a, M4c, M4d will have identical gate-source voltage. After a few simple manipulations, the bias current of input differential pairs is obtained as follows:

$$I_{3a} = \left(1 + \frac{\left(\frac{W}{L}\right)_{4c} + \left(\frac{W}{L}\right)_{4d}}{\left(\frac{W}{L}\right)_{2a}}\right) I_{1a} \tag{1}$$

where $\left(\frac{W}{L}\right)$ and I denote the aspect ratio and current of the relevant transistor, respectively. Since we have chosen identical aspect ratios for M4a, M4b, M4c, and M4d, so all of them have identical current as given below:

$$I_{4a.4b.4c.4d} = \frac{\left(\frac{W}{L}\right)_{4d}}{\left(\frac{W}{L}\right)_{2a}} I_{1a} \tag{2}$$

The first stage of the OTA utilizes two current mirrors as active load; (M23a, M25a, M25b,) and (M24a, M26a, M26b). Making use of these current mirrors equations, the bias current of other branches is obtained easily. The output common-mode voltage of the first stage, adjusted by the CMFB#1 (common-mode feedback) circuit, controls the gate voltage of M19, and consequently the bias current of the output stage is also found.

B. VOLTAGE GAIN

When a small signal is applied to the OTA input, this signal also appears across the gate-source of M9 and M10 by means of FVF. This fact is proven according to Fig. 2, in which the voltage of nodes V_X and V_Y can be calculated as follows:

$$V_X = \frac{V_i}{2} \tag{3}$$

$$V_Y = -\frac{g_{m4c} + g_{m4d}}{g_{m3a}} V_i \tag{4}$$

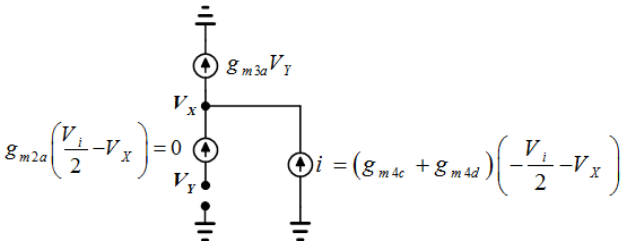

FIGURE 2. Small-signal model for calculating the voltages of the V_X and V_Y nodes.

Thus, the effective trans-conductance of the first stage increases as given below:

$$G_{m_{eff_1}} = g_{m4a} + g_{m4d}\frac{g_{m25a}}{g_{m25b}} + g_{m9} \tag{5}$$

where g_m denotes the trans-conductance of transistor. Assuming identical sizing of input transistors $M_{4a,4b,4c,4d}$, and $\alpha_1 = \frac{g_{m25a}}{g_{m25b}}$, equation (5) is rewritten:

$$G_{m_{eff_1}} = g_{m4a}(1+\alpha_1) + g_{m9} \tag{6}$$

Definition of $\alpha_1 = \frac{g_{m25a}}{g_{m25b}}$ means that M25a aspect ratio is α_1 times greater than that of M25b. In our design (more detail is given in section III), α_1 is chosen identical to 6.

This equation indicates that the proposed OTA can achieve higher trans-conductance compared with the methods reported in [16], [26], and [30].

Neglecting the body effect, DC-gain is found as follows:

$$A_d = A_1 \times A_2 \tag{7}$$

in which A_1 represents the DC-gain of the first stage as shown below:

$$A_1 = G_{m_{eff_1}} R_{out1} \tag{8}$$

where R_{out1} denotes the output resistance of the first stage:

$$R_{out1} = g_{m7} r_{ds7} r_{ds9} || \left(g_{m5} r_{ds5}\left(r_{ds4a} || r_{ds25a}\right)\right) \tag{9}$$

In the above equation, r_{ds} represents the drain-source resistor of the relevant transistor. In equation (7), A_2 stands for the DC-gain of the second stage as follows:

$$A_2 = G_{m_{eff_2}} R_{out2} \tag{10}$$

where $G_{m_{eff_2}}$ represents the effective trans-conductance of the second stage and R_{out2} is the output resistance of the second stage as given below:

$$R_{out2} = r_{ds17} || r_{ds19} || r_{ds21} \tag{11}$$

In order to derive $G_{m_{eff_2}}$, the equivalent resistance of the nonlinear current mirror should be determined (see Fig. 3.a). As mentioned in section II.D, in this nonlinear current mirror, M15 must work in the triode region. Making use of Fig. 3.b, after a few manipulation, we will have $R \cong r_{ds13}$ It is interesting to note that in the conventional current mirror, in which M15 is biased in the saturation region, R is identical to $1/g_{m15}$ [1]. Finally, $G_{m_{eff_2}}$ is obtained as follows:

$$G_{m_{eff_2}} \cong g_{m19} + g_{m11} g_{m17}\left(r_{ds11} || r_{ds13}\right) \tag{12}$$

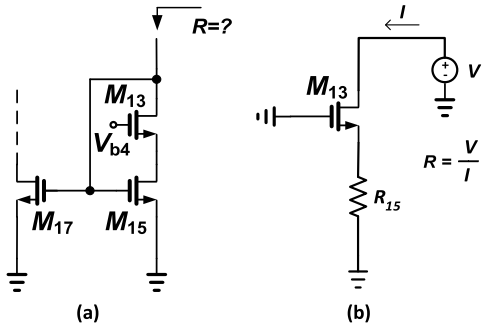

FIGURE 3. (a) Nonlinear current mirror. (b) Equivalent small-signal model.

C. FREQUENCY RESPONSE

Making use of formulas derived in [1] for conventional two-stage OTA, the UGBW is determined as follows in which C_c denotes the Miller compensation capacitor. It is easily understood that increasing the first stage trans-conductance causes UGBW improvement.

$$UGBW = \frac{G_{m_{eff_1}}}{C_c} \tag{13}$$

In addition, the second pole (ω_{p2}) is given in equation (14), where C_p denotes the parasitic capacitance at the output of the first stage (node V_{o-}) [1]. It is obvious the second stage effective trans-conductance enhancement has pushed the second pole to higher frequencies, ensuring the designer to increase UGBW appropriately without any concern about the stability problem.

$$\omega_{p2} \cong \frac{G_{m_{eff_2}}}{C_L + C_p} \tag{14}$$

It is noticeable that the large values of C_L decrease the second pole, and consequently worsen the OTA stability. In this work, we want to drive the large 100pF capacitive load, which lowers the second pole as a serious challenge.

In addition, the transfer function zero (ω_z) is obtained as shown in equation (15), in which the compensation resistor R_c provides more degrees of freedoms for designer to locate the ω_z appropriately. For this purpose, there are three conventional zero-cancellation, pole-zero cancellation, and lead compensation methods [1]; in this design the last one is exploited.

$$\omega_z \cong \frac{1}{\left(\frac{-1}{G_{m_{eff_2}}} + R_c\right) C_c} \tag{15}$$

D. EXPLOITING NONLINEAR CURRENT MIRROR FOR SR IMPROVEMENT

If the designer chooses V_{b4} properly to bias M_{15} in the triode region, we will have:

$$I_{17} = \frac{1}{2}\beta_{17} V_{od17}^2 \tag{16}$$

$$I_{15} = \beta_{15} V_{od15} V_{DS15} \tag{17}$$

where $\beta = \mu_n C_{ox} \frac{W}{L}$ and V_{od} denotes the overdrive voltage of the transistor. Moreover; μ_n, C_{ox}, W and L are electron mobility, gate-channel capacitance density ($\frac{fF}{\mu m^2}$), transistor channel width, and transistor channel length, respectively. Assuming $\beta_{17} = \beta_{15}$ and manipulating equations (16) and (17), we have:

$$I_{17} = \frac{I_{15}^2}{2\beta_{17} V_{DS15}^2} \tag{18}$$

Since $V_{DS15} = V_{b4} - V_{tn} - V_{od13}$ (V_{tn} is the threshold voltage), I_{17} is found as follows:

$$I_{17} = \frac{I_{15}^2}{2\beta_{17}\left(V_{b4} - V_{tn} - \sqrt{\frac{2I_{15}}{\beta_{13}}}\right)^2} \tag{19}$$

It is obvious there is a nonlinear relation between I_{17} and I_{15}. It is important to note that biasing M_{15} in the saturation region results in the conventional linear current mirrors ($I_{17} = I_{15}$). In other words, we have nonlinear current mirror only if M_{15} is biased in the triode region.

In this work, this nonlinear current mirror is exploited to speed up the discharge of the large load capacitance in the slewing mode. In addition, increasing the tail currents ($I_{3a} - I_{1a}.I_{3b} - I_{1b}$) of the input differential pairs improve the SR. In contrast, increasing the compensation capacitor and the load capacitor reduces the SR [1]. Furthermore, in spite of class-A OTAs which have constant bias current, the proposed class-AB OTA has dynamic bias in the slewing mode, which causes the currents of both the nonlinear current mirror and tail of the input differential pairs to increase. For example, if $V_{i+} > V_{i-}$), by making use of equations (3), (4), it is easily understood that the gate of M3a decreases, which means the increase of I_{3a} in comparison with the quiescent current of equation (1). This mechanism is called dynamic bias or adaptive bias [17]–[25].

E. INPUT-REFERRED THERMAL NOISE

The input-referred thermal noise of transistors M_{4b}, M_{4c}, M_{26a}, M_{26b} and M_9 are given by:

$$\overline{V_{ni,M4b}^2} = \left(\frac{g_{m4b}}{G_{meff1}}\right)^2 \alpha_1^2 \times \overline{V_{n,4b}^2} \tag{20}$$

$$\overline{V_{ni,M4c}^2} = \left(\frac{g_{m4c}}{G_{meff1}}\right)^2 \times \overline{V_{n,4c}^2} \tag{21}$$

$$\overline{V_{ni,M26a}^2} = \left(\frac{g_{m26a}}{G_{meff1}}\right)^2 \times \overline{V_{n,26a}^2} \tag{22}$$

$$\overline{V_{ni,M26b}^2} = \left(\frac{g_{m26b}}{G_{meff1}}\right)^2 \alpha_1^2 \times \overline{V_{n,26b}^2} \tag{23}$$

$$\overline{V_{ni,M9}^2} = \left(\frac{g_{m9}}{G_{meff1}}\right)^2 \times \overline{V_{n,9}^2} \tag{24}$$

Finally by considering $\overline{V_n^2} = \frac{4kT\gamma}{g_m}$, the total input-referred thermal noise voltage per unit bandwidth of the OTA can be found as follows:

$$\overline{V_{ni,pro}^2} = \frac{8kT\gamma}{G_{meff1}^2}\left[g_{m4b}(1+\alpha_1^2) + (g_{m26a} + g_{m26b}\alpha_1^2) + g_{m9}\right] \tag{25}$$

Therefore, increasing $G_{m_{eff_1}}$ can significantly reduce the total input-referred thermal noise voltage of the proposed OTA.

F. INPUT OFFSET

Mismatch between MOS transistors with various electrical parameters can be considered as a function of device areas, distances, and orientations [29]. It has been shown that the difference of an electrical parameter P between two rectangular devices is modeled by the standard deviation:

$$\sigma^2(\Delta P) = \frac{A_P^2}{WL} + S_P^2 D_x^2 \tag{26}$$

where A_p is the area proportionality constant for P, W and L are the width and length of the transistor, and S_P is the variation of P under the device spacing D_x. The input offset variance of the OTA is obtained using the method proposed in [26].

$$\sigma^2(I_{D,M4b}) = \frac{g_{m4b}^2 \alpha_1^2 A_{VTP}^2}{W_{4b}L_{4b}} \tag{27}$$

$$\sigma^2(I_{D,M4c}) = \frac{g_{m4c}^2 A_{VTP}^2}{W_{4c}L_{4c}} \tag{28}$$

$$\sigma^2(I_{D,M26a}) = \frac{g_{m26a}^2 A_{VTN}^2}{W_{26a}L_{26a}} \tag{29}$$

$$\sigma^2(I_{D,M26b}) = \frac{g_{m26b}^2 \alpha_1^2 A_{VTN}^2}{W_{26b}L_{26b}} \tag{30}$$

$$\sigma^2(I_{D,M9}) = \frac{g_{m9}^2 A_{VTP}^2}{W_9 L_9} \tag{31}$$

$$\sigma^2(V_{OS}) = \frac{2}{G_{meff1}^2}\left[\frac{g_{m4b}^2(1+\alpha_1^2)A_{VTP}^2}{W_{4b}L_{4b}} + \frac{g_{m26a}^2 A_{VTN}^2}{W_{26a}L_{26a}} + \frac{g_{m26b}^2 \alpha_1^2 A_{VTN}^2}{W_{26b}L_{26b}} + \frac{g_{m9}^2 A_{VTP}^2}{W_9 L_9}\right] \tag{32}$$

where A_{VTP} and A_{VTN} are the area proportionality constant for threshold voltage of PMOS and NMOS, respectively.

III. SIMULATION AND EXPERIMENTAL RESULTS

The proposed OTA (Fig. 1) is designed and fabricated in a 0.18-μm 1.8-V CMOS technology. The width and length of transistors, passive components, and bias voltages of the proposed OTA are given in Table 1. The common-mode feedbacks (CMFBs) and bias circuit are demonstrated in Figs. 4 and 5, respectively. It should be noted that in the proposed fully-differential OTA, it is necessary to add two CMFBs to determine the output common-mode voltage of each stage separately and to control it to be equal to a specified voltage. The size of transistors (width and length) and passive components of the CMFBs and bias circuit are reported in Table 2 and 3, respectively. It should be note that R_{es1}

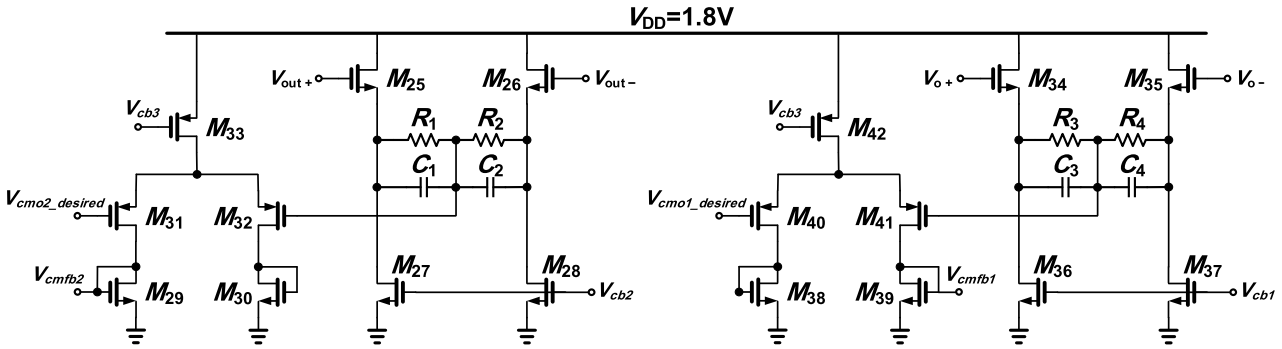

FIGURE 4. CMFB circuitries.

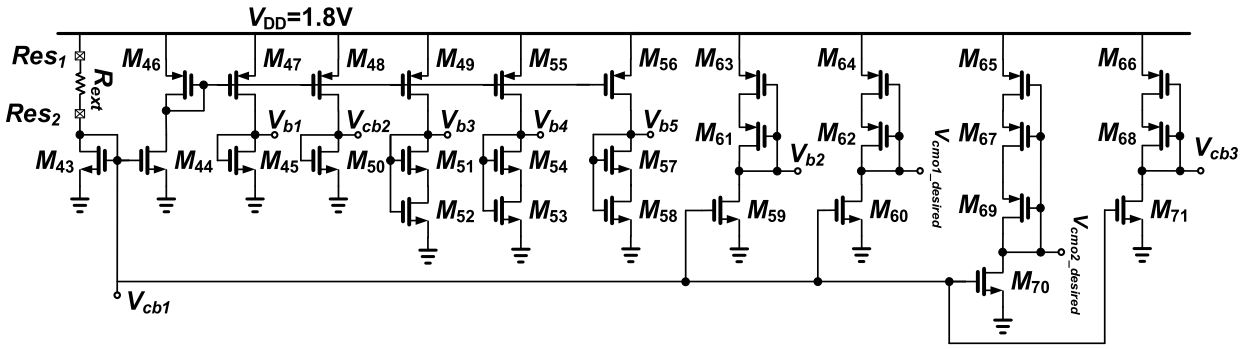

FIGURE 5. Bias circuitries.

TABLE 1. Size of transistors and passive components for the proposed OTA.

Parameter	Value	Parameter	Value
$(W/L)_{1a,1b}$	1×5μm/0.18μm	$(W/L)_{19,20}$	2×40μm/0.36μm
$(W/L)_{2a,2b}$	1×25μm/0.18μm	$(W/L)_{21,22}$	2×10μm/0.36μm
$(W/L)_{3a,3b}$	50μm/0.18μm	$(W/L)_{23a,24a}$	2μm/0.18μm
$(W/L)_{4a,4b,4c,4d}$	1×12.5μm/0.18μm	$(W/L)_{23b,24b}$	0.8μm/0.18μm
$(W/L)_{5,6}$	1×30μm/0.18μm	$(W/L)_{25a,26a}$	6×2μm/0.18μm
$(W/L)_{7,8}$	1×60μm/0.18μm	$(W/L)_{25b,26b}$	2μm/0.18μm
$(W/L)_{9,10}$	1×60μm/0.18μm	$(W/L)_{25c,26c}$	0.8μm/0.18μm
$(W/L)_{11,12}$	2×40μm/0.36μm	C_s	30 pF
$(W/L)_{13,14,15,16}$	2×10μm/0.36μm	C_L	100 pF
$(W/L)_{17,18}$	2×10μm/0.36μm	R_s	500Ω

TABLE 2. Size of transistors and passive components for the CMFBs.

Parameter	Value	Parameter	Value
$(W/L)_{25,26}$	1×20μm/0.18μm	$(W/L)_{36,37}$	1×20μm/0.18μm
$(W/L)_{27,28}$	1×20μm/0.18μm	$(W/L)_{38,39}$	1×4.25μm/0.18μm
$(W/L)_{29,30}$	2×20μm/0.18μm	$(W/L)_{40,41}$	1×20μm/0.18μm
$(W/L)_{31,32}$	1×20μm/0.18μm	$(W/L)_{42}$	2×20μm/0.18μm
$(W/L)_{33}$	2×20μm/0.18μm	R_1, R_2, R_3, R_4	20 kΩ
$(W/L)_{34,35}$	1×20μm/0.18μm	C_1, C_2, C_3, C_4	1.5 pF

and R_{es2} terminals shown in Fig. 5, are connected externally to a highly precise off-chip 100-kΩ resistor to generate the required bias voltages. Table 4 shows the simulation results

TABLE 3. Size of transistors for Bias Circuit.

Parameter	Value	Parameter	Value
$(W/L)_{43,44,45}$	1×0.5μm/0.18μm	$(W/L)_{57}$	0.5μm/0.18μm
$(W/L)_{46}$	1×5μm/0.18μm	$(W/L)_{58}$	0.85μm/3μm
$(W/L)_{47}$	1×3μm/0.18μm	$(W/L)_{59,60}$	0.5μm/0.18μm
$(W/L)_{48}$	1×6.5μm/0.18μm	$(W/L)_{61,62}$	1×4μm/0.18μm
$(W/L)_{49}$	1×4μm/0.18μm	$(W/L)_{63}$	1×1μm/0.6μm
$(W/L)_{50,51}$	1×0.5μm/0.18μm	$(W/L)_{64,65}$	1×1μm/1.6μm
$(W/L)_{52}$	1×0.85μm/3μm	$(W/L)_{66}$	1×5μm/0.2μm
$(W/L)_{53}$	1×0.5μm/0.2μm	$(W/L)_{67}$	1×1μm/1μm
$(W/L)_{54}$	1×0.7μm/0.18μm	$(W/L)_{68,69}$	1×4μm/0.18μm
$(W/L)_{55}$	1×4μm/0.18μm	$(W/L)_{70}$	1×0.3μm/0.18μm
$(W/L)_{56}$	4μm/0.18μm	$(W/L)_{71}$	1×0.5μm/0.18μm

of DC-gain, input-referred noise, input offset, differential output swing, phase margin, power dissipation, slew rate, and UGBW for the proposed OTA in three process and temperature corners. As can be seen from the results, the proposed OTA has high DC-gain due to trans-conductance improvement and also because of using multi-path scheme. For the slew rate measurement, a square wave, 1 V_{pp} at 2 MHz was applied to the OTA in the unity gain capacitive buffer configuration [26] and the results are reported.

The proposed OTA was fabricated using 1P6M 180-nm CMOS technology. The chip microphotograph is

TABLE 4. Specifications of the proposed OTA in various process and temperature corners.

Specification	Proposed OTA		
	TT(27° C)	FF(−40° C)	SS(90° C)
Technology	0.18 µm	0.18 µm	0.18 µm
DC-Gain (dB)	105	96	107
Input-Reffered Noise@100kHz $(\mu v/\sqrt{Hz})$	0.25	0.21	0.29
Input Offset (3σ) [mV]	14.6	14.5	14.8
Differential Output Swing (peak to peak) (V)	2.8	2.8	2.8
Phase Margin (°)	79	78	79
Power Dissipation (mW)	2.9	4	2.3
Slew Rate (V/µs)	61	87	42
UGBW (MHz)	25	35	18
Loading Capacitance (pF)	100	100	100

TABLE 5. Performance comparison of the proposed OTA and the existing methods.

Specifications	This work	[13]	[15]	[7]
Technology	0.18µm	0.5µm	0.5µm	0.18µm
Supply Voltage (V)	1.8	±1	±1	1.8
Loading Capacitance (pF)	100	80	70	200
Fully Differential	Yes	No	No	Yes
Compensation	Miller	Load Cap.	Load Cap.	Load Cap.
SR+ (V/µs)	51	20	13.2	74.1
SR- (V/µs)		-54	-25.3	
DC Gain (dB)	98	39	76.8	72
Phase Margin (°)	71	58	75.1	50
UGBW (MHz)	21	3.46	3.4	86.5
Input-Referred Noise $(\frac{\mu V}{\sqrt{Hz}})$	0.25 @100kHz	0.044 @100kHz	0.023 @1MHz	---
Power Dissipation (mW)	3	0.14	0.1	11.9
Area (mm^2)	0.053	0.054	0.03	0.07

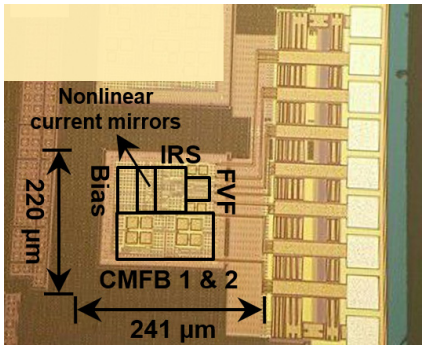

FIGURE 6. Microphotograph of the chip.

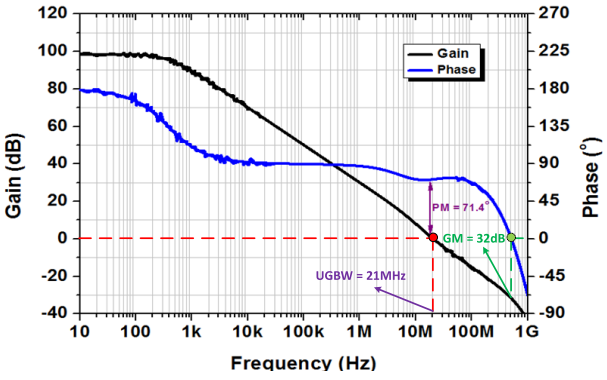

FIGURE 7. The measured open loop frequency responses for the proposed OTA.

demonstrated in Fig. 6. Silicon area of the OTA is 0.053 mm^2. The open loop frequency responses are measured using the E5061B network analyzer, and the results are shown in Fig. 7. The results indicate that DC-gain, UGBW, and phase margin of the OTA are 98 dB, 21 MHz and 71.4°, respectively. Besides phase margin, another measure of stability is the gain margin. This is defined to be $1/|Gain(j\omega)|$ in decibels at the frequency where $phase(Gain(j\omega))$ changes $-180°$, and this must be greater than 0 dB for stability. As shown in Fig. 7, according to measurement results, gain margin is almost 32dB in this work. For the slew rate measurement, a square wave with amplitude 1 V_{pp} at 2 MHz is applied to the OTA and the result obtained from GDS-2104 oscilloscope is shown in Fig. 8. The average SR of the OTA is 51 $V/\mu s$.

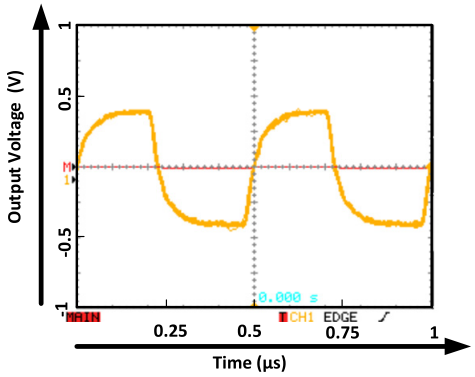

FIGURE 8. The measured OTA large signal step response.

Measurement results of the proposed OTA are compared with existing class-AB works and the results are summarized in Table 5. This table shows that the proposed OTA has DC-gain higher than the other works, but like [7] suffers from high power consumption. In spite of [13] and [15] utilizing the single-ended structure, the proposed OTA and [7] use the fully differential structure, which inherently increases the overall power consumption because of the CMFB circuit requirement. Furthermore, these works drive the larger load capacitance, while maintaining higher SR and UGBW compared to [13] and [15].

IV. CONCLUSION

In this paper, a new two-stage class-AB OTA in a 0.18μm CMOS process with a 1.8 V supply voltage has been proposed. The effective trans-conductance of the first stage has been improved by employing active loads in the first stage and an IRS technique. SR enhancement has been achieved using a nonlinear current in order to boost the output current. The OTA has high DC-gain due to trans-conductance enhancement and a multi-path scheme. In order to evaluate the performance of the proposed method, several simulations and measurements have been carried out.

REFERENCES

[1] T. C. Carusone, D. Johns, and K. Martin, *Analog Integrated Circuit Design*, 2nd ed. Hoboken, NJ, USA: Wiley, 2012.

[2] C. Briseno-Vidrios *et al.*, "A 44-fJ/conversion step 200-MS/s pipeline ADC employing current-mode MDACs," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3280–3292, Nov. 2018. doi: 10.1109/JSSC.2018.2863959.

[3] M. Marx, D. De Dorigo, S. Nessler, S. Rombach, and Y. Manoli, "A 27 μW 0.06 mm^2 background resonance frequency tuning circuit based on noise observation for a 1.71 mW CT-$\Delta\Sigma$ MEMS gyroscope readout system with 0.9°/h bias instability," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 174–186, Jan. 2018. doi: 10.1109/JSSC.2017.2747215.

[4] V. Sarma, N. A. Jacob, B. D. Sahoo, V. Narayanaswamy, and V. Choudhary, "A 250-MHz pipelined ADC-based fs/4 noise-shaping bandpass ADC," in *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 6, pp. 1785–1794, Jun. 2018. doi: 10.1109/TCSI.2017.2766883.

[5] A. Maity and A. Patra, "Dynamic slew enhancement technique for improving transient response in an adaptively biased low-dropout regulator," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 7, pp. 626–630, Jul. 2015. doi: 10.1109/TCSII.2015.2415311.

[6] A. Maity and A. Patra, "A hybrid-mode operational transconductance amplifier for an adaptively biased low dropout regulator," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1245–1254, Feb. 2017. doi: 10.1109/TPEL.2016.2554400.

[7] S. Sutula, M. Dei, L. Terés, and F. Serra-Graells, "Variable-mirror amplifier: A new family of process-independent class-AB single-stage OTAs for low-power SC circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 8, pp. 1101–1110, Aug. 2016. doi: 10.1109/TCSI.2016.2577838.

[8] K. Ueno, T. Hirose, T. Asai and Y. Amemiya, "A 300 nW, 15 ppm/°C, 20 ppm/V CMOS voltage reference circuit consisting of subthreshold MOSFETs," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 2047–2054, Jul. 2009.

[9] L. H. C. Ferreira, T. C. Pimenta, and R. L. Moreno, "An ultra-low-voltage ultra-low-power CMOS Miller OTA with rail-to-rail input/output swing," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 10, pp. 843–847, Oct. 2007. doi: 10.1109/TCSII.2007.902216.

[10] L. H. C. Ferreira and S. R. Sonkusale, "A 60-dB gain OTA operating at 0.25-V power supply in 130-nm digital CMOS proces," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 6, pp. 1609–1617, Jun. 2014. doi: 10.1109/TCSI.2013.2289413.

[11] G. Raikos and S. Vlassis, "Low-voltage bulk-driven input stage with improved transconductance," *Int. J. Circuit Theory Appl.*, vol. 39, no. 3, pp. 327–339, Mar. 2011. doi: 10.1002/cta.637.

[12] A. J. López-Martín, S. Baswa, J. Ramirez-Angulo, and R. G. Carvajal, "Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1068–1077, May 2005.

[13] J. A. Galan, A. J. Lopez-Martin, R. G. Carvajal, J. Ramirez-Angulo, and C. Rubia-Marcos, "Super class-AB OTAs with adaptive biasing and dynamic output current scaling," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 3, pp. 449–457, Mar. 2007. doi: 10.1109/TCSI.2006.887639.

[14] M. R. Valero, S. Celma, N. Medrano, B. Calvo, and C. Azcona, "An ultra low-power low-voltage class AB CMOS fully differential OpAmp," in *Proc. IEEE Int. Symp. Circuits Syst.*, Seoul, South Korea, May 2012, pp. 1967–1970. doi: 10.1109/ISCAS.2012.6271661.

[15] M. P. Garde, A. López-Martín, R. G. Carvajal, and J. Ramírez-Angulo, "Super class-AB recycling folded cascode OTA," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2614–2623, Sep. 2018. doi: 10.1109/JSSC.2018.2844371.

[16] S. M. Anisheh and H. Shamsi, "Two-stage class-AB OTA with enhanced DC gain and slew rate," *Int. J. Electron. Lett.*, vol. 5, no. 4, pp. 438–448, 2016. doi: 10.1080/21681724.2016.1253780.

[17] G. Ferri, "Low-power adaptive biased integrated amplifiers," *Analog Integr. Circuits Signal Process.*, vol. 33, no. 3, pp. 251–264, Dec. 2002.

[18] Ozaki, T., T. Hirose, K. Tsubaki, N. Kuroki, and M. Numa, "Nano watt power rail-to-rail CMOS amplifier with adaptive biasing circuits for ultralow-power analog LSIs," *Jpn. J. Appl. Phys.*, vol. 54, Mar. 2015, Art. no. 04DE13.

[19] J. Torfifard and A. K. B. A'ain, "A power-efficient CMOS adaptive biasing operational transconductance amplifier," *ETRI J.*, vol. 35, no. 2, pp. 226–233, 2013.

[20] Y. Tsuruya, T. Hirose, Y. Osaki, T. Kuroki, M. Numa, and O. Kobayashi, "A nano-watt power CMOS amplifier with adaptive biasing for power-aware analog LSIs," in *Proc. ESSCIRC*, Bordeaux, France, Sep. 2012, pp. 69–72.

[21] T. Hirose, Y. Osaki, N. Kuroki, and M. Numa, "A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities," in *Proc. ESSCIRC*, Seville, Spain, Sep. 2010, pp. 114–117.

[22] T. V. Cao, D. T. Wisland, T. S. Lande, and F. Moradi, "Rail-to-rail low-power fully differential OTA utilizing adaptive biasing and partial feedback," in *Proc. IEEE Int. Symp. Circuits Syst.*, Paris, France, May/Jun. 2010, pp. 2820–2823.

[23] M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and H. J. de man, "Adaptive biasing CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-17, no. 3, pp. 522–528, Jun. 1982.

[24] G. Ferri, G. C. Cardarilli, and M. Re, "Rail-to-rail adaptive biased low-power Op-Amp," *Microelectron. J.*, vol. 32, no. 3, pp. 265–272, Mar. 2001.

[25] G. Barile *et al.*, "Power-efficient dynamic-biased CCII," in *Proc. ECCTD*, Sep. 2017, pp. 1–4.

[26] R. S. Assaad and J. Silva-Martinez, "The recycling folded cascode: A general enhancement of the folded cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2535–2542, Sep. 2009. doi: 10.1109/JSSC.2009.2024819.

[27] Y. L. Li, K. F. Han, X. Tan, N. Yan, and H. Min, "Transconductance enhancement method for operational transconductance amplifiers," *Electron. Lett.*, vol. 46, no. 19, pp. 1321–1323, 2010. doi: 10.1049/el.2010.1575.

[28] R. G. Carvajal *et al.*, "The flipped voltage follower: A useful cell for low-voltage low-power circuit design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 7, pp. 1276–1291, Jul. 2005. doi: 10.1109/TCSI.2005.851387.

[29] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989. doi: 10.1109/JSSC.1989.572629.

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