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Hardware-Based Synchronous Envelope Detection Strategy for Resolver Supplied With External Excitation Generator

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ABSTRACT In most of resolver-to-digital converters, it is necessary to detect the sinusoidal and cosinusoidal envelopes of rotor angle position from the amplitude-modulated signals the resolver outputs. Conventional synchronous envelope detection methods usually adopt a microprocessor to generate excitation signal and sample resolver signals, which is easy to ensure the synchronization of sampling. However, these methods may result in too large consumption of microprocessor resources, especially when the excitation frequency is very high. In order to reduce the burden of the microprocessor, external excitation can be used instead, and the synchronization pulse for sampling trigger can usually be generated by comparing the externally generated carrier with a reference through comparison circuit. However, the unexpected factors in hardware may cause deviations of the synchronization pulse instants and thus affect the accuracy of the detected envelopes. In order to solve this problem, a novel strategy of synchronous envelope detection by using hardware circuits is proposed in this paper. First, error propagation of the unexpected factors to the synchronization pulse is minimized by optimizing the reference voltage for the comparison circuit. Second, the effects of the synchronization pulse instant deviations on the accuracy of the detected envelopes are minimized by optimizing the sampling phase of the resolver signals. Theoretical analysis indicates that high-accuracy synchronous envelope detection can be realized since the minimum effects of unexpected factors. Experimental results support the conclusion of theoretical analysis, and prove the effectiveness and feasibility of the proposed strategy.

INDEX TERMS Resolver, synchronous envelope detection, error propagation, noise suppression.

I. INTRODUCTION

Resolver is featured by strong anti-interference capacity and high accuracy, and has been widely used in aerospace, military affairs, industrial robot and other servo-controlled systems requiring highly reliable position sensors [1], [2]. The resolver is a sinusoidal position encoder, which outputs two amplitude-modulated signals. The two signals respectively contain sinusoidal envelope and cosinusoidal envelope of the rotor angle position. In order to obtain the information of the rotor angle position, a resolver-to-digital conversion (RDC) is necessary.

The most convenient solution to RDC is the special integrated circuit (IC), such as AD2S80A, AD2S1210, AU6802, PGA411. Most of RDC ICs are PLL-based closed-loop tracking systems and can offer simple and reliable interfaces between resolvers and computers. However, they are lack of competitiveness in expansibility and cost [3]. Hardware-based strategy offers an alternative solution to resolver conversion. The schemes purposed in [4]–[6] were implemented using analogue circuitry, which could obtain accurate angle information without using digital links. However, such converters increase the volume and weight of system, and electronic components need to have sufficiently high standards to ensure consistency between the two channels.

Software-based RDCs can avoid the problems in RDC ICs and hardware-based converters. Their working principles are to carry out envelope detection on the resolver signals firstly, and then calculate the rotor angle position from the envelopes with software algorithms. With the continuous optimization

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of algorithms and the continuous updating of processors, software-based RDCs have more obvious advantages in performance, cost and volume, etc.

In software-based RDCs, envelope detection is always carried out before the demodulation of the angular position and velocity in order to remove the carrier from resolver outputs [7], [8]. The methods proposed in [9]–[12] performed envelope detection in microprocessor after resolver signals were sampled. Real-time envelope detection was adopted in [9], which got envelopes from digital resolver signals by high-gain amplifiers and low-pass filters. Another approach proposed in [10] and [11] was carried out digital filtering with a 16th-order finite impulse response (FIR) band-pass filter (BPF), reducing the band width of modulated signals, and then improving resolution ratio of sampling by the over sampling technique. Aung and Bi put forward an envelope detection algorithm based on numerical integration in [12], which could not only effectively restrain noise effects in the envelopes, but also have its accuracy uninfluenced by phase shift between sensor input and outputs.

Actually, digital envelope detection techniques have been used in a wide variety of other signal processing applications, such as automatic gain control, amplitude modulation (AM) radio demodulation, ultrasound signal analysis, and modulated optical signal detection [13]. Lyons [13] collected and assessed all kinds of common envelope detection methods in, which is of great guiding significance. However, digital envelope detection requires sampling to satisfy the Nyquist theory, which increases the burden of analog-to-digital converter (ADC), especially if resolver requires high frequency excitation. Although performing envelope detection before sampling can reduce the burden of the ADC, if the performance of two envelope conditioning channels are not completely consistent, non-orthogonal errors will be introduced, including DC offsets, amplitude deviation, and phase shift [14], [15], which need to be calibrated [16], [17].

In order to avoid the above problems, synchronous envelope detection method was put forward in [18]– [20], which obtained good effects. The method firstly produced carrier in the microprocessor, which was used as the excitation signal of resolver, then controlled the microprocessor to output synchronization pulse at the peak of the carrier to trigger the Sample/Hold (S/H) circuits, and finally got digital envelopes after sampling on the resolver signals. Compared with the other methods, synchronous envelope detection not only effectively avoids delays and non-orthogonal errors, but also greatly reduces the burden of ADC because the sampling frequency is lower than the Nyquist rate.

To ensure that the sampling pulse is synchronized with the resolver outputs, the method presented in [18] and [19] was designing a digital generator inside the microprocessor to produce a sinusoidal carrier for resolver excitation. Although this method can determine the carrier phase in real time and realize accurate sampling, outputting a 1-kHz carrier requires 16-kHz running algorithm [19], which undoubtedly adds the burden of the microprocessor. As the carrier frequency is difficult to increase, this method is limited to low-speed applications below 1000r/min [20]. Khaburi [20] proposed an improved approach based on square wave excitation to enable synchronous envelope detection for high-speed applications. The square wave was generated by the EPWM module of microprocessor, increasing the excitation frequency to 5-kHz. However, harmonics and noise are more easily introduced into square waves, which reduce system accuracy.

It can be seen that the conventional software-based synchronous envelope detection methods increase the workload of the microprocessor due to the large consumption of resources, especially in high speed applications where high frequency excitation is required. In order to reduce the burden of microprocessor, resolver should be supplied with external sinusoidal generator. As it is difficult for the microprocessor to realize accurate synchronization between sampling and external excitation, the synchronization pulse used to control sampling (S/H circuits) can be directly generated by comparing the external excitation signal with a reference, which is generally determined simply by the phase shift of resolver. However, due to the unexpected factors in analog circuits, such as noises, offsets, and drifts, the conventional comparators for sampling pulse generation often cause instant deviations and thus affect the accuracy of envelope detection. Currently, there are no relevant reports about how to suppress the effects of unexpected factors to realize high-accuracy synchronous envelope detection when the resolver is powered by an external excitation generator.

This paper proposes a hardware-based strategy of synchronous envelope detection and designs an implementation circuit to solve the above problem. Based on the error propagation theory, the proposed strategy optimizes the synchronization pulse generation circuit, which minimizes the error propagation of the unexpected factors in the circuit to envelope detection. First, the reference voltage for comparison is optimized to minimize the effects of unexpected factors on pulse instants. Second, the sampling phase of the resolver signals is optimized to further minimize the effects of pulse instant deviations on the accuracy of envelope detection. Theoretical analysis and experimental results indicate that the envelopes detected by the proposed strategy not only have no delay and non-orthogonal error, but also have the minimum noise. Compared with the conventional synchronous envelope detection methods, operation without microprocessor and associated digital elements means that the proposed strategy reduces the computational pressure of actual systems and can be applied to resolvers with any excitation frequency.

II. RESOLVER PRINCIPLES AND SYNCHRONOUS ENVELOPE DETECTION

In a resolver, the primary winding resides on the rotor, inputting high-frequency carrier, and two secondary windings which are in orthogonal position locate on the stator, outputting amplitude-modulated signals containing the information of rotor angle position, as shown in Fig.1.

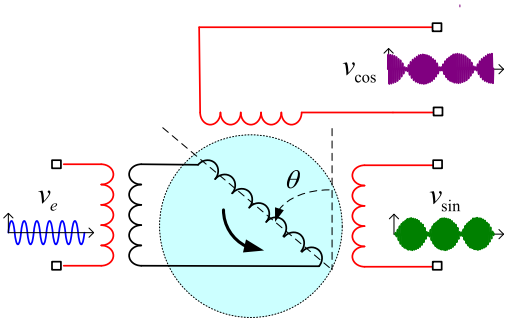

FIGURE 1. Schematics of electrical structure for a resolver.

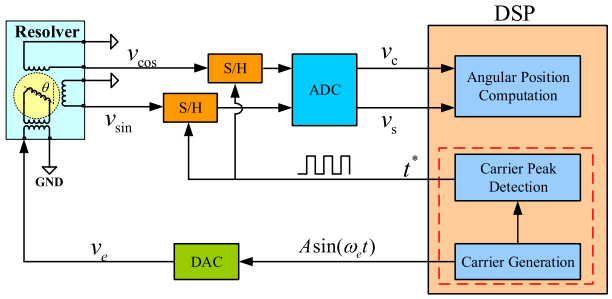

FIGURE 2. Software-based synchronous envelope detection method.

Ideally, the high-frequency carrier input into the resolver as an excitation signal can be described as:

$$v_e = A\sin(\omega_e t) \tag{1}$$

where A and ω_e are the amplitude and angular frequency of the carrier, respectively.

With excitation, the resolver outputs two amplitude-modulated signals $v_{\sin}$ and $v_{\cos}$, which can be expressed as:

$$\begin{cases} v_{\sin} = \alpha A\sin(\omega_e t + \phi)\sin\theta \\ v_{\cos} = \alpha A\sin(\omega_e t + \phi)\cos\theta \end{cases} \tag{2}$$

where α is the transformation ratio, ϕ is the phase shift between input and outputs caused by internal windings of the resolver, and θ represents the rotor angle position that needs to be measured.

The principle of synchronous envelope detection is to directly sample $v_{\sin}$ and $v_{\cos}$ with the frequency of ω_e to separate the sinusoidal and cosinusoidal envelopes of θ. The method can be expressed with the following equations:

$$\begin{cases} v_s = \alpha A\sin(\omega_e t^* + \phi)\sin\theta \\ v_c = \alpha A\sin(\omega_e t^* + \phi)\cos\theta \end{cases} \tag{3}$$

where t^* is the ideal sampling instant, v_s and v_c are the digital sinusoidal and cosinusoidal envelopes detected from $v_{\sin}$ and $v_{\cos}$, respectively. In order to maximize the amplitudes of v_s and v_c, t^* needs to satisfy $\omega_e t^* + \phi = \pi/2 + 2k\pi$, $k \in Z$. That is, the sampling point needs to be set at the peak of the carrier of resolver signals. Since this method directly samples the resolver signals without adding analog conditioning, the obtained envelopes have no delay, nor does it produce non-orthogonal errors due to inconsistent circuit characteristics, such as DC offsets, amplitude deviation, and phase shift.

The key to achieve synchronous envelope detection of resolver signals is how to determine the sampling instant t^* quickly and accurately. At present, a common method is to design a digital sinusoidal generator inside the microprocessor to generate the carrier v_e, and then convert v_e into an analog signal by DAC for resolver excitation. In this way, the microprocessor can directly determine the accurate sampling instant t^* by performing peak detection on v_e. The main working principle of the method is shown in Fig.2 [18].

As shown in the content circled by the red dotted line in Fig.2, this software-based synchronous envelope detection method requires the microprocessor to calculate the carrier v_e and the sampling instant t^*. Although this method is not affected by noise and error of hardware, the frequency of v_e is restricted due to the limited computing power of microprocessor. The calculation frequency needs to reach at least 15-kHz if a carrier with the frequency of 1-kHz is required. As the excitation frequency of resolver is usually within the range of 1 to 10-kHz [21], the conventional method may be lack of practicality in actual systems when the excitation frequency is very high. Therefore, the software carrier generator inside the microprocessor should be avoided as the excitation source of resolver.

However, if the resolver is powered by an external excitation generator, the microprocessor is difficult to synchronize with the externally generated carrier accurately. Therefore, the synchronization pulse used to control sampling can no longer be obtained by digital approach. Designing an equivalent hardware-based synchronization circuit is a feasible solution, and the conventional implement is a simple comparator that generates the synchronization pulse by comparing the excitation signal with a constant reference, as shown in Fig.3. However, the presence of unexpected factors (such as noises, offsets and drifts) in hardware circuit will produce ambiguity in synchronization pulse generation, thereby introducing deviations from the expected envelopes. Starting from this problem, a hardware-based synchronous envelope detection strategy is proposed in this paper. The proposed strategy minimizes the effects of unexpected factors by taking effective optimization measures and realizes high-precision envelope detection for resolver, which has more practicality and a wider application range than the conventional method.

III. SYNCHRONOUS ENVELOPE DETECTION UNDER EXTERNAL EXCITATION

As discussed in Section II, if the resolver is powered by an external excitation generator, an analog circuit should be designed to control the synchronous sampling on the resolver signals. In general, the excitation signal can be compared with a constant reference voltage to obtain a synchronization pulse, and then put the pulse to trigger the S/H circuits. However, the reference voltage inevitably has an error due

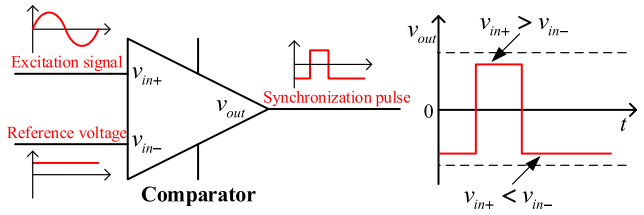

FIGURE 3. Conventional method of synchronization pulse generation.

to the influences of conditioning accuracy and circuit noise, which will be transmitted to the synchronization pulse and cause a deviation at the sampling instant. In this case, how to set the reference voltage and select the sampling phase of the resolver signals so as to minimize the influence of the error is the primary task for improving the envelope detection accuracy. Therefore, this section will design the reference voltage and sampling phase for error suppression.

A. DESIGN OF REFERENCE VOLTAGE FOR PULSE GENERATION

As the microprocessor can not get the accurate frequency and phase of carrier, the synchronization pulse used to control sampling can only be extracted from the excitation signal by analog circuit when the resolver is powered by an external excitation generator. From Eq.(1) and (2), it can be seen that the simplest method is to input the excitation signal and a constant reference voltage into a comparator at the same time, as shown in Fig.3.

From Eq.(1), the relationship between the synchronization pulse instant (rising edge) and the reference voltage can be expressed as:

$$t = \frac{1}{\omega_e}\arcsin(\frac{v_{ref}}{A}) + \frac{2k\pi}{\omega_e} \tag{4}$$

where $k \in Z$. It can be seen that the comparator can directly output a synchronization pulse whose rising edge coincides with the carrier peak of the resolver signals if the value of the reference voltage is $A\sin(\pi/2 - \phi)$.

However, in practical systems, the reference voltage is not ideal but with error due to the influence of actual factors such as circuit noise and component accuracy. Therefore, the reference voltage for the comparator needs to be designed to suppress the propagation of the error.

The reference voltage with error can be expressed as:

$$v_{ref} = v^*_{ref} + \Delta v_{ref} \tag{5}$$

where v^*_{ref} and v_{ref} are the set value and measured value of the reference voltage respectively, Δv_{ref} is the systematic error of the reference voltage and there is $|\Delta v_{ref}| \le \varepsilon$. For a typical analog circuit, the value of ε is about 10∼30mV.

By combining Eq.(4) and (5), it can be known that, as the pulse instant is determined by v_{ref}, Δv_{ref} will be propagated to the obtained pulse and cause pulse instant error. The influences of Δv_{ref} on the output of the comparator under different reference voltages are shown in Fig.4. It can be seen that the

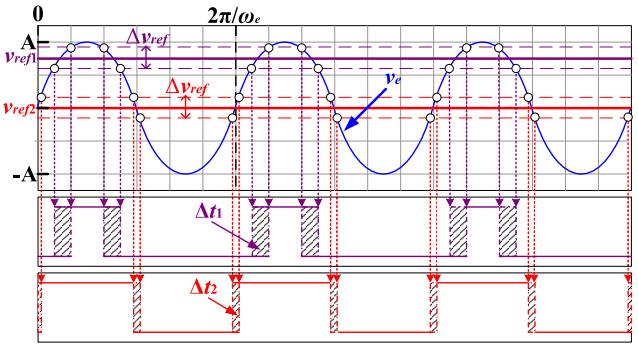

FIGURE 4. Relation of pulse error and reference voltage.

pulse instant errors are respectively Δt_1 and Δt_2 when the reference voltages are respectively given as v_{ref1} and v_{ref2}. As $\Delta t_1 > \Delta t_2$, the magnitude of the pulse instant error is related to the set value of the reference voltage.

Following the principles of the error propagation theory, the pulse instant error can be obtained from Eq.(4) as:

$$\Delta t \approx \frac{dt}{dv_{ref}}\Delta v_{ref} = \frac{1}{\omega_e\sqrt{A^2 - v^2_{ref}}}\Delta v_{ref} \tag{6}$$

It can be seen from Eq.(6) that the error propagation coefficient $1/(\omega_e\sqrt{A^2 - v^2_{ref}})$ is the minimum when $v_{ref} = 0$. In order to minimize the effect of the reference voltage error Δv_{ref} on the synchronization pulse, the set value of the reference voltage should be designed as $v^*_{ref} = 0$.

Substitute $v^*_{ref} = 0$ and Eq.(5) into (4), then the pulse instant error can be expressed as:

$$|\Delta t| = \frac{1}{\omega_e}\left|\arcsin(\frac{v_{ref}}{A})\right| \le \frac{1}{\omega_e}\arcsin(\frac{\varepsilon}{A}) \tag{7}$$

From the above derivation, it can be concluded that the error of the synchronization pulse caused by Δv_{ref} is the minimum when the set value of the reference voltage $v^*_{ref} = 0$. Even so, this error will still be propagated to the digital envelopes after synchronous sampling.

B. DESIGN OF SAMPLING PHASE FOR ENVELOPE DETECTION

In Fig.5, after the resolver signals $v_{\sin}$ and $v_{\cos}$ pass through the S/H circuits and ADC, the digital signals of sinusoidal and cosinusoidal envelopes can be obtained. From Eq.(3), it is known that there are no noises (errors) of v_s and v_c because the sampling instant t^* is a constant under ideal conditions. However, in an actual system, since the sampling instant has the error Δt, envelope noises will be caused during sampling. Therefore, Eq.(3) can be rewritten to express the actual envelopes as:

$$\begin{cases} v_s = \alpha A\sin[\omega_e(t^* + \Delta t) + \phi]\sin\theta \\ v_c = \alpha A\sin[\omega_e(t^* + \Delta t) + \phi]\cos\theta \end{cases} \tag{8}$$

In the existing synchronous envelope detection methods, the carrier peaks of the resolver signals are usually selected

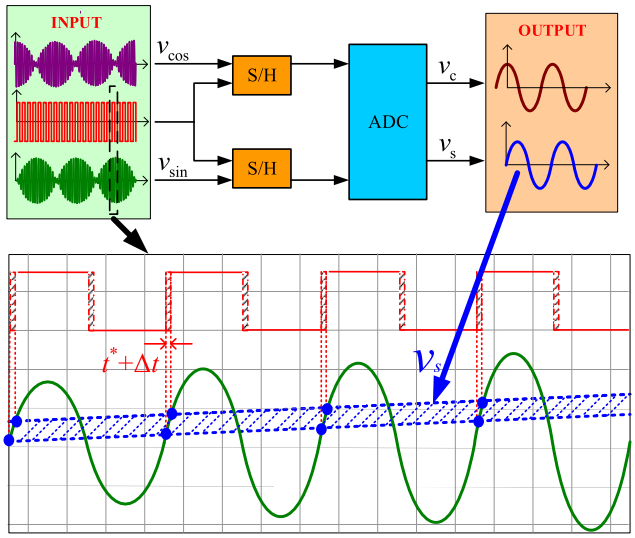

FIGURE 5. Envelope noise caused by pulse error.

as the sampling points to obtain the sinusoidal and cosinusoidal envelopes with the largest amplitude. However, in the proposed method, in addition to factors such as the amplitude, the noises of envelopes caused by Δt should be analyzed in order to select the sampling phase that can achieve the highest Signal-to-Noise Ratio (SNR).

Take the sinusoidal envelope v_s as an example. According to Eq.(3) and (8), the envelope noise caused by Δt can be expressed as:

$$|\Delta v_s| = |\alpha A \sin\theta||\sin[\omega_e(t^* + \Delta t) + \phi] - \sin(\omega_e t^* + \phi)| \tag{9}$$

where Δv_s is the noise (error) of v_s. Assume that the rotor angle position θ is a constant during each sampling period. According to the error propagation theory, we can approximate the envelope noise Δv_s by the following linear formula:

$$\Delta v_s \approx \frac{dv_s}{dt^*}\Delta t = \alpha A\omega_e \sin\theta\cos(\omega_e t^* + \phi)\Delta t \tag{10}$$

From Eq.(10), it is obvious that Δv_s will be approximately equal to 0 if the sampling phase $\omega_e t^* + \phi = \pi/2 + k\pi, k \in Z$. Hence, it can be concluded that designing the sampling phase at the peaks of the carrier $\alpha A\sin(\omega_e t + \phi)$ will minimize the envelope error Δv_s. For the cosinusoidal envelope v_c, the derivation and conclusion are similar.

Substitute $\omega_e t^* + \phi = \pi/2 + k\pi$ and Eq.(7) into (9), Δv_s can be calculated as:

$$|\Delta v_s| = \alpha A|\sin\theta|(1-\cos\omega_e\Delta t) \le \alpha|\sin\theta|(A - \sqrt{A^2 - \varepsilon^2}) \tag{11}$$

This implies that the noise of the obtained envelope caused by the error of sampling instant is the minimum when the sampling phase is designed at the carrier peak of resolver signal. Because the amplitude of the obtained envelope is the largest at the same time, this design achieves the highest SNR.

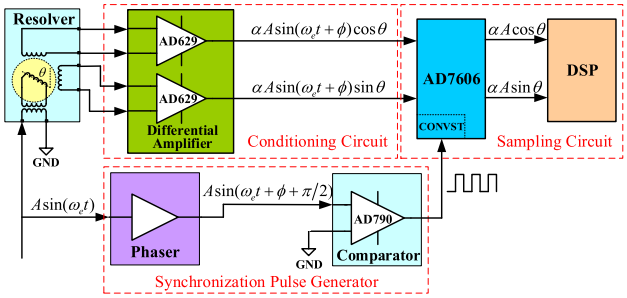

FIGURE 6. Schematic structure of the proposed circuit.

C. DESIGN OF THE PROPOSED STRATEGY

Theoretical analysis shows that the errors propagation to the resulting envelopes can be effectively suppressed by two steps: the first step is to obtain the synchronization pulse with the minimum error; the second step is to select the best sampling phase.

Hence, a hardware-based strategy of synchronous envelope detection for resolver can be designed as follows:

Step 1: Transform the output signals of resolver to single-ended signals by differential amplifiers with high common mode rejection ratio (CMRR), and then feed them into the S/H circuits.

Step 2: Carry out phase shift on the excitation signal of resolver to obtain a synchronization signal that the zero-crossing point coincides with the carrier peak of the resolver signals. Then compare the synchronization signal with zero to obtain the synchronization pulse with the minimum error.

Step 3: Use the synchronization pulse to trigger the S/H circuits and then sample the resolver signals by ADC.

It can be seen that the proposed strategy not only suppresses the envelope errors to the minimum, but also avoids any delay and non-orthogonal error to the envelopes because the resolver signals are not filtered and amplified.

Compared with the conventional software-based methods, the synchronous sampling for resolver signals can be completely implemented by hardware circuit, which reduces the burden of the microprocessor and applies to any resolver with a high excitation frequency.

IV. HARDWARE DESIGN

In order to realize the proposed strategy, a low-cost and high-accuracy circuit is designed in this section. According to the implementation steps of the proposed strategy, the circuit is divided into three parts for design, as shown in Fig.6.

A. DESIGN OF CONDITIONING CIRCUIT FOR RESOLVER SIGNALS

The first part is the conditioning circuit for resolver signals. This part only consists of two differential amplifiers and several decoupling capacitors, with function of converting the two pairs of differential signals the resolver outputs into single-ended signals for ADC sampling. The differential amplifier is AD629 produced by ADI Company, whose

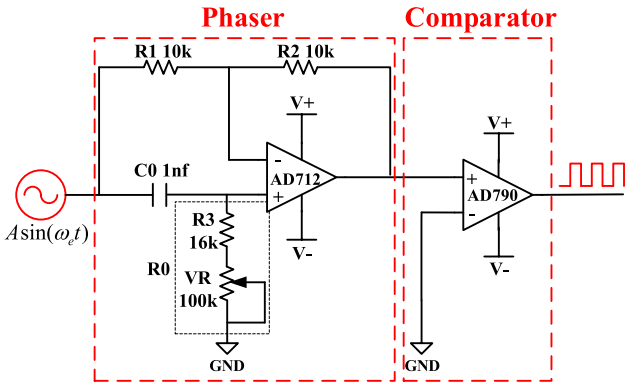

FIGURE 7. Schematic diagram of synchronization pulse generator.

typical value of the offset voltage is only 0.2mV. With the excellent CMRR over a wide frequency range, AD629 can effectively restrain the common-mode noise in the resolver signals. According to Eq.(2), as there is a phase shift between input and outputs due to resistance of the resolver windings, the actual resolver signals output from this part can be expressed as $\alpha A \sin(\omega_e t + \phi) \sin\theta$ and $\alpha A \sin(\omega_e t + \phi) \cos\theta$.

B. DESIGN OF SYNCHRONIZATION PULSE GENERATOR

The second part is the circuit for synchronization pulse generation. This circuit includes a phaser and a zero-crossing comparator, and is used to extract the synchronization pulse from the excitation signal utilized to trigger the S/H circuits. The schematic diagram of this part is shown in Fig. 7. Wherein, the phaser consists of an operational amplifier AD712, a precision rheostat and several high-accuracy constant resistances and capacitances. The frequency characteristic of the phaser can be written as:

$$G(j\omega_e) = \frac{-R_2 + R_1 R_0 C_0 \omega_e j}{R_1 + R_1 R_0 C_0 \omega_e j} \tag{12}$$

From Eq.(12), the amplitude-frequency and phase-frequency characteristics can be obtained as:

$$|G(j\omega_e)| = \sqrt{\frac{R_2^2 + R_1^2 R_0^2 C_0^2 \omega_e^2}{R_1^2 + R_1^2 R_0^2 C_0^2 \omega_e^2}} \tag{13}$$

$$\angle G(j\omega_e) = \pi - \arctan\frac{R_1 R_0 C_0 \omega_e}{R_2} - \arctan\frac{R_1 R_0 C_0 \omega_e}{R_1} \tag{14}$$

In order to achieve $|G(j\omega_e)| = 1$, R_1 and R_2 should be set to the same value. So Eq.(14) can be simplified to:

$$\angle G(j\omega_e) = \pi - 2\arctan R_0 C_0 \omega_e \tag{15}$$

It can be seen from Eq.(15) that, for a fixed ω_e, the phase interval that the excitation signal can be shifted is $(0, \pi)$ by adjusting $R_0 C_0$. In order to shift the zero-crossing point of the excitation signal to coincide with the carrier peak of resolver signals, we should let $\angle G(j\omega_e) = \phi + \pi/2$ to obtain the synchronization signal $\alpha A \sin(\omega_e t + \phi + \pi/2)$. Therefore, the values of R_0 and C_0 can be calculated by Eq.(15).

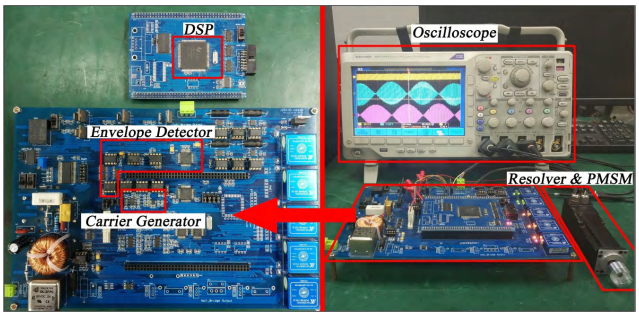

FIGURE 8. Experimental platform.

However, the value of $R_0 C_0$ can not always be constant since the excitation frequency ω_e and phase shift ϕ may be changed by different resolvers. For ease of adjustment, C_0 is set to a constant capacitance, and R_0 is divided into a constant resistance R_3 and a rheostat VR, as shown in Fig.7. By adjusting VR, the phaser can be applied to most resolvers with an excitation frequency ranging from 2-kHz to 10-kHz and a phase shift angle less than 20°.

The comparator is AD790 from ADI Company, with a maximum propagation delay of 45ns and an input offset voltage of 0.25mV. The two inputs of the comparator are the output signal of the phaser and ground respectively, and the output is the synchronization pulse used to trigger the S/H circuits.

C. DESIGN OF SAMPLING CIRCUIT

The third part is sampling circuit. This part completes the sampling on the resolver signals by ADC, and sends the digital envelopes to DSP for demodulation. 16-bit ADC AD7606 from ADI Company is selected, the chip supports the input of bipolar analog signal with the maximum range of ±10V. Therefore, it is unnecessary for most resolver signals to use operational amplifier to conduct amplitude conditioning before sampling, which reduces the source of non-orthogonal errors. In addition, with S/H circuits inside the chip, multiple signals can be sampled synchronously by external pulse. The microprocessor used in the system is DSP-TMS320F28335 from TI Company.

It can be seen that the designed synchronous envelope detection circuit only contains two differential amplifiers, one operational amplifier, one comparator, one ADC chip and several resistors and capacitors, with a simple structure and low cost. The specific performance of this circuit will be introduced in Section V.

V. EXPERIMENTAL RESULTS

A real resolver connected with a permanent magnet synchronous motor (PMSM) is used in the experimental platform to verify the designed circuit, as shown in Fig.8. Main parameters of the resolver and the PMSM are listed in Table 1.

In the experiment, the PMSM is controlled by a drive and control board to operate at fixed angle and constant speed, respectively. Excitation signal with a frequency of 10-kHz

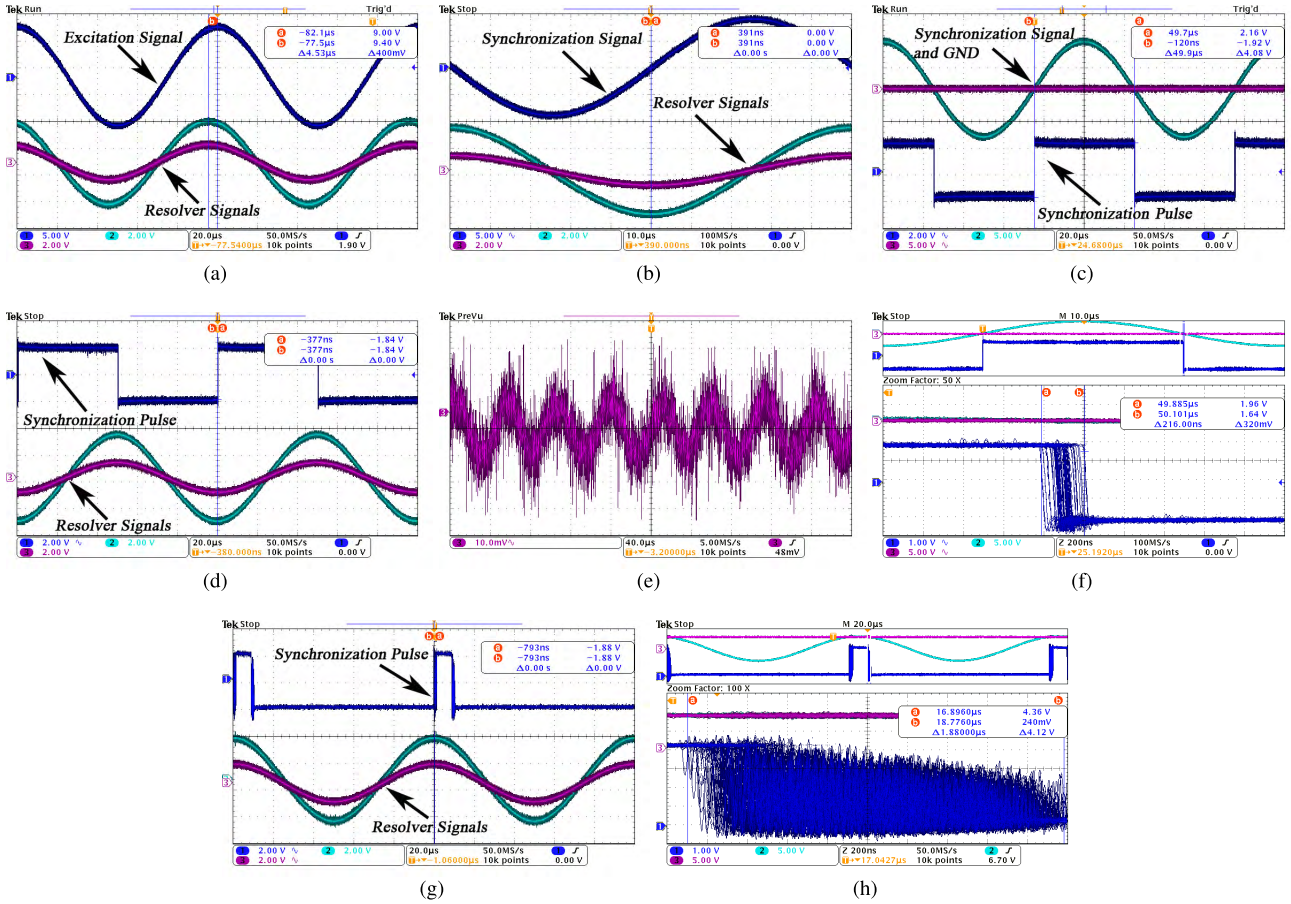

FIGURE 9. Waveforms measured at a fixed angle (a) excitation signal and resolver signals; (b) synchronization signal output by the phaser and resolver signals; (c) inputs and output of the comparator;(d) synchronization pulse and resolver signals; (e) noise at GND pin of the comparator; (f) error of synchronization pulse; (g) synchronization pulse and resolver signals (direct comparison circuit); (h) error of synchronization pulse (direct comparison circuit).

TABLE 1. Main parameters of the resolver and the PMSM.

PMSM		Resolver	
Pole pairs	2	Pole pairs	1
Rated voltage	110V(AC)	Input voltage	5-10V(AC)
Rated speed	3000 r/min	Input frequency	10 kHz
Torque constant	0.15 Nm/A	Input impedance	95±14 Ω
Phase resistance	8 Ω	Phase shift	<18°
Phase inductance	10 mH	Electrical error	≤10’

and amplitude of 9V is generated by a DDS chip AD9833, followed by filtering and amplification. Resolver signals are connected to the designed circuit for envelope detection. A Tektronix DPO3014 oscilloscope is used for measurement.

A. EXPERIMENT AT FIXED ANGLE

Waveforms of the excitation signal and the single-ended resolver signals are shown in Fig.9(a). It can be seen that the carrier of the resolver signals exceeds about 45μs than the excitation signal because of the influence of the resolver windings. Thus, the phaser needs to produce a phase-shifted angle of $\phi+\pi/2 \approx -4.53/100\times 2\pi+\pi/2$. By adjusting the rheostat VR, the phaser outputs the required synchronization signal, whose zero-crossing point coincides with the carrier peak of the resolver signals, as shown in Fig.9(b).

The synchronization signal is converted into pulse through the zero-crossing comparator. The inputs and output of the comparator are shown in Fig.9(c). The phase relationship between the synchronization pulse and the resolver signals is shown in Fig.9(d). It can be seen that the rising edge of the synchronization pulse is coincided with the carrier peak of the resolver signals. Therefore, the synchronous sampling on the resolver signals at the carrier peak can be realized by using this pulse to trigger the S/H circuits.

Next, actually measure the systematic error. Fig.9(e) shows the noise waveform at the ground (GND) pin of the comparator. Since the ground is used as the comparator reference, in this experimental system, $|\Delta v_{ref}| \leq \varepsilon \approx 30$mV. From theoretical analysis, it is known that this noise will cause an error of the synchronization pulse. Substituting $\varepsilon \approx 30$mV into Eq.(7), the theoretical range of the pulse instant error can be obtained as:

$$|\Delta t| \leq \frac{\arcsin(\varepsilon/A)}{2\pi f} \approx \frac{\arcsin(3\times 10^{-2}/9)}{2\times 3.14\times 10^{4}} \approx 53\text{ns} \qquad (16)$$

The actual error range of the synchronization pulse is measured by the oscilloscope on rising edge trigger mode, and the result is shown in Fig.9(f). It can be observed that the sum of the errors of the pulse rising edge and falling edge is about 216ns, and then the measured range of Δt can be obtained as:

$$|\Delta\hat{t}| \leq \frac{216\text{ns}}{4} = 54\text{ns} \tag{17}$$

Comparing the calculation results of Eq.(16) and (17), it can be seen that the theoretical derivation is consistent with the actual situation.

In order to prove that using this synchronization pulse to sample the resolver signals at the carrier peaks can get the envelopes with the minimum noise, we can adjust the rheostat *VR* of the phaser to set the sampling phase at the peak and any other phase respectively, and then compare the two sets of sampling results.

The envelopes shown in Fig.10(a) and Fig.10(b) are respectively obtained by sampling at the carrier peaks and non-peak points when the resolver is fixed. It can be seen that under the same conditions of the resolver signals and synchronization pulse, selecting the carrier peak as the sampling point can obtain envelopes with larger amplitude and less noise, which means the improvement of the accuracy of envelope detection. According to Eq.(8), the accuracy of the two pairs of envelopes can be compared by calculating and analyzing the factor item $m = \sin[\omega_e(t^* + \Delta t) + \phi]$. Since the sampling points set in this experiment are all with in the negative period of the carrier, the expression of m can be derived from Eq.(8) as:

$$m = -\frac{\sqrt{v_s^2 + v_c^2}}{\alpha A} \tag{18}$$

Substituting the sampling results shown in Fig.10(a) and Fig.10(b) into Eq.(18), curves m_1 and m_2 used to measure the noise characteristics of envelopes can be obtained respectively, as shown in Fig.11.

The major parameters of m_1 and m_2 are shown in Table 2. Although the average value of m_1 is greater than m_2, the peak-to-peak value and the standard deviation of m_1 are only about one-fifth and one-sixth of m_2, respectively. It can be illustrated that the envelopes obtained by sampling the resolver signals at the carrier peaks not only have the maximum amplitude, but also have the minimum noise.

B. EXPERIMENT AT CONSTANT SPEED

As mentioned in Section III, another way to get the synchronous pulse that coincides with the carrier peak is to directly compare the excitation signal to a constant voltage of $A\sin(\pi/2 - \phi)$ without phaser, which is simpler than the proposed circuit. However, this direct comparison circuit ignores the circuit error and noise. In order to support the theoretical analysis in Section III, the effects of the direct comparison circuit and the proposed circuit on the accuracy of envelope detection are compared in this experiment.

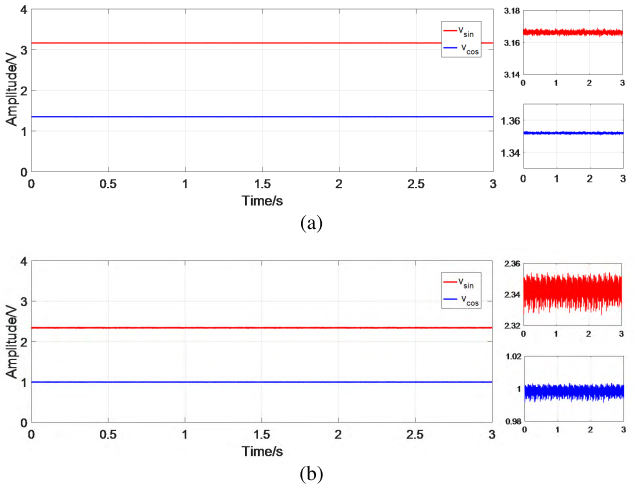

FIGURE 10. The waveforms of envelopes at a fixed angle (a) sampling at peaks; (b) sampling at off-peak points.

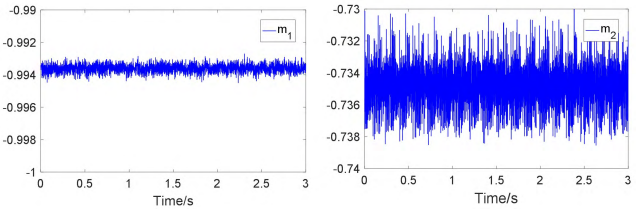

FIGURE 11. The waveforms of m_1 and m_2.

TABLE 2. Comparison of major parameters of m_1 and m_2.

Parameters	m_1	m_2
Maximum	-0.99271	-0.72998
Minimum	-0.99449	-0.73853
P-P value	1.78131e-3	8.55191e-3
Average value	-0.99361	-0.73483
Standard deviation	2.55363e-4	1.44254e-3

Fig.9(g) and Fig.9(h) show the measured waveforms of the direct comparison circuit. Compared with Fig.9(d) and Fig.9(f), although the rising edge of the pulse is also coincided with the carrier peak of the resolver signals in Fig.9(g), the pulse instant error is significantly magnified in Fig.9(h).

In the experiment, the PMSM is controlled to rotate at 2π rad/s by the drive and control board. Using the proposed circuit and the direct comparison circuit to perform envelope detection of resolver signals at the same time, and then the sinusoidal and cosinusoidal envelopes $v_{\sin 1}$, $v_{\cos 1}$ and $v_{\sin 2}$, $v_{\cos 2}$ are obtained, respectively, as shown in Fig.12(a) and Fig.12(b). It can be seen that although the two pairs of envelopes have approximate amplitudes, the noises and distortions of $v_{\sin 1}$, $v_{\cos 1}$ are significantly samller than $v_{\sin 2}$, $v_{\cos 2}$.

The four curves $v_{\sin 1}$, $v_{\cos 1}$, $v_{\sin 2}$ and $v_{\cos 2}$ are processed by using the Fast Fourier Transform (FFT). The resulting amplitude-frequency curves are shown in Fig.13. It is obvious

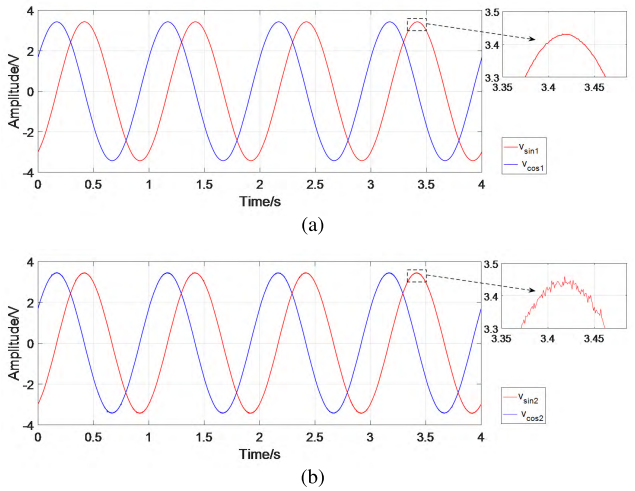

FIGURE 12. The waveforms of envelopes at constant speed (a) obtained by the proposed circuit; (b) obtained by the direct comparison circuit.

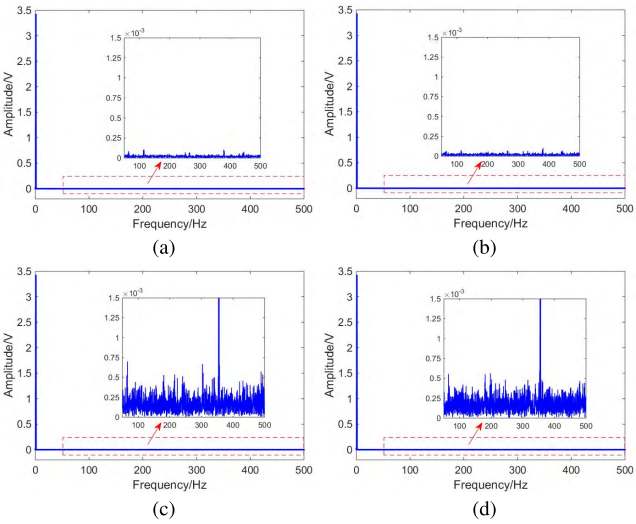

FIGURE 13. Amplitude-frequency curves of the two pairs of envelopes (a) $v_{\sin 1}$; (b) $v_{\cos 1}$; (c) $v_{\sin 2}$; (d) $v_{\cos 2}$.

that the amplitudes of the harmonic components in $v_{\sin 1}$ and $v_{\cos 1}$ are much less than that in $v_{\sin 2}$ and $v_{\cos 2}$. Major parameters of the two pairs of envelopes are calculated according to the mathematical outcomes of FFT, as shown in Table 3.

The results in Table 3 show that the fundamental and DC components of the two pairs of envelopes are approximate, but the Total Harmonic Distortions (THDs) of $v_{\sin 1}$ and $v_{\cos 1}$ are only about one-fifth of $v_{\sin 2}$ and $v_{\cos 2}$, which indicates that designing reference voltage $v^*_{ref} = 0$ can effectively suppress the effect of Δv_{ref} to improve the envelope detection accuracy. Thus, the conclusion of the theoretical analysis is supported.

To compare the effects of the two envelope detection circuits on the demodulation accuracy, the two pairs of envelopes in Fig.12 are demodulated respectively by the demodulation algorithm in [8]. The error between the demodulation result and the actual angular position can be expressed

TABLE 3. Major parameters of the two pairs of envelopes.

Parameter	$v_{\sin 1}$	$v_{\cos 1}$	$v_{\sin 2}$	$v_{\cos 2}$
Total harmonic distortion	5.79602e-4	5.51976e-4	2.66519e-3	2.64507e-3
Fundamental amplitude/V	3.43103	3.43093	3.43081	3.43118
Fundamental phase/°	-150.18535	-60.21522	-150.18414	-60.21398
DC component/V	1.30174e-3	1.21859e-3	1.32710e-3	1.22605e-3
Amplitude difference/V	1.04644e-4		-3.74370e-4	
Phase difference/°	89.97013		89.97016	

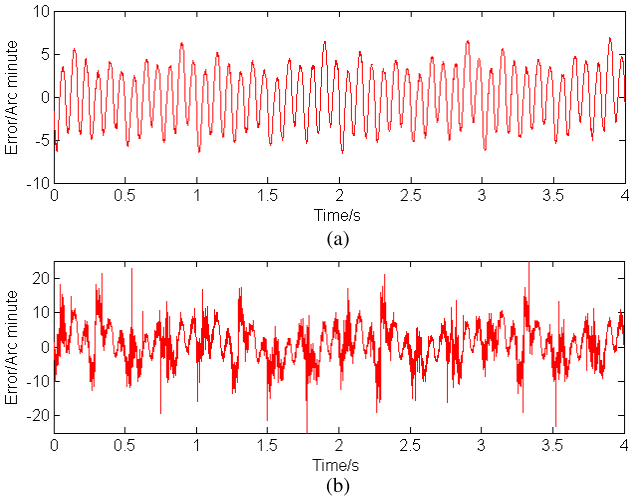

FIGURE 14. Demodulation errors of the envelopes in Fig.12 (a) obtained by the proposed circuit; (b) obtained by the direct comparison circuit.

by $\Delta\theta$. As the actual angular position can not be known in this experiment, the demodulation error $\Delta\theta$ can not be directly obtained. Therefore, the approximate method for $\Delta\theta$ in [17] is used to evaluate the demodulation accuracy and the results are shown in Fig.14. It can be seen that the error in Fig.14(a) fluctuates within ±6' electrical angle, which is only about one quarter of Fig.14(b).

The experimental results indicate that the proposed strategy realizes envelope detection of 10-kHz resolver signals and meets the requirement of high-precision RDC. Compared with the conventional synchronous envelope detection methods in [18]– [20], the proposed strategy can be applied to resolvers with higher excitation frequency because it does not occupy any microprocessor resources.

VI. CONCLUSION

In this paper, a hardware-based strategy of synchronous envelope detection for resolver is proposed to obtain the sinusoidal and cosinusoidal envelopes of rotor angle position from resolver signals. The proposed strategy only requires simple analog circuits to be implemented. First, the zero-crossing comparator is designed to get the synchronization pulses, which can minimize the effects of unexpected factors in hardware on the sampling instants. Second, the phaser is designed to adjust the sampling phase to the carrier peak, which can further minimize the effects of the sampling instant deviations. Finally, the envelopes with the highest SNR can

be detected by the sampling circuit since the minimum propagation of unexpected factors in hardware. Unlike conventional methods, the proposed strategy does not occupy any resources of the microprocessor, and improves the practicability and application range while realizing high-precision. The effectiveness of the proposed envelope detection strategy is verified by the experimental results.

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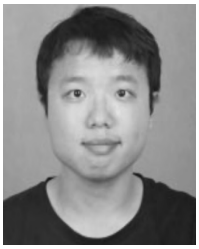

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