IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received January 4, 2019, accepted January 27, 2019, date of publication February 7, 2019, date of current version March 1, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2898154

A Biomedical Sensor System With Stochastic A/D Conversion and Error Correction by Machine Learning

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This work was supported in part by the Adaptable and Seamless Technology Transfer Program through Target-driven R&D (A-STEP) of the Japan Science and Technology Agency (JST), and in part by the Funding Program for Strategic Support Industry through the Ministry of Economy, Trade and Industry.

ABSTRACT This paper presents a high-precision biomedical sensor system with a novel analog-front-end (AFE) IC and error correction by machine learning. The AFE IC embeds an analog-to-digital converter (ADC) architecture called successive stochastic approximation ADC. The proposed ADC integrates a stochastic flash ADC (SF-ADC) into a successive approximation register ADC (SAR-ADC) to enhance its resolution. The SF-ADC is also used as a digitally controlled variable threshold comparator to provide error correction of the SAR-ADC. The proposed system also calibrates the ADC error using the machine learning algorithm on an external PC without additional power dissipation at a sensor node. Due to the flexibility of the system, the design complexity of an AFE IC can be relaxed by using these techniques. The target resolution is 18 bits, and the target bandwidth (without digital low-pass filter) is about 5 kHz to deal with several types of biopotential signals. The design is fabricated in a 130-nm CMOS process and operates at 1.2-V supply. The fabricated ADC achieves the SNDR of 88 dB at a sampling frequency of 250 kHz by using the proposed calibration techniques. Due to the high-resolution ADC, the input-referred noise is 2.52 μV_{rms} with a gain of 28.5 dB.

INDEX TERMS Biomedical sensor, ECG, error correction, machine learning, SAR-ADC, stochastic A/D conversion.

I. INTRODUCTION

Recently, spendings on health is becoming a big problem in many countries. Leading causes of these spendings are cardiovascular diseases [1]. In order to reduce these costs, it is important to detect diseases in early stage by continuous monitoring of biopotential signals such as electrocardiograms (ECGs). Therefore, the demands for low-cost wearable biomedical sensors are rapidly expanding. These kinds of sensors are driven by batteries and required to operate for a long time. In addition, a high resolution is also required because the level of a biopotentinal signal is up to few mV.

A typical block diagram for an wearable ECG monitoring system is shown in Fig. 1. It consists of an analog-front-end (AFE) IC, micro processing unit (MPU), and wireless transceiver. A low-power and high-resolution AFE is required for this application. However, it is not easy to realize such an AFE because resolution and power dissipation are in trade-off. This trade-off leads to increasing design complexity and cost. Especially, power consumption must be kept as low as possible because it directly affects the battery lifetime and size [2].

In addition, different applications have different bandwidth, resolution, number of channels and power requirements. In order to monitor various biopotential signals, a flexible and reconfigurable AFE design platform is required. Although the previous study [3] can realize low-cost reconfigurable systems, the design complexity is usually increased by controlling analog circuits. On the other hand, a high-resolution ADC with digital-centric circuits is

The associate editor coordinating the review of this manuscript and approving it for publication was Nan Liu.

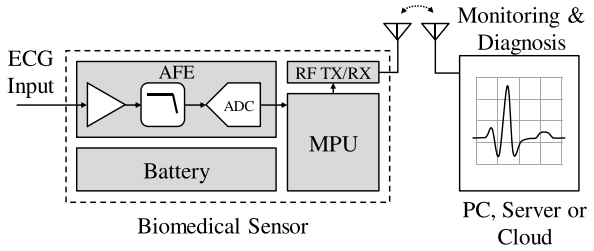

FIGURE 1. Typical configuration of an wearable ECG monitoring system.

preferable to a reconfigurable system than an AFE with a high-gain amplifier and low-resolution ADC architecture.

The successive-approximation-register ADC (SAR-ADC) is a good selection for low-voltage and low-power biomedical sensor interface circuits [4]–[6]. Since the frequency range of biomedical signals is the DC to a few kHz [7], the SAR-ADC can realize low power operations in exchange for low speed operations. However, the resolution of the SAR-ADC is limited by the insufficient accuracy of the internal digital-to-analog converter (DAC). Δ-Σ ADCs [8], [9] are often used for high resolution applications. However, they are not easy to use in fast and multi-channel applications [10], [11]. Therefore, in order to achieve a high-resolution SAR-ADC, a digital error correction technique is important.

To break through the above issues, the novel ADC called successive-stochastic-approximation ADC (SSA-ADC) has been proposed [11], [12]. This architecture is based on the basic SAR-ADC and utilizes a stochastic flash ADC (SF-ADC) [13] to detect a small signal under noise level. A similar architecture called stochastic approximation register (StAR) ADC was also proposed [14]. However, the StAR ADC enhances its resolution by increasing the input range of the SF-ADC with a SAR architecture and noise sources. Therefore, it is not suitable for low voltage operation with smaller input range. On the other hand, the SSA-ADC uses SF-ADC to enhance its resolution under noise level. It also uses the SF-ADC as a digitally controlled variable threshold comparator (DCVTC) to cancel the DAC error of a SAR-ADC. The SSA-ADC is one of the good digital-centric selections for a flexible architecture, because trade-offs between power and resolution can be adjusted by the number of comparators. In this paper, the system-level implementation of the biomedical sensor system (especially ECG sensor) using the SSA-ADC is described, which is based on previous AFE IC implementation [12]. In addition, off-chip calibration based on machine learning algorithm is also described briefly based on the previous work [11].

This paper is organized as follows. In Section II, the system architecture is presented. In Section III, the detail of the proposed AFE and its implementation are described. The DAC error correction technique by the DCVTC is introduced in Section IV. The error correction by machine learning algorithm is presented in Section V. The experimental results are introduced in Section VI. Conclusions are given in Section VII.

II. SYSTEM ARCHITECTURE

The system architecture of the proposed biomedical sensor system is shown in Fig. 2. For prototyping, a wireless link is not included in this system. The proposed system consists of an AFE IC and digital processing on an external PC. In this paper, the proposed AFE IC is implemented in 130-nm CMOS process. It consists of a low noise amplifier (LNA), a low pass filter (LPF), the proposed SSA-ADC, and other peripheral circuits such as a clock generator (Xtal Oscillator, XO), bias circuit and SPI interface (SPI I/F). The LNA reduces flicker noise by chopper modulation. The frequency of the chopping clock can be chosen from 31.25 kHz and 62.5 kHz. The gain is also selectable as 16.0 dB or 28.5 dB. The gain is lower than other AFEs [1] by using a high-resolution ADC. This leads to the lower supply voltage of 1.0 V for the LNA.

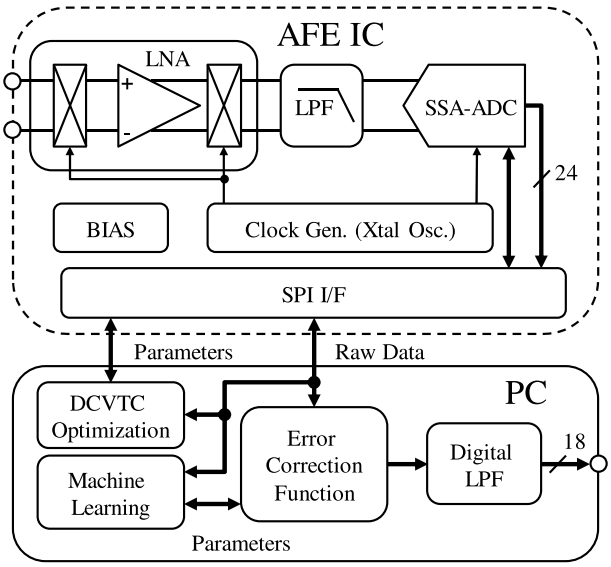

FIGURE 2. Architecture of the proposed biomedical sensor system.

The proposed SSA-ADC determines upper bits by SAR-ADC operations (SAR-ADC mode). The lower bits are determined by SF-ADC operations (SF-ADC mode). Due to the resolution enhancement by the SF-ADC, the comparators (described later in Sec. III) can operate with 0.5 V supply. In order to cancel the DAC error, a DCVTC realized by the SF-ADC is used in the SAR-ADC mode. The sampling frequency can be chosen from 62.5 kHz, 125 kHz and 250 kHz. For high-resolution applications, the sampling frequency of 250 kHz can be used to reduce noise by over-sampling. For low-power applications, sampling frequency of 62.5 kHz can be used to reduce dynamic power dissipations. The raw ADC results are 24-bit combined data of SAR-ADC and SF-ADC modes. In this study, in order to

transmit the 24-bit and 250 kHz outputs, the AFE IC and the external PC are connected with a wired (SPI) interface, which is simplified from the typical case shown in Fig. 1

In the proposed system, an error correction and post filtering are carried out on the external PC in order to enhance the resolution without any additional power dissipation on the sensor side. The error correction is based on machine learning algorithm, and parameters are obtained by foreground tests. 18-bit output is obtained from the 24-bit output by applying an error correction function. In addition, the DCVTC optimization is also carried out on the PC through controlling the AFE IC. These parameters are fed back to the AFE IC through the SPI interface.

III. AFE IC AND IMPLEMENTATION

A. STOCHASTIC FLASH ADC

The SF-ADC is a novel ADC architecture which utilizes a stochastic resonance [13], [15]. Stochastic resonance is a phenomenon that a weak periodic signal is emphasized by optimum level of noise [16]. A single comparator can only detect periodic and optimum level signal, but aperiodic signal can also be detected by configuring a summing network of comparators [17].

The block diagram of the SF-ADC is shown in Fig. 3. The SF-ADC consists of an array of N comparators, which are connected in parallel, and a ones adder. The ones adder outputs a summation of comparator outputs. The ones adder output is a binary code which corresponds to the number of comparators outputting 'high' [13], [18]. The SF-ADC uses random input-referred offset voltages $V_{os,i}(i = 1, 2, \cdots, N)$ and noise $V_{n,i}$ of each comparator as thresholds. Note that the input-referred offsets can be treated as DC noises. According to the central limiting theorem, it can be assumed that the $V_{os,i}$ and $V_{n,i}$ follow a Gaussian distribution when the number of comparators N is large enough [18]. The standard deviation of the offset and noise σ_{tot} can be estimated as follows [11]:

$$\sigma_{tot} = \sqrt{\sigma_{off}^2 + \sigma_n^2}, \tag{1}$$

where σ_{off} and σ_n are the standard deviations of $V_{off,i}$ and $V_{n,i}$, respectively. Therefore, the probability that the output of a comparator is high $P(V_{in})$ follows a cumulative distribution function of the Gaussian distribution, and can be written as follows [15]:

$$P(V_{in}) = \frac{1}{2} + \frac{1}{2}\mathrm{erf}\left(\frac{V_{in}}{\sqrt{2}\,\sigma_{tot}}\right) \approx \frac{n_H}{N}, \tag{2}$$

where $\mathrm{erf}(x) = (2/\sqrt{\pi})\int_0^x \exp(-u^2)du$ is the error function, V_{in} is an input voltage. Here, it is assumed that the means of $V_{os,i}$ and $V_{n,i}$ are zero. In addition, n_H is the number of comparators which output high. Note that the n_H is the ones adder output of the SF-ADC. Figure 4 shows the I/O characteristic of an SF-ADC. The output code n_H monotonically increases depending on the input level.

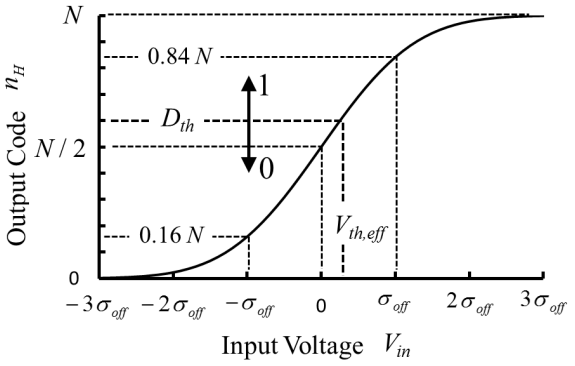

FIGURE 4. I/O characteristics of the SF-ADC and the principle of the DCVTC.

According to the I/O characteristic of an SF-ADC, a DCVTC can be realized by using a digital comparator as shown in Fig. 5. The digital comparator compares the SF-ADC output n_H with a digital threshold D_{th} and quantizes it to one-bit code. This can also be described in Fig. 4. According to Eq. (2), the effective threshold voltage $V_{th,eff}(D_{th})$ can be expressed by using the inverse error function erf^{-1} as follows [19]:

$$V_{th,eff}(D_{th}) \approx \sqrt{2}\sigma_{tot}\,\mathrm{erf}^{-1}\left\{2\left(\frac{D_{th}}{N} - \frac{1}{2}\right)\right\}. \tag{3}$$

In the present study, the DCVTC carries out the DAC error correction. In the previous study, the error correction for an internal DAC of a multi-bit Δ-Σ ADC was also proposed [19].

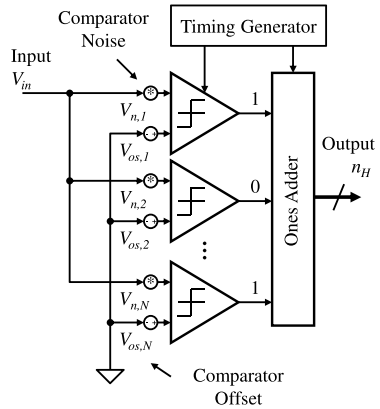

FIGURE 3. Stochastic flash ADC (SF-ADC).

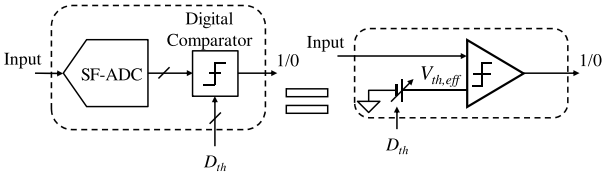

FIGURE 5. DCVTC with an SF-ADC and digital comparator in the SAR-ADC mode.

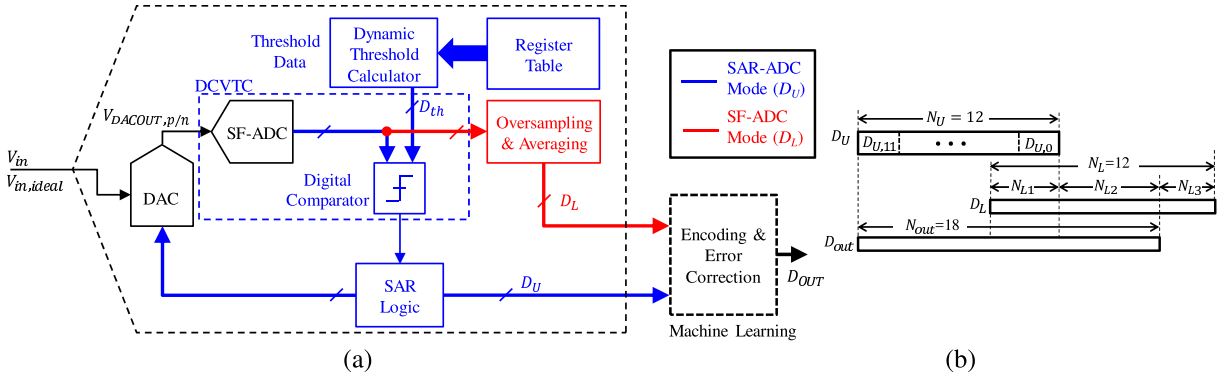

FIGURE 6. (a) Block diagram and (b) bit configuration of the proposed SSA-ADC.

B. SSA-ADC

The detailed block diagram of the SSA-ADC is shown in Fig. 6. The SSA-ADC consists of an SF-ADC, digital comparator, dynamic threshold calculator and register table as well as conventional SAR-ADC building blocks (a capacitor DAC and SAR logic). In the SAR-ADC mode, a DCVTC is used, which consists of the SF-ADC and the digital comparator. The dynamic threshold calculator dynamically generates a digital threshold D_{th} in order to cancel the DAC error. The D_{th} is generated from the data stored in the register table. In the SF-ADC mode, the error remaining after the SAR-ADC mode is quantized. The shared noises generated by a DAC and a buffer (described later and shown in Fig. 7.) cannot be reduced enough by taking an ensemble mean [20]. Therefore, the SF-ADC output is sampled by N_s times and averaged in order to enhance resolution. Finally, The averaged SF-ADC output becomes the lower bit output D_L.

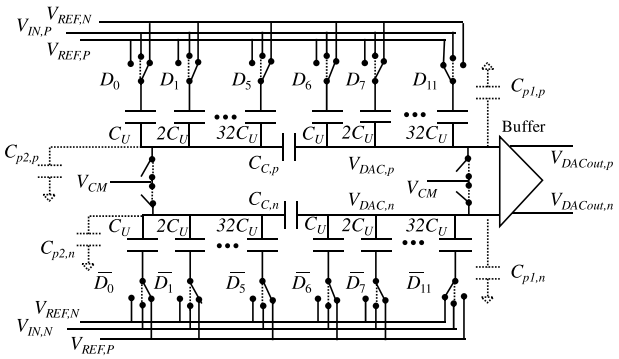

FIGURE 7. Capacitor DAC in the SSA-ADC ($N_U = 12$).

Outputs from the SAR-ADC mode (MSB side) and SF-ADC mode (LSB side) have N_U bits and N_L bits, and are denoted as D_U and D_L, respectively. The total output D_{out} is generated by an off-chip error correction function. The parameters for this error correction are obtained by supervised machine learning described later.

The number of conversion steps for one sampling point is at least $N_U + N_s + 1$. In this design, one sampling period is divided into 32 steps. 13 and 4 steps are used for the SAR-ADC and SF-ADC modes, respectively. Sampling phase uses time duration corresponding to 15 steps. The total number of comparators is determined by the offset and noise distribution and desired resolution. In the present study, the total number of comparators $N = 511$, and oversampling ratio $N_s = 8$ (using both clock edge for the above 4 steps), to achieve the target resolution of 18 bits under limited speed and area occupation. This is smaller than the previous studies of the SF-ADC [13]. As a result, $N_L = \log_2((N+1)N_s) = 12$. In addition, $N_U = 12$, $N_{L2} = 6$, and $N_{out} = 18$. Upper $N_{L1} = 4$-bits are overlapped with D_U in order to cancel the error of the SAR-ADC mode. The N_{L1} is determined by the upper bit LSB ($D_{U,0}$ in Fig. 6(b)) and the estimated σ_{tot}. In the previous study, non-linearity of the SF-ADC is canceled by re-quantization [21]. In this study, $N_{L3} = 2$ bits are assigned in D_L as a fractional part for this purpose. For high resolution, simple summation of the D_U and D_L is not so sufficient. As detailed in Sec. V, encoding and error correction are important.

C. CAPACITOR DAC

The capacitor DAC used in the SSA-ADC is shown in Fig. 7. It consists of MIM capacitor array and MOS switches. Due to a number of comparator array, the SF-ADC has a large input capacitance. In order to drive this capacitance, a buffer is implemented in the capacitor DAC. This buffer consists of a class AB amplifier to satisfy settling requirement under low power consumption. The supply voltage of the buffer is 1.0 V and output swing is ≈0.25 V. The sample and hold function is embedded in the capacitor DAC. In the sampling period, the switches connect the capacitors to input terminals ($V_{IN,P}$, $V_{IN,N}$). In the conversion period, the capacitors are connected to $V_{REF,P}$ ($D_i = 1$) or $V_{REF,N}$ ($D_i = 0$), according to the DAC input D_i ($i = 0, \cdots, 11$). Note that the $V_{REF,P}$, $V_{REF,N}$ and V_{CM} are generated by a band gap reference, regulators, and a resistive divider. They are buffered to drive the capacitor DAC. In this design, split capacitors $C_{C,p(n)}$ is used in order to reduce the area occupation. These split capacitors have unit capacitance of C_U, and cause some errors [22].

The mismatch of C_U causes non-linearity error, therefore the capacitor size must be large enough in conventional designs. In this design, the capacitor mismatch is assumed to be 0.3 %. In the proposed AFE, the unit capacitors C_U can be minimized unless the kT/C noise does not limit the target resolution of 18 bit. In this design, the $C_U = 1.2$ pF to reduce kT/C noise to 7.34 μV. Considering the oversampling ratio of 25 (maximum sampling frequency of 250 kHz and bandwidth of 5 kHz), the kT/C noise is reduced to less than 18-bit LSB = 1.47 μV. Note that the switch size is determined to satisfy the settling requirement.

D. COMPARATOR

A comparator is the key building block of the SF-ADC. In this design, a dynamic latched comparator is used in order to reduce the power dissipation. The dynamic comparator is attractive for low power applications, because of no static power consumption [23]. The schematic diagram of the comparator is shown in Fig. 8.

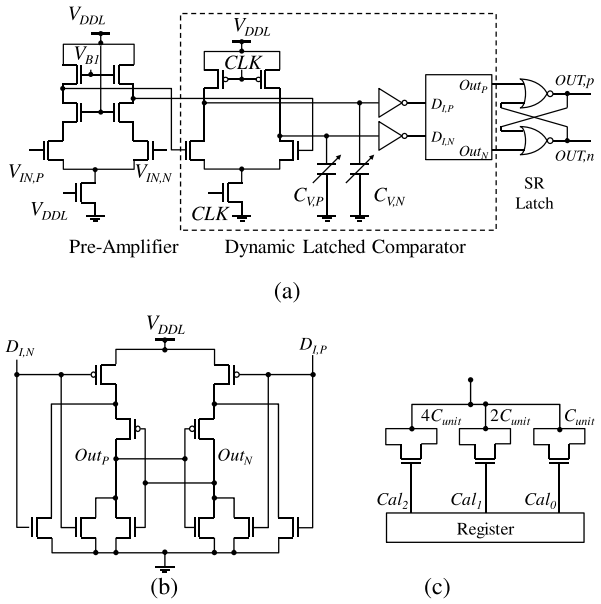

FIGURE 8. (a) Dynamic latched comparator used in the SF-ADC, (b) dynamic latch in the last stage of the comparator, and (c) MOS capacitors for offset calibration $C_{V,P(N)}$.

In the SF-ADC, a number of comparators are connected in parallel, therefore kick-back noise and clock feedthrough become a serious problem. The kick-back noise is caused by the coupling of the voltage swing of the regenerative node, and clock feedthrough is caused by feeding through the clock signal to the input terminal. In the present study, a static pre-amplifier with small gain is used as a buffer in order to reduce kick-back noise and clock feedthrough. The NMOS load resistance in the pre-amplifier is useful for this purpose. The supply voltage of the comparator $V_{DDL} \approx 0.5$ V, and bias voltage $V_{B1} \approx 1.0$ V. The NMOS load in the pre-amplifier operates in linear region.

The input range and resolution of the SF-ADC is determined by σ_{tot}. In this design, the offset voltage can be adjusted by digital control of the capacitances: $C_{V,P}$ and $C_{V,N}$ [24]. According to Monte Carlo simulations, the σ_{off} is estimated to be 3 mV after the offset calibration by $C_{V,P(N)}$. The σ_{off} of 3 mV can ensure 12-bit resolution of the SAR-ADC mode output ($\approx$ 120 μV) by using the DCVTC. The estimated comparator input-referred noise $\sigma_n = 875$ μV. This is usually too large for 18-bit resolution, but the SF-ADC realizes a detection of signals under the noise in the proposed system. The power consumption of each comparator is estimated at $\approx$ 1.4 μW under a sampling frequency of 250 kHz and a 0.5 V supply.

E. CHOPPER-STABILIZED LNA AND LPF

In the proposed AFE, a chopper-stabilized LNA [25] shown in Fig. 9 is used as an input amplifier in order to ensure flicker noise reduction regardless of device characteristics, although some papers do not use this technique [26], [27]. The gain can be selected from 16.0 or 28.5 dB by switching the feedback resistance R_F. Dummy switches are used in the CMOS switches in order to reduce the charge injection. In addition, low-swing ($\approx$ 0.5 V) clock is used as chopping clock in order to reduce clock feedthrough.

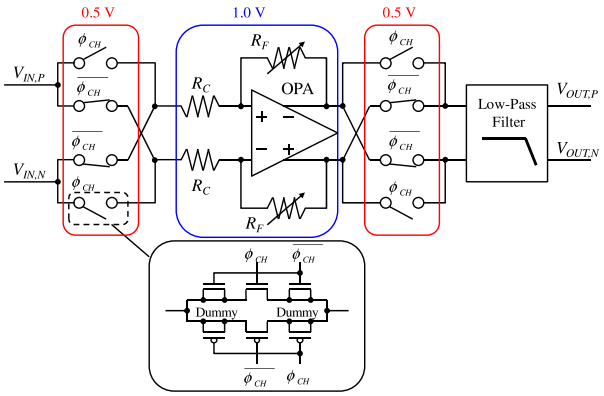

FIGURE 9. Chopper-stabilized LNA with low-swing (0.5 V) chopping clock and LPF in the AFE.

The LNA output is filtered by a passive RC-type LPF. This LPF is used as an anti-aliasing filter and attenuates out-of-band noise including flicker noises modulated by the LNA. The cut-off frequency is $\approx$ 5 kHz in order to address various kinds of biopotential signals. The total resolution at the input of the AFE is $\approx$ 2 μV with a gain of 28.5 dB because of the high-resolution SSA-ADC. The power consumption is estimated to be 200 μW with a supply of 1.0 V.

IV. DAC ERROR CORRECTION BY DCVTC

The positive-side (negative-side) capacitors $C_{i,p(n)}$ are weighted by powers of two. However, these capacitors include errors originated from mismatches expressed as

follows [4], [11]:

$$C_{i,p(n)} = \begin{cases} 2^i C_U \left(1 + \varepsilon_i + s_{p(n)} \dfrac{\Delta\varepsilon_i}{2}\right), & i \leq 5 \\ 2^{i-6} C_U \left(1 + \varepsilon_i + s_{p(n)} \dfrac{\Delta\varepsilon_i}{2}\right), & i > 5, \end{cases} \tag{4}$$

where $s_p = 1$, $s_n = -1$, C_U is a unit capacitance, ε_i is the relative deviation from $(C_{i,p} + C_{i,n})/2$, and $\Delta\varepsilon_i$ is the relative difference between positive-side capacitance $C_{i,p}$ and negative-side capacitance $C_{i,n}$. The split capacitor $C_{C,p(n)}$ is used in order to scale $C_{i,p(n)}$ and reduce the capacitance area. This split capacitor causes some errors because the $C_{C,p(n)}$ has a capacitance of C_U instead of fractional value of C_U [22]. In addition, parasitic capacitances $C_{p1,p(n)}$ and $C_{p2,p(n)}$ such as wiring capacitances lead to the DAC errors. Because of these mismatches, split capacitors, and parasitic capacitances, the actual DAC output V_{DAC} is different from the ideal DAC output $V_{DAC,ideal}$. Considering the non-linearity of capacitances (voltage coefficient of MIM capacitors, the buffer input capacitance, and the parasitic capacitance of MOS switches connected to V_{CM} as shown in Fig. 7), the DAC error $\Delta V_{DAC} = V_{DAC} - V_{DAC,ideal}$ depends on capacitance selection by the digital input $D_{in} = (D_{N_U-1}, \cdots, D_1, D_0)_2$ [11].

According to the DAC error modeling by the previous study [11], the DAC error can be divided into the errors which are independent from capacitance selections, and the errors which depend on capacitance selections. As a result, the DAC error for the digital input D_{in} can be simplified as follows:

$$\Delta V_{DAC}(D_{in}) = E_{off} + \sum_{i=0}^{N_U-1} E_i(D_i), \tag{5}$$

where E_{off} is the error which does not depend on the input code D_i. and $E_i(D_i)(i = 0, \cdots, N_U - 1)$ is the error which only depends on the input code D_i. The DAC error can be canceled when $V_{th,eff}(D_{th}) = \Delta V_{DAC}(D_{in})$. Therefore, the optimal values of the digital threshold $D_{th,opt}$ is the function of the DAC input D_{in}. The number of $D_{th,opt}$ for all cases of D_i $(i = 1, \cdots N_U - 1)$ is 2^{N_U-1}. In this design, $N_U = 12$ and the number of $D_{th,opt}$ is 2,048. It is not practical considering the area occupation for registers storing these $D_{th,opt}$. Therefore, the proposed SSA-ADC dynamically generates the $D_{th,opt}$ according to D_{in}. As shown in Fig. 6, this function is implemented as the dynamic threshold calculator.

In order to generate $D_{th,opt}$ efficiently, the configuration data $D_{th,std}$ and $D_{th,j}(j = 0, \cdots, N_U - 1)$ are used. $D_{th,std}$ is the standard value of digital threshold for all zero input $(D_i = 0\ (i = 0, \cdots, N_U - 1))$. Its effective threshold $V_{th,eff}(D_{th,std})$ equals to the DAC error of all zero input. Thus, $V_{th,eff}(D_{th,std})$ can be expressed as follows:

$$V_{th,eff}(D_{th,std}) = E_{off} + \sum_{i=0}^{N_U-1} E_i(0). \tag{6}$$

The $D_{th,j}$ is the difference of digital thresholds from the $D_{th,std}$ for the input with $D_i = \delta_{ij}$ $(i = 0, \cdots, j, \cdots, N_U - 1)$. Note that the δ_{ij} is the Kronecker's delta and can be expressed as follows:

$$\delta_{ij} = \begin{cases} 1 & (i = j) \\ 0 & (i \neq j). \end{cases} \tag{7}$$

Therefore, the effective threshold $V_{th,eff}(D_{th,std} + D_{th,j})$ can be expressed as follows:

$$V_{th,eff}(D_{th,std} + D_{th,j}) = E_{off} + \sum_{i=0}^{N_U-1} E_i(0) + E_j(1) - E_j(0). \tag{8}$$

In the proposed system, the $D_{th,opt}$ is generated by using $D_{th,std}$ and $D_{th,j}$ as follows. First, D_{th} is set to $D_{th,std}$. Then, when $D_j = 1$, $D_{th,j}$ is added to D_{th}. Otherwise, nothing is done. As a result, the $D_{th,opt}$ for the DAC input D_{in} can be expressed as follows:

$$D_{th,opt}(D_{in}) = D_{th,std} + \sum_{j=0}^{N_U-1} D_j D_{th,j}. \tag{9}$$

From Eqs. (8)-(9), the effective threshold $V_{th,eff}(D_{th,opt}(D_{in}))$ becomes approximately equal to the DAC error $\Delta V_{DAC}(D_{in})$. By using this technique, the proposed DAC error correction for all patterns (2^{N_U-1}) of DAC input codes can be carried out with one standard value $D_{th,std}$ and N_U differences $D_{th,j}$. In this design, $N_U = 12$ and $D_{th,opt}$ can be generated from only 13 data. These data are written in the register table. In the SAR-ADC mode, these configuration data are read from the register table and the $D_{th,opt}$ is calculated by the dynamic threshold calculator.

The configuration data $D_{th,std}$ and $D_{th,j}$ are obtained by sinusoidal test signal inputs so as to maximize the SNDR performance. First $D_{th,std}$ is swept around $(N + 1)/2 = 256$, and the value which provides the maximum SNDR is stored. Next, D_{th,N_U-1} is swept around 0 based on the same criteria. Then, the same operations are carried out down to $D_{th,0}$.

V. ENCODING AND ERROR CORRECTION BY BAYESIAN LINEAR REGRESSION

A. RE-QUANTIZATION FOR 18-BIT OUTPUTS

In the SF-ADC mode, lower-bit output D_L corresponds to the probability of the residual error in the SAR-ADC mode. However, the full scale range of the SF-ADC mode does not correspond to the LSB of the SAR-ADC mode as shown in Fig. 10. This is because the SF-ADC uses the comparator offsets including input-referred noise as reference voltages, and the full scale range is determined by these random references. This means that the full scale range of the SF-ADC is independent from the SAR-ADC reference. Therefore, in order to generate total ADC output D_{out}, D_L must be encoded as the code having the same scale of the D_U. This function can be realized by re-quantization of the output D_L. The parameters for this encoding should be determined after the chip is fabricated. This function is implemented in software level on an external PC, therefore additional power

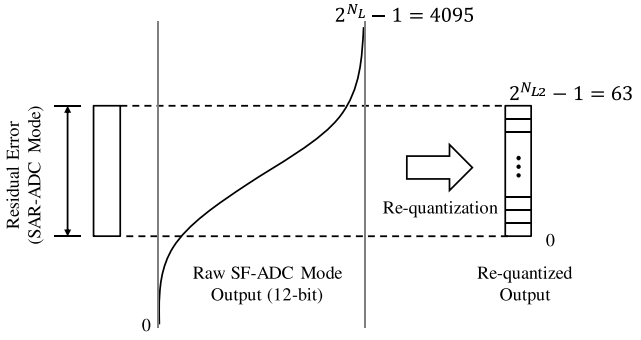

FIGURE 10. Re-quantization of the SF-ADC mode outputs.

and area are not required at sensor nodes. In the previous study, the encoding with re-quantization improved the SNDR characteristics of the SF-ADC [21]. Similarity to the previous study, the encoding in the SSA-ADC can also improve the SNDR performance and resolution. As described in the previous section, lower N_L bits are prepared for this function.

Note that the DAC error can be corrected by the DCVTC in the SAR-ADC mode. The main target of the error correction by the DCVTC is the error caused by capacitance mismatches. In the present study, the encoding with error correction is used for generating 18-bit ADC output D_{out} and minimizing the error which remains even after the DAC error correction described in section IV. In order to carry out this encoding and error correction, parameters are required and must be determined. In the present study, supervised machine learning using Bayesian linear regression [28], [29] was introduced in order to obtain these parameters.

B. DEFINITION OF ERROR MINIMIZATION PROBLEM

In the present study, the test analog voltage $V_{in,ideal}$ is applied to the ADC input and training data set is obtained. The training data set D includes the MSB-side outputs D_U and the LSB-side output D_L from SSA-ADC. D also includes the ideal output codes corresponding to the each test inputs, $D_{out,ideal}$. Therefore, $D^{(k)} = (D^{(k)}_{out,ideal}, D^{(k)}_U, D^{(k)}_L)$, where k is the index of the training data set. The $D^{(k)}$ has the following bit configurations.

$$\begin{aligned} D^{(k)}_U &= (D^{(k)}_{U,N_U-1}, \ldots, D^{(k)}_{U,0}), \\ D^{(k)}_L &= (D^{(k)}_{L,N_L-1}, \ldots, D^{(k)}_{L,0}), \\ D^{(k)}_{out,ideal} &= (D^{(k)}_{out,ideal,N_{out}-1}, \ldots, D^{(k)}_{out,ideal,0}). \end{aligned} \tag{10}$$

Here, an error correction function $h_{\boldsymbol{w}}(D^{(k)}_U, D^{(k)}_L)$ is introduced. This correction function predicts the ideal output code $D^{(k)}_{out,ideal}$ by using the measured upper and lower outputs $D^{(k)}_U$ and $D^{(k)}_L$. In this work, $h_{\boldsymbol{w}}(D^{(k)}_U, D^{(k)}_L)$ is defined as follows [11]:

$$\begin{aligned} h_{\boldsymbol{w}}(D^{(k)}_U, D^{(k)}_L) = &\sum_{i=0}^{N_U-1} 2^{i+N_{L2}} D^{(k)}_{U,i} \\ &+ \sum_{i=0}^{N_U-1} 2^{i+N_{L2}} e_i D^{(k)}_{U,i} \\ &+ \sum_{i=0}^{N_U-1} 2^{i+N_{L2}} D^{(k)}_{U,i} \sum_{j=i+1}^{N_U-1} f_{i,j} D^{(k)}_{U,j} \\ &+ \sum_{i=1}^{2^{N_{L1}+N_{L2}}-1} h_i p^{(k)}_i \\ &+ \sum_{i=0}^{N_{L3}-1} 2^{i-N_{L3}} D^{(k)}_{L,i} (g_i + 1) \\ &+ \delta, \end{aligned} \tag{11}$$

where $D^{(k)}_{U,i}$ is the i-th digit of $D^{(k)}_U$ in binary code, and $p^{(k)}_i$ is the i-th bit of a $(2^{N_L-N_{L3}} - 1)$-bit thermometer code, which corresponds to the $D^{(k)}_L$. The parameters of the $h_{\boldsymbol{w}}(D^{(k)}_U, D^{(k)}_L)$, $\boldsymbol{e}, \boldsymbol{f}, \boldsymbol{h}, \boldsymbol{g}$, and δ:

$$\boldsymbol{e} = (e_0, \ldots, e_{N_U-1})^{\mathsf{T}}, \tag{12}$$

$$\begin{aligned} \boldsymbol{f} = \big(&f_{0,1}, \ldots, f_{0,N_U-1}, f_{1,2}, \ldots, f_{1,N_U-1}, \\ &\ldots, f_{N_U-3,N_U-2}, \ldots, f_{N_U-2,N_U-1}\big)^{\mathsf{T}}, \end{aligned} \tag{13}$$

$$\boldsymbol{h} = (h_1, \ldots, h_{2^{N_{L1}+N_{L2}}-1})^{\mathsf{T}}, \tag{14}$$

$$\boldsymbol{g} = (g_0, \ldots, g_{N_{L3}-1})^{\mathsf{T}}, \tag{15}$$

are determined by machine learning algorithm. The superscript T indicates transpose, and in addition, a vector is defined as follows:

$$\boldsymbol{w} = (\boldsymbol{e}^{\mathsf{T}}, \boldsymbol{f}^{\mathsf{T}}, \boldsymbol{h}^{\mathsf{T}}, \boldsymbol{g}^{\mathsf{T}}, \delta)^{\mathsf{T}}. \tag{16}$$

The second and third terms on the right-hand side of Eq. (11) are corrections for the error of binary weighted value and the error depending on switch selections, respectively. These errors are caused by the capacitor mismatches. The fourth term is for encoding and error correction for the SF-ADC mode output. The fifth term is also the correction for the SF-ADC mode, but for the N_{L3} bits of the fractional part.

By determining the set of parameters $\boldsymbol{w}$, a corrected ADC output $D_{out} = (D_{out,N_{out}-1}, \ldots, D_{out,0})$ can be calculated from D_U and D_L by using $D_{out,D} = h_{\boldsymbol{w}}(D_U, D_L)$. The $D_{out,D}$ is the decimal expression of the corrected output as follows:

$$D_{out,D} = \sum_{i=0}^{N_{out}-1} 2^i D_{out,i}. \tag{17}$$

The error of the corrected output $E_{\boldsymbol{w}}(D^{(k)})$, is defined as the difference from the ideal code as follows:

$$E_{\boldsymbol{w}}(D^{(k)}) = \left| h_{\boldsymbol{w}}(D^{(k)}_U, D^{(k)}_L) - D^{(k)}_{out,ideal,D} \right|, \tag{18}$$

$$D^{(k)}_{out,ideal,D} = \sum_{i=0}^{N_{out}-1} 2^i D^{(k)}_{out,ideal,i}, \tag{19}$$

and the optimal set of $\boldsymbol{w}$ minimizes the $E_{\boldsymbol{w}}(D^{(k)})$. Therefore, the targeted error minimization problem can be expressed as follows:

$$\begin{aligned} \min_{\boldsymbol{w}} \sum_{k \in T} &E_{\boldsymbol{w}}(D^{(k)})^2 + c_{r1}||\boldsymbol{e}||_2^2 + c_{r1}||\boldsymbol{f}||_2^2 \\ &+ c_{r2}||\boldsymbol{g}||_2^2 + c_{r3}||\boldsymbol{h}||_2^2, \end{aligned} \tag{20}$$

where $||\cdot||_2$ is the Euclidean norm, c_{r1}, c_{r2}, and c_{r3} are regularization constants [29], [30]. Their related terms are used in order to prevent e_i, $f_{i,j}$, g_i, and h_i from becoming extremely large values.

In the proposed system, the above minimization problem is solved by machine learning algorithm (Bayesian linear regression), as described in the next subsection.

C. BAYESIAN LINEAR REGRESSION

Now, we define the vector $\boldsymbol{\phi}(D_U, D_L)$ of basis functions as follows:

$$\begin{aligned}\boldsymbol{\phi}(D_U, D_L) = (&2^{N_{L2}} D_{U,0}, \ldots, 2^{N_{out}-1} D_{U,N_U-1},\\ &2^{N_{L2}} D_{U,0} D_{U,1}, \ldots, 2^{N_{L2}} D_{U,0} D_{U,N_U-1},\\ &2^{N_{L2+1}} D_{U,1} D_{U,2}, \ldots, 2^{N_{out}-1} D_{U,N_U-2} D_{U,N_U-1},\\ &p, 2^{N_{L3}-1} D_{L,N_{L3}-1}, \ldots, 2^0 D_{L,0}, 1)^{\mathsf{T}},\end{aligned} \tag{21}$$

where p is a $(2^{N_L - N_{L3}} - 1)$-bit thermometer code. The error correction function $h_{\boldsymbol{w}}$ can be rewritten as,

$$h_{\boldsymbol{w}}(D_U, D_L) = \boldsymbol{w}^{\mathsf{T}} \boldsymbol{\phi}(D_U, D_L). \tag{22}$$

The error minimization problem expressed by Eq. (20) can be solved analytically. However, the training data set includes errors due to the thermal noise, external disturbance and insufficient accuracy of an external test input source. Under this constraint, the linear regression using the Bayes estimation (Bayesian linear regression) is suitable for obtaining the optimal value of $\boldsymbol{w}$ [11], [29]. The Bayes estimation is a method of estimating the posterior distribution under the prior distribution of the parameters of a model from obtained data set [29].

First, we assume that the training data follows a normal distribution $\mathcal{N}\left(D_{out,ideal,D} | \, h\boldsymbol{w}(D_U, D_L), \beta_{out}^{-1}\right)$, where β_{out} is the constant which is related to the variance of the corrected data. In addition, the prior distribution of $\boldsymbol{w}$ follows a normal distribution $\mathcal{N}(\boldsymbol{w} | \, 0, \boldsymbol{\Sigma}_c)$, where

$$\boldsymbol{\Sigma}_c^{-1} = diag\{c_{r1}, \ldots, c_{r1}, c_{r3}, \ldots, c_{r3}, c_{r2}, \ldots, c_{r2}, 0\} \tag{23}$$

Note, it is assumed that δ follows a uniform distribution.

The posterior distribution after obtaining the training data set D_T can be expressed as $p(\boldsymbol{w}|D_T)$. Here, by maximizing $p(\boldsymbol{w}|D_T)$ for $\boldsymbol{w}$, we can obtain [29],

$$p(\boldsymbol{w} | \, D_T) = \mathcal{N}(\boldsymbol{w} | \, \boldsymbol{\mu}_T, \boldsymbol{S}_T), \tag{24}$$

$$\boldsymbol{\mu}_T = \beta_{out} \, \boldsymbol{S}_T \boldsymbol{\Phi}_T^{\mathsf{T}} \boldsymbol{d}_T, \tag{25}$$

$$\boldsymbol{S}_T^{-1} = \boldsymbol{\Sigma}_c^{-1} + \beta_{out} \, \boldsymbol{\Phi}_T^{\mathsf{T}} \boldsymbol{\Phi}_T, \tag{26}$$

where $\boldsymbol{\Phi}_T$ is a matrix of which rows consist of $\boldsymbol{\phi}(D_U^{(k)}, D_L^{(k)})^{\mathsf{T}}, k \in T$. $\boldsymbol{d}_T$ is a column vector of which elements are $D_{out,ideal,D}^{(k)} - D_{U,D}^{(k)}, k \in T$. $\boldsymbol{\mu}_T$ is the optimal value of $\boldsymbol{w}$ obtained by D_T.

Bayesian linear regression is suitable for incremental learning which can realize effective learning with a limited number of training data [11]. An incremental learning with the Bayes estimation was proposed [29]. The parameter set $\boldsymbol{w}_l$ for l-th training, can be renewed by $\boldsymbol{S}_{T_l}$, where T_l is the index set of l-th training data set [11].

VI. EXPERIMENTAL RESULTS

The proposed AFE IC was fabricated in 130-nm CMOS process. The total chip area of the AFE IC is 2×2 mm^2, and it was packaged in a 24-pin QFN. Figure 11 shows the die micrograph and physical layout with the annotated blocks. The chip is the same as the previous study [12], but bias conditions are changed in this paper. In the following measurement results, the performances are evaluated on an evaluation board.

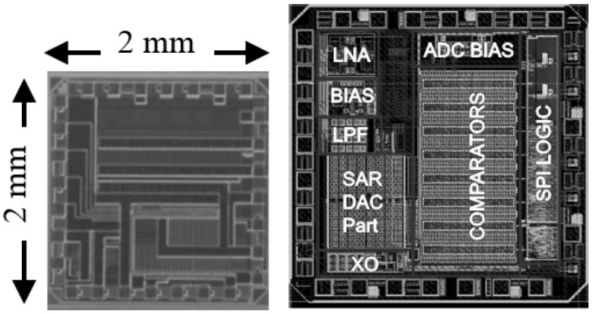

FIGURE 11. (a) Chip micrograph and (b) layout image of the prototype AFE IC.

Power dissipation of each block is shown in Fig. 12. The power consumption is 5.48 mW in total. The supply voltages of the analog circuits (e.g., LNA, comparators) are provided by a regulator from 1.2 V supply. In the following measurement results, the supply of comparators $V_{DDL} = 0.53$ V is provided by the regulator. The chopping clock swing is also 0.53 V. The V_{B1} in Fig. 8 is 1.0 V. The measured reference voltages of the capacitor DAC ($V_{REF,P}$ and $V_{REF,N}$ in Fig. 7) are 0.40 V and 0.14 V, respectively. Note that the power dissipation of the digital blocks in the SSA-ADC (ones adder, SAR logic and so on) is included in the power of logic circuits. The power consumption of the LNA is kept low by using the high-resolution SSA-ADC. In this design, the noise of the capacitor DAC is not dominant, therefore, the power consumption of the LNA and the reference buffers

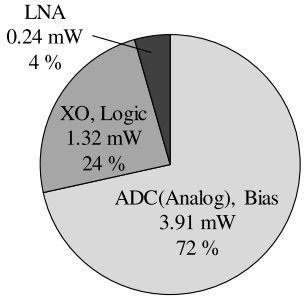

FIGURE 12. Power dissipation of each block (total 5.48 mW).

can be reduced by reducing the unit capacitance C_U. Note that increasing mismatches can be canceled by the proposed error correction techniques. The power of the buffer in Fig. 7 and the 511 comparator array (both are included in the power of the ADC) are 1.83 mW and 1.77 mW, respectively. The power of the buffer is large in order to drive the input capacitances of the comparators. This power consumption can be reduced by using a fine process to reduce these input capacitances.

Figure 13 shows the DNL and INL of 12-bit D_U output before the proposed DCVTC optimization. The DNL and INL are measured by a 2^{19} points histogram test with a 20.5 Hz full scale sinusoidal input. The peak DNL and INL are −0.82/+0.82 LSB and −1.32/+0.82 LSB, respectively. Figure 14 shows the DNL and INL after the DCVTC optimization and both DNL and INL are −0.54/+0.76 LSB and −0.77/+0.94 LSB of 12-bit D_U.

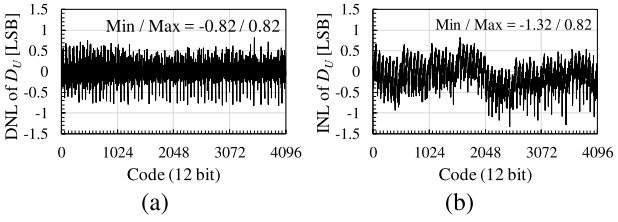

FIGURE 13. (a) DNL errors and (b) INL errors of the upper 12-bit output D_U before the DCVTC configuration is optimized (2^{19} samples).

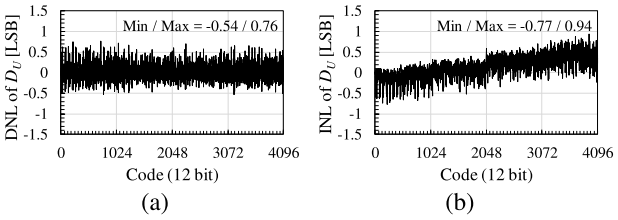

FIGURE 14. (a) DNL errors and (b) INL errors of the upper 12-bit output D_U after the DCVTC configuration is optimized (2^{19} samples).

Figure 15 shows the error of 18-bit output D_{OUT} without and with the machine learning. The errors are difference between actual ADC output codes and ideal (expected) output codes. The output code of the result without machine learning is generated by simply combining the upper and lower bits as shown in Fig. 6(b). The training data set is obtained by a sinusoidal input from a high precision audio analyzer (Audio Precision SYS-2722). As shown in Fig. 15(a), the standard deviation of code errors is 45.0 LSB without machine learning. The standard deviation of code errors with machine learning is reduced to 26.7 LSB as shown in Fig. 15(b). Note that 200 training data sets are used for the initial learning and the number of incremental learning is 5. The number of data at each incremental learning is 100. As a result, the total number of data sets is 700. This is only 0.27% of all 2^{18} patterns of data. The proposed technique can reduce the errors with less than 1 % of all patterns of data. The residual errors are caused by shared noise which is different in each training situation,

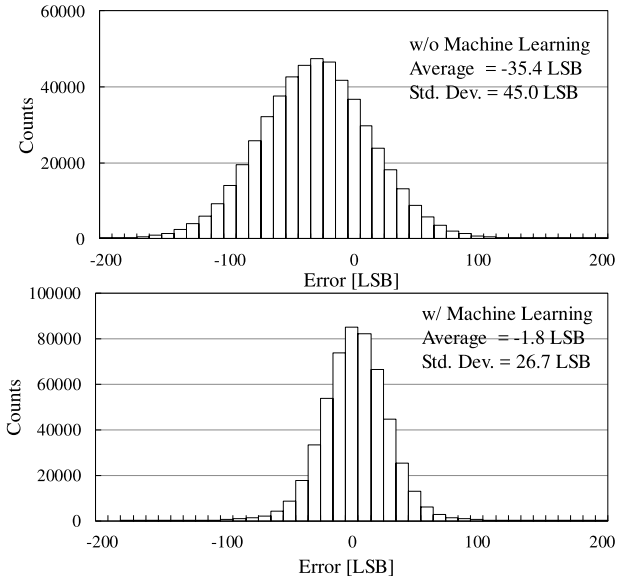

FIGURE 15. 18-bit ADC code error histogram with and without machine learning (without LPF, 2^{19} samples).

therefore cannot be canceled enough. However these noises can be filtered by a digital LPF to some extent.

Figure 16 shows the measured spectrum of the 18-bit ADC output after the DCVTC optimization and the machine learning for a full scale sinusoidal input. The input frequency F_{in} is 20.5 Hz and sampling frequency F_{samp} is 250 kHz and the number of FFT points are 2^{19}. The ADC outputs were filtered by a 6-th order digital LPF with a cut-off frequency of 70 Hz, which was also implemented in software level. The cut-off frequency is typical bandwidth for ECG monitoring systems. As shown in Fig. 16, the total SNDR is 88.2 dB, therefore the effective number of bits (ENOB) is 14.4 bits. Without the digital LPF, ENOB is 10.6 bits. The total harmonic distortion (THD) and SFDR are −93.7 dB and 94.4 dB, respectively. The ENOB is slightly improved comparing with the previous study [12], even though the full-scale range is reduced. This is because the characteristics of the buffer in Fig. 7 is adjusted to reduce noise. The ENOB is limited

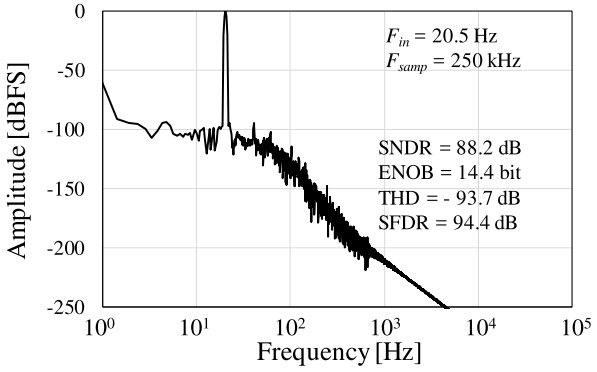

FIGURE 16. 2^{19} points FFT spectrum of corrected and filtered ADC output for full-scale input (bandwidth of digital LPF: 70 Hz).

as a 18-bit ADC, this is because of the shared noise of the buffer shown in Fig. 7

Figure 17 shows the AFE (LNA and SSA-ADC) I/O characteristics for two types of gain settings. Input signal frequency is 20.5 Hz and chopping frequency is 62.5 kHz. The AFE demonstrated a 78.9 dBμV and 91.0 dBμV maximum input for the gain of 28.5 dB and 16.0 dB, respectively. The maximum input is defined as an input level at the 1-dB compression point.

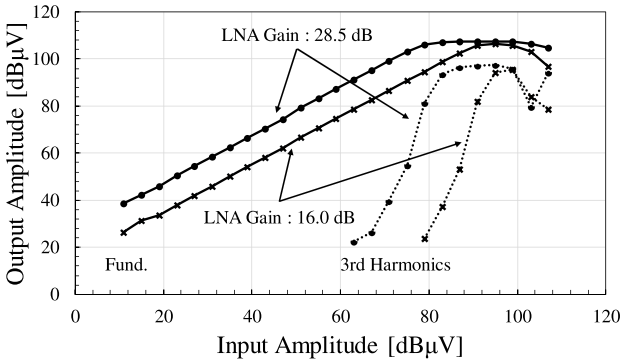

FIGURE 17. I/O characteristics of the AFE with the LNA gain of 28.5 dB and 16.0 dB.

Figure 18 shows the frequency responses of the AFE gain for two gain settings. The input amplitude is 71 dBμV and AFE outputs are not filtered by a digital LPF. The -3 dB cut-off frequencies are both 5.3 kHz. The cut-off frequency is determined by the anti-aliasing LPF in Fig. 9. Due to the relatively high bandwidth, the proposed AFE can be used for several applications, such as ECG, electroencephalogram (EEG) or electromyogram (EMG)). The bandwidth of the system can be configured by a off-chip digital LPF.

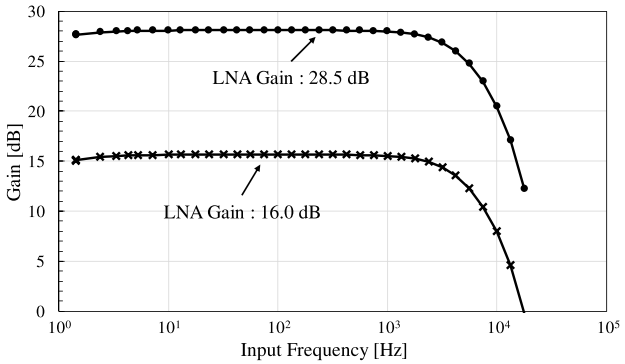

FIGURE 18. Gain frequency response of the AFE.

Figure 19 shows the input-referred noise spectral density of the AFE. The LNA gain is 28.5 dB and chopping frequency is 62.5 kHz. The total noise is 2.52 μV_{rms} in a bandwidth of 1 - 70 Hz. Therefore, the dynamic range is 70.9 dB for the gain of 28.5 dB. Note that the dynamic range is smaller than the previous study [12]. In the previous study, the dynamic range was calculated as the ratio of the maximum input level and the input-referred 18-bit LSB. In this paper, the dynamic

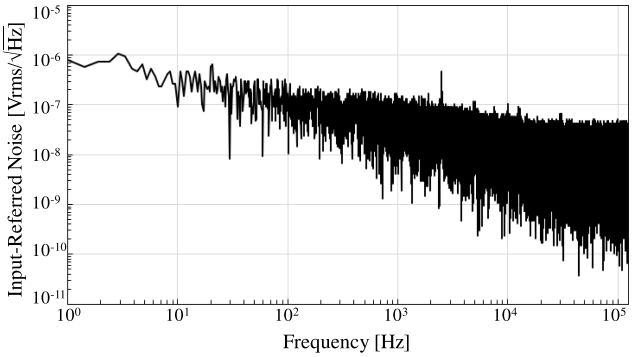

FIGURE 19. Measured input-referred noise spectral density of the AFE (LNA gain: 28.5 dB).

range is calculated as the ratio of the maximum input level and the input-referred noise. The performance summary of the prototype AFE is shown in Table 1.

TABLE 1. Performance summary of the prototype AFE.

Parameters	Values
Technology	130 nm CMOS
Supply	1.2 V
Power (analog)	4.2 mW
Power (digital)	1.3 mW
LNA gain	28.5, 16.0 dB
Chopping clock frequency	31.25 kHz, 62.5 kHz
Input-referred noise	2.52 μV_{rms} (1 - 70 Hz)
Sampling frequency	62.5 kHz, 125 kHz, 250 kHz
ADC ENOB	14.4
ADC THD	-93.7 dB
ADC SFDR	94.4 dB

The ECG monitoring function is demonstrated with the prototype AFE IC. An ECG signal with 60 beats per minute (bpm) is generated by an ECG checker (NIHON KOHDEN AX-301D) and captured by the AFE IC. The measured ECG signal is shown in Fig. 20. Note that the result is 18-bit output and filtered by a 6-th order LPF with cut-off frequency of 70 Hz. Table 2 shows the comparison with state-of-the-art biomedical sensor AFE with high resolution ($>$ 12 bits). The proposed system realizes similar resolution even under lower supply voltage and smaller full-scale range.

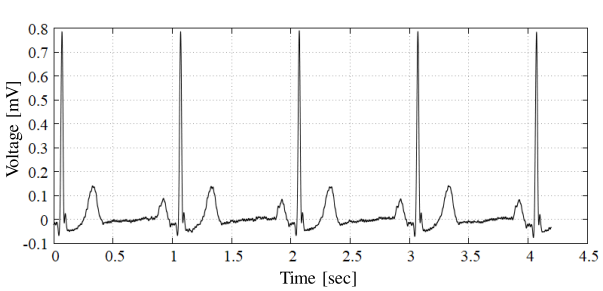

FIGURE 20. ECG waveform measured by the proposed system.

TABLE 2. Performance comparison with high-resolution (> 12 bit), state-of-the-art biomedical sensor AFEs.

	[10]	[31]	This work
Technology [nm]	130	-	130
Supply [V]	3.3	3.3	1.2
Electrode channels	8	5	1
Power/channel [mW]	2.1	11	5.5
Bandwidth [Hz]	100	150	70
Full-scale range [V]	1.6	1.8	0.53
Resolution [bits]	13.5	19	14.4
LNA gain [dB]	-	12.5	28.5
Input-referred noise [μV_{rms}]	0.89	1.13	2.52

VII. CONCLUSION

The paper proposed a biomedical sensor system with a novel SSA-ADC which integrates an SF-ADC into a SAR-ADC. The SSA-ADC is a flexible architecture because it is a digital-centric architecture. The proposed system also includes the error correction technique based on machine learning. In the proposed SSA-ADC, the SF-ADC is embedded in a simple SAR-ADC and used as a DCVTC with a digital comparator in MSB-side conversion. The SF-ADC also used for the conversion of the lower bits to enhance a resolution under noise level. In this paper, the encoding and error correction are defined as a minimization problem. The parameters for an error correction function is obtained by incremental learning based on Bayesian linear regression. The DNL and INL performance was improved by the proposed error correction technique using the DCVTC for 12-bit output. The error correction by machine learning also improved the performance of the AFE. The ADC in the proposed AFE achieved 88 dB SNDR at a sampling frequency of 250 kHz with 20.5 Hz full-scale input. Since the present study is focusing on the feasibility of the proposed system, the performance of an AFE IC can be improved by circuit level. For example, as the SSA-ADC is a scalable architecture, the power and area occupation can be reduced without degrading resolution and speed by using a more advanced process. As an example, the ECG waveform was measured by the AFE. The proposed system can also be used for other multi-channel biomedical sensors (e.g., EEG or EMG) due to its high sampling rate up to 250 kHz.

ACKNOWLEDGMENT

The authors wish to thank Proassist, Ltd. for their technical support.

REFERENCES

[1] C. J. Deepu, X. Zhang, W.-S. Liew, D. L. T. Wong, and Y. Lian, "An ECG-on-chip with 535 nW/channel integrated lossless data compressor for wireless sensors," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2435–2448, Nov. 2014.

[2] J. Hulzink *et al.*, "An ultra low energy biomedical signal processing system operating at near-threshold," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 546–554, Dec. 2011.

[3] S. Mondal, C. L. Hsu, R. Jafari, and D. Hall, "A dynamically reconfigurable ECG analog front-end with a 2.5 × data-dependent power reduction," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Jul. 2017, pp. 1–4.

[4] J.-Y. Um, Y.-J. Kim, E.-W. Song, J.-Y. Sim, and H.-J. Park, "A digital-domain calibration of split-capacitor DAC for a differential SAR ADC without additional analog circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 11, pp. 2845–2856, Nov. 2013.

[5] D. Jeon *et al.*, "An implantable 64 nW ECG-monitoring mixed-signal SoC for arrhythmia diagnosis," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2014, pp. 416–417.

[6] P. Harpe, H. Gao, R. van Dommele, E. Cantatore, and A. Van Roermund, "A 3 nW signal-acquisition IC integrating an amplifier with 2.1 NEF and a 1.5 fJ/conv-step ADC," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 58, Feb. 2015, pp. 382–383.

[7] X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067–1077, Apr. 2009.

[8] P. Schonle *et al.*, "A DC-connectable multi-channel biomedical data acquisition ASIC with mains frequency cancellation," in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2013, pp. 149–152.

[9] D. G. Gata *et al.*, "A 1.1-V 270-μA mixed-signal hearing aid chip," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1670–1678, Dec. 2002.

[10] S. Fateh, P. Schönle, L. Bettini, G. Rovere, L. Benini, and Q. Huang, "A reconfigurable 5-to-14 bit SAR ADC for battery-powered medical instrumentation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 11, pp. 2685–2694, Nov. 2015.

[11] S. Tani *et al.*, "Behavior-level analysis of a successive stochastic approximation analog-to-digital conversion system for multi-channel biomedical data acquisition," *IEICE Trans. Fundam. Electron., Commun. Comput. Sci.*, vol. E100-A, no. 10, pp. 2073–2085, Jun. 2017.

[12] T. Kamata *et al.*, "An analog front-end employing 87 dB SNDR stochastic SAR-ADC for a biomedical sensor," in *Proc. IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2017, pp. 301–304.

[13] S. Weaver, B. Hershberg, P. Kurahashi, D. Knierim, and U.-K. Moon, "Stochastic flash analog-to-digital conversion," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 11, pp. 2825–2833, Nov. 2010.

[14] F. Farahbakhshian, A. Waters, J. Muhlestein, and U. K. Moon, "Stochastic approximation register ADC," in *Proc. IEEE Int. New Circuits Syst. Conf. (NEWCAS)*, Jun. 2014, pp. 189–192.

[15] H. Ham, T. Matsuoka, J. Wang, and K. Taniguchi, "Design of a 500-MS/s stochastic signal detection circuit using a non-linearity reduction technique in a 65-nm CMOS process," *IEICE Electron. Express*, vol. 8, no. 6, pp. 353–359, Mar. 2011.

[16] R. Benzi, A. Sutera, and A. Vulpiani, "The mechanism of stochastic resonance," *J. Phys. A, Math. Gen.*, vol. 14, no. 11, pp. L453–L457, Nov. 1981.

[17] J. J. Collins, C. C. Chow, and T. T. Imhoff, "Stochastic resonance without tuning," *Nature*, vol. 376, no. 6537, pp. 236–238, Jul. 1995.

[18] M.-K. Jeon, W.-J. Yoo, C.-G. Kim, and C. Yoo, "A stochastic flash analog-to-digital converter linearized by reference swapping," *IEEE Access*, vol. 5, pp. 23046–23051, 2017.

[19] Y. Hirai, S. Yano, and T. Matsuoka, "A delta-sigma ADC with stochastic quantization," *IPSJ Trans. Syst. LSI Des. Methodol.*, vol. 8, pp. 123–130, Aug. 2015.

[20] H. Ham, T. Matsuoka, and K. Taniguchi, "Application of noise-enhanced detection of subthreshold signals for communication systems," *IEICE Trans. Fundam. Electron., Commun. Comput. Sci.*, vol. E92-A, no. 4, pp. 1012–1018, Apr. 2009.

[21] T. Asano, Y. Hirai, S. Tani, S. Yano, I. Jo, and T. Matsuoka, "An offset distribution modification technique of stochastic flash ADC," *IEICE Electron. Express*, vol. 13, no. 6, Mar. 2016, Art. no. 20160115.

[22] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "A 9.4-ENOB 1V 3.8 μW 100 kS/s SAR ADC with time-domain comparator," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2008, pp. 246–248.

[23] Y. Lin, K. Doris, H. Hegt, and A. van Roermund, "A dynamic latched comparator for low supply voltages down to 0.45 V in 65-nm CMOS," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2012, pp. 2737–2740.

[24] H. Jeon, Y.-B. Kim, and M. Choi, "Offset voltage analysis of dynamic latched comparator," in *Proc. IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2011, pp. 1–4.

[25] T. Denison, K. Consoer, A. Kelly, A. Hachenburg, and W. Santa, "A 2.2 μW 94 nV/$\sqrt{Hz}$, chopper-stabilized instrumentation amplifier for EEG detection in chronic implants," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 162–164.

[26] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.
[27] S. Orguc, H. S. Khurana, H.-S. Lee, and A. P. Chandrakasan, "0.3 V ultra-low power sensor interface for EMG," in *Proc. IEEE Eur. Solid State Circuits Conf.*, Sep. 2017, pp. 219–222.
[28] C. M. Bishop, *Pattern Recognition and Machine Learning*. New York, NY, USA: Springer, 2007.
[29] K. Tatsumi and T. Matsuoka, "A software level calibration based on bayesian regression for a successive stochastic approximation analog-to-digital converter system," *IEEE Trans. Cybern.*, to be published. doi: 10.1109/TCYB.2018.2795238.
[30] K. Pelckmans, J. A. K. Suykens, and B. De Moor, "Regularization constants in LS-SVMs: A fast estimate via convex optimization," in *Proc. IEEE Int. Joint Conf. Neural Netw.*, Jul. 2004, pp. 699–704.
[31] *Low Power, Five Electrode Electrocardiogram (ECG) Analog Front end, ADAS1000 Data Sheet*, Analog Devices, Norwood, MA, USA, 2012.

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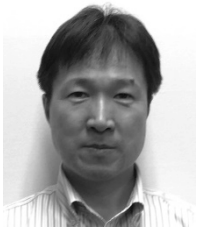

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