IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received December 25, 2018, accepted January 13, 2019, date of publication February 5, 2019, date of current version February 22, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2897577

A 55-65 GHz Internal Differentially Matched Silicon Power Amplifier With Spirally Folded 1:2 Balun

WEI PING CAO[1], JINXIN LI[2], WEN-BIN YE[3], (Member, IEEE), AND JIANG-AN HAN[4]

[1]Key Laboratory of Cognitive Radio and Information Processing, Ministry of Education, Guilin University of Electronic Technology, Guilin 541004, China
[2]College of Computer Science of Electronic Engineering, Hunan University, Changsha 410082, China
[3]School of Electronic Science and Technology, Shenzhen University, Shenzhen 518060, China
[4]Microsystem and Terahertz Research Center, Institute of Electronic Engineering, China Academy of Engineering Physics, Mianyang 610200, China

Corresponding author: Jiang-An Han (jhan3@e.ntu.edu.sg)

ABSTRACT A 55–65-GHz CMOS high power amplifier (PA) is designed with the help of a spirally folded 1:2 balun. By this size-folded balun, balance–unbalanced conversion and high-power combination are accomplished concurrently. Within the internal of PA, differential signal pairs benefit simplification of inter-stage matching topologies. The designed three-stage PA offers above 16.3-dB gain from 55.1 to 65.0 GHz. It is able to deliver 17.8-dBm output referred 1-dB compression point ($P_{1\ \mathrm{dB}}$) and 22.2-dBm saturated output power (P_{sat}) with a peak power-added efficiency of 10.9%.

INDEX TERMS CMOS, power amplifier, balun, power combination, differential matching, RFIC.

I. INTRODUCTION

Integration of microwave/millimeter-wave silicon PA compatible with digital and analog blocks has become a trend as continuous advancement of transistor scaling [1]–[4]. One hot research topic is high-performance CMOS power amplifier for the unlicensed band around 60 GHz [5]–[8].

Although scaling gate length of CMOS transistor is desirable for f_t/f_{max} and *PAE*, it also lowers the maximum supply voltage [9]. This phenomenon would pose challenges to CMOS PA design because the output ac voltage swing is constrained accordingly. In semiconductor device level, the maximum supply voltage to PA could be increased by stacking-FET in CMOS SOI technology [8], [10]. In PA architecture level, the method of improving power is to combine output signals from multiple transistor cells. By this way, Wilkinson combiner can demonstrate high output in CMOS [11]–[13]. A ticklish problem in Wilkinson PA design is to arrange both matching and bias feeding circuits together in single-ended circuit architecture. To add dc feeding to transistors, transmission line with one-fourth wave length is relatively bulky. Within such PAs, inter-stage multiple ways operate in common mode so that feeding path may also complicate matching topology and become a sensitive part to circuit performances. Compared to Wilkinson combiner PAs, transformer coupled ones [5], [14]–[17] save area of additional bias circuits by using center taps. This type of PA generally requires single-ended to differential signal conversion for the external I/O. Although transformer may turn a signal into out-of-phase ones, this solution does not always work well when the out-of-phase signal pairs are not in a good condition of differential status [18], [19]. If Balun is alternatively used to accomplish single-ended to differential conversion, classical configurations implemented by multiple layers routing or transmission lines with two quarter wave-length are bulky for CMOS power amplifiers [20]–[22]. Moreover, the physical I/O configurations of transformer and Balun are hard to place nearby large-size transistors for high power output. Recently, miniaturized Marchand Balun has been utilized in combining power from four cells in a W-band PA [23]. Multiple way combination solutions including Balun are still highly demanded to achieve high output power in CMOS.

In this paper, an internal differentially matched CMOS power amplifier architecture has been realized with the help of 1:2 spirally-folded Balun. The proposed Balun demonstrated in Fig. 1 achieves wideband balanced-unbalanced conversion and is designed for high power combination. Its work principle of folding Balun has been analyzed. By using this Balun in an eight-way combiner, 22.2 dBm Psat with 10.9 %

The associate editor coordinating the review of this manuscript and approving it for publication was Vittorio Camarchia.

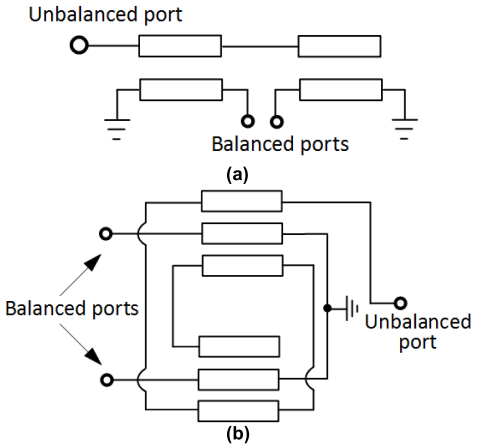


FIGURE 1. (a) Classic balun with two quarter wave-length transmission lines. (b) The folded 1:2 balun.

PAE at 60 GHz is obtained in 65 nm low-power (LP) CMOS PA. This Balun also creates virtual ground points so that long dc-feeding lines and bypass capacitances can be eliminated in PA architecture. Then inter-stage matching can take the advantage of differential circuit like transformers so that a PA's schematic/layout is simplified.

This paper is organized as follows. Section II details the PA overall architecture, inter-stage matching scheme and power distribution networks together with analysis and implementation of the spirally folded 1:2 Balun. In section III, the fabricated CMOS PA are demonstrated and measured. Conclusions are given in Section V finally.

II. CMOS PA DESIGN

A. PA ARCHITECTURE

The proposed CMOS power amplifier architecture is illustrated in Fig. 2. Basically, it employs three amplification stages and eight power units combined in the final stage. In the input port, a spirally folded 1:2 Balun splits unbalanced signal into two power amplification units with balanced phase status. Each power unit consists of a transistor pair along with neutralization capacitors. Then the output power of the first stage is further divided by current dividing. In this way, the adjacent power units of the succeeding stage are still with differential signals. The inter-stage matching is accomplished by transmission lines and capacitors. The dc injection point is also regarded as circuit common in matching and virtual ground makes dc feeding and matching parts insensitive to dimensions. The proposed inter-stage topology is also applied between the second and third amplification stages. In the final stage, output signals from eight power units are combined through current combining and the proposed spirally folded Balun.

B. INTER-STAGE MATCHING SCHEME

The inter-stage matching starts with investigating power units' impedance characteristics. Since the topologies of the two inter-stages are similar, matching schematic between the first and second stages is discussed as an example. In Fig. 3. (a), components with the same signal polarity are extracted out to consider how to realize inter-stage matching in which dc injection point is regarded as virtual ground. By Smith Chart, the inter-stage matching is a flow of impedance transformation demonstrated in Fig. 3. (b). As transistors with large gate width are employed to deliver high power, the optimal matching impedances of both the drive stage ⑧ and the succeeding stage ① are of low values in real and imaginary parts. More difficulty is two ways of the succeeding stage paralleled in the middle connection point, which would further lower their overall input impedance in ⑤. To solve this problem, shorted stub TL_2 is firstly utilized to increase the real part to ③. Then TL_3 is adopted for power division and physical connection. It is made of broad width transmission lines to reduce superfluous imaginary part. In the left of parallel connection point, a series capacitor brings the input impedance into weak capacitive region ⑥ so that the equivalent shorted stub TL_4 can be inserted to feed the drain bias of the drive stage. Finally, series transmission line TL_5 is adopted for adjusting matching impedance slightly. By this inter-stage matching scheme, the dc bias feed path is equivalent to only 9° wave length and multiple ways inside PA keeps good uniformity.

C. POWER COMBINATION DESIGN WITH THE SPIRALLY FOLDED 1:2 BALUN

For this multiple way power combination using Balun and power distribution networks, design implementation can be accomplished by three steps. In the first step, an ideal circuit is constructed to plan the overall matching scheme as illustrated in Fig. 4. In this topology, equivalent shorted stub TL_c is used to shift the input impedance of power combining networks into inductive region and meanwhile inject part of dc current. With branches TL_b paralleled in the inputs, a Balun itself can achieve power combination from four ways. In power combination view, the input balanced signals are combined in a series way. Due to large size transistor adopted for delivering high power, the impedance seen to an active device is 2.1-j∗5.1 so that the turn ratio of resistance part to 50Ω output is around 1:23.8. The impedance transformation is realized by the stated transmission lines and the spirally folded 1:2 Balun together. From TL_a to spirally-folded balun and then TL_b, input resistance is largely decreased to a low level.

In the second step, the spirally-folded 1:2 Balun is devised according to this matching scheme. Its work principle is illustrated in Fig. 5. In this diagram, excitation is at the unbalanced port to a winding trace with four sections. Then differential signals are induced by two connected trace sections to the balanced ports. These coupled traces are ideally analyzed as lossless transmission lines. According to wave interference theory, the voltages and currents at the balanced ports are

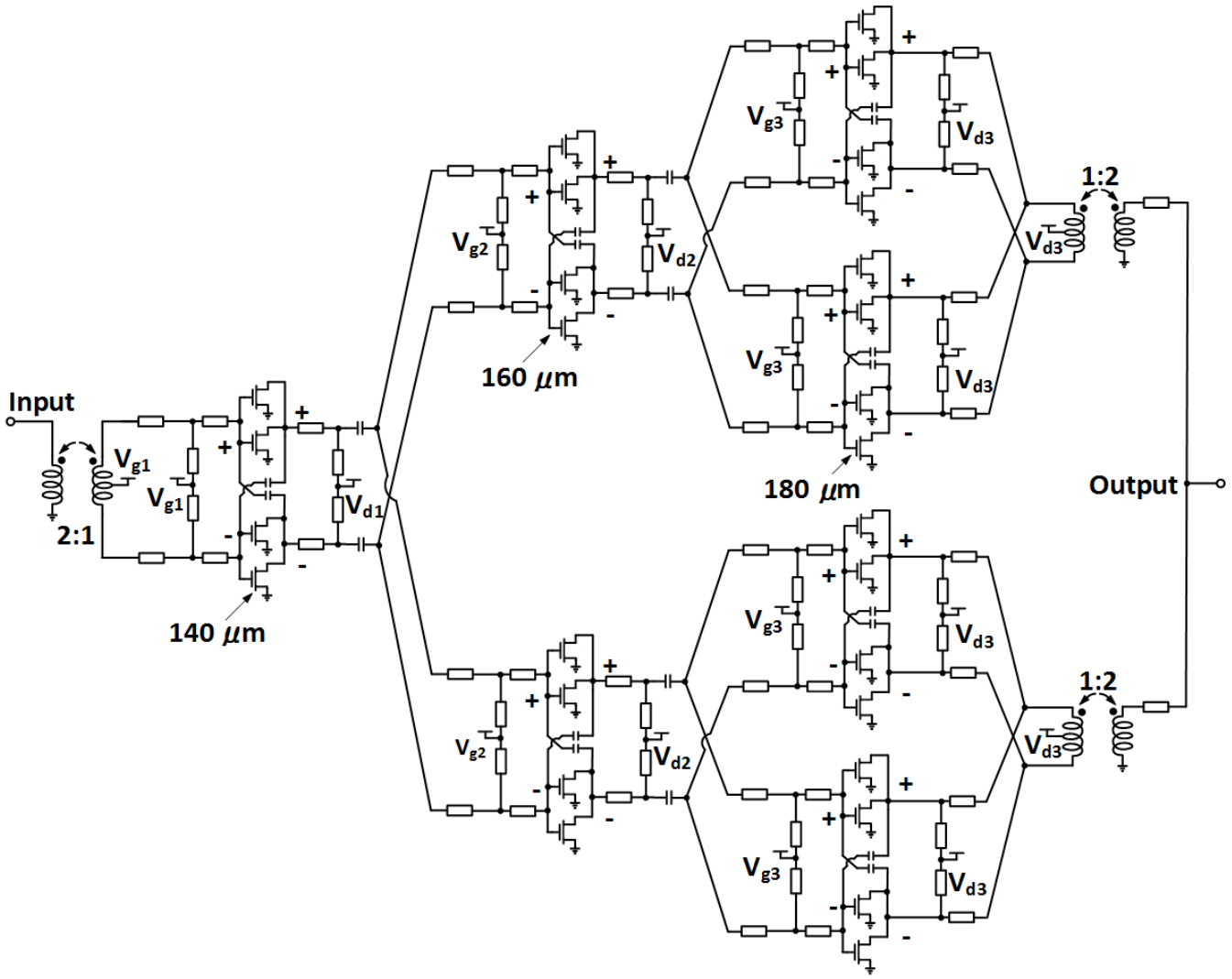


FIGURE 2. CMOS PA architecture.

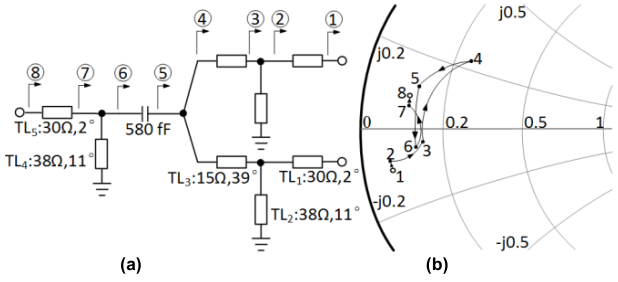


FIGURE 3. (a) Equivalent circuit topology between the first and second stage. (b) Impedance transformation flow in Smith Chart.

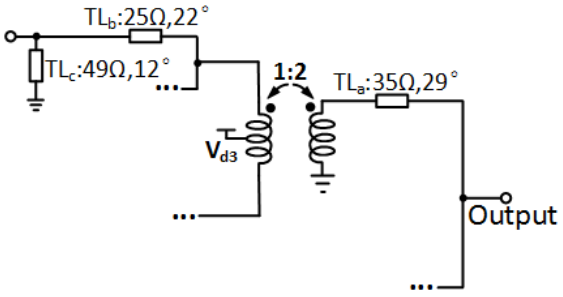


FIGURE 4. Simplified circuit topology of the final power combining networks.

derived as

$$V_{in+} = V_{in-} = 2V_0^+\cos(-\theta) + 2V_0^+\cos(-3\theta) = 4V_0^+\cos(2\theta)\cos(\theta) \quad (1)$$

$$I_{in+} = -\frac{2jV_0^+}{Z_m}\sin(-\theta) - \frac{2jV_0^+}{Z_m}\sin(-3\theta) = \frac{4jV_0^+}{Z_m}\sin(2\theta)\cos(\theta) \quad (2)$$

$$I_{in-} = \frac{2jV_0^+}{Z_m}\sin(-\theta) + \frac{2jV_0^+}{Z_m}\sin(-3\theta) = -\frac{4jV_0^+}{Z_m}\sin(2\theta)\cos(\theta) \quad (3)$$

Then the input impedances seen from the two balanced ports are

$$Z_{in+} = jZ_m\cot(-2\theta) = jZ_m\cot(\theta_1) \quad (4)$$

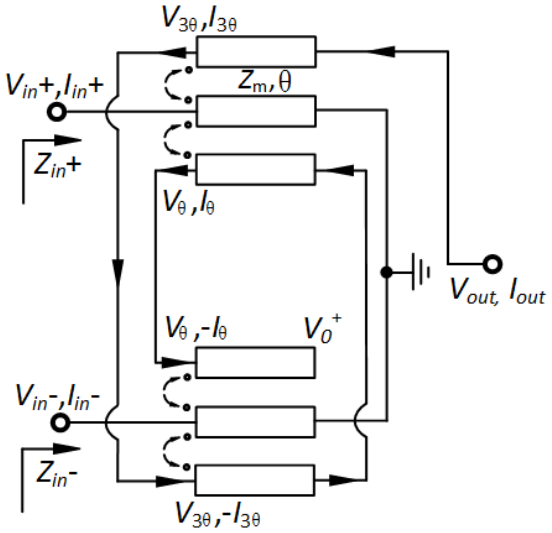


FIGURE 5. The Simplified diagram of the spirally folded 1:2 balun.

$$Z_{in-} = jZ_m \cot(2\theta) = jZ_m \cot(\theta_2) \tag{5}$$

In the condition of unbalanced-balanced conversion is achieved, phase condition of θ_1 and θ_2 should be

$$\theta_2 - \theta_1 = 4\theta = \pi + 2k\pi \quad (k = \text{integer}) \tag{6}$$

When k equals to 0, θ is only $\pi/4$. Its according wave length of coupling traces is $\lambda/8$ for a folded 1:2 Balun. By the proposed folding scheme, Balun length could be reduced by half in comparison with that of classic ones.

Applying the proposed folded Balun concept in on-chip PA design, its trace sections are spirally winded along octagon shape for better integration compatibility. As demonstrated in Fig. 6 (a), most of the winded sections are realized by M7-M8 while M6 is used to enhance conductivity at junction backside. The two balanced signals are excited by broad trace sharing one winding turn. In the middle of broad trace, dc feeding point is tapped from lower metal layers M4 and M5. The unbalanced signal is coupled out by a two turn octagon trace with total wave length approximating to $\lambda/2$. In Fig. 6 (b) and (c), the simulated spirally-folded Balun demonstrates less than 5° phase unbalances below 140 GHz and the insertion loss is about 1.3 dB at 60 GHz. Compared to 1:1 transformer with the fourth port connecting to the ground, the proposed spirally folded Balun can effectively make balanced-unbalanced conversion at a much wider frequency range. In 65nm LP CMOS process, the proposed Balun occupies an area of $160\times140\mu m^2$, which is very suitable for high power PA design. If Marchand Balun basing on the same process is used alternatively, its dimension would be $905\times12\ \mu m^2$.

After the Balun is designed and preliminarily simulated, its configuration is inserted into Fig. 4's circuit topology in the final step. The other ideal lumped elements are substituted by on-chip transmission lines and the whole networks including Balun are further optimized by full-wave EM simulation.

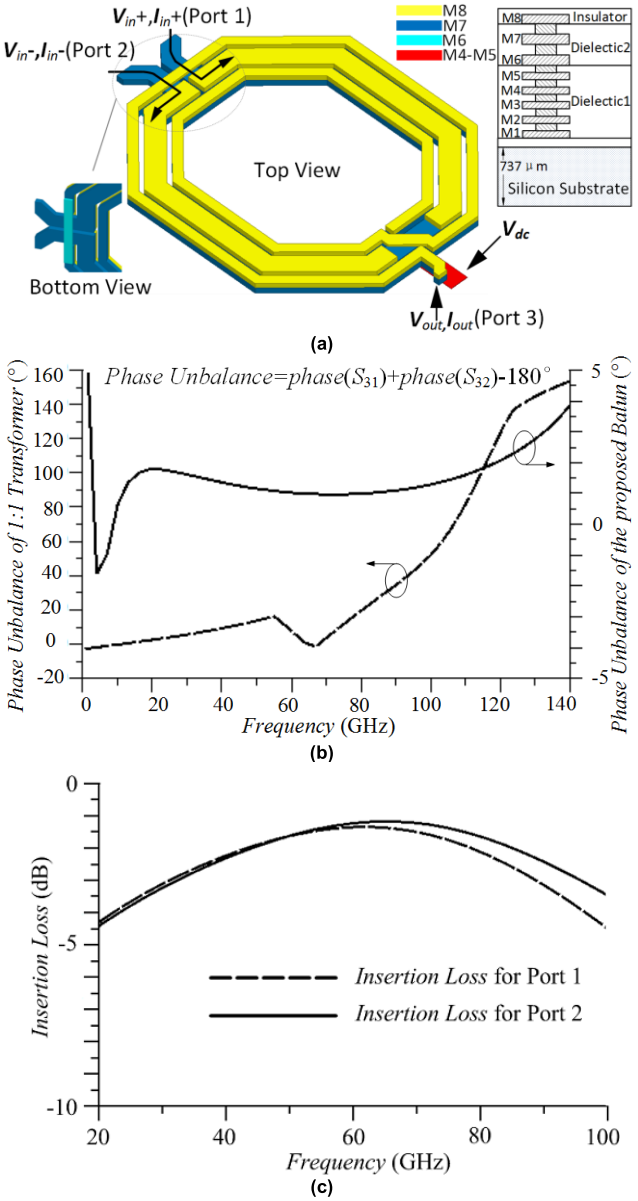


FIGURE 6. (a) Configuration of the spirally-folded balun. (b) Phase unbalances comparison. (c) Insertion loss of the spirally-folded balun.

This proposed Balun is also applied in power division circuits of the first stage. Its design method is similar to the output distribution networks. With the spirally-folded Baluns in both input and output, the internal signals between adjacent ways are in differential so that bias circuits basing upon transmission lines can be incorporated into matching part like transformers.

III. EXPERIMENT RESULTS

The proposed PA was fabricated in 65 nm low-power (LP) CMOS process which is for applications of low cost multi-media wireless and consumer electronics. Its f_t and f_{max} are around 210 GHz and 230 GHz respectively. The designed PA size is 1.20×0.95 mm^2 as illustrated in Fig. 7. In the final

TABLE 1. Summary of state-of-the-art 60 GHz silicon PAs.

Ref.	Tech. (nm)	3dB Bandwidth (GHz)	Circuit Topology	Supply Voltage (V)	Gain (dB)	Area (mm^2)	*PAE*	P_{-1} (dBm)	P_{sat} (dBm)
[3]	90 GP CMOS	41.8-66.3	3CS	1.2	20.1	0.432	20.3	17.6	20.6
[5]	40 GP CMOS	60.3-65.8*	3PP	1.8	22.4	0.4	23	13.9	16.4
[6]	40 GP CMOS	52-64	3CS	1.2	20.3	0.66	18.3	16.2	19.6
[7]	28 GP CMOS	56-67	3CC	2.1	24.4	0.64	12.6	11.7	16.5
[8]	65 SOI. CMOS	60-65	2CC	2.6	15	0.57	18.2	15.2	16.5
[11]	90 LP CMOS	58-66	4CS	1.2	20.6	0.64	14.2	18.2	19.9
[12]	65 Sd. CMOS	48.8-73.9	3CS	1.2	16.3	1.88*	10.0	19.4	23.2
[24]	250 SiGe C HBT	55-63*	1CC	3.3	14.2	0.62	16.3	12.2	17.4
[25]	130 SiGe HBT	59-64	2CC	4.0	22*	3.42	6.3	21*	23
[26]	130 SiGe HBT	55-65	3CG	1.8	20.6	0.72	18	19.7	20.1
[27]	130 SiGe HBT	60-75	4CE	1.8	22	3.38	12	19*	24
This Work	**65 LP CMOS**	**55.1-65.0**	**3CS**	**1.2**	**16.3**	**1.14**	**10.9**	**17.8**	**22.2**

* Estimated value from paper cited. BW is abbreviation of 3-dB bandwidth estimated by S-parameters.
GP.: General Purpose CMOS; Dg.: Digital CMOS
CS: common source; CC: cascade; PP: Push-pull; CG: Common-gate; CE: Common-emitter;

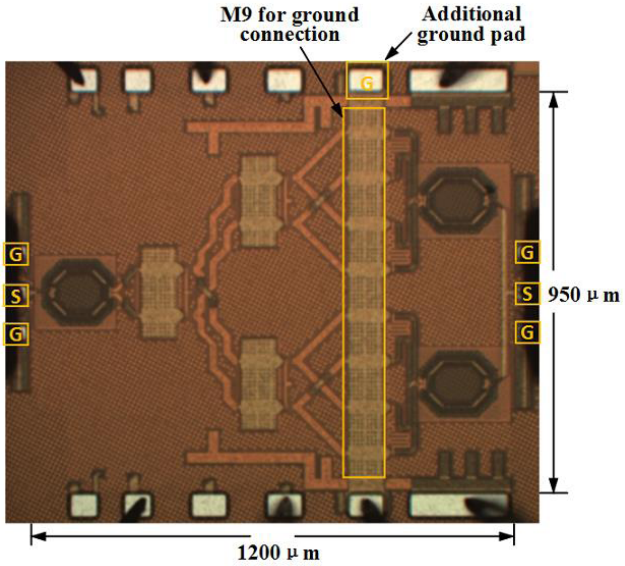


FIGURE 7. The fabricated CMOS PA with the spirally folded 1:2 balun.

stage layout design, two additional ground pads provide more return path of drain dc current. Top thick metals and bottom ground plane are connected to these ground pads for better thermal dissipation.

The small signal performance was characterized by Programmable Network analyzer (PNA) and Semiconductor Analyzer. The instrument calibration is accomplished by line-reflect-reflect-match (LRRM) method. The measurement results of the S-parameters are shown in Fig. 8. (a). The fabricated PA can provide more than 13.3 dB gain at 55.1-65.0 GHz (3dB bandwidth) and the peak gain is 16.3 dB obtained at 60.1 GHz. The S_{11} is below −18.9 dB from 55G to 65 GHz while the S_{22} is less than −10 dB at 56.9-61.2 GHz. Basing on the results of S-parameters, the stability factor k and $|\Delta|$ are then calculated by equation. As illustrated in Fig. 8 (b), k is above 1.35 from DC to 67.5 GHz while $|\Delta|$ is below 0.79.

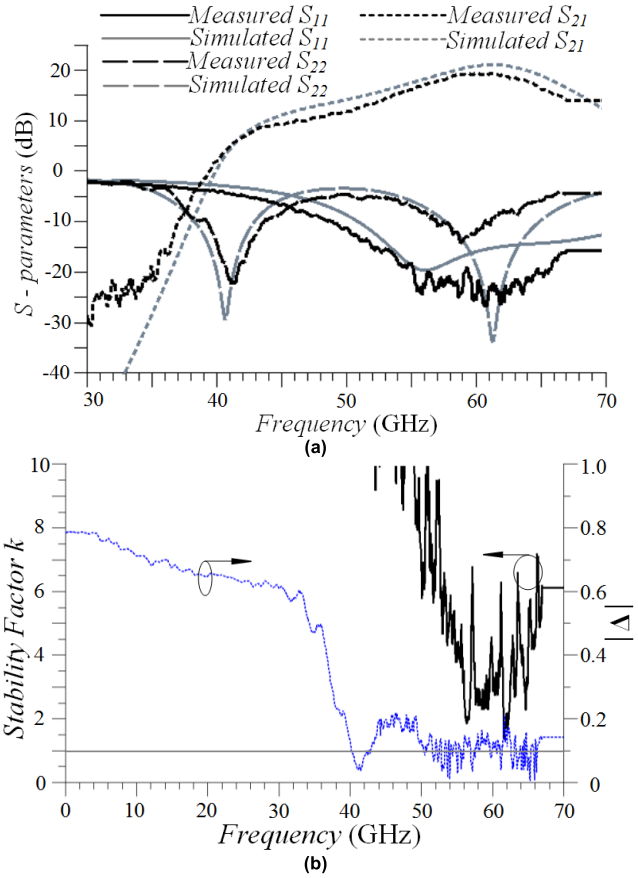


FIGURE 8. (a) The simulated and measured S-parameters. (b) The calculated stability factor k and $|\Delta|$ basing on S-parameter results.

In large signal test, instruments including spectrum analyzer, semiconductor analyzer, amplifier module HHPAV-335 and vector network analyzer are used to deliver sufficient drive power to the design-under-test (DUT) as illustrated in Fig. 9. (a). The fabricated PA integrated with the spirally folded 1:2 Balun offers 22.2 dBm P_{sat} and 10.9% peak *PAE* at 60 GHz. Its output P_{1dB} is about 17.8 dBm with about 4.5° phase shift caused by *AM*/*PM* conversion. The performances

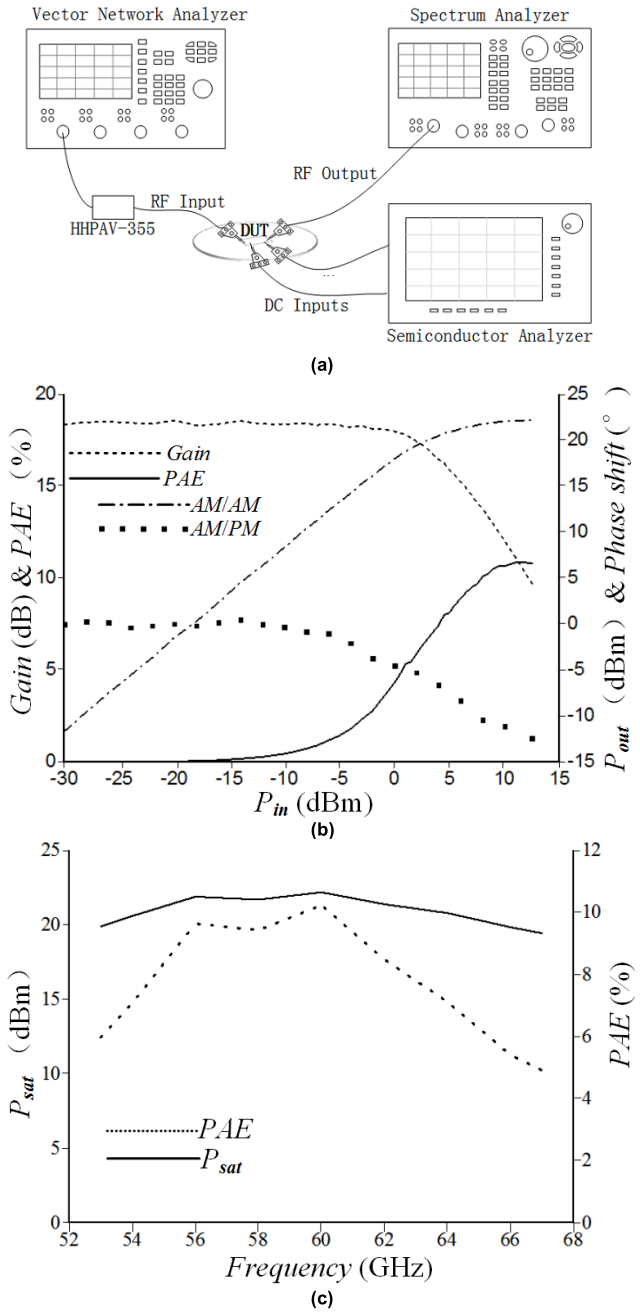


FIGURE 9. (a) PA measurement setup for characterizing its large signal performances. (b) The measured gain, *PAE*, *AM/AM* and *AM/PM* versus P_{in}. (c) The measured *PAE* and P_{sat} versus frequencies.

of P_{sat} and *PAE* are also measured from 53 GHz to 67 GHz, as shown in Fig. 9. (c). This PA can offer above 19.5 dBm saturated output power at 53 – 67 GHz and the *PAE* is above 4.9 % across this 14 GHz bandwidth. The measurement results of this PA are compared with state-of-the-art in Table 1.

IV. CONCLUSION

In this paper, a high power amplifier utilizing novel spirally folded 1:2 Balun has been implemented in 65nm LP CMOS. The proposed Balun is able to achieve wideband unbalance-balance conversion and suitable for multiple way power combination networks. By this configuration, the internal of a PA can be treated as differential circuit so that virtual ground points are created to simplify matching and bias parts. Accordingly, a three-stage PA is demonstrated for high power amplifier design using large-size CMOS transistors. The fabricated PA provides more than 16.3 dB gain at 55.1-65.0 GHz and high output power of 22.2 dBm P_{sat} with 10.9% peak *PAE* at 60 GHz. Moreover, the proposed Balun configuration and matching methods are applicable to other designs of silicon based high power amplifiers.

REFERENCES

[1] K.-L. Wu, K.-T. Lai, R. Hu, C. F. Jou, D.-C. Niu, and Y.-S. Shiao, "77–110 GHz 65-nm CMOS power amplifier design," *IEEE Trans. THz Sci. Technol.*, vol. 4, no. 3, pp. 391–399, May 2014.

[2] A. M. Niknejad, D. Chowdhury, and J. Chen, "Design of CMOS power amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1784–1796, Jun. 2012.

[3] C.-F. Chou, Y.-H. Hsiao, Y.-C. Wu, Y.-H. Lin, C.-W. Wu, and H. Wang, "Design of a V-band 20-dBm wideband power amplifier using transformer-based radial power combining in 90-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 12, pp. 4545–4560, Dec. 2016.

[4] J. R. Long, W. L. Chan, Y. Zhao, and M. Spirito, "Silicon VLSI catches the millimeter wave," *IEEE Commun. Mag.*, vol. 49, no. 10, pp. 182–189, Oct. 2011.

[5] S. Kulkarni and P. Reynaert, "A 60-GHz power amplifier with AM–PM distortion cancellation in 40-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2284–2291, Jul. 2016.

[6] C.-W. Tseng and Y.-J. Wang, "A 60 GHz 19.6 dBm power amplifier with 18.3% PAE in 40 nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 2, pp. 121–123, Feb. 2015.

[7] S. V. Thyagarajan, A. M. Niknejad, and C. D. Hull, "A 60 GHz drain-source neutralized wideband linear power amplifier in 28 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 8, pp. 2253–2262, Aug. 2016.

[8] A. Siligaris *et al.*, "A 60 GHz power amplifier with 14.5 dBm saturation power and 25% peak PAE in CMOS 65 nm SOI," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1286–1294, Jul. 2010.

[9] P.-I. Mak and R. P. Martins, "High-/mixed-voltage RF and analog CMOS circuits come of age," *IEEE Circuits Syst. Mag.*, vol. 10, no. 4, pp. 27–39, 4th Quart., 2010.

[10] J. Cui, S. Helmi, Y. Tang, and S. Mohammadi, "Stacking the deck for efficiency: RF-to millimeter-wave stacked CMOS SOI power amplifiers," *IEEE Microw. Mag.*, vol. 17, no. 12, pp. 55–69, Dec. 2016.

[11] C. Y. Law and A.-V. Pham, "A high-gain 60 GHz power amplifier with 20 dBm output power in 90 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 426–427.

[12] Y.-H. Hsiao, Z.-M. Tsai, H.-C. Liao, J.-C. Kao, and H. Wang, "Millimeter-wave CMOS power amplifiers with high output power and wideband performances," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4520–4533, Dec. 2013.

[13] T. Quemerais, L. Moquillon, J.-M. Fournier, P. Benech, and V. Huard, "Design-in-reliable millimeter-wave power amplifiers in a 65-nm CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 4, pp. 1079–1085, Apr. 2012.

[14] D. Chowdhury, P. Reynaert, and A. M. Niknejad, "Design considerations for 60 GHz transformer-coupled CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2733–2744, Oct. 2009.

[15] J. Chen and A. M. Niknejad, "A compact 1 V 18.6 dBm 60 GHz power amplifier in 65 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 432–433.

[16] T. LaRocca, J. Y.-C. Liu, and M.-C. F. Chang, "60 GHz CMOS amplifiers using transformer-coupling and artificial dielectric differential transmission lines for compact design," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1425–1435, May 2009.

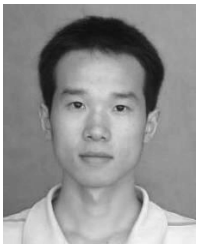
[17] A. Larie, E. Kerhervé, B. Martineau, V. Knopik, and D. Belot, "A 1.2 V 20 dBm 60 GHz power amplifier with 32.4 dB gain and 20% peak PAE in 65nm CMOS," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 175–178.
[18] S. Aloui, B. Leite, N. Demirel, R. Plana, D. Belot, and E. Kerherve, "High-gain and linear 60-GHz power amplifier with a thin digital 65-nm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 6, pp. 2425–2437, Jun. 2013.
[19] Y.-N. Jen, J.-H. Tsai, T.-W. Huang, and H. Wang, "Design and analysis of a 55–71-GHz compact and broadband distributed active transformer power amplifier in 90-nm CMOS process," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 7, pp. 1637–1646, Jul. 2009.
[20] H.-K. Chiou and T.-Y. Yang, "Low-loss and broadband asymmetric broadside-coupled balun for mixer design in 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 4, pp. 835–848, Apr. 2008.
[21] K. Nishikawa, I. Toyoda, and T. Tokumitsu, "Compact and broad-band three-dimensional MMIC balun," *IEEE Trans. Microw. Theory Techn.*, vol. 47, no. 1, pp. 96–98, Jan. 1999.
[22] H.-M. Hsu, J.-S. Huang, S.-Y. Chen, and S.-H. Lai, "Design of an on-chip balun with a minimum amplitude imbalance using a symmetric stack layout," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 4, pp. 814–819, Apr. 2010.
[23] H. Jia, B. Chi, L. Kuang, and Z. Wang, "A W-band power amplifier utilizing a miniaturized Marchand balun combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 719–725, Feb. 2015.
[24] D. Grujic, M. Savic, C. Bingol, and L. Saranovac, "60 GHz SiGe: C HBT power amplifier with 17.4 dBm output power and 16.3% PAE," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 4, pp. 194–196, Apr. 2012.
[25] U. R. Pfeiffer and D. Goren, "A 23-dBm 60-GHz distributed active transformer in a silicon process technology," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 5, pp. 857–865, May 2007.
[26] Y. Zhao and J. R. Long, "A wideband, dual-path, millimeter-wave power amplifier with 20 dBm output power and PAE above 15% in 130 nm SiGe-BiCMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 1981–1997, Sep. 2012.
[27] E. C. Wagner and G. M. Rebeiz, "An 8-way combined E-band power amplifier with 24 dBm psat and 12% PAE in 0.12 μm SiGe," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Philadelphia, PA, USA, Jun. 2018, pp. 1342–1344.

WEI PING CAO received the B.S. degree from Hunan Normal University, Hunan, China, in 1995, and the M.Sc. and Ph.D. degrees in electromagnetic field and microwave technology from the University of Electronic Science and Technology of China, Chengdu, China, in 2003 and 2012, respectively. From 1999 to 2002, he was an Assistant Professor with the Millimeter Wave Laboratory, 10th Research Institute, China Electronic Technology Group Corporation. From 2010 to 2011, he was a Visiting Professor with the Department of Electrical and Computer Engineering, University of Manitoba. In 2002, he joined the Department of Communication and Information Engineering, Guilin University of Electronic Technology, Guangxi, China, where he is currently the Assistant Head and a Professor. His current research interests include computational electromagnetics, broadband electrically small antennas, smart antennas, and RF/microwave circuits.

JINXIN LI received the B.S. degree in electronic information science and technology and the Ph.D. degree in electromagnetics and microwave technology from the University of Electronic Science and Technology of China, Chengdu, in 2008 and 2017, respectively. In 2015, he was a Visiting Ph.D. Student with the Department of Electrical and Computer Engineering, Duke University, Durham, NC, USA.

He is currently an Assistant Professor with the College of Computer Science and Electronic Engineering, Hunan University, Changsha. His research interests include antennas, antenna arrays, metamaterials, passive devices and circuit, microwave and millimeter-wave circuits and their integrated circuits.

WEN-BIN YE (S'12–M'14) received the B.S. degree in microelectronics from Sichuan University, Chengdu, China, in 2009, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2014. From 2014 to 2015, he was a Project Officer with Nanyang Technological University. Since 2015, he has been with the College of Electrical Science and Technology, Shenzhen University, where he is currently an Assistant Professor. His research interests include digital filter design, nonuniformly sampled data processing, and bio-medical signal processing.



JIANG-AN HAN was born in Guilin, China, in 1984. He received the B.Sc. and M.Sc. degrees from the University of Electronic Science and Technology of China, Chengdu, China, in 2008 and 2011, respectively, and the Ph.D. degree from Nanyang Technological University, Singapore, in 2016.

His research focuses on millimeter-wave circuits design in GaAs, CMOS, and SiGe technologies.