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Single-Phase Inverter With Wide Input Voltage and Power Decoupling Capability

YONGLU LIU[1,2], (Student Member, IEEE), MEI SU[1,2], FULIN LIU[1,2], MINGHUI ZHENG[3], XIAO LIANG[4], GUO XU[1,2], AND YAO SUN[1,2], (Member, IEEE)

[1]School of Information Science and Engineering, Central South University, Changsha 410083, China
[2]Hunan Provincial Key Laboratory of Power Electronics Equipment and Grid, Changsha 410083, China
[3]Department of Mechanical and Aerospace Engineering, University at Buffalo, Buffalo, NY 14260, USA
[4]Department of Civil, Structural and Environmental Engineering, University at Buffalo, Buffalo, NY, 14260, USA

Corresponding author: Guo Xu (xuguocsu@csu.edu.cn)

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ABSTRACT This paper proposes a single-phase inverter to achieve high power factor, wide input voltage range, and ripple power decoupling without using large passive components. The proposed inverter is obtained by rearranging the positions of the switches and passive components in the exiting circuit. Given that, a wider dc input voltage range can be obtained since it is no longer bounded by half the grid peak voltage. In addition, the inherent low-frequency ripple power is buffered, rather than through increasing the capacitance, by swinging the decoupling capacitor voltage resulting in an improvement of the power density and system lifetime. Furthermore, with adopting a closed-loop control method, no dedicated power-buffering controller is required. This paper starts with introducing the derivation of the proposed inverter followed by the operation principles and circuit analysis. A comparison between the derived circuit and the original one is carried out to show the pros and cons. Finally, a 200-W prototype is constructed to demonstrate the effectiveness of the proposed topology.

INDEX TERMS Active power decoupling, closed-loop control, low-frequency ripple power, single-phase inverter, wide input voltage.

I. INTRODUCTION

The single-phase power conversion technique is widely used in low-power applications, such as photovoltaic (PV) system [1], fuel cells system [2], light-emitting diode (LED) drivers [3], and electric vehicle chargers [4]. It is well-known that the twice ripple power inherently exists in the single-phase system. When it flows into the dc side, the low-frequency voltage/current ripple will be introduced. Consequently, a bulky capacitor or inductor must be employed to restrict the voltage/current ripple within an allowable range [1], [5]. This is usually referred to the passive power decoupling method. However, the use of a large capacitor (where electrolytic capacitors are usually accompanied) or inductor degrades the power density and the system reliability is also reduced when electrolytic capacitors are employed [6].

Many research efforts focus on the active power decoupling method [7]–[32]. It buffers the ripple power by swinging the decoupling capacitor voltage. Therefore, instead of using electrolytic capacitors, small-valued capacitors (e.g., film or ceramic capacitors) can be employed, which increases the lifetime and reliability of the system. For a front-end boost dc/dc circuit cascaded by a downstream H-bridge inverter, as an example of a two-stage converter, the ripple power can be buffered by swinging the dc bus voltage without adding any extra component [7]–[10]. In this case, the ripple power is buffered at the cost of increasing the dc bus voltage. The differential inverters, as one of the single-stage circuits, is consisted of two dc/dc circuits. This type of inverters can also achieve the power decoupling without adding any extra component [11]–[15], where the ripple power is buffered by controlling the common voltages. For other single-stage

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circuits, however, additional decoupling circuits are usually needed [1], [5]. They can be categorized as the parallel power buffer [16]–[18] and the series power one [19], [20]. The parallel power buffer is usually in parallel with the dc capacitor in the voltage source converter. The ripple power flowing into the dc capacitor can be diverted into an added decoupling capacitor such that a constant dc bus voltage can be obtained. For this type of decoupling methodology, the decoupling circuit together with the dc capacitor can be treated as an active capacitor [21], [22] or a virtual infinite capacitor [23]. The series power buffer is usually in series with the dc inductor in the current source converter. The decoupling circuit provides an equivalent series voltage to retain the voltage-second balance of the dc inductor such that a constant dc current is obtained. Similarly, this type of decoupling concept treats the decoupling circuit together with dc inductor as an active inductor.

Recently, other functions (e.g., leakage current suppression in PV system and power factor correction (PFC)) have been merged into the decoupling circuits [24]–[32]. This type of decoupling circuits makes the most of the active and passive components. In [24] and [25], the decoupling capacitors play the roles of the high-frequency filter and provide a pass for the common voltage to eliminate the leakage current in a PV system. In [26] and [27], the decoupling capacitor voltage also serves as the dc link to accomplish dc-ac inversion. In [28], the output voltage step-up function is integrated with the decoupling circuit. Ohnuma and Itoh [29] investigated a decoupling circuit with PFC function based on the buck PFC rectifier. Using a similar derivation, a single-phase current-source PV inverter with power decoupling capability was proposed in [30]. However, for both of them, the dc voltage has to be lower than half the grid peak voltage, which restricts the scope of applications. Also, an extra dc/dc circuit is needed when the dc voltage is relatively high. To address this issue, Li *et al.* [31] proposed a modified PFC rectifier by rotating the three-terminal cell in [29] to achieve a wider output voltage range. However, the polarity of the output voltage is inverted, and particular caution has to be paid to the start-up period to avoid negative spike voltage. In [29]–[31], the control of decoupling and PFC are coupled. By adding an extra switch, Liu *et al.* [32] proposed a PFC rectifier, which releases the operation constraints and then makes the control easier to achieve.

This paper proposes a current source inverter with wide input voltage range and power decoupling capability. This paper is extended work of [29]–[31]. The proposed inverter possesses the same active and passive components as those in [30], and it also operates at unity power factor. However, the dc input voltage is not bounded by half the grid peak voltage. Therefore, similar to [31] and [32], the dc side voltage range is wide and no bulky electrolytic capacitor is employed. In addition, the low-frequency ripple power is automatically stored in the decoupling capacitor, and thus no dedicated power-buffering controller is needed. Moreover, the start-up issue in [31] does not exist in the proposed inverter. The remainder of the paper is organized as follows. Section II introduces the topology of the proposed converter. Section III presents the circuit analysis and the controller design. Section IV gives a comparison between the proposed inverter and the existing one. Experimental results are provided in Section V. Finally, Section VI concludes the paper.

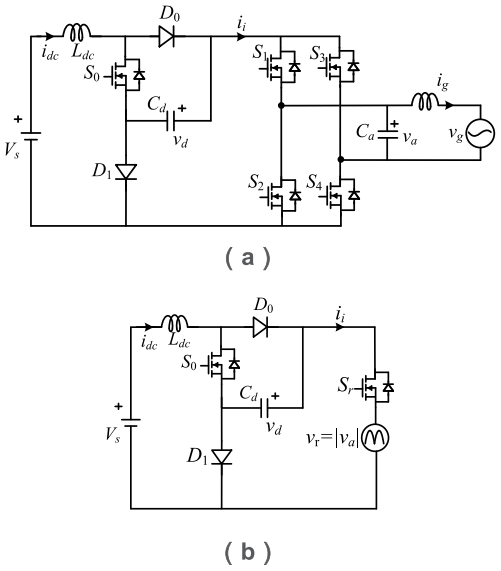


FIGURE 1. Proposed inverter in [30] (a) and its equivalent circuit (b).

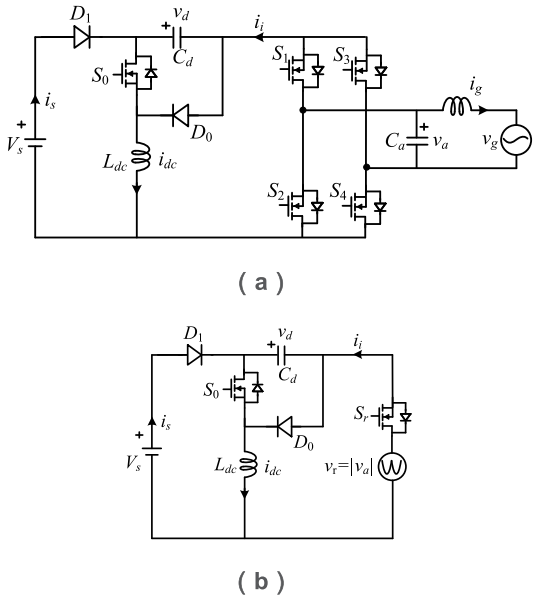


FIGURE 2. Proposed inverter in this paper (a) and its equivalent circuit (b).

II. PROPOSED CIRCUIT AND OPERATION STATES

A. CIRCUIT CONFIGURATION

Fig. 1 outlines the inverter proposed in [30] and its equivalent circuit. v_r is the rectified output voltage, and S_r is an equivalent switch, which is used to indicate whether the dc inductor

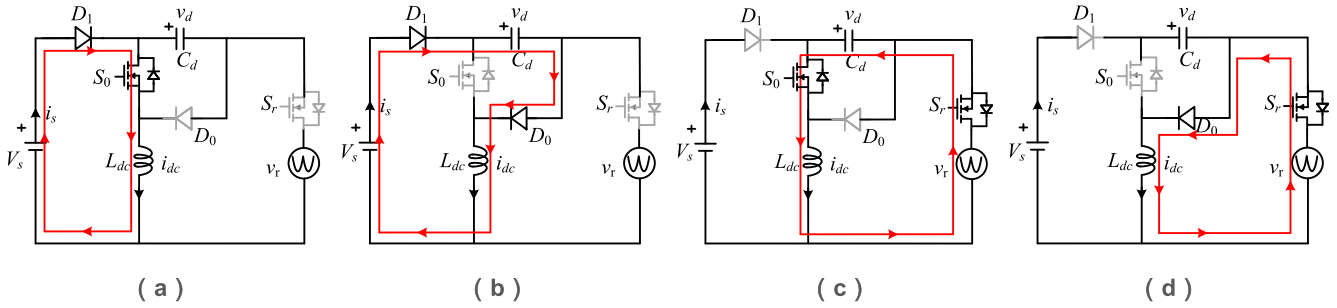


FIGURE 3. Operating states of the proposed inverter. (a) State 1 (S_0 = ON, S_r = OFF). (b) State 2 (S_0 = OFF, S_r = OFF). (c) State 3 (S_0 = ON, S_r = ON). (d) State 4 (S_0 = OFF, S_r = ON).

current i_{dc} passes through the grid side. It can be found that whether S_r is turned on or off, the whole circuit can be viewed as a boost circuit. According to the power balance, the grid voltage amplitude V has to be higher than dc source voltage V_s [30]. In this circuit, the decoupling capacitor voltage v_d should be larger than v_r to prevent $D_1(S_r)$ from being turned on when i_{dc} flows through S_r (D_1).

Fig. 2 shows the proposed inverter in this paper and its equivalent circuit. Compared to the inverter in Fig. 1, the design is obtained by exchanging the positions of $L_{dc}(C_d)$ and D_1 (D_0) and reversing the direction of S_i (i = 1, 2, 3, 4) without adding any extra active or passive component. When S_r is turned off, the circuit is a boost dc/dc circuit from V_s to v_d. When S_r is turned on, the diode D_1 is reverse-biased, and the circuit is a buck dc/dc circuit from V_d to v_r. Therefore, the entire circuit can be viewed as a buck-boost circuit from V_s to v_r. In this circuit, v_d should be larger than $(v_r + V_s)$ to prevent $D_1(S_r)$ from being turned on when i_{dc} flows through $S_r(D_1)$.

B. OPERATION STATES

In the proposed inverter, as previously mentioned, when S_0 (S_r) is turned on, the diode D_0 (D_1) is reverse biased. Therefore, as shown in Fig. 3, it has four operation states. The specific switching patterns are summarized in Table 1.

TABLE 1. Switching pattern.

Switching state	S_0	S_r	S_1		S_2		S_3		S_4	
1	ON	OFF	OFF		OFF		OFF		OFF	
2	OFF	OFF								
3	ON	ON	$v_a \le 0$	$v_a > 0$	$v_a \le 0$	$v_a > 0$	$v_a \le 0$	$v_a > 0$	$v_a \le 0$	$v_a > 0$
			ON	OFF	OFF	ON	OFF	ON	ON	OFF
4	OFF	ON	$v_a \le 0$	$v_a > 0$	$v_a \le 0$	$v_a > 0$	$v_a \le 0$	$v_a > 0$	$v_a \le 0$	$v_a > 0$
			ON	OFF	OFF	ON	OFF	ON	ON	OFF

In States 1 and 2, as shown in the Figs. 3(a) and (b) respectively, S_r is always turned off. In this case, the grid side is idle, and the dc current i_{dc} always flows through dc source. In State 2, the switch S_0 is turned off and the decoupling capacitor C_d is charged to absorb the ripple power. In States 3 and 4, as shown in the Figs. 3(c) and (d) respectively, S_r is always turned on. The dc source is then idle, and the dc current i_{dc} always flows through the grid side. In State 3, switch S_0 is turned on and the decoupling capacitor C_d is discharged to release the ripple power. It can be found that S_r is used to control the energy transfer through determining that i_{dc} flows through the dc source or the grid. On the other hand, S_0 is used to control whether i_{dc} passes through the decoupling capacitor C_d to accomplish power decoupling. Note that only State 2 (charging C_d and discharging L_{dc}) or State 3 (discharging C_d and charging L_{dc}) is carried out during each switching period to reduce switching power losses.

III. CIRCUIT ANALYSIS AND CONTROL STRATEGY

A. CIRCUIT ANALYSIS

Assuming that i_{dc} is continuous and d_i is the duty ratio of state i. Therefore, the dc source current i_s and the output current i_i can be expressed as

$$i_s = (d_1 + d_2)i_{dc} = d_{12}i_{dc} \tag{1}$$

$$i_i = (d_3 + d_4)i_{dc} = d_{34}i_{dc} \tag{2}$$

The duty ratios satisfy

$$d_{12} + d_{34} = 1 \tag{3}$$

According to (1)-(3), the steady-state value of i_{dc} is expressed as follows,

$$i_{dc} = i_i + i_s \tag{4}$$

Accordingly, i_{dc} is determined by dc source current and the grid current. Ignoring the effects of the LC filter at the grid side, v_r and i_i can be expressed as

$$v_r = |v_g| = V\,|\cos(\omega t)| \tag{5}$$

$$i_i = |i_g| = I\,|\cos(\omega t)| \tag{6}$$

where V and ω, respectively, are the amplitude and the angular frequency of the grid voltage, and I is peak grid current. Considering that the power losses are ignored, we have

$$P_{ave} = P_d + v_r i_i = P_d + \frac{VI}{2}(1 + \cos(2\omega t)) \tag{7}$$

where P_{ave} is the average power of the system and P_d is the power buffered by the decoupling capacitor C_d. It is noted that, if $P_d > 0$, the decoupling capacitor is charged, and it is discharged if $P_d \leq 0$. In (7), the average power and ripple power can be, respectively, expressed as

$$\begin{cases} P_{ave} = V_s i_s = \frac{VI}{2} \\ P_d = -\frac{VI}{2}\cos(2\omega t) \end{cases} \tag{8}$$

According to (1) and (8), the voltage transfer ratio can be obtained as follows

$$\frac{V_s}{V} = \frac{I}{2i_{dc}}\frac{1}{d_{12}} \tag{9}$$

Compared to the one given in [30], i.e., I/($2i_{dc}$), the voltage transfer ratio of the proposed inverter has an extra boosting term 1/(d_{12}). Therefore, a much wider voltage conversion is achieved.

According to the voltage-second balance of dc inductor L_{dc}, the following equation is obtained.

$$\frac{V_s}{V} = \frac{I}{2i_{dc}}\frac{1}{d_{12}} \tag{10}$$

Combining (1), (2), and (10) yields

$$d_{23} = d_3 - d_2 = \frac{v_r i_i - V_s i_s}{v_d i_{dc}} = \frac{-P_d}{v_d i_{dc}} \tag{11}$$

According to previous analysis, States 2 and 3 are not carried out at the same time during each switching cycle. Therefore, d_2 or d_3 is zero at any time. According to (1)-(3) and (11), the duty ratio d_i can be obtained,

$$\begin{cases} d_1 = \begin{cases} d_{12}, & \text{when } d_{23} > 0 \\ d_{12} + d_{23}, & \text{when } d_{23} \leq 0 \end{cases} \\ d_2 = \begin{cases} 0, & \text{when } d_{23} > 0 \\ -d_{23}, & \text{when } d_{23} \leq 0 \end{cases} \\ d_3 = \begin{cases} d_{23}, & \text{when } d_{23} > 0 \\ 0, & \text{when } d_{23} \leq 0 \end{cases} \\ d_4 = \begin{cases} d_{34} - d_{23}, & \text{when } d_{23} > 0 \\ d_{34}, & \text{when } d_{23} \leq 0 \end{cases} \end{cases} \tag{12}$$

Supposing that the ripple power is buffered fully by the decoupling capacitor C_d, the decoupling capacitor voltage and current are

$$v_d = \sqrt{\bar{v}_d^2 - \frac{P_{ave}\sin(2\omega t)}{\omega C_d}} \tag{13}$$

$$i_d = \frac{P_d}{v_d} \tag{14}$$

where $\bar{v}_d$ is the dc component that is controllable. Finally, as shown in Fig. 4, the switching averaged circuit of the proposed inverter is obtained. It can be seen that an average voltage $d_{23}v_d$ provided by the decoupling circuit can be used to regulate the dc inductor current.

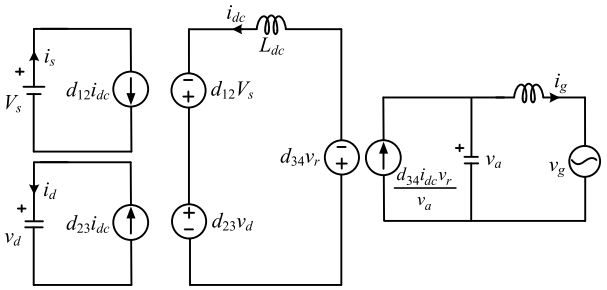


FIGURE 4. Equivalent circuit of the proposed inverter.

B. CONTROL STRATEGY

Fig. 5 shows the control block diagram of the proposed inverter. The required sampling signals include the grid voltage v_g, the decoupling capacitor voltage v_d, the dc source voltage V_s, and the dc inductor current i_{dc}. Three control aspects are identified: PFC, decoupling capacitor voltage control, and power control. This paper mainly aims to validate the fundamental operation of the proposed inverter, and thus the dc source current reference i_s^* is directly given in the power control. For practical applications such as in a PV system, i_s^* is obtained by employing a maximum power point tracking controller and a proportional-integral (PI) controller.

A dual closed-loop control method is adopted to achieve PFC and decoupling capacitor voltage control. The control principle is well-documented in [20], [28], and [31]–[34], and thus only a brief introduction of the adopted control method is given. Its control principle is that the given dc component of the decoupling capacitor voltage $\bar{v}_d$ can be maintained by modifying the magnitude of current reference I^*. As shown in Fig. 5, the dc component of the actual decoupling capacitor voltage is obtained by a moving average filter (MAF). To achieve zero steady-state error, a simple PI controller is used. The angular frequency of the grid voltage is obtained by a phase lock loop. Then output current reference i_i^* is obtained.

After obtaining i_s^* and i_i^*, the dc current reference i_{dc}^* can be calculated by modifying the variable d_{23}. The forward-feed term -P_d/($v_d i_{dc}$) is used to improve the system dynamic response and can be obtained according to Fig. 5. The dc inductor current is an indirect indicator of the decoupling performance. Once there exists the residual ripple power, it will be imposed on the dc inductor and cause current distorted. Therefore, we adopt a closed-loop control strategy for power decoupling. In contrast, in [30], the power decoupling is achieved by controlling the decoupling capacitor voltage to track its reference. It is an open loop control strategy, and the decoupling performance depends on the accuracy of the reference.

IV. COMPARISON

Table II gives a comparison between the inverters proposed in [30] and the one in this paper. The values in the brackets are obtained by using parameters in this paper and the dc

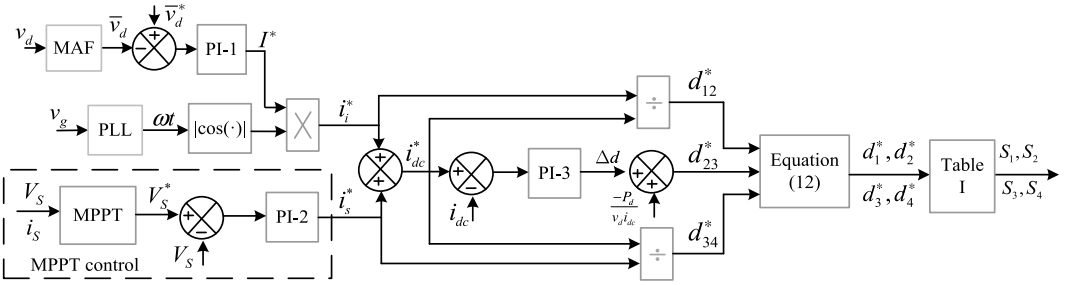


FIGURE 5. Control block diagram.

TABLE 2. Comparison between the proposed inverters in [30] and this paper.

	Inverter proposed in [30]		Inverter proposed in this paper		Comments: Proposed over [30]
	Theoretical value	Calculated value using parameters in this paper	Theoretical value	Calculated value using parameters in this paper	
Number of active and passive components	5 swiches+2 diodes+2 inductors+2 capacitors	—	5 swiches+2 diodes+2 inductors+2 capacitors	—	Same
Average voltage conversion ratio	$\frac{V_s}{V}=\frac{I}{2i_{dc}}$	0.45	$\frac{V_s}{V}=\frac{I}{2i_{dc}d_{12}}$	0.45	Larger
Decoupling capacitor voltage v_d (V)	$v_d=\sqrt{\overline{v}_d^2-\frac{P_{ave}\sin(2\omega t)}{\omega C_d}}$	$\sqrt{96721-31831\sin(2\omega t)}$	$v_d=\sqrt{\overline{v}_d^2-\frac{P_{ave}\sin(2\omega t)}{\omega C_d}}$	$\sqrt{96721-31831\sin(2\omega t)}$	Same
Minimum v_d (V)	V	155	$V+V_s$	225	Larger
Inductor current i_{dc} (A)	i_s	2.86	$i_s+\lvert i_g\rvert$	$2.86+2.58\lvert\cos(\omega t)\rvert$	Larger
Duty ratio S_0	$1-\frac{\lvert i_g\rvert+i_d}{i_s}$	$1-0.9\lvert\cos\ \omega t\rvert+\frac{69.93\cos\ 2\omega t}{\sqrt{96721-31831\sin(2\omega t)}}$	$1-\frac{\lvert i_g\rvert+i_d}{i_{dc}}$	$1-\frac{0.9\lvert cos\ \omega t\rvert-\frac{69.93\cos(2\omega t)}{\sqrt{96721-31831\sin(2\omega t)}}}{1+0.9\lvert cos\ \omega t\rvert}$	Larger
Duty ratio S_r	$\frac{\lvert i_g\rvert}{i_s}$	$0.9\lvert\cos(\omega t)\rvert$	$\frac{\lvert i_g\rvert}{i_{dc}}$	$\frac{0.9\lvert cos\ \omega t\rvert}{1+0.9\lvert cos\ \omega t\rvert}$	Smaller
Voltage rating D_0 (V)	v_d	358.54	v_d	358.54	Same
Voltage rating D_1 (V)	v_d-v_r	310.80	$v_d-v_r-V_s$	240.80	Smaller
Voltage rating S_0 (V)	v_d	358.54	v_d	358.54	Same
Voltage rating S_r (V)	v_d-v_r	310.80	$v_d-v_r-V_s$	240.80	Smaller
Average current D_0 (A)	$\frac{2I}{\pi}$	1.64	$\frac{2I}{\pi}$	1.64	Same
Average current D_1 (A)	$i_s-\frac{2I}{\pi}$	1.21	i_s	2.86	Larger
Average current S_0 (A)	$i_s-\frac{2I}{\pi}$	1.21	i_s	2.86	Larger
Average current S_r (A)	$\frac{2I}{\pi}$	1.64	$\frac{2I}{\pi}$	1.64	Same
RMS current D_0 (A)	$\sqrt{\frac{2Ii_s}{\pi}}$	2.17	$\sqrt{\frac{2Ii_s}{\pi}+\frac{I^2}{2}+\frac{1}{\pi}\int_{-\pi/2}^{\pi/2}\lvert i_g\rvert i_d d\omega t}$	2.77	Larger
RMS current D_1 (A)	$\sqrt{i_s^2-\frac{2Ii_s}{\pi}}$	1.86	i_s	2.86	Larger
RMS current S_0 (A)	$\sqrt{i_s^2-\frac{2Ii_s}{\pi}}$	1.86	$\sqrt{\frac{2Ii_s}{\pi}+i_s^2-\frac{1}{\pi}\int_{-\pi/2}^{\pi/2}\lvert i_g\rvert i_d d\omega t}$	3.63	Larger
RMS current S_r (A)	$\sqrt{\frac{2Ii_s}{\pi}}$	2.17	$\sqrt{\frac{2Ii_s}{\pi}+\frac{I^2}{2}}$	2.83	Larger

voltage is 70 V. It also provides a basis for the selection of the appropriate semiconductor devices. As seen, in both inverters, the same active and passive components are utilized. However, the circuit structures vary significantly, which leads to different circuit characteristics. The main differences are listed as follows:

(i) Because the amplitude of the grid current I must be less than dc inductor current i_{dc}, the circuit proposed in [30] has

a limited voltage conversion ratio. This limitation does not exist in the proposed one in this paper. Therefore, the proposed inverter is expected to have broader applications, which is deemed to be the chief merit compared to that in [30]. For examples, in PV applications, the proposed inverter can track maximum power point (MPP) over entire PV characteristics irrespective of the atmospheric conditions. While, the inverter in [30] can only track MPP in a region where the PV voltage is less than half the grid voltage. From this perspective, the proposed inverter can be a candidate for PV applications.

(ii) The formulations of the decoupling capacitor voltage v_d are the same. However, in this paper, the minimum value of v_d is lower-bounded by $(V_s + v_r)$ compared to that of v_r in [30]. Therefore, the voltage stress of the decoupling capacitor in this paper is more significant. However, as shown in Fig. 6, such difference is only tens of volts and is reduced with the increase of the system power.

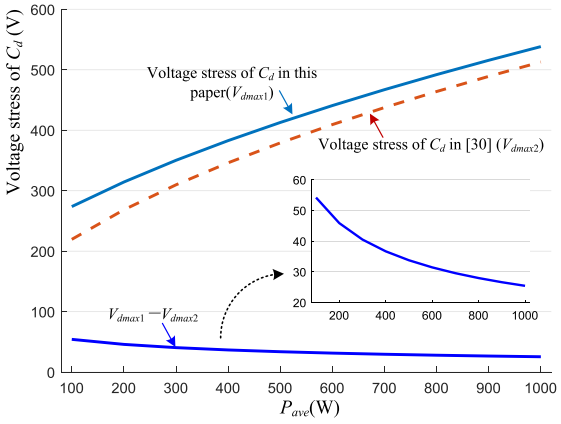


FIGURE 6. Voltage stresses of the decoupling capacitor in [30] and this paper with $V_s = 70$ V, $V = 156$ V, and $C_d = 20$ μF.

(iii) The dc inductor current i_{dc} in [30] is constant and equal to i_s. While, in this paper, the dc inductor current is time-variant and equal to $(i_s + |i_g|)$. It tends to increase the current stress of the dc inductor and switches, which potentially leads to higher power losses. This is the main compromise of the proposed inverter compared to that in [30].

V. EXPERIMENTAL RESULTS

A 200-W prototype is built to validate the previous theoretical analysis. The photo of the prototype is shown in Fig. 7. The control algorithm of the converter is realized by a universal control board which consists of a digital signal processor (DSP) TMS320F28335 [35] and a field programmable gate array (FPGA) EP2C8T144C8N [36]. DSP is used to accomplish the control process and outputs duty ratios to FPGA. FPGA is used to achieve the modulation and outputs switching driving signals. In this paper, a dc power supply is directly connected at the input for simplicity for that the primary purpose is to verify the operation principles. The circuit is designed for 110 V_{rms} ac-output, 100 V dc-input, and runs at $f_s = 20$ kHz. The semiconductors used are FCH072N60F

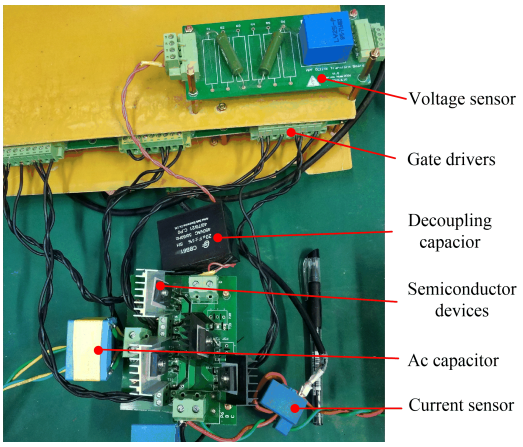


FIGURE 7. Photo of the prototype.

MOSFETs [37] and DSEI60-12A [38] diodes. As the constraints of the decoupling capacitor in [31] are identical to those in this paper, the same selection principle of C_d is adopted with C_d selected to be 20 μF. In practice, ceramic capacitors may be better choice for power decoupling [39]. Other specifications are given as follows. L_{dc} and L_g are 5 mH and 1 mH, respectively. The value of C_a is 10 μF. To account for the proper margin, the dc component of v_d is set to be 310 V. It is noted that the dc source current i_s is discontinuous and a low-pass filter is used to obtain its average value.

Fig. 8 shows the steady-state experimental results. As can be observed, the dc source voltage is 100 V, which is higher than half the peak grid voltage (78 V). The input current i_g is sinusoidal and in phase with the input voltage v_g. The PF is 0.99 and the total harmonic distortion is 4.3%. The grid current harmonics are in compliance with the requirement of IEC 61000-3-2 [40]. As seen, the dc source current i_s is flat with only minimal fluctuations because the ripple power is diverted to the decoupling capacitor C_d. Therefore, there exists a large fluctuation in the decoupling capacitor voltage v_d. The waveform of the inductor current i_{dc} is a sum of the dc source current i_s and the rectified grid current $|i_g|$ with 2 A minimum, which matches well with the theoretical analysis. Fig. 9 shows the experimental results when a 30 V and 70 V dc source voltage (less than half the peak grid voltage 78 V) is connected. As seen, the minimum of the dc inductor current is raised to 2.86 A (in Fig. 9(a)) and 6.67 A (in Fig. 9(b)). The decoupling capacitor voltage has the same fluctuation range (100 V) as that in Fig. 8(b) due to the same load power.

Fig. 10 shows the grid voltage, inductor current i_{dc}, and the gate-emitter voltages of the switches S_0 and S_2. As indicated by the switching patterns in Table I, the switch S_0 is always driven by a pulse width modulation (PWM) signal, and S_2 only works under positive half line cycle. Figs. 10(b) and (c) give the Zoom-in waveforms. In Fig. 10(b), the power absorbed by the grid is smaller than that provided by the dc

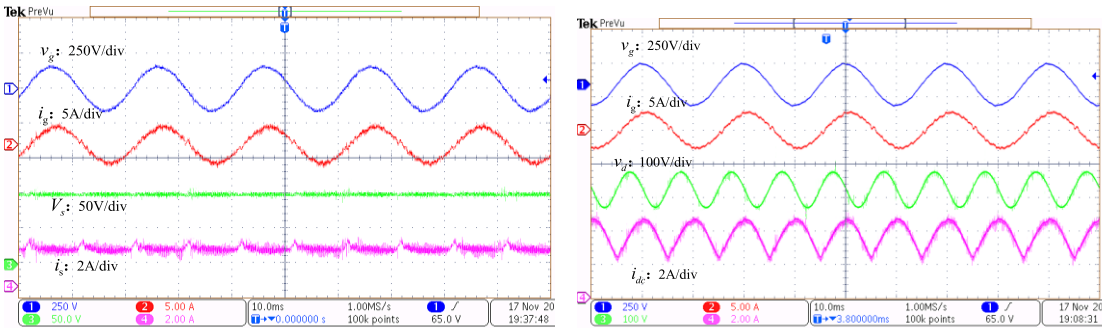


FIGURE 8. Steady-state experimental waveforms when 100V input voltage is connected. (a) Grid voltage v_g, grid current i_g, dc source voltage V_s, and dc source current i_s. (b) Grid voltage v_g, grid current i_g, decoupling capacitor voltage v_d, and inductor currents i_{dc}.

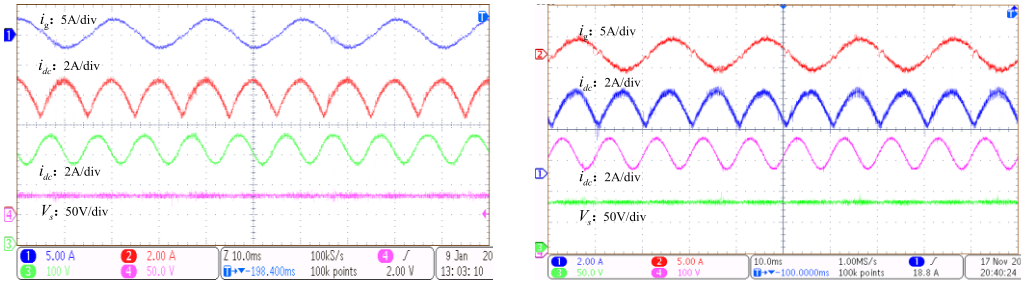


FIGURE 9. Steady-state experimental waveforms under lower dc voltage. (a) 30 V dc voltage. (b) 70 V dc voltage.

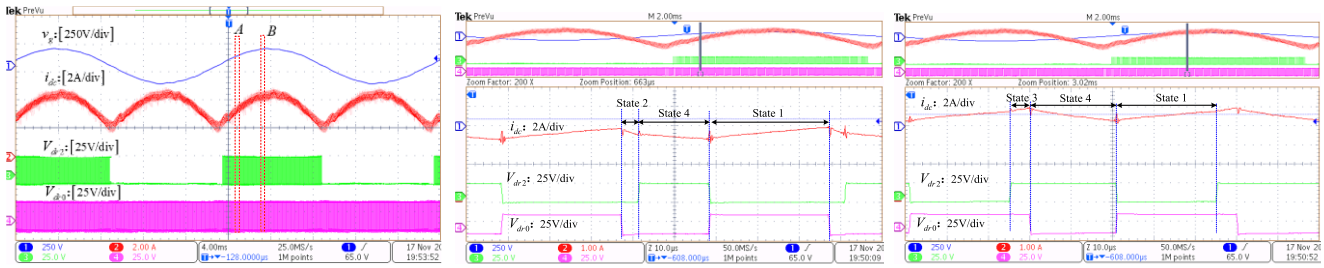
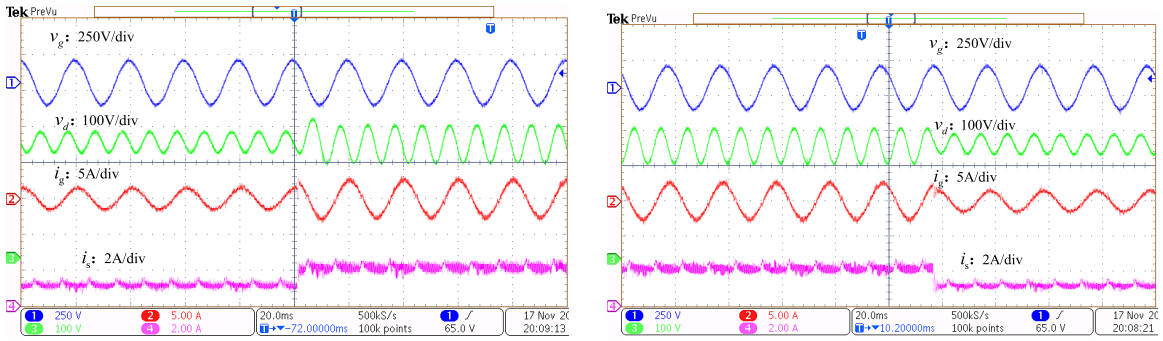


FIGURE 10. Experimental waveforms of the grid voltage, inductor currents i_{dc}, and gate-emitter voltages for switches S_0 and S_1 (V_{dr0} and V_{dr2}). (a) Overview. (b) Zoom-in waveforms of point A (charging C_d). (b) Zoom-in waveforms of point B (discharging C_d).

source such that the decoupling capacitor is charged. Therefore, switching State 3 is prevented such that the switching time and power losses are reduced. Within each switching cycle, the inductor is charged once and discharged twice. In Fig. 10(c), the power absorbed by the grid is observed to be larger than that provided by the dc source such that the decoupling capacitor is discharged. In this case, switching State 2 is not used, and the inductor is charged twice and discharged once within each switching cycle.

Fig. 11 shows the dynamic response of the system. In Fig. 11(a), the load is subjected to the step-up change from100 W to 200 W. As seen, the transient process is smooth and no obvious distortion is observed in the grid current. The fluctuation range of v_d increases accordingly due to the increased ripple power. Fig. 11(b) shows the opposite transient process.

Fig. 12 shows the variations of the efficiency and the grid current power factor (PF) as a function of the output power.



(a) (b)

FIGURE 11. Dynamic experimental waveforms. (a) Step-up load change from 100 W to 200 W. (b) Step-down load change from 200 W to 100 W.

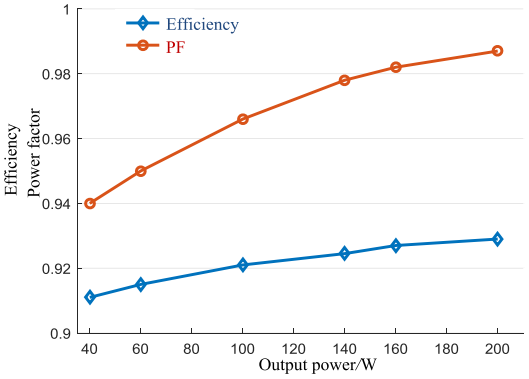


FIGURE 12. System efficiency and power factor of the proposed inverter.

Both efficiency and PF increase with increasing output power. The peak efficiency is 93.3% and the PF is 0.99 at the rated power. The PF is comparable to that in [30]. However, the efficiency is lower due to larger dc inductor current and decoupling capacitor voltage as mentioned before.

VI. CONCLUSION

This paper proposes a single-phase inverter by reconstructing an existing one. The obtained inverter inherits the advantages of the existing one, such as the single-stage power conversion, high power factor (0.99 at rated load power), and no electrolytic capacitors (E-cap-less structure) involved. In addition, the proposed inverter breaks the bottleneck of the limited input voltage range. With the adopted control method, a dedicated power-buffering controller is not needed, which simplifies the controller design. A laboratory prototype is built to verify the effectiveness of the theoretical analysis. The results indicate that the proposed inverter can potentially be applicable to volume-critical and lifetime-critical applications, especially when a wide input voltage range is required.

REFERENCES

[1] H. Hu, S. Harb, N. Kutkut, I. Batarseh, and Z. J. Shen, "A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2711–2726, Jun. 2013.

[2] G. R. Zhu, S. C. Tan, Y. Chen, and C. K. Tse, "Mitigation of low-frequency current ripple in fuel-cell inverter systems through waveform control," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 779–792, Feb. 2013.

[3] B. Lehman and A. J. Wilkins, "Designing to mitigate effects of flicker in LED lighting: Reducing risks to health and safety," *IEEE Power Electron. Mag.*, vol. 1, no. 3, pp. 18–26, Sep. 2014.

[4] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[5] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.

[6] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.

[7] J.-M. Kwon, E.-H. Kim, B.-H. Kwon, and K.-H. Nam, "High-efficiency fuel cell power conditioning system with input current ripple reduction," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 826–834, Mar. 2009.

[8] W. Wang and X. Ruan, "A modified reference of an intermediate bus capacitor voltage-based second-harmonic current reduction method for a standalone photovoltaic power system," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5562–5573, Aug. 2016.

[9] J. M. Galvez and M. Ordonez, "Swinging bus operation of inverters for fuel cell applications with small DC-link capacitance," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1064–1075, Feb. 2015.

[10] Y. Shi, B. Liu, and S. Duan, "Low-frequency input current ripple reduction based on load current feedforward in a two-stage single-phase inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7972–7985, Nov. 2016.

[11] N. Lu, S. Yang, and Y. Tang, "Ripple current reduction for fuel-cell-powered single-phase uninterruptible power supplies," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6607–6617, Aug. 2017.

[12] D. B. W. Abeywardana, B. Hredzak, and V. G. Agelidis, "A rule-based controller to mitigate DC-side second-order harmonic current in a single-phase boost inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1665–1679, Feb. 2015.

[13] I. Serban, "Power decoupling method for single-phase H-bridge inverters with no additional power electronics," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4805–4813, Aug. 2015.

[14] S. Li, G.-R. Zhu, S.-C. Tan, and S. Y. Hui, "Direct AC/DC rectifier with mitigated low-frequency ripple through inductor-current waveform control," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4336–4348, Aug. 2015.

[15] S. Huang, F. Tang, Z. Xin, Q. Xiao, and P. C. Loh, "Grid-current control of a differential boost inverter with hidden LCL filters," *IEEE Trans. Power. Electron.*, vol. 34, no. 1, pp. 889–903, Jan. 2019.

[16] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.

[17] X. Cao, Q.-C. Zhong, and W.-L. Ming, "Ripple eliminator to smooth DC-bus voltage and reduce the total capacitance required," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2224–2235, Apr. 2015.
[18] R. Wang *et al.*, "A high power density single-phase PWM rectifier with active ripple energy storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430–1443, May 2011.
[19] H. Han, Y. Liu, Y. Sun, M. Su, and W. Xiong, "Single-phase current source converter with power decoupling capability using a series-connected active buffer," *IET Power Electron.*, vol. 8, no. 5, pp. 700–707, May 2015.
[20] Y. Sun, Y. Liu, M. Su, X. Li, and J. Yang, "Active power decoupling method for single-phase current-source rectifier with no additional active switches," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5644–5654, Aug. 2016.
[21] Y. Liu and F. Z. Peng, "Real DC capacitor-less active capacitors," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2017, pp. 44–51.
[22] R. Chen, Y. Liu, and F. Z. Peng, "A solid state variable capacitor with minimum capacitor," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5035–5044, Jul. 2017.
[23] G. Yona and G. Weiss, "The virtual infinite capacitor," *Int. J. Control*, vol. 90, no. 1, pp. 78–89, Jan. 2017.
[24] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Highly reliable transformerless photovoltaic inverters with leakage current and pulsating power elimination," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 1016–1026, Feb. 2016.
[25] H. V. Nguyen, D.-H. Park, and D.-C. Lee, "Single-phase transformerless PV power conditioning systems with low leakage current and active power decoupling capability," *J. Power Electron.*, vol. 18, no. 4, pp. 997–1006, Jul. 2018.
[26] L. C. Breazeale and R. Ayyanar, "A photovoltaic array transformer-less inverter with film capacitors and silicon carbide transistors," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1297–1305, Mar. 2015.
[27] Y. Shi, B. Liu, and S. Duan, "Modelling, control and performance analysis of a single-stage single-phase inverter with reduced low-frequency input current ripple," *IET Power Electron.*, vol. 11, no. 6, pp. 1074–1082, May 2018.
[28] Y. Liu, Y. Sun, and M. Su, "Family of two-port switching networks with ripple power decoupling and output voltage step-up functions," *IET Power Electron.*, vol. 10, no. 10, pp. 1175–1182, Aug. 2017.
[29] Y. Ohnuma and J.-I. Itoh, "A novel single-phase buck PFC AC–DC converter with power decoupling capability using an active buffer," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1905–1914, May/Jun. 2014.
[30] Y. Ohnuma, K. Orikawa, and J.-I. Itoh, "A single-phase current-source PV inverter with power decoupling capability using an active buffer," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 531–538, Jan./Feb. 2015.
[31] S. Li, W. Qi, S.-C. Tan, and S. Y. R. Hui, "A single-stage two-switch PFC rectifier with wide output voltage range and automatic ac ripple power decoupling," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6971–6982, Sep. 2017.
[32] Y. Liu, Y. Sun, M. Su, M. Zhou, Q. Zhu, and X. Li, "A single-phase PFC rectifier with wide output voltage and low-frequency ripple power decoupling," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5076–5086, Jun. 2018.
[33] M. Mellincovsky, V. Yuhimenko, M. M. Peretz, and A. Kuperman, "Low-frequency DC-link ripple elimination in power converters with reduced capacitance by multiresonant direct voltage regulation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2015–2023, Mar. 2017.
[34] S. Li, S. W. Qi, S.-C. Tan, and S. Y. R. Hui, "Enhanced automatic-power-decoupling control method for single-phase AC-to-DC converters," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1816–1828, Feb. 2018.
[35] Texas Instruments, Dallas, TX, USA. *TMS320F28335*. Accessed: Jan. 1, 2019. [Online]. Available: http://www.ti.com/lit/ds/symlink/tms320f28335.pdf
[36] ALTERA, San Jose, CA, USA. *TMS320F28335*. Accessed: Jan. 1, 2019. [Online]. Available: https://pdf1.alldatasheet.com/datasheet-pdf/view/527249/ALTERA/EP2C8T144C8N.html
[37] Fairchild Semiconductor, San Jose, CA, USA. *FCH072N60F*. Accessed: Jan. 1, 2019. [Online]. Available: https://pdf1.alldatasheet.com/datasheet-pdf/view/572757/FAIRCHILD/FCH072N60F.html
[38] IXYS Corporation, Milpitas, CA, USA. *DSEI60-12A*. Accessed: Jan. 1, 2019. [Online]. Available: https://pdf1.alldatasheet.com/datasheet-pdf/view/99507/IXYS/DSEI60-12A.html
[39] C. B. Barth, T. Foulkes, I. Moon, Y. Lei, S. Qin, and R. C. N. Pilawa-Podgurski, "Experimental evaluation of capacitors for power buffering in single-phase power converters," *IEEE Trans. Power Electron.*, to be published, doi: 10.1109/TPEL.2018.2878825.
[40] *Electromagnetic Compatibility (EMC)—Part 3-2: Limits—Limits for Harmonic Current Emissions (Equipment Input Current Under ≤16 A Per Phase)*, Standard EN 61000-3-2, 2006.

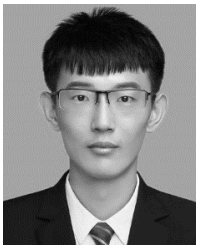
YONGLU LIU (S'16) was born in Chongqing, China, in 1989. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Central South University, Changsha, China, in 2012, 2015, and 2017, respectively, where he has been an Associate Professor with the School of Information Science and Engineering.

His research interests include power electronics and renewable energy power conversion systems.

MEI SU was born in Hunan, China, in 1967. She received the B.S. degree in automation and the M.S. and Ph.D. degrees in electric engineering from the School of Information Science and Engineering, Central South University, in 1989, 1992, and 2005, respectively, where she has been a Professor with the School of Information Science and Engineering, since 2006.

Her research interests include matrix converter, adjustable speed drives, and wind energy conversion systems.

Dr. Su is currently an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS.



FULIN LIU was born in Shandong, China, in 1994. He received the B.S. degree in electronic engineering from Central South University, Changsha, China, in 2016, where he is currently pursuing the M.S. degree.

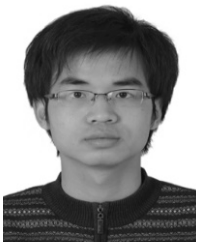
His research interests include matrix converter and dc/dc converters.

MINGHUI ZHENG received the B.E. and M.E. degrees from Beihang University, Beijing, China, in 2008, 2011, and 2017, respectively, and the Ph.D. degree in mechanical engineering from the University of California at Berkeley, Berkeley, CA, USA. She joined the University at Buffalo, in 2017, where she is currently an Assistant Professor in mechanical and aerospace engineering.

Her research interests include advanced learning, estimation, and control with applications to high-precision systems.

XIAO LIANG received the B.E. degree from Hunan University, Changsha, China, in 2010, and the M.S. and Ph.D. degrees from the University of California at Berkeley, Berkeley, CA, USA, in 2011 and 2016, respectively, all in civil engineering. He joined the Department of Civil, Structural and Environmental Engineering, University at Buffalo, in 2018.

His research interests include health monitoring and autonomous inspection of infrastructure systems through advanced data analytics, model-based and machine learning.



GUO XU received the B.S. degree in electrical engineering and automation and the Ph.D. degree from the Beijing Institute of Technology, Beijing, China, in 2012 and 2018, respectively. From 2016 to 2017, he was a Visiting Student with the Center for Power Electronics System, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA. Since 2018, he has been with the School of Information Science and Engineering, Central South University, Changsha, China, where he is currently an Associate Professor.

His research interests include modeling and control of power electronics converters, high-efficiency power conversion, and magnetic integration in power converters.

YAO SUN (M'13) was born in Hunan, China, in 1981. He received the B.S., M.S., and Ph.D. degrees from the School of Information Science and Engineering, Central South University, Changsha, China, in 2004, 2007, and 2010, respectively, where he has been an Associate Professor.

His research interests include matrix converter, micro-grid, and wind energy conversion systems.