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Low Leakage Current Symmetrical Dual-k 7 nm Trigate Bulk Underlap FinFET for Ultra Low Power Applications

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ABSTRACT The main purpose of this paper is to achieve as low as possible leakage current (I_{OFF}) to meet the requirements for ultra-low power (ULP) applications. The proposed methodology is based on studying the effect of the most effective FinFET design parameters that directly impact its leakage current. The parameters explored in this paper are the effective channel lengths L_{eff}, gate stacks, gate contact materials, and gate-sidewall spacers (L_{sp}). The results show that utilizing a symmetrical dual-k material for 7-nm underlap tri-gate FinFETs appreciably allows a sufficient ON current and low leakage current and hence low stand by power consumption. Specifically, the effect of spacer length L_{sp} and L_{HK} is investigated to get low leakage current keeping I_{ON}/I_{OFF} as high as possible. Moreover, the effective channel length in subthreshold conduction (L_{eff}) is maintained greater than the gate length (L_g) and the threshold voltage (V_{th}) is adjusted by the proper metal gate work function. The performance of the proposed n- and p-FinFET devices is verified using Sentaurus TCAD simulator from Synopsys. The resulted I_{OFF} is 17 pA/μ m for n-FinFET and 14.7 pA/μm for p-FinFET which are the lowest leakage currents found in recent publications. The achieved I_{ON}/I_{OFF} ratio for both proposed devices is found to be 12.3×10^6 and 11×10^6, respectively, which are comparable to the published data. These parameters are obtained for an appropriate choice of $L_{sp} = 10$ nm and $L_{HK} = 5$ nm. In addition, the short channel effects variations with L_{HK} have been investigated.

INDEX TERMS 7 nm Bulk FinFET, leakage current, SymD-k spacer, TCAD, ultra-low power.

I. INTRODUCTION

The driving force of electronic industry is to reach better performance with very high level of integration while keeping up with Moore's law [1]. As a result of scaling down the planner MOSFET, the static leakage power became one of the vital parameters for circuit design. FinFET is an attractive technology as it surpasses the Short Channel Effects (SCEs) and improves the power consumption [2]. It can replace the planer CMOS for technologies less than 32 nm [2]. In addition, FinFET shows a high device scalability and simple fabrication process [4]. According to ITRS 2.0 roadmap, the reduction of the FinFET device size is accompanied by a reduction in the supply voltage that can reach 0.75 V and 0.7 V for 10 nm and 7 nm respectively [5]. One of the approaches to reduce leakage current is the use of gate-source/drain underlap, but because it increases the series resistance R_{SD}, it will apparently decrease the driving current [6], [7]. Equating the fin width to the gate length can suppress the SCEs without affecting the driving current as found in [8]. In [9] a dual-k spacer is used to reduce the R_{SD} resistance for 14 nm FinFET devices as the field lines form gate to drain terminate at the edge of the high-k spacer and consequently the effective channel length is reduced. However, under weak inversion, the effective channel length is larger leading to a reduced leakage current [7]. The analog performance of dual-k underlap FinFET is considered in [10]. The results show that the dual-k spacer with underlap FinFET has an analog performance better than the conventional low-k FinFET. Asymmetric dual-k spacers and asymmetric drain

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extension are investigated for 14 nm technology in order to decrease the device leakage current and improve the on-off current ratio I_{on}/I_{off} [11].

This paper explores the effect of the key design parameters of 7 nm bulk Tri-gate underlap FinFET for ULP applications by adopting the symmetrical dual-k spacer. It examines the variation of high-k spacer length and its effect on the device I_{off}, I_{on}, and I_{on}/I_{off} ratio. The ON current is not of prime concern in this study since this work targets ULP applications. In addition, the proposed devices employ the high-k metal gate (HKMG) technology for the gate stack. The proposed p- and n- FinFET devices are designed and simulated using Sentaurus TCAD tools from Synopsys [12].

The geometrical parameters and doping profile for the proposed devices are introduced in section II. Section III presents the devices design methodology utilized for minimizing the leakage current. Section IV presents the simulation setup and discusses the simulation results. The conclusion of this paper is drawn in Section V.

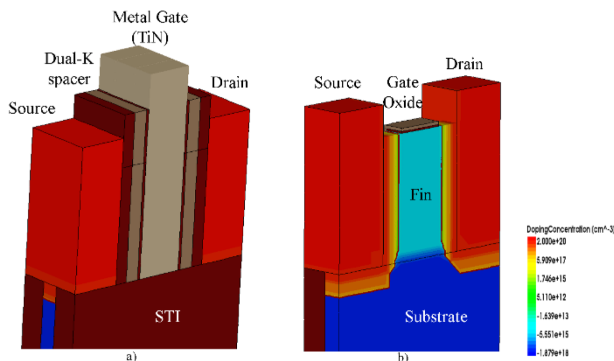

FIGURE 1. a) 3D view of the bulk FinFET tri-gate structure, b) 3D cross section without gate electrode and gate spacers.

II. PROPOSED TRI-GATE FINFET DEVICE

A 3D view of the proposed 7 nm bulk tri-gate FinFET structure is shown in Fig. 1. The main geometrical device parameters such as the physical gate length (L_g) and fin thickness (T_{fin}) are set to 16 nm and 6 nm respectively which follow the 8/7 nm technology node in the ITRS 2015 [5]. The fin height (H_{fin}) is 40 nm which is adopted from [13]. For the tri-gate FinFET the effective width (W_{eff}) is equal to ($2H_{fin} + T_{fin}$) and thus the W_{eff} of the proposed devices is set to 86 nm. The main geometrical device dimensions are illustrated in Fig. 2.

The channel region is kept lightly doped with 2×10^{15} cm^{-3} doping concentration for both n- and p-FinFETs. This concentration is chosen to reduce threshold voltage (Vth) variations due to random dopant fluctuations (RDF) [13]. Although, light doping gives rise to a huge benefit in minimizing the RDF effect, but on the other hand, it results on increasing the punch through current. As a result, heavy doping punch-through stopper (PTS) region is added at the base of the fin to alleviate the punch through current. This work proposes a PTS with a concentration of 1×10^{18} cm^{-3} to eliminate the undesired current. In addition, the

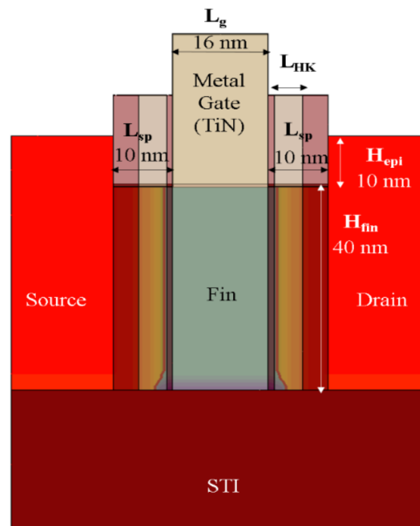

FIGURE 2. 2D view of the bulk FinFET tri-gate structure.

S/D extensions doping (S/D Ext.doping) has a gradient doping profile 2 nm/dec to control the effective channel length (L_{eff}) [13]. The device structure includes heavily doped raised source/drain (S/Ddoping) to reduce the S/D series resistance. The S/D height is 50 nm with raised height 10 nm (H_{epi}) above the fin [14]. The nominal design parameter values are summarized in Table 1 for n- and p-FinFETs. The gate work function (WF) is left tunable to be able to achieve the targeted leakage current for ultra-low power applications.

TABLE 1. 7 nm bulk FinFET design parameters.

Design parameter	NOMINAL VALUE
L_g(nm)	16
EOT (nm)	0.66
H_{fin}(nm)	40
T_{fin}(nm)	6
Fin_{doping}(cm^{-3})	2x10^{15}
S/D_{doping}(cm^{-3})	2x10^{20}
S/D doping grad. @ 2x10^{19} cm^{-3} (nm/dec)	2
L_{eff} N/P	27/28
L_{sp}	10

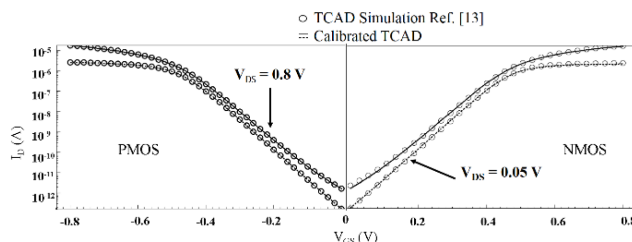

FIGURE 3. Calibrated TCAD I_D-V_{GS} characteristic curves versus Ref [13].

The TCAD tool is calibrated to the devices in [13] at 0.05 V and 0.8V. Figure 3 shows the I_D-V_{GS} characteristic curves for the calibrated devices verses those in [13]. Since the results are comparable, the calibrated TCAD devices are utilized.

III. DESIGN METHODOLOGY, SIMULATION RESULTS AND DISCUSSION

The leakage current range of ULP varies from 10 pA/μm to 50 pA/μm [14]. In order to reach this range and hence maximize the I_{on}/I_{off} ratio, the key design parameters that affect the device power consumption are studied. In this study, the targeted I_{off} is achieved by carefully adjusting the main device effective parameters. The parameters investigated in this paper are the effective channel length (L_{eff}), the gate-sidewall spacers (L_{sp}), the gate-dielectric stack, and the gate stack materials.

A. EFFECT OF INNER HK SPACER LENGTH

It is well known that the series resistance value increases as the underlap length increases resulting in a degradation of I_{on}. In order to improve I_{on}, high-k material is utilized in the spacer region. According to [15], materials with k greater than 20 will improve I_{on} by enhancing the gate fringe induced barrier lowering (GFIBL). The proposed devices adopt the symmetrical dual-k spacers made of Hafnium dioxide (HfO_2) as a high-k spacer (k = 22) and Silicon dioxide (SiO_2) as a low-k spacer (k = 3.9). HfO_2 is known to be highly compatible with silicon process technology when compared to other high-k materials [16]. The effect of varying the high-k spacer length (L_{HK}) on I_{on}, I_{off} and I_{on}/I_{off} ratio will be investigated for both the n- and p-FinFETs.

The inner spacer length L_{HK} is varied from 3 to 7 nm for two different spacer lengths of 8 and 10 nm with a fixed underlap length (L_u) equals to 4 nm. Sidewall SiO_2 of length 1 nm is necessary to comply with the gate-last technology steps [8] and consequently its length is subtracted from the total L_{sp}. When $L_{HK} = 7$ nm the device with $L_{sp} = 8$ nm will act as a single high-k spacer device, while at $L_{sp} = 10$ nm the device will act as SymD-k device. The simulation results in Fig. 4 present the effect of varying L_{HK} on I_{on}, I_{off} and I_{on}/I_{off} ratio at $V_{GS} = V_{DS} = 0.7$ V for the ON state and $V_{GS} = 0$ V and $V_{DS} = 0.7$ V for the OFF state. Figure 4a shows that I_{on} is slightly increasing with L_{HK}, while it is inversely dependent on L_{sp}. The reduction of I_{on} with spacer length is clearly attributed to the increase in the series resistance. To explain the effect of L_{HK} we refer to the simplified top-view figure in the following section. When the HK spacer covers all the underlap area or slightly larger area into the low-doping D/S edge regions, the gate electrostatic fringe coupling strongly modulates the carrier density in the covered area and a slight enhancement in I_{on} is obtained. The highest I_{on} is clearly obtainable when the entire extension region is covered by a single HK as in case of 8 nm spacer ($L_{HK} = 7$ nm). This situation is not reachable for the 10 nm spacer. This explains the missing of the steep change in I_{on} for 10 nm spacer when compared to the 8 nm one at $L_{HK} = 7$ nm (Fig. 4a). In summary, the longer the HK spacer the higher the channel charge density in the underlap area and part of the S/D low-doping edge causing a higher I_{on}.

I_{off} simulation results for both devices are shown in Fig. 4b. The enhancement in leakage in the subthreshold region can

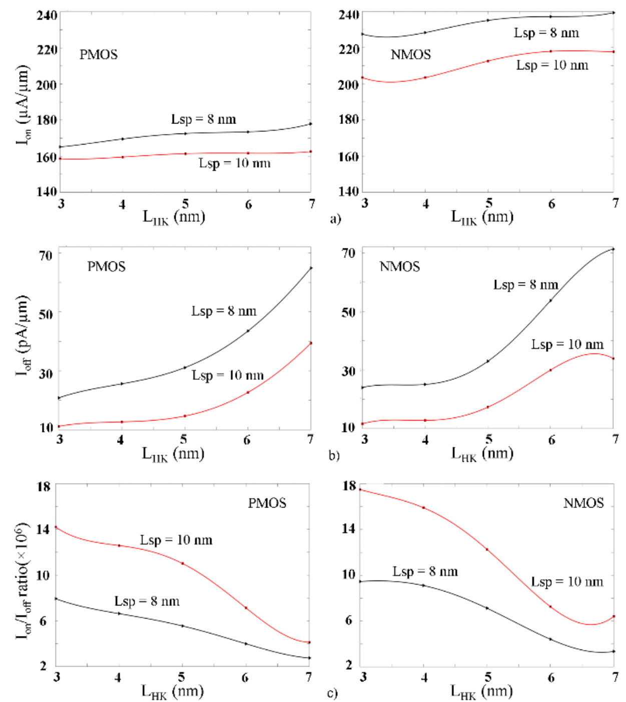

FIGURE 4. L_{HK} variation effect on a) I_{on}, b) I_{off} and c) I_{on}/I_{off} ratio for n- and p-FinFETs.

be explained by the fact that the device behaves like a bipolar transistor in the OFF state where the current is exponentially dependent on the source-fin voltage. This driving voltage is increased for high coupling fringe capacitance between the gate and the source. At zero gate voltage, the drain-induced barrier lowering (DIBL) allows the injection of carriers from the source into the fin, resulting in increased leakage current.

The I_{on}/I_{off} ratio is inversely proportional to L_{HK}, due to the rapid increase in I_{off} especially beyond L_{HK} of 5 nm. Fig.4b shows that I_{off} is equal to 17 pA/μm for NMOS and 14.7 pA/μm for PMOS at $L_{sp} = 10$ nm and $L_{HK} = 5$ nm. The 10 nm spacer is chosen as our working design because of its lower leakage current as compared to the 8 nm spacer. As can be observed in Fig. 4c at 10 nm spacer, the I_{on}/I_{off} ratio degrades rapidly beyond $L_{HK} = 5$ nm.

The effect of varying L_{HK} on the devices DIBL and the subthreshold swing (SS) is presented in Fig. 5 for the 10 nm spacer device ($L_{sp} = 10$ nm). At $L_{HK} = 5$ nm, the DIBL is found to be 40 mV/V and 39.5 mV/V for the p- and n-FinFETs respectively (Fig. 5a), while SS equals 69.4 mV/dec for the p-FinFET and 69.8 mV/dec for the n-FinFET. The observed increase in these SCE parameters as well as in I_{off} is likely attributed to the increased interface states between the HK dielectric and the fin extension.

B. EFFECTIVE CHANNEL LENGTH

The effective channel length (L_{eff}) is a key parameter that affects the device performance. It is defined as the lateral distance between two points where the S/D dopant falls

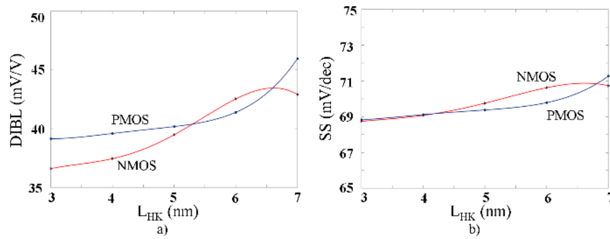

FIGURE 5. L_{HK} **variation effect on a) DIBL, b) SS for p and n- FinFETs.**

to a certain doping level [13]. At this concentration level, the inverse slope of the doping profile equals 2 nm/decade of concentration variation and is referred to as the S/D edge doping gradient [13]. The device effective channel length has a direct impact on the device characteristics, since it is the main parameters causing SCEs while directly affecting the channel resistance [17].

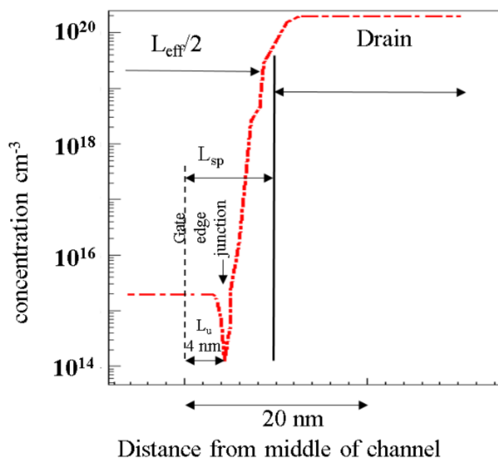

FIGURE 6. Dopant profile along half the symmetrical device showing L_{eff} **and** L_u**.**

L_{eff} is measured at S/D doping concentration of 2×10^{19} cm^{-3} as can be seen from Fig. 6. illustrating the doping profile along half of the n-device as in Fig. 7. The measured values are 27 nm and 28 nm for the designed n- and p-FinFETs, respectively. As mentioned above, the S/D edge doping gradient is set to 2 nm/ dec to get a sufficiently low parasitic S/D series resistance [8], [13]. In order to reduce the band-to-band tunneling (BTBT) in the p-FinFET, which can increase the off-state leakage current, the L_{eff} of p-FinFET has to be slightly larger than the n FinFET [13]. This makes the drain region slightly far away from the gate and hence the field causing the BTBT becomes weaker.

C. GATE STACK AND CONTACT MATERIAL

The gate leakage current increases due to the continuous thinning of the gate-oxide thickness that can reach few atomic layers. This leakage is influenced by the probability of charge tunneling through the gate oxide. Increasing the gate oxide thickness will decrease the gate leakage current at the expense

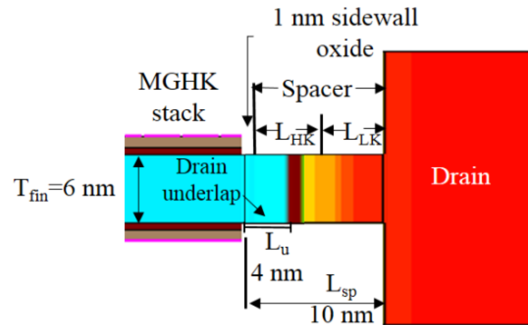

FIGURE 7. Simplified half-transistor top-view showing the D/S extension, underlap and spacer regions.

of the device performance as the I_{on} value will deteriorate. In order to preserve the electric oxide thickness a high-k material and metal gate (HKMG) technology is utilized.

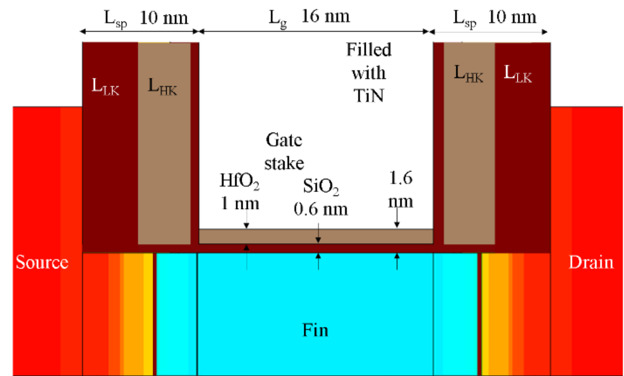

FIGURE 8. Proposed gate-stack.

The proposed gate stack is formed starting with the low-k material SiO_2 with 0.6 nm thickness at the silicon interface followed by HfO_2 with 1 nm thickness as shown in Fig. 8. The equivalent oxide thickness (EOT) of the proposed devices in the gate-stack is equal to 0.66 nm. Metal gate is utilized to enhance the carrier mobility. It reduces the electron scattering by screening the surface phonons caused by the high-k material [18]–[20]. Titanium Nitride (TiN) is used as a metal gate in the proposed devices. In order to control I_{off} and V_{th}, the metal gate work function (WF) is adjusted around the mid-gap value of 4.6 eV. To achieve the targeted I_{off} value, the WF is tuned to 4.59 eV and 4.66 eV for the n- and p-channel devices.

IV. COMPARISON WITH PUBLISHED WORK

3D device simulation using Sentaurus tools [21] is performed for the proposed FinFET devices to extract the I-V characteristics. In the simulation, for carrier transport the drift-diffusion models are used as recommended by [22] and [23]. The carriers mobility is calculated by Philips unified mobility model [24]. The density gradient quantization model is included to define the 2D and 3D quantization effects [21]. The Thin-layer mobility model is used in conjunction with inversion and accumulation layers mobility model [25]

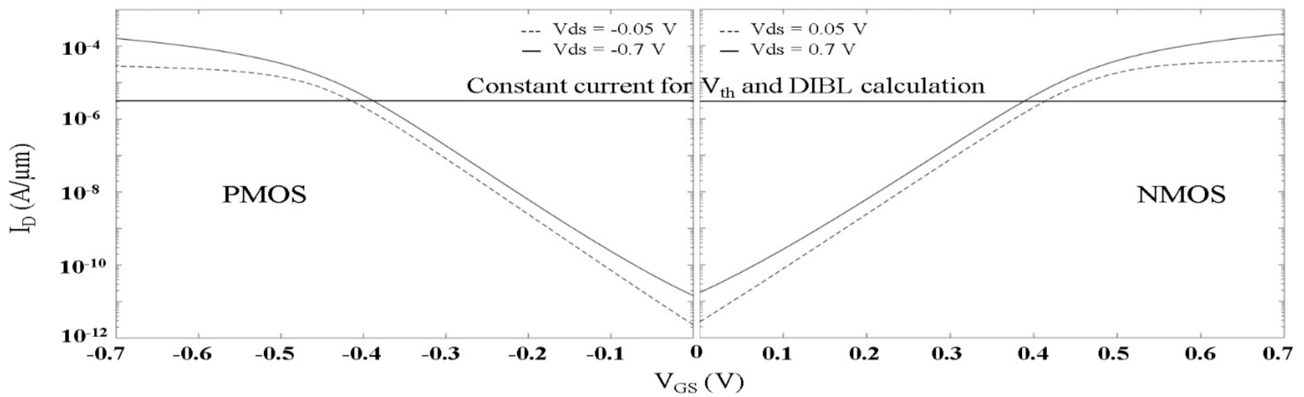

FIGURE 9. I_d vs V_{gs} for a) n-channel b) p-channel FinFETs.

TABLE 2. Devices performance comparison.

Technology	*This work* 7 nm bulk FinFET		[13] 7 nm bulk FinFET		[31] 7 nm SOI FinFET	
Design parameter	*n-FinFET*	*p-FinFET*	*n-FinFET*	*p-FinFET*	*n-FinFET*	*p-FinFET*
L_g (nm)	16	16	15	15	15	15
EOT (nm)	0.66	0.66	0.64	0.64	0.64	0.64
H_{fin} (nm)	40	40	40	40	40	40
T_{fin} (nm)	6	6	8	8	8	8
Channel doping (cm^{-3})	$2x10^{15}$	$2x10^{15}$	$2x10^{15}$	$2x10^{15}$	$2x10^{15}$	$2x10^{15}$
S/D doping (peak) (cm^{-3})	$2x10^{20}$	$2x10^{20}$	$2x10^{20}$	$2x10^{20}$	$2x10^{20}$	$2x10^{20}$
S/D Ext. doping (cm^{-3})	$2x10^{19}$	$2x10^{19}$	$2x10^{19}$	$2x10^{19}$	$2x10^{19}$	$2x10^{19}$
S/D Doping Gradient (nm/dec)	2	2	2	2	2	2
L_{eff} (nm)	27	28	26	28	24	27
Performance parameter	*n-FinFET*	*p-FinFET*	*n-FinFET*	*p-FinFET*	*n-FinFET*	*p-FinFET*
V_{DD} (V)	0.7	-0.7	0.8	0.8	0.8	0.8
V_{dslin} (V)	0.05	-0.05	0.05	0.05	0.05	0.05
V_{thsat} (mV)	388	-390	250	-258	248	-253
V_{thlin} (mV)	413	-418	279	-281	278	-276
I_{off} (pA/μm)	17	14.7	30	30	30	30
I_{on}/I_{off} ratio	$12.3 x10^6$	$11 x10^6$	$9.2 x10^6$	$8.5 x10^6$	$9.5 x10^6$	$8.7 x10^6$
SS (mV/dec)	69.8	69.4	69	67	68	66
DIBL (mV/V)	39.5	40	40	31	40	30
WF (eV)	4.59	4.66	4.57	4.64	4.58	4.64

because, at very thin thickness, the quantum-mechanical effects have significant impact on low-field mobility [26] which must be taken into consideration. The bandgap narrowing model, the band-to-band tunneling Hurkx model and Auger recombination model are also included [21]. The threshold voltages extracted based on the constant current method [27]–[30]. Fig. 9 shows the transfer characteristics under linear and saturation regimes. Table 2 summarizes the obtained results.

A comparison between the proposed FinFET devices and recently published 7 nm FinFET devices in [13] and [31] is summarized in Table 2. The table compares the design technology parameters (geometrical and doping profile) as well as performance parameters. The device simulation is performed using the same TCAD tool with the same type of models enabled. The comparison focuses on I_{off} and I_{on}/I_{off} ratio since we are targeting low power operation, all currents are normalized by W_{eff}.

As can be observed from Table 2 the leakage current in this research is almost half those in [13] and [31] for both n- and p-FinFETs. This can be attributed to the higher WF and the larger L_{sp}. The proposed devices also have higher V_{th}, which gives an advantage in reducing the leakage current and the overall device power consumption.

The proposed n-FinFET device enhanced the I_{on}/I_{off} ratio by 34% when compared to [13] and by 30% when compared to [31]. For the p-FinFET device, the current ratio is enhanced by 29 % and 26% as compared to [13] and [31] respectively. As for the SS and DIBL, the proposed devices show comparable results. Consequently, our 7 nm devices have appropriate characteristics for ULP applications.

V. CONCLUSION

The aim of this paper is to design a SymD-k 7 nm tri-gate underlap bulk n- and p-FinFET devices with a low leakage current suitable for ULP applications. It is well known that the leakage current is the main contributor for the static power consumption.

The reduction in the leakage current is achieved by adjusting the spacer length L_{sp}, subthreshold L_{eff}, WF and the gate stack materials in order to reach as low as possible I_{off} while the I_{on}/I_{off} ratio is enhanced. It is observed that L_{sp} of 10 nm and L_{HK} = 5 nm is a condition after which the leakage current and SCEs rapidly deteriorate.

The subthreshold L_{eff} of the n- and p-FinFET devices are around 27 nm. HKMG technology is utilized with gate stack consisting of 1 nm HfO_2 and 0.6 nm SiO_2 and TiN as a metal gate. The resulted EOT is 0.66 nm for both devices. The TCAD simulations showed that the I_{off} for the n- and p-FinFET are 17 pA/μm and 14.7 pA/μm respectively. When compared to recently published studies for bulk 7nm node, the proposed adjustment of the devices' key parameters resulted in 43.3% and 51% reduction in I_{off} values for the n- and p-FinFETs respectively. In addition, I_{on}/I_{off} ratio increased by 34% for the n-FinFET and 29% for the p-FinFET. Finally, the two SCE parameters SS and DIBL are found to be almost equal to those published. Beyond L_{HK} = 5nm, a rapid rate of increase in theses parameters is obtained. Again, this puts a limit to the largest useable L_{HK} of 5 nm. It is concluded that the proposed devices meet the requirements of the ULP application.

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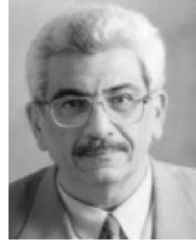

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