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A Novel Multi-Attractor Period Multi-Scroll Chaotic Integrated Circuit Based on CMOS Wide Adjustable CCCII

XIN ZHANG AND CHUNHUA WANG

College of Computer Science and Electronic Engineering, Hunan University, Changsha 410082, China

Corresponding author: Chunhua Wang (wch1227164@hnu.edu.cn)

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ABSTRACT This paper proposes a multi-attractor period multi-scroll chaotic system and a second-generation current-controlled current conveyor (CCCII) with a wide tunable range of intrinsic resistance. The newly proposed multi-attractor period multi-scroll chaotic system is constructed by this CCCII. The proposed chaotic system can generate single-attractor period, double-attractor period, three-attractor period, and even more attractor period multi-scroll. The four-dimensional state equation of the chaotic system contains four nonlinear functions for generating multi-attractor period multi-scroll chaos. Since the intrinsic resistance of the CCCII can be adjusted by external voltages or currents, the multi-attractor period multi-scroll chaotic integrated circuit based on the proposed CCCII have a tunable characteristic. It is worth noting that a chaotic integrated circuit has been implemented completely using current signals instead of voltage signals, and more interestingly, it does not contain any passive resistor. The dynamic characteristics of the multi-attractor period multi-scroll chaotic system are given. The circuit designs of the CMOS CCCII and the corresponding chaotic circuit are made in detail. We conduct the numerical and circuit simulations of the proposed chaotic system and the integrated circuit implementation of the chaotic circuit based on the CMOS CCCII. The correctness of the CCCII circuit and the chaotic system are proved through hardware experiments. The comparison between the implementation scheme of the chaotic circuit in this paper and several reported chaotic circuits is conducted.

INDEX TERMS Chaotic integrated circuit, CMOS CCCII, current mode, intrinsic resistance-tunable, multi-attractor period, multi-scroll, passive resistor.

I. INTRODUCTION

Chaos has important applications in secure communication [1], data encryption [2] and biomedicine [3], and so on. Chaos can be divided into single-scroll [4], double-scroll [5], multi-scroll [6], and multi-wing [7] chaotic systems, depending on the number and shape of these chaotic systems' attractors [8]. Compared with single-scroll and double-scroll chaotic systems, multi-scroll and multi-wing chaotic systems possess more complex dynamic characteristics. The data encryption systems and communication systems made up of these kind of systems would have better confidentiality [9]. The state equations of multi-wing chaotic systems contain product term of state variables, which need to be realized by analog multipliers [10]. However, analog multipliers are not only complex in circuit structure, but also have large nonlinear distortion, which can easily affect the stability of chaotic attractors. The state equations of multi-scroll chaotic systems do not contain product term of state variables, such that the corresponding chaotic circuits possess simple structure and favorable stability.

As time goes by, increasingly various complex chaotic systems have been discovered. The chaotic system with hidden attractors was first found and analyzed in [11]. The chaotic systems with no-equilibrium, only stable equilibrium and or a line of equilibriums can be defined as chaotic system with hidden attractors [12], [13]. Reference [14] designed a switching controller to realize the recombination of the attractors between different chaotic systems [15]. If different attractors of a chaotic system can be obtained by setting different initial values without changing any other parameters, and then the chaotic system can be called chaotic system with coexistence attractors [16]. The coexistence phenomenon in chaotic systems can also be called as multistability [17], and if the numbers of coexisting attractors tend to be infinite, it is known as extreme multistability [18], [19]. There are quite a few other types of complex chaotic systems have recently

been proposed. As an example, a multi-scroll hyperchaotic system with coexistence of multiple attractors was realized by introducing a time delay into Jerk system [20]. Besides, there are a host of other chaotic systems, the equilibrium points of them arranged in various shapes [21], [22], and so on.

If the attractors of multi-scroll chaotic systems are arranged in periodic form and their periods appear as single, double and three attractors, then we respectively call these systems single-attractor period, double-attractor period, and three-attractor period multi-scroll chaotic systems. According to the foregoing definition, as of now, in addition to a few multi-double-scroll chaotic systems [23], [24], the majority multi-scroll chaotic systems proposed in existing literatures can be called single-attractor period multi-scroll chaotic system. Namely, the attractors of these chaotic systems arranged in periodic form, and their periods behave as single attractor. In this paper, we will propose a multi-scroll chaotic system with multi-attractor period; that is, there are multiple attractors within one period. Compared with single-attractor period chaotic systems, the multi-attractor period chaotic system proposed in this paper can possible effectively improve the system dynamics complexity and may be better applied to secure communication.

Most of the chaotic circuits are realized so far based on operational amplifiers (OA) [25], [26]. Operational amplifier belongs to voltage mode circuit, and it has two problems in the realization of chaotic circuits [27], [28]. The one is that it has a relatively small dynamic range, therefore, when the sizes of the scrolls are certain, there are fewer scrolls that can be realized; the second is the low working frequency, and the center frequency of the multi-scroll chaotic circuit realized based on OA is low. Current mode devices such as current feedback operational amplifiers (CFOA) and current conveyors (CCII) have developed rapidly due to their high dynamic range and high working frequency in recent years [29], [30]. Compared with traditional voltage mode circuits, the current mode circuits, which are composed of current mode devices, have the advantages of simple circuit structure, low power consumption and high working frequency [31], [32].

The chaotic circuits based on CFOA or CCII have been reported in quite a few literatures [33], [34]. The multi-scroll attractors generated by the chaotic circuits based on CFOA or CCII have the advantages of large number of scrolls and high center frequency, when the sizes of the scrolls are certain. But CFOA and CCII still have two problems when used to realize chaotic circuits. Firstly, since CCII and CFOA do not possess electronic tunable characteristics, the chaotic integrated circuits based on CCII or CFOA are not convenient for adjusting once they are fabricated. Therefore, it only makes sense that using CFOA or CCII realize chaotic circuits with discrete components. Chaos phenomenon can be observed by adjusting passive variable resistors when chaotic circuits are implemented by discrete components. However, when integrated, the passive resistors cannot be adjusted. Consequently, the realizations of multi-scroll chaotic integrated circuits based on CFOA or CCII are of little significance. Meanwhile, the volumes of the chaotic circuits implemented by discrete components are too large to convenient applied to the encryption of mobile communication equipments, which require smaller and smaller volume. Secondly, the chaotic circuits composed of CFOA or CCII require passive resistors, but the deviation values of the integrated passive resistors are large, that makes the chaotic circuits which can generate chaos in the original theory and simulation may not to generate chaos after chip fabrication.

The CCCII [35] is a current mode device developed on the basis of CCII, which can overcome the deficiencies of CFOA and CCII devices in the aspect of lacking electronic tunability. The intrinsic resistance of CCCII can be adjusted by external bias, thus, the chaotic integrated circuits based on CCCII can be adjusted by external bias current or voltage. However, the CCCII circuits reported in the existing literatures have some problems such as narrow input dynamic range, narrow adjust range of X-terminal intrinsic resistance, and tuning the intrinsic resistance would affect the dynamic range of the CCCII [36], [37]. This paper proposes a new CMOS CCCII circuit, it not only has wide input dynamic range and wide adjustable range of intrinsic resistance, but also does not affect its input dynamic range when adjusting the intrinsic resistance.

In this paper, we propose a novel multi-attractor period multi-scroll chaotic system and a new low-voltage high-linearity wide intrinsic resistance-tunable CMOS CCCII. On this basis, we use the proposed CMOS CCCII circuit to realize the multi-attractor period multi-scroll chaotic system. In this way, the chaos phenomenon of integrated chaos chip can be expediently adjusted by external bias current or voltage.

The rest of this paper is structured as follows: In Section II, the state equation of the novel multi-attractor period multi-scroll chaotic system is introduced and the dynamic behaviors of the system are analyzed. In Section III, the new high performance intrinsic resistance-tunable CMOS CCCII is proposed, and we analyzed it theoretically. In Section IV, we introduced the circuit implementation scheme of the multi-attractor period multi-scroll chaotic system based on CCCII. The simulation and experiment results are listed in Section V. Finally, Section VI concludes our work.

II. THE MULTI-ATTRACTOR PERIOD MULTI-SCROLL CHAOTIC SYSTEM

A. SYSTEM STATE EQUATION AND NUMERICAL SIMULATION IN MATLAB

The state equation of the new multi-attractor period multi-scroll chaotic system is listed in (1):

$$\begin{cases} dx/dt = a[w - f_4(w)] \\ dy/dt = bw + c[x - f_1(x)] \\ dz/dt = dw - e[z - f_3(z)] \\ dw/dt = -hw - m[y - f_2(y)], \end{cases} \tag{1}$$

where $a, b, c, d, e, h,$ and m are constant coefficients of the state equation, $x, y, z,$ and w are state variables of the chaotic system.

In system (1), the three nonlinear functions, $f_1(x), f_2(y)$, and $f_3(z)$, determine whether the system generates multi-scroll chaotic attractors in the directions of $x, y,$ and z, $f_4(w)$ is the key to determine whether the system can generate multi-attractor period chaos. The four nonlinear functions in (1) are selected as the saturation function sequences, their expressions can be selected as:

$$f_a(u) = \frac{\xi_u}{2q}\sum_{m=-M}^{M}\{|u-2m\xi_u+q|-|u-2m\xi_u-q|\}, \quad (2)$$

$$f_b(u) = \frac{\xi_u}{2q}\sum_{n=-N,n\neq 0}^{N}\left\{\left|u-\xi_u\left(2n-\frac{|n|}{n}\right)+q\right| - \left|u-\xi_u\left(2n-\frac{|n|}{n}\right)-q\right|\right\}, \quad (3)$$

where $u \in \{x, y, z, w\}$, $\xi_u \in \{\xi_x, \xi_y, \xi_z, \xi_w\}$, q is the control parameter of $f_a(u)$ and $f_b(u)$, M is a nonnegative integer, N is a positive integer. System (1) combined with (2) or (3) can generate even or odd number of scrolls in the corresponding direction.

The distribution of the equilibrium points in $x-y$ phase plane is used to illustrate the relation between $f_4(w)$ and $f_1(x), f_2(y), f_3(z)$. In system (1), making $a=2, b=c=e=h=m=1, d=1.5, dx/dt=dy/dt=dz/dt=dw/dt=0, f_1(x)\neq 0, f_2(y)\neq 0, f_3(z)\neq 0, f_4(w)=0$, the equilibrium points of the system can be obtained by the following expressions:

$$f_1\left(x_i^E\right)=x_i^E, \quad f_2\left(y_i^E\right)=y_i^E, \; f_3\left(z_i^E\right)=z_i^E, \; w_i^E=0. \quad (4)$$

In system (1), $f_1(x)$, $f_2(y)$, and $f_3(z)$ are chosen as $f_b(u)$ in (3), and $f_4(w)=0$. In which, the parameters of $f_1(x), f_2(y)$, and $f_3(z)$ are $\xi_x=\xi_y=\xi_z=0.1, N=1, q=0.01$. Therefore, the numerical expressions of these nonlinear functions are

$$\begin{cases} f_i(u) = 5\sum\limits_{n=-1,n\neq 0}^{1}\left\{\left|u-0.1\left(2n-\frac{|n|}{n}\right)+0.01\right| - \left|u-0.1\left(2n-\frac{|n|}{n}\right)-0.01\right|\right\} \\ f_4(w)=0, \end{cases} \quad (5)$$

where $f_i(u) \in \{f_1(x), f_2(y), f_3(z)\}$, $u \in \{x, y, z\}$.

Combining (5), system (1) can generate single-attractor period $3\times 3\times 3$ scroll chaos, the chaotic phase portraits are shown in Fig.1. Fig.4(a) shows the corresponding equilibrium distribution of the 3×3 scroll chaotic attractors in $x-y$ phase plane. The black dot "$\bullet$" in Fig.4 denotes the saddle-foci with index 2. According to (4) and (5), the corresponding numerical values of the $3\times 3\times 3$ equilibrium points $\left(x_i^E, y_i^E, z_i^E, w_i^E\right)$ are $x_i^E \in \{0, \pm 0.2\}$, $y_i^E \in \{0, \pm 0.2\}$, $z_i^E \in \{0, \pm 0.2\}$, and $w_i^E = 0$.

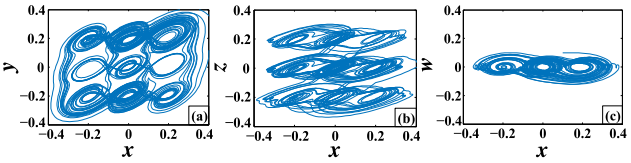

FIGURE 1. Single-attractor period $3\times 3\times 3$ scroll chaotic phase portraits. (a) $x-y$ plane projection; (b) $x-z$ plane projection; (c) $x-w$ plane projection.

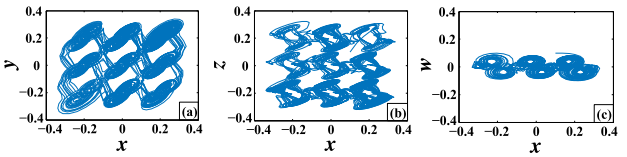

FIGURE 2. Double-attractor period $3\times 3\times 3$ scroll chaotic phase portraits. (a) $x-y$ plane projection; (b) $x-z$ plane projection; (c) $x-w$ plane projection.

In system (1), making $a=2, b=c=e=h=m=1, d=1.5, dx/dt=dy/dt=dz/dt=dw/dt=0, f_1(x)\neq 0, f_2(y)\neq 0, f_3(z)\neq 0, f_4(w)\neq 0$, the equilibrium points of the system can be obtained by the following expressions:

$$f_1\left(x_i^E\right)=x_i^E+w_i^E, \quad f_2\left(y_i^E\right)=y_i^E+w_i^E, \quad f_3\left(z_i^E\right)=z_i^E-1.5w_i^E, \quad f_4\left(w_i^E\right)=w_i^E. \quad (6)$$

On this occasion, $f_1(x)$, $f_2(y)$, and $f_3(z)$ are selected as $f_b(u)$ in (3), and $f_4(w)$ is selected as $f_a(u)$ in (2). In which, the parameters of $f_1(x)$, $f_2(y)$, and $f_3(z)$ are $\xi_x=\xi_y=\xi_z=0.1, N=1, q=0.01$, the parameters of $f_4(w)$ are $\xi_w=0.04, M=0, q=0.01$. Accordingly, we can get the numerical expressions of these nonlinear functions:

$$\begin{cases} f_i(u) = 5\sum\limits_{n=-1,n\neq 0}^{1}\left\{\left|u-0.1\left(2n-\frac{|n|}{n}\right)+0.01\right| - \left|u-0.1\left(2n-\frac{|n|}{n}\right)-0.01\right|\right\} \\ f_4(w)=2\{|u+0.01|-|u-0.01|\}, \end{cases} \quad (7)$$

where $f_i(u) \in \{f_1(x), f_2(y), f_3(z)\}$, $u \in \{x, y, z\}$.

Combining (7), system (1) can generate double-attractor period $3\times 3\times 3$ scroll chaos, the chaotic phase portraits are shown in Fig.2. The corresponding equilibrium distribution of the 3×3 scroll chaotic attractors in $x-y$ phase plane is shown in Fig.4(b). According to (6) and (7), the corresponding numerical values of $2\times(3\times 3\times 3)$ (denotes double-attractor period) equilibrium points $\left(x_i^E, y_i^E, z_i^E, w_i^E\right)$ are $x_i^E \in \{\pm 0.04, \pm(0.2\pm 0.04)\}$, $y_i^E \in \{\pm 0.04, \pm(0.2\pm 0.04)\}$, $z_i^E \in \{-1.5\times(\pm 0.04), \pm[0.2-1.5\times(\pm 0.04)]\}$, and $w_i^E \in \{\pm 0.04\}$. In Fig.4(a), the 9 equilibrium points correspond to 9 regions, in which the green region is the one that we use to illustrate the transformation of the corresponding equilibrium points from single-attractor period to multi-attractor period. By introducing the nonlinear function $f_4(w)$ that shown in (7), the single equilibrium point in all 9 regions in Fig.4(a) becomes the double equilibrium points in the corresponding regions in Fig.4(b). Therefore, this implies that

the nonlinear function $f_4(w)$ is the key to determine whether the multi-attractor period can be generated.

Similarly, the nonlinear functions $f_1(x)$, $f_2(y)$, and $f_3(z)$ are kept the same as those in (7), $f_4(w)$ is selected as $f_b(u)$ in (3), and the parameters of $f_4(w)$ are $\xi_w = 0.025, N = 1$, $q = 0.01$. The corresponding numerical expression of $f_4(w)$ is

$$f_4(w) = 1.25 \sum_{n=-1,n\neq 0}^{1} \left\{ \left| w - 0.1\left(2n - \frac{|n|}{n}\right) + 0.01 \right| - \left| w - 0.1\left(2n - \frac{|n|}{n}\right) - 0.01 \right| \right\}. \quad (8)$$

In consequence, system (1) can generate three-attractor period $3 \times 3 \times 3$ scroll chaos, the chaotic phase portraits are shown in Fig.3. Fig.4(c) shows the corresponding equilibrium distribution of the 3×3 scroll chaotic attractors in $x-y$ phase plane, and the equilibrium points in 9 corresponding regions are increased to three. The corresponding numerical values of $3 \times (3 \times 3 \times 3)$ (denotes three-attractor period) equilibrium points $\left(x_i^E, y_i^E, z_i^E, w_i^E\right)$ are $x_i^E \in \{0, \pm 0.05, \pm 0.2, \pm(0.2 \pm 0.05)\}$, $y_i^E \in \{0, \pm 0.05, \pm 0.2, \pm(0.2 \pm 0.05)\}$, $z_i^E \in \{0, -1.5 \times (\pm 0.05), \pm 0.2, \pm[0.2 - 1.5 \times (\pm 0.05)]\}$, and $w_i^E \in \{0, \pm 0.05\}$.

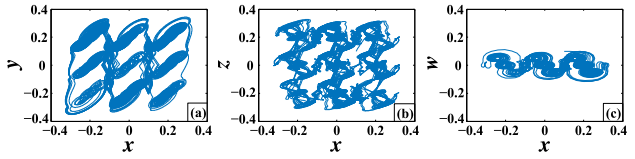

FIGURE 3. Three-attractor period 3 × 3 × 3 scroll chaotic phase portraits. (a) $x-y$ plane projection; (b) $x-z$ plane projection; (c) $x-w$ plane projection.

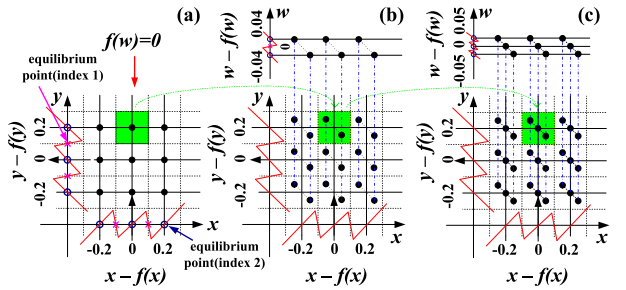

FIGURE 4. Equilibrium distribution of the n-attractor period 3 × 3 scroll in $x-y$ phase plane ($n = 1, 2, 3$). (a) Single-attractor period; (b) double-attractor period; (c) three-attractor period.

The arrows in Fig.4 is indicative of that if the multi-scroll chaotic system are transformed from single-attractor period to double-attractor period or three-attractor period, the equilibrium points in the same region will be changed from one to two or three. It is obvious that $f_4(w)$ is the key factor for generating multi-attractor period from single-attractor period, and $f_1(x)$, $f_2(y)$, $f_3(z)$ determine the number and size of the scrolls in the corresponding direction. Therefore, through the combination of different nonlinear functions, the system (1) can realize multi-attractor period multi-scroll chaos, and it is easy to expand.

B. DYNAMIC BEHAVIOR ANALYSIS

Let us analyze the general situation of system (1), which does not include nonlinear functions $f_1(x)$, $f_2(y)$, $f_3(z)$, and $f_4(w)$, so as to find the primary equilibrium point. Rewriting (1) into a matrix form(nonlinear functions are not included):

$$\begin{pmatrix} \dot{x} \\ \dot{y} \\ \dot{z} \\ \dot{w} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & a \\ c & 0 & 0 & b \\ 0 & 0 & -e & d \\ 0 & -m & 0 & -h \end{pmatrix} \cdot \begin{pmatrix} x \\ y \\ z \\ w \end{pmatrix} = J \cdot \begin{pmatrix} x \\ y \\ z \\ w \end{pmatrix}, \quad (9)$$

where J is the coefficient matrix(here equal to Jacobi matrix) of (9). If appropriate system parameters are selected to make J a nonsingular matrix, (9) has a unique equilibrium point $E^O(0, 0, 0, 0)$. In this case, the characteristic polynomial of (9) at equilibrium point E^O is

$$\lambda^4 + A\lambda^3 + B\lambda^2 + C\lambda + D = 0. \quad (10)$$

Assume that $\lambda_1, \lambda_2, \lambda_3$, and λ_4 are the four eigenvalue roots of (10), the following expressions can be obtained through the coefficient comparison and the *Vieta theorem*:

$$\begin{cases} \lambda_1 + \lambda_2 + \lambda_3 + \lambda_4 = -A = -(e+h) \\ \lambda_1\lambda_2 + \lambda_1\lambda_3 + \lambda_1\lambda_4 + \lambda_2\lambda_3 + \lambda_2\lambda_4 + \lambda_3\lambda_4 = B = (bm + eh) \\ \lambda_1\lambda_2\lambda_3 + \lambda_1\lambda_2\lambda_4 + \lambda_1\lambda_3\lambda_4 + \lambda_2\lambda_3\lambda_4 = -C = -(acm + bem) \\ \lambda_1\lambda_2\lambda_3\lambda_4 = D = acem. \end{cases} \quad (11)$$

According to the *Descartesformula*, the four roots of (10) are respectively

$$\begin{cases} \lambda_1 = \dfrac{-k_0 + \sqrt{k_0^2 - 4t_0}}{2} - \dfrac{A}{4} = \sigma_1 + j\omega_1 \\ \lambda_2 = \dfrac{-k_0 - \sqrt{k_0^2 - 4t_0}}{2} - \dfrac{A}{4} = \sigma_2 + j\omega_2 \\ \lambda_3 = \dfrac{k_0 + \sqrt{k_0^2 - 4\tau_0}}{2} - \dfrac{A}{4} = \sigma_3 + j\omega_3 \\ \lambda_4 = \dfrac{k_0 - \sqrt{k_0^2 - 4\tau_0}}{2} - \dfrac{A}{4} = \sigma_4 + j\omega_4, \end{cases} \quad (12)$$

where $k_0 = \{[-u/2 + (v^2/4 + u^3/27)^{1/2}]^{1/3} + [-u/2 - (v^2/4 + u^3/27)^{1/2}]^{1/3} - 2p/3\}^{1/2}$, $t_0 = (k_0^3 + pk_0 - q)/2k_0 (k_0 \neq 0)$, $\tau_0 = (k_0^3 + pk_0 + q)/2k_0 (k_0 \neq 0)$, $u = -(p^2 + 12r)/3$, $v = (27pr - 2p^3 - 27q^2)/27$, $p = (8B - 3A^2)/8$, $q = (A^3 + 4AB + 8C)/8$, $r = (16AB^2 - 3A^4 - 64AC + 256D)/256$.

In (12), if the characteristic roots meet the following conditions: $\sigma_1 < 0, \omega_1 = 0, \sigma_2 \neq \sigma_1 < 0, \omega_2 = 0, \sigma_3 = \sigma_4 > 0$, $\omega_3 = -\omega_4$, and $|\sigma_3/\sigma_1| < 1$ or $|\sigma_2/\sigma_1| < 1$, then the equilibrium point E^O of system (9) is a saddle-focus point with index 2. Letting $a = 2, b = c = e = h = m = 1$,

$d = 1.5$, then $A = (e + h) = 2, B = (bm + eh) = 2$, $C = (acm + bem) = 3, D = acem = 2$. The values of characteristic roots are $\lambda_1 = -1, \lambda_2 = -1.3532, \lambda_{3,4} = 0.1766 \pm 1.2028j$, which are calculated from (12). Therefore, these characteristic roots meet the chaotic decision condition of *Shilnikov inequalities*.

System (1) is naturally symmetric under the coordinates transform (x, y, z, w) to $(-x, -y, -z, -w)$. By using this property, it is easy to extend the saddle-foci with index 2 by constructing multi-piecewise functions with odd symmetry. The system (1) is dissipative by calculating $\nabla \cdot V = \partial\dot{x}/\partial x + \partial\dot{y}/\partial y + \partial\dot{z}/\partial z + \partial\dot{w}/\partial w = -e - h = -2 < 0$.

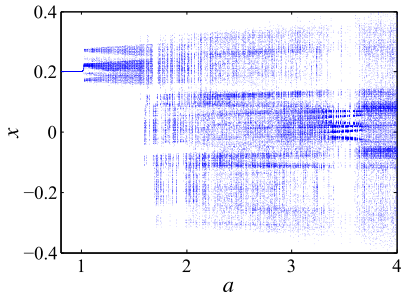

FIGURE 5. Bifurcation diagram of variable *x* regarding parameter *a*.

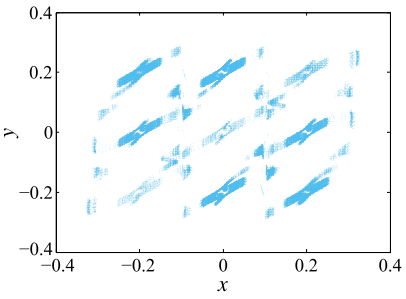

FIGURE 6. *Poincare* map in $x - y$ plane with $w = 0$.

In order to further verify the existence of chaos in system (1), we have simulated and analyzed some other characteristics of the three-attractor period $3 \times 3 \times 3$ scroll chaotic system. The bifurcation diagram of the state variable x regarding parameter a and the *Poincare* map diagram in plane $x - y$ with $w = 0$ are respectively shown in Fig.5 and Fig.6. Fig.5 shows that the value of the coefficient a in the range of 0-4 determines whether the system is chaotic. If appropriate value of coefficient a is selected, such as $2 < a < 4$, the system will enter chaotic state. As can be seen from Fig.6, the *Poincare* map of the system in plane $x - y$ with $w = 0$ has a number of dense points, and it is very similar to Fig.3(a), which proves the characteristics of bifurcation and foldability that chaos possesses. Fig.7 shows the Lyapunov exponent (LE) spectrum regarding parameter a. When $a = 2$, the Lyapunov exponents are respectively $LE1 = 0.1504, LE2 = 0, LE3 = -0.9674, LE4 = -1.142$. Therefore, in this case, the system is once again proved to be chaotic.

Fig.8 shows the time-domain dynamic simulation for all state variables. The motion state of each state variable can

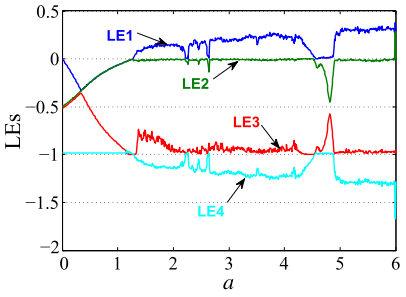

FIGURE 7. Lyapunov exponent (LE) spectrum regarding parameter *a*.

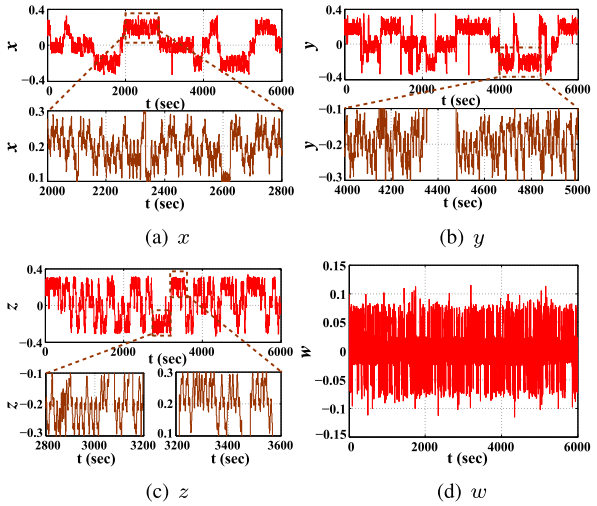

FIGURE 8. Time-domain waveform diagrams with simulation time t = 6000. (a) $x - t$; (b) $y - t$; (c) $z - t$; (d) $w - t$.

be clearly seen from these time-domain waveform diagrams. The local time-domain waveforms of the state variables x, y, and z marked with dotted box are also enlarged and displayed in Fig.8. Therefore, the three-attractor periodic behaviors in every local enlarged time-domain waveform diagram can be seen.

Through the above rigorous simulation analyses, it is proved that the proposed system has the basic characteristics of chaos, and its phase portraits show a new form of chaotic attractor.

III. LOW-VOLTAGE HIGH-LINEARITY WIDE INTRINSIC RESISTANCE-TUNABLE CCCII

Compared with voltage mode devices, current mode devices possess better performance in speed, bandwidth and dynamic range, and so on. We will implement the chaotic system proposed above based on a current mode device CCCII. However, the dynamic input range of the existing CCCII circuits are not wide enough, and the adjustable range of internal parasitic resistance is too narrow. Consequently, it is arduous to realize the proposed chaotic system based on the existing CCCIIs. To overcome this problem, a new high performance CCCII with wide range of intrinsic resistance-adjustable and wide dynamic input range will be designed in this section.

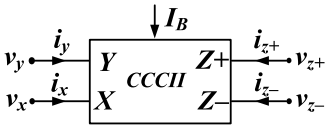

FIGURE 9. Circuit symbol of elementary CCCII.

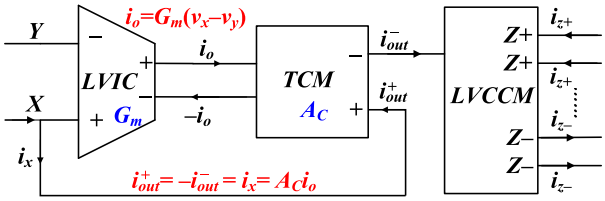

FIGURE 10. The implementation scheme of the new CMOS CCCII.

A. BASIC PRINCIPLE OF CCCII CIRCUIT

Fig.9 is the circuit symbol of elementary CCCII. I_B is external bias current, Y and X are respectively voltage and current input terminal, $Z+$ and $Z-$ are respectively plus and minus current output terminal. The port relations of CCCII could be characterized by the following matrix [35]:

$$\begin{pmatrix} i_y \\ v_x \\ i_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & R_X & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \cdot \begin{pmatrix} v_y \\ i_x \\ v_z \end{pmatrix}, \tag{13}$$

where R_X is the intrinsic resistance of CCCII.

B. IMPLEMENTATION SCHEME OF THE NOVEL CMOS CCCII

Fig.10 is the implementation scheme of the new CMOS CCCII. This CMOS CCCII is composed of linear voltage-current convertor (LVIC), tunable current mirror (TCM), and low voltage cascade current mirrors (LVCCM).

The following expressions can be obtained according to the scheme shown in Fig.10:

$$i_x = i_{out}^+ = A_C i_o = A_C G_m \left(v_x - v_y\right), \tag{14}$$
$$R_X = \left(v_x - v_y\right)/i_x = 1/A_C G_m, \tag{15}$$
$$i_{z+} = -i_{z-} = i_x, \tag{16}$$

where G_m is the linear transconductance gain of the LVIC, A_C is the current gain of the TCM.

According to (13)-(16), and only if the input current of Y-terminal of the LVIC is zero, the implementation scheme in Fig.10 will conform to the port characteristics of CCCII. Next we analyze step by step to verify the correctness of the proposed scheme.

1) LINEAR V-I CONVERTOR

Fig.11 is the internal core circuit structure of the proposed linear $V-I$ convertor. M_1-M_3, M_4-M_6 are respectively two linear $V-I$ convertor units [38], and the symmetrical structure is used to improve the linear dynamic range. The output current i_a is equal to the sum of the drain currents of M_2 and M_4, and the output current i_b is equal to the sum of

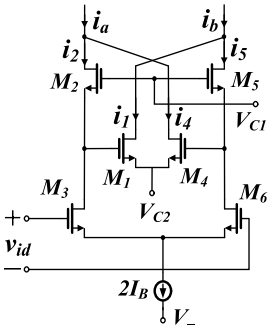

FIGURE 11. Internal core circuit structure of the linear $V-I$ convertor.

the drain currents of M_1 and M_5. M_3 and M_6 make up basic source coupling differential input, and they are biased with constant tail current $2I_B$ to improve common-mode rejection ability. V_{C1} and V_{C2} are bias voltages.

To facilitate calculation, suppose that the six NMOS transistors in the circuit have the same K(transconductance parameter of MOSFET) and V_{th}(threshold voltage) parameter values. Then, one has

$$i_a = i_2 + i_4, \tag{17}$$
$$i_b = i_1 + i_5. \tag{18}$$

Make the difference of i_a and i_b as the output current:

$$i_o = i_a - i_b = (i_2 - i_1) - (i_5 - i_4). \tag{19}$$

v_{id} is the differential input voltage that can form two gate-source voltages v_{gs3} and v_{gs6}, and these two voltages are equal and opposite:

$$v_{gs3} = -v_{gs6} = v_{id}/2. \tag{20}$$

Refering to [38] and further analyzing the circuit shown in Fig.11, we can get

$$i_o = 2K\left(V_{C1} - V_{C2} - 2V_{thn}\right) v_{id}, \tag{21}$$

where $K = (W/L) \cdot \left(\mu C_{ox}/2\right)$ and V_{thn} are the transconductance parameter and threshold voltage of the NMOS transistor, respectively. In the expression of the transconductance parameter, μ, C_{ox}, W, and L are the mobility, oxide capacitance per unit area, and channel width and length, respectively.

Equation (21) can also be written as $i_o = G_m v_{id}$, where G_m is transconductance gain of the LVIC and $G_m = 2K\left(V_{C1} - V_{C2} - 2V_{thn}\right)$. Therefore, the output current i_o has a favorable linear relationship with the input voltage v_{id}, and the transconductance gain G_m of this circuit can be adjusted by V_{C1} and V_{C2}. The linear input range of the circuit shown in Fig.11 can be calculated as

$$-\sqrt{2I_B/K} \le v_{id} \le \sqrt{2I_B/K}. \tag{22}$$

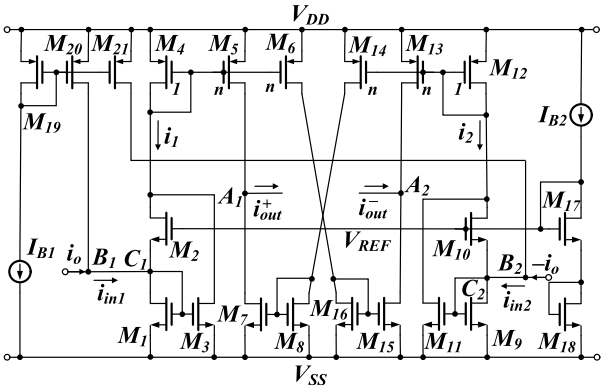

FIGURE 12. Circuit structure of the tunable current mirror (TCM).

2) TUNABLE CURRENT MIRROR

Fig.12 is the internal circuit structure of the tunable current mirror(TCM) [39]. All MOS transistors are biased in saturation region to satisfy the square rate characteristic. M_1-M_3 and M_9-M_{11} are respectively two current-squaring circuits [38]. The current-controlled bias circuit consists of M_{17}, M_{18}, and the current source I_{B2} to provide bias voltage for M_2 and M_{10}. M_4-M_6 and $M_{12}-M_{14}$ are double output current mirrors with current gain n. Assume that the differential current signals i_o and $-i_o$ flow in from points B_1 and B_2, respectively. Accordingly, the current signals flowing into points C_1 and C_2 are respectively $i_{in1} = I_{B1} + i_o$ and $i_{in1} = I_{B1} - i_o$.

The two current signals i_1 and i_2 of the two current-squaring circuits can be, respectively, expressed as [38], [39]

$$i_1 = 2I_{B2} + (I_{B1} + i_o)^2 \Big/ 8I_{B2}, \tag{23}$$

$$i_1 = 2I_{B2} + (I_{B1} - i_o)^2 \Big/ 8I_{B2}. \tag{24}$$

For keeping all MOSFETs in the on state, the condition $|I_{B1}| + |i_o| \le 4I_{B2}$ must be satisfied. A_C is the current gain of the tunable current mirror and it can be expressed as

$$A_C = nI_{B1} \Big/ 2I_{B2}. \tag{25}$$

The output current at points A_1 and A_2 can be calculated as

$$i_{out}^{+} = -i_{out}^{-} = n\,(i_1 - i_2) = \left(nI_{B1} \Big/ 2I_{B2}\right) i_o = A_C i_o. \tag{26}$$

As can be seen from (26), the output current i_{out} can be electronically tuned by the external DC currents I_{B1} and I_{B2}. The parameter n is the current gain of the two double output current mirrors. The gain of traditional current mirror is determined by a single bias current, whereas the gain of the tunable current mirror in this paper can be determined by the ratio of two bias currents. Compared with the adjustment of a single bias current, the ratio adjustment range of two bias currents is obviously much larger.

3) LOW-VOLTAGE CASCADE CURRENT MIRROR WITH BANDWIDTH COMPENSATION

Since the above TCM is mainly composed of basic current mirror circuits, such that the tracking error would be caused due to the mismatch between the transistors. This kind of tracking error can be effectively reduced by introducing the LVCCM mentioned below.

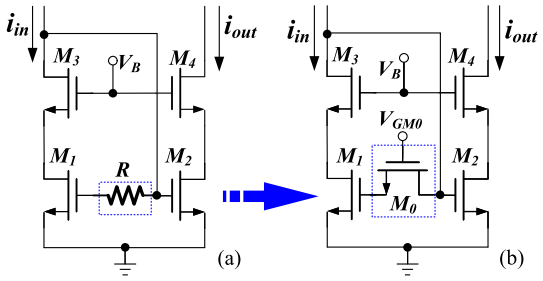

FIGURE 13. LVCCM with bandwidth compensation. (a) Passive resistor compensation; (b) Active resistor compensation.

Two kinds of resistor compensating circuit of LVCCM for achieving a high bandwidth are shown in Fig.13, in which, Fig.13(a) and Fig.13(b) are passive and active resistor compensating LVCCM, respectively. Neglecting the parasitic capacitances and conductances of the input and output, and making small-signal analysis for the circuit, one can yield the following transfer function and angular frequency [40]:

$$H(S) = \begin{cases} \dfrac{A}{2} \cdot \dfrac{1}{S^2 + S(\frac{g_{m1}}{C_1} + \frac{g_{m2}}{C_2}) - \frac{A}{2}}, & R = 0 \\ A \cdot \dfrac{S + 1/RC_1}{B}, & R \neq 0 \\ A \cdot \dfrac{1}{S^2 + S(\frac{2g_{m1}C_2 + g_{m2}C_1}{C_1C_2}) - A}, & R = \dfrac{1}{g_{m1}}, \end{cases} \tag{27}$$

$$\omega_0 = \begin{cases} \sqrt{g_{m1}g_{m2}/2C_1C_2}, & R = 0 \\ \sqrt{g_{m1}g_{m2}/C_1C_2}, & R = 1/g_{m1}, \end{cases} \tag{28}$$

where $A = -g_{m1}g_{m2}/C_1C_2$, $B = S^3 + S^2(g_{m1}/C_1 + g_{m2}/C_2 + 2/C_1R) + S(2g_{m1}/C_1^2R + 2g_{m2}/C_1C_2R) - A/R$. $C_1 = C_{GS1} = C_{GS2}$, $C_2 = C_{GS3} = C_{GS4}$, $g_{m1} = G_{m1} = G_{m2}$, $g_{m2} = G_{m3} = G_{m4}$.C_{GSi} and $G_{mi}(i = 1, 2, 3, 4)$ are respectively the gate-source capacitance and tansconductance of the corresponding transistor.

As can be seen from (27), the transfer function contains only two poles when no compensation resistors exist ($R = 0$), and it adds a zero and a pole when compensation resistor is include($R \neq 0$). Consequently, the zero of the transfer function can cancel out a major pole by appropriately choosing a resistor value, namely $R = 1/g_{m1}$. It can be seen from (28) that if $R = 1/g_{m1}$, the bandwidth of LVCCM is significantly improved compared with $R = 0$.

In CMOS process, passive resistor is usually doped poly or well resistor, which will occupy a relatively large chip area. Moreover, the fabrication of passive resistor in chip will produce a large temperature and process deviation [41]. The drawback of a passive resistor can be compensated by using a MOS transistor that acts as an active resistor (biased in

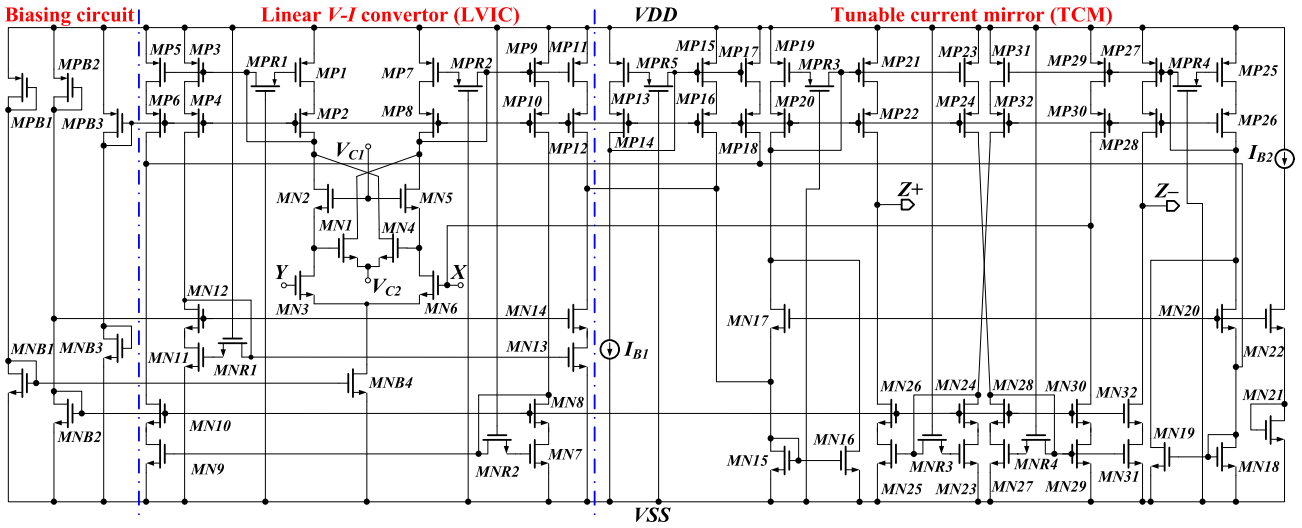

FIGURE 14. Complete circuit of the proposed CMOS CCCII.

triode region). Fig.13(b) shows an active realization of the compensation resistor. The resistance value of M_0 operating in triode region ($V_{DS} \ll 2\,(V_{GS} - V_{th})$) is

$$r_{M0} = 1/\left[\mu C_{ox}\left(W/L\right)_0 (V_{GS0} - V_{th})\right], \tag{29}$$

where $\mu, C_{ox}, W, L, V_{GS0}$, and V_{th} are respectively the mobility, oxide capacitance per unit area, channel width, channel length, gate-to-source voltage, and threshold voltage of the transistor M_0. Therefore, the bandwidth of the active resistor compensating LVCCM can be adjusted by varying the parameters of M_0.

C. COMPLETE CIRCUIT SCHEMATIC OF THE CMOS CCCII

Fig.14 shows the complete circuit based on the CCCII implementation scheme, in which LVCCMs are used in combination with other circuits. The complete circuit structure consists of three functional parts, which contains bias circuit, linear $V - I$ convertor, and tunable current mirror. The X-terminal of the LVIC is connected to point A of the TCM to satisfy the port characteristics of CCCII. Since active equivalent resistors $MNR1 - MNR4$ and $MPR1 - MPR5$ must always operate in triode region, the gates of these transistors require a high working voltage and they are respectively connected to the corresponding power supply voltage accordingly. $MNB2$ and $MPB2$, $MNB3$ and $MPB3$ constitute two independent bias circuits that provide bias voltages for corresponding LVCCM circuit. Long channel transistors $MNB1$, $MNB4$, and $MPB1$ constitute a current bias circuit, which provides the tail current for LVIC.

For any high-performance application that requires high bandwidth, the MOS transistors should be biased in strong inversion region, namely the overdrive voltage $V_{GS} - V_{th} \geq 0.2V$. The MOS transistors can act as transconductors or current sources as long as $V_{ds} > V_{dsat}$. Since a good estimate value of V_{dsat} at the edge of strong and moderate inversions is approximately $0.15V$, in any working region, we need to maintain V_{ds} at least $0.15V$ [42]. The LVCCM can operate with voltage as low as $V_{th} + V_{dsat}$. For the *GlobalFoundries'* $0.18\mu m$ CMOS process, the threshold voltages of NMOS and PMOS transistors are approximately $0.42V$ and $-0.49V$ at the *typical* process corner, respectively. Therefore, the proposed structure, thus, has the potential to operate at supply voltages of $V_{thn} + V_{thp} + 3V_{dsat}$, that is $\pm 0.68V$.

The expression of the output current shown in (30) can be obtained by equations (21), (26), and Fig.14:

$$\begin{aligned} i_{z+} &= -i_{z-} = i_x = A_C i_o \\ &= 2K\,(V_{C1} - V_{C2} - 2V_{thn}) \cdot \frac{nI_{B1}}{2I_{B2}} \cdot v_{xy}. \end{aligned} \tag{30}$$

Convert (30) into the form of (31):

$$v_{xy} = v_x - v_y = i_x R_X, \tag{31}$$

where R_X is the equivalent adjustable intrinsic resistance. We can get the following expression by comparing (30) and (31):

$$R_X = \frac{1}{K\,(V_{C1} - V_{C2} - 2V_{thn})} \cdot \frac{I_{B2}}{nI_{B1}} = K_T \cdot \frac{I_{B2}}{I_{B1}}, \tag{32}$$

where $K_T = 1/[nK\,(V_{C1} - V_{C2} - 2V_{thn})]$.

Since the gate of the transistor has exceedingly high input impedance, it is easy to know that the current of Y-terminal in Fig.14 is basically zero. Therefore, According to (30), (31), (32), and the foregoing analyses, the circuit in Fig.14 satisfies the basic port characteristics of CCCII.

Equation (32) indicates that the intrinsic resistance R_X of the proposed CCCII can be linearly adjusted by the ratio of external bias current (I_{B2}/I_{B1}) and the difference of two bias voltages ($V_{C1} - V_{C2}$). Compared with the published CCCIIs (only have single external bias current), the CCCII circuit proposed in this paper has a larger adjustable range of intrinsic resistance.

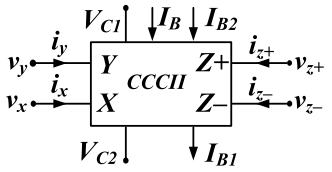

FIGURE 15. Improved symbol of the new CCCII circuit.

As can be seen from (22), the dynamic voltage input range of the proposed CCCII circuit is $-\sqrt{2I_B/K} \le v_{id} \le \sqrt{2I_B/K}$. However, the dynamic voltage input range of the traditional translinear loop [43], [44] and balanced differential pair [45], [46] CCCII circuits are $-\sqrt{I_B/K} \le v_{id} \le \sqrt{I_B/K}$. Accordingly, the voltage input range of the proposed CCCII is 1.41 times that of the traditional structures.

The intrinsic resistance and dynamic input voltage range of the proposed CCCII are respectively related to I_{B2}/I_{B1} and I_B, where I_{B1}, I_{B2}, and I_B are different currents, therefore, adjusting R_X value does not affect the dynamic range of CCCII.

According to the complete circuit that shown in Fig.14, the modified form of the new CCCII circuit symbol in this paper is shown in Fig.15. Compared with the elementary CCCII, it increases two bias voltages and two bias currents.

IV. IMPLEMENTATION OF MULTI-ATTRACTOR PERIOD MULTI-SCROLL CURRENT-MODE CHAOTIC CIRCUIT BASED ON THE PROPOSED CCCII

A. BLOCK CIRCUIT STRUCTURE OF THE CHAOTIC SYSTEM

Fig.16 shows the block circuit realization scheme of the proposed multi-attractor period multi-scroll current mode chaotic circuit, we take CCCII as the basic block to realize the multi-attractor period multi-scroll chaotic system that shown in (1).

From a signal processing perspective, the circuit in Fig.16 includes two types of functional parts: (i) four integral blocks consisting of Ai and Ci ($i = 1, 2, 3, 4$), Ai and Ci are respectively CCCII (of which, $A4$ is multi-output CCCII) and capacitor; (ii) four saturation nonlinear function circuit blocks composed of CCCIIs, which are $f_1(I_1), f_2(I_2), f_3(I_3)$, and $f_4(I_4)$. The whole chaotic circuit has no passive resistors, and it is relatively easy for integrated implementation.

In Fig.16, current I_4, nonlinear function $f_4(I_4)$, $A1$, and $C1$ make up a current signal integrator. Assume that the intrinsic resistance of X-terminal of the $A1$ is R_{X1}. The symbol such as $\times a$ in Fig.16 denotes that the output current will be multiplied by a. According to the port relationship of CCCII, it can be deduced that the differential equation of the state variable I_1 is

$$C_1 \cdot \frac{d\left(R_{X1} I_1\right)}{dt} = R_{X1} C_1 \cdot \frac{dI_1}{dt} = a \cdot \left[I_4 - f_4\left(I_4\right)\right]. \tag{33}$$

Similarly, the differential equation of state variables $I_2 \sim I_4$ can also be deduced according to Fig.16, and simultaneous differential equations of the four state variables I_1, I_2, I_3, and I_4 can be obtained as

$$\begin{cases} R_{X1} C_1 \cdot \dfrac{dI_1}{dt} = a \cdot \left[I_4 - f_4\left(I_4\right)\right] \\ R_{X2} C_2 \cdot \dfrac{dI_2}{dt} = b \cdot I_4 + c \cdot \left[I_1 - f_1\left(I_1\right)\right] \\ R_{X3} C_3 \cdot \dfrac{dI_3}{dt} = d \cdot I_4 - e \cdot \left[I_3 - f_3\left(I_3\right)\right] \\ R_{X4} C_4 \cdot \dfrac{dI_4}{dt} = -h \cdot I_4 - m \cdot \left[I_2 - f_2\left(I_2\right)\right]. \end{cases} \tag{34}$$

Among them, R_{X1}-R_{X4} are respectively the adjustable intrinsic resistances of $A1$-$A4$. The value of R_{X1}-R_{X4} can be adjusted by external bias voltages (V_{C1}, V_{C2}) and bias currents (I_{B1}, I_{B2}). According to the foregoing description, the coefficients of the state equation are made as $a = 2, b = c = e = h = 1, d = 1.5$. The theoretical calculation formula of the proposed CCCII's intrinsic resistance is shown in (32).

B. CURRENT MODE SATURATION FUNCTION CIRCUIT BASED ON CCCII

The saturation function sequence circuits $f_1(I_1)$, $f_2(I_2)$, $f_3(I_3)$, and $f_4(I_4)$ in Fig.16 are also composed of CCCIIs. Fig.17 shows the saturation function circuit that are composed of CCCIIs. In order to analyze the saturation function circuit from the viewpoint of signal processing, the primary CCCII in Fig.17 is equivalent to the $A1$-$A4$ in Fig.16, which is used to realize integral conversion combining with corresponding capacitor. R_{in} is an active equivalent resistance composed of CCCII to achieve current-voltage conversion. V_F is a voltage follower composed of CCCII to achieve impedance matching. The CCCIIs in the dotted box are used as comparators. The CCCIIs in the same comparator array

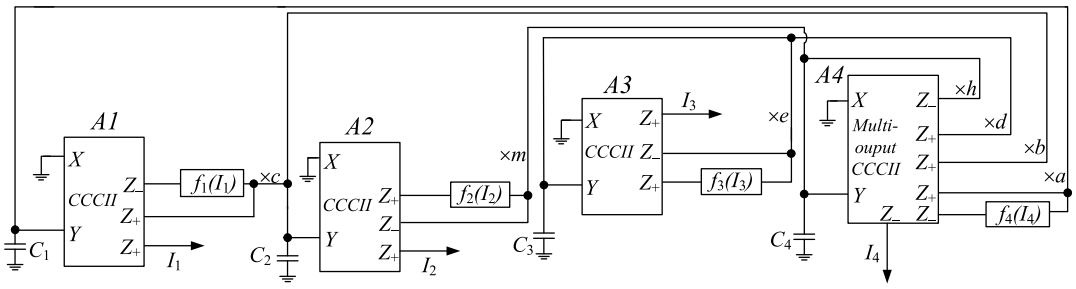

FIGURE 16. Block circuit realization scheme of multi-attractor period multi-scroll current-mode chaos.

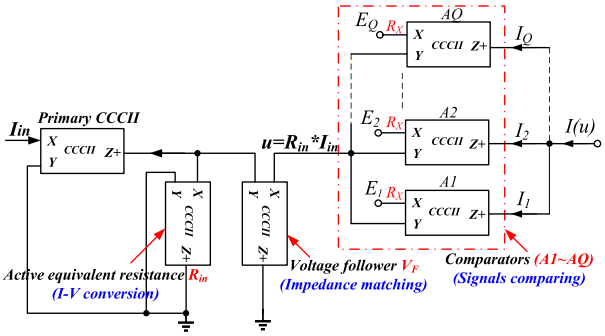

FIGURE 17. Current mode saturation nonlinear function circuit.

have the same bias conditions, but have different comparison voltages.

The proposed saturation function circuit is analyzed from the point of signal processing. Firstly, assume that the current I_{in} flows into the X-terminal of the primary CCCII. Since the active equivalent resistance(R_{in}) is far less than the output resistance of the primary CCCII and the input resistance of the voltage follower V_F, and then all output current of the primary CCCII will be converted to voltage by active equivalent resistance R_{in}. Then the output voltage signal obtained from the voltage follower is compared with the corresponding voltage in the comparator array, and finally the output saturation current function $I(u)$ is obtained. According to the port characteristics of CCCII, the output current of the A_Q in the dotted box of Fig.17 is

$$I_Q = \frac{(E_Q - u)}{R_X} = -\frac{(I_{in}R_{in} - E_Q)}{R_X} = -\frac{R_{in}}{R_X} \cdot \left(I_{in} - \frac{E_Q}{R_{in}}\right), \tag{35}$$

where E_Q is the comparison voltage of A_Q, R_X is a controllable intrinsic resistance of the CCCII that in the dotted box.

According to the nonlinear principle of CCCII, when the value of right side of the expression in (35) grows to a certain extent, the left and right sides of this equation are no longer equal. That means the current of Z-terminal of $Ai(1, 2, \ldots, Q)$ no longer follows the current of X-terminal, and the output current of Z-terminal reaches the output saturation value. Therefore, the output current behaves as a relationship of bilateral saturation function:

$$\begin{aligned} I_j &= S\left(I_{in} - E_j/R_{in}\right) \\ &= -\frac{|I_Z|}{2q} \cdot \left(\left|I_{in} - E_j/R_{in} + q\right| - \left|I_{in} - E_j/R_{in} - q\right|\right) \\ &= \begin{cases} |I_Z|, & I_{in} < \left(E_j/R_{in} - q\right); \\ -\dfrac{|I_Z|}{q} & \\ \cdot \left(I_{in} - E_j/R_{in}\right), & \left(E_j/R_{in} - q\right) \le I_{in} \le \left(E_j/R_{in} + q\right); \\ -|I_Z|, & I_{in} > \left(E_j/R_{in} + q\right); \end{cases} \end{aligned} \tag{36}$$

where $|I_Z|$ and E_j are respectively the saturation current and comparison voltage of $Aj(j = 1, 2, \ldots, Q)$, $\pm q$ is the value

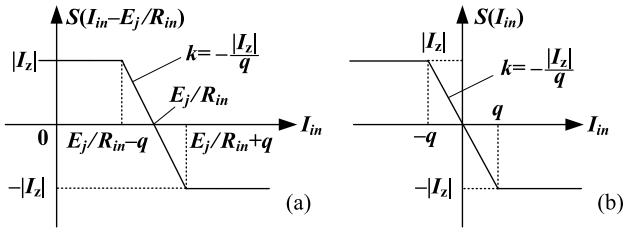

FIGURE 18. Bilateral saturation function curves. (a) Bilateral translation saturation function; (b) Bilateral saturation function.

TABLE 1. W/L ratio of the MOS in Fig.14.

MOS transistors	$W/L(\mu m/\mu m)$
$MN1 - MN6$	6/0.5
$MN7 - MN32$	7.2/0.3
$MNB1, MNB4$	60/1
$MNB2$	1.5/1
$MNB3$	30/1
$MNR1 - MNR2$	1.92/0.3
$MNR3 - MNR4$	3.36/0.3
$MP1 - MP32$	34/0.3
$MPB1$	10.5/1
$MPB2$	81.5/1
$MPB3$	6.3/1
$MPR1 - MPR2$	12/0.3
$MPR3 - MPR4$	23.1/0.3
$MPR5$	10.8/0.3

of turning point and $q = |I_Z| \cdot R_X / R_{in}$. $S\left(I_{in} - E_j/R_{in}\right)$ is a bilateral translation saturation function, as shown in Fig.18(a), and if $E_j = 0$, the bilateral saturation function $S(u)$ is shown in Fig.18(b). In Fig.18, k is the slope of the broken line and $k = -R_{in}/R_X$.

In Fig.17, the output current of all comparators are added to obtain the output of the saturation function circuit:

$$\begin{aligned} I\left(I_i\right) &= \sum_{j=1}^{Q} I_j = \sum_{j=1}^{Q} S\left(I_{in} - E_j/R_{in}\right) \\ &= -\frac{|I_Z|}{2q} \cdot \sum_{j=1}^{Q} \left(\begin{array}{l} \left|I_{in} - E_j/R_{in} + q\right| \\ -\left|I_{in} - E_j/R_{in} - q\right| \end{array} \right). \end{aligned} \tag{37}$$

V. SIMULATION RESULTS AND ANALYSIS

A. PERFORMANCE SIMULATION OF THE CCCII

Simulations are carried out in Cadence, and the BSIM3v3 model for thin-gate (1.8V) CMOS process are used, which are all based on *GlobalFoundries'* $0.18\mu m$ technology for SPICE model in SPECTRE simulator. According to the previous analysis regarding operating voltage, we select $\pm 0.8V$ as DC power supply voltage.

The channel width and length of all MOS transistors in Fig.14 are obtained through repeated experimental simulation and theoretical calculation, which are shown in Table. 1. Fig.19 shows the DC and AC voltage transfer characteristics of the proposed CCCII ($Z+$ and $Z-$ grounded). We can see from the Fig.19(a) that the voltage of X-terminal follows the voltage of Y-terminal very well in different process corners at corresponding bias condition. Fig.19(b) shows that the -3dB bandwidth of the AC voltage transfer characteristics (Y to X) in different process corners are respectively $910.6MHz$, $1.331GHz$, $1.402GHz$, $1.402GHz$, and $1.778GHz$.

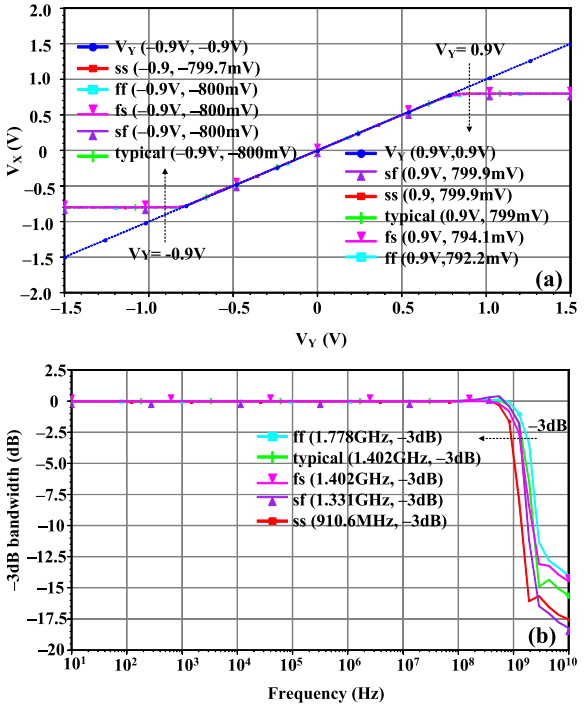

FIGURE 19. Voltage transfer characteristics of the CCCII. (a) DC voltage transfer characteristic with the simulation conditions: $V_{C1} = -V_{C2} = 0.4V$, $I_{B1} = I_{B2} = 0$; (b) AC voltage transfer characteristic with the simulation conditions: $V_{C1} = -V_{C2} = 0.8V$, $I_{B1} = 200\mu A$, $I_{B2} = 10\mu A$.

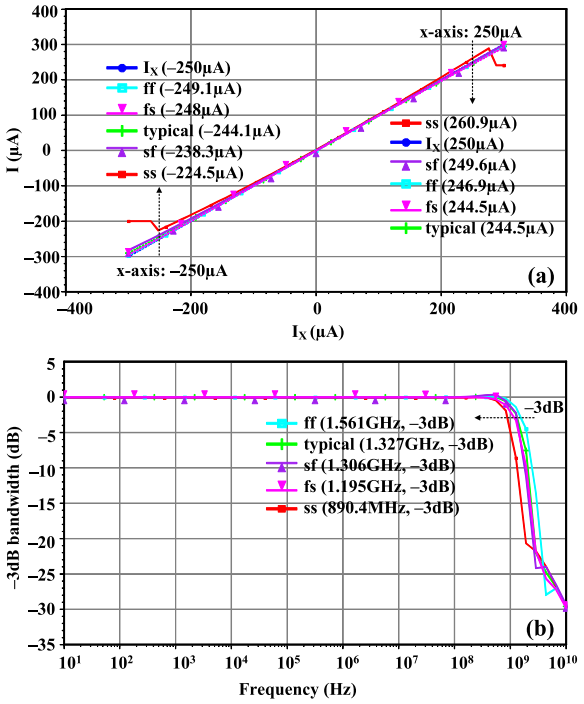

FIGURE 20. Current transfer characteristics of the CCCII with the simulation conditions: $V_{C1} = -V_{C2} = 0.8V$, $I_{B1} = 200\mu A$, $I_{B2} = 10\mu A$. (a) DC current transfer characteristic; (b) AC current transfer characteristic.

Similarly, the DC and AC current transfer characteristics of the CCCII (Y grounded) are shown in Fig.20. We can see from the Fig.20(a) that the CCCII has a wide linear current tracking range in different process corners. The -3dB bandwidth of the AC current transfer characteristics (X to Z) in different process corners are respectively $890.4MHz$, $1.195GHz$, $1.306GHz$, $1.327GHz$, and $1.561GHz$, which are shown in Fig.20(b).

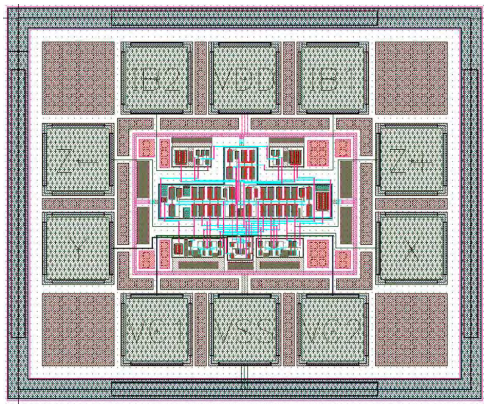

FIGURE 21. Layout of the proposed CMOS CCCII.

In order to implement the actual chip fabrication, based on the layout symmetry design and other key points, the post-simulation results are compared with pre-simulation results by repeated extract parasitic parameters of different designed layouts to get the relatively optimal performance. Fig.21 shows the final layout of the CMOS CCCII, and its chip area is only $0.315 \times 0.383mm^2$, which contains scribe line and guard ring. The main simulation results of the CMOS CCCII are listed in Table 2.

B. SIMULATION OF MULTI-ATTRACTOR PERIOD MULTI-SCROLL CHAOTIC CIRCUIT BASED ON CCCII

1) SINGLE-ATTRACTOR PERIOD $3 \times 3 \times 3$ SCROLL CHAOTIC CIRCUIT

Fig.22 shows the circuit realization schematic of the three-step saturation function in *Cadence*. The circuit in this diagram is connected according to the previous saturation nonlinear function circuit that shown in Fig.17. In Fig.22, all functional devices are composed of CCCIIs under different bias conditions. Different CCCIIs have different functional roles, they are numbered in order to facilitate subsequent analysis, as shown in Fig.22. The power supply voltages in all circuits are $\pm 0.8V$.

According to the port characteristics of CCCII and the bias conditions that shown in Fig.22, the input impedance of X-terminal of (b) is much less than the output impedance of Z-terminal of (a) and the input impedance of Y-terminal of (c). As a result, almost all the output current of (a) will flow into (b) and is converted to voltage. The voltage signal is basically absorbed by (c) because of its higher input impedance, and then the voltage following action is realized. Finally, the output signal of (c) is compared with two comparators (d) and (e) to get the output saturation current. Fig.23 shows the simulation results of the circuit in Fig.22 with the

TABLE 2. Main performances of the proposed CMOS CCCII.

Performance characteristics	Simulation	Post-simulation
Supply voltage	$\pm 0.8V$	$\pm 0.8V$
Max linear voltage input range of Y (1% error)	$-0.79 \sim 0.713V$	$-0.79 \sim 0.7V$
Max linear current input range of X (1% error)	$-322 \sim 375\mu A$	$-270 \sim 310\mu A$
Voltage transfer ratio/bandwidth(Y to X)	$0.999/1.402GHz$	$0.999/1.009GHz$
Current transfer ratio/bandwidth(X to Z)	$0.996/1.327GHz$	$0.993/868.1MHz$
Impedance at Y, Z ($V_{C1} = -V_{C2} = 0.8V, I_{B1} = 200\mu A, I_{B2} = 10\mu A, n = 1$)	$\infty, 1.33M\Omega$	$\infty, 1.85M\Omega$
R_X adjustable range($n = 1$)	$223.5\Omega \sim 321.7K\Omega$	$241.9\Omega \sim 310K\Omega$
Static power consumption($V_{C1} = -V_{C2} = 0.8V, I_{B1} = 200\mu A, I_{B2} = 10\mu A, n = 1$)	$3.785mW$	$3.66mW$

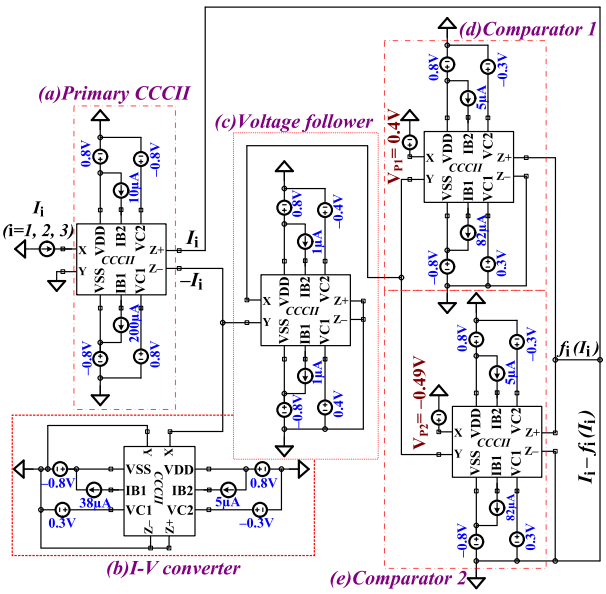

FIGURE 22. Circuit realization schematic of the three-step saturation function in Cadence.

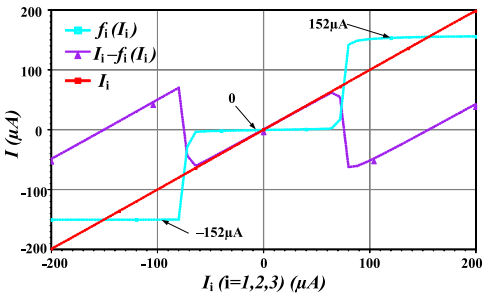

FIGURE 23. Simulation results of three-step saturation function circuit.

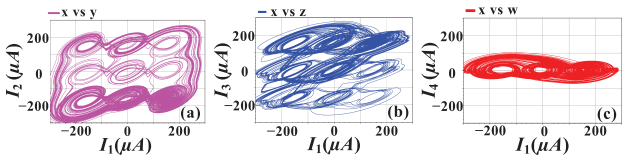

FIGURE 24. Circuit simulation of single-attractor period 3 × 3 × 3 scroll chaotic phase portraits. (a) $I_1 - I_2$ ($x - y$) plane projection; (b) $I_1 - I_3$($x - z$) plane projection; (c) $I_1 - I_4$ ($x - w$) plane projection.

listed bias conditions. The three step-values of the saturated functions f_i (I_i) in Fig.23 are respectively 0 and $\pm 152\mu A$.

In order to realize single-attractor period 3 × 3 × 3 scroll chaotic circuit in *Cadence*, the circuit connection mode in Fig.16 is adopted. The three-step saturation function circuit shown in Fig.22 is applied in the three directions of $x(I_1)$, $y(I_2)$, and $z(I_3)$. Except for CCCII, the single-attractor period 3 × 3 × 3 scroll chaotic circuit contains only four additional capacitors for integral action. There is a little different from the connection mode that in Fig.22, four capacitors are connected to the Y-terminals of the four primary CCCIIs, as shown in Fig.16. The X-terminals of these primary CCCIIs are grounded. According to (5) and the aforementioned generating method of single-attractor period multi-scroll chaotic system, there is no need to add the nonlinear function f_4 (w) [f_4 (I_4)] in the $w(I_4)$ direction. In accordance with the coefficient values and the state equation form of system (1), the primary CCCII in $w(I_4)$ direction must have multiple output terminals and each output terminal can achieve arbitrary multiple current output. The multi-output CCCII (*A*4 in Fig.16) with arbitrary output current ratio can be realized by adding several multi-output LVCCMs (with the same or different W/L ratio) on the proposed CCCII. The coefficient values $a = 2$ and $d = 1.5$ of the single-attractor period 3 × 3 × 3 scroll chaotic circuit can be set by just adjusting the corresponding W/L ratio of the multi-output CCCII.

The simulated saturation functions in the three directions of $x(I_1)$, $y(I_2)$, and $z(I_3)$ are shown in Fig.23, and the bias condition of multi-output CCCII in the $w(I_4)$ direction is the same as that of (a) in Fig.22. Fig.24 shows the phase portraits obtained from the transient simulation in *Cadence*.

2) DOUBLE-ATTRACTOR PERIOD 3 × 3 × 3 SCROLL CHAOTIC CIRCUIT

Compared with the single-attractor period 3 × 3 × 3 scroll chaotic circuit, the double-attractor period 3 × 3 × 3 scroll chaotic circuit only adds a two-step saturation function circuit (as shown in Fig.25) in the direction of $w(I_4)$. The two-step saturation function circuit just need one CCCII comparator, and the comparison voltage of this comparator is $V_P = 0$.

The simulation results of the circuit in Fig.25 are shown in Fig.26. The two step-values of the saturation function f_4 (w) [f_4 (I_4)] in Fig.26 are respectively $\pm 28\mu A$. The coefficient values $a = 2$ and $d = 1.5$ of the double-attractor period 3 × 3 × 3 scroll chaotic circuit can be obtained by respectively adding a current mirror made up of CCCII and adjusting

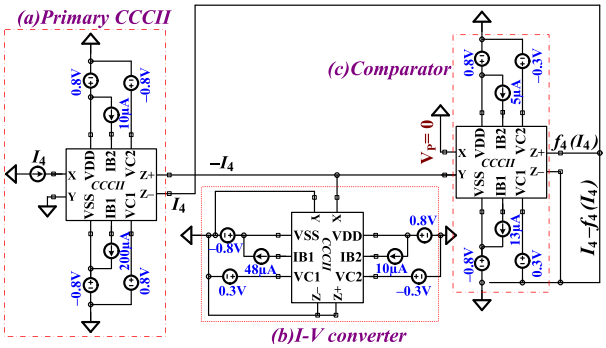

FIGURE 25. Circuit realization schematic of the two-step saturation function in Cadence.

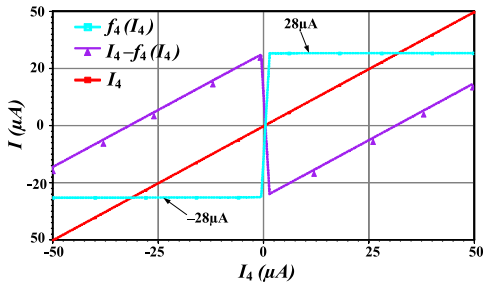

FIGURE 26. Simulation results of two-step saturation function circuit in $w(I_4)$ direction.

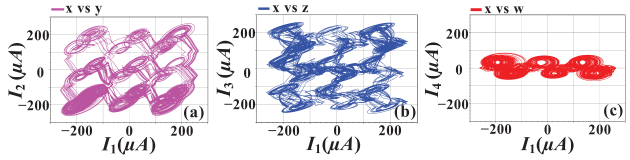

FIGURE 27. Circuit simulation of double-attractor period 3 × 3 × 3 scroll chaotic phase portraits. (a) $I_1 - I_2$ $(x - y)$ plane projection; (b) $I_1 - I_3$ $(x - z)$ plane projection; (c) $I_1 - I_4$ $(x - w)$ plane projection.

the corresponding W/L ratio of the multi-output CCCII. The phase portraits obtained from the transient simulation in *Cadence* are shown in Fig.27.

3) THREE-ATTRACTOR PERIOD 3 × 3 × 3 SCROLL CHAOTIC CIRCUIT

In order to realize the three-attractor period 3 × 3 × 3 scroll chaotic circuit, a three-step saturation function circuit with lower saturation value is introduced in the $w(I_4)$ direction. The structure of this three-step saturation circuit is the same as Fig.22, but the bias conditions are different: (a) $V_{C1} = -V_{C2} = 0.8V, I_{B1} = 200\mu A, I_{B2} = 10\mu A$; (b) $V_{C1} = -V_{C2} = 0.3V, I_{B1} = 7\mu A, I_{B2} = 5\mu A$; (c) $V_{C1} = -V_{C2} = 0.4V, I_{B1} = -I_{B2} = 0\mu A$; (d) and (e) $V_{C1} = -V_{C2} = 0.3V, I_{B1} = 7\mu A, I_{B2} = 2\mu A, V_{P1} = 0.22V, V_{P2} = -0.22V$.

The simulation results of the three-step saturation function circuit with lower saturation value are shown in Fig.28. The three step-values of the saturated function $f_4(w)$ $[f_4(I_4)]$ in Fig.28 are respectively 0 and $\pm 38\mu A$. The realization method of coefficients $a = 2$ and $d = 1.5$ is the same as

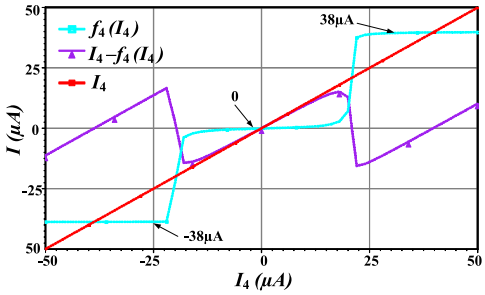

FIGURE 28. Simulation results of three-step saturation function circuit in $w(I_4)$ direction.

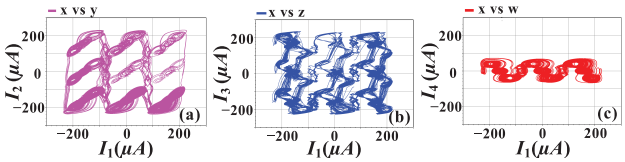

FIGURE 29. Circuit simulation of three-attractor period 3 × 3 × 3 scroll chaotic phase portraits. (a) $I_1 - I_2$ $(x - y)$ plane projection; (b) $I_1 - I_3$ $(x - z)$ plane projection; (c) $I_1 - I_4$ $(x - w)$ plane projection.

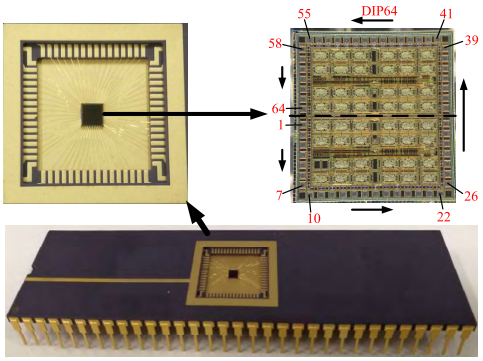

FIGURE 30. Packaged IC and chip micrograph of the multi-attractor period 3 × 3 × 3 scroll chaotic circuit based on CMOS CCCII.

that of double-attractor period 3 × 3 × 3 scroll chaotic circuit. The bias conditions of all CCCII in the three directions of $x(I_1)$, $y(I_2)$, and $z(I_3)$ are kept the same as that listed in Fig.22, the phase portraits obtained from the transient simulation in Cadence are shown in Fig.29. It can be seen from the above circuit simulation results that the chaotic parameters can be adjusted by just changing the external bias. The corresponding chaotic circuit can be adjusted by external bias even after chip fabrication. Therefore, the multi-attractor period multi-scroll chaotic circuit based on the proposed CMOS CCCII has this natural advantage.

C. CHIP TEST OF MULTI-ATTRACTOR PERIOD MULTI-SCROLL CHAOTIC CIRCUIT

Fig.30 shows the packaged IC and chip micrograph of the multi-attractor period 3 × 3 × 3 scroll chaotic circuit based on CMOS CCCII. The fabricated chip includes double-attractor period and three-attractor period 3 × 3 × 3 scroll chaotic integrated circuits. To facilitate practical testing, the encapsulation of this chip after fabrication is in the form of the Dual

TABLE 3. Comparison of related chaotic circuits.

Refs	Published years	Attractor forms	Active devices	Passive components	Electronic tunability	Supply voltages	State variables	Hardware experiments
[33]	2014	Multi-scroll/2×2	CFOA	Resistor, Capacitor	No	±10V	Voltage	Yes/AD844
[30]	2014	Multi-scroll/4×3×3	CCII+	Resistor, Capacitor	No	±15V	Voltage	Yes/AD844
[34]	2014	Multi-scroll/ 4×2×2×2×2	CCII	Resistor, Capacitor	No	±15V	Voltage	Yes/AD844
[47]	2016	Multi-scroll/3×4	CCII+	Resistor, Capacitor	No	±5V	Voltage	Yes/AD844
[25]	2018	Double-scroll	OA	Resistor, Capacitor, Inductor	No	±2.5V	Voltage	No/CMOS-based CADENCE simulation
[26]	2018	Multi-scroll/3×3×3	OA	Resistor, Capacitor	No	±2.5V	Voltage	No/CMOS-based CADENCE simulation
[36]	2016	Single-direction multi-scroll/20	Traditional CCCII	Resistor, Capacitor	No	±1.5V	Voltage	No/CMOS-based PSPICE simulation
This paper	**—**	**Multi-attractor period multi-scroll/3×(3×3×3)**	**Novel CCCII**	**Only capacitor**	**Yes**	**±0.8V**	**Current**	Yes/**Chaotic IC**

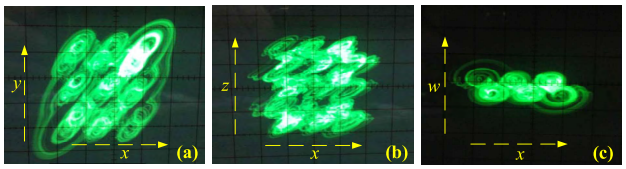

FIGURE 31. Test results of the double-attractor period 3 × 3 × 3 scroll chaotic integrated circuit, where $x = y = z = w = 1V/div$. (a) $x - y$ plane projection; (b) $x - z$ plane projection; (c) $x - w$ plane projection.

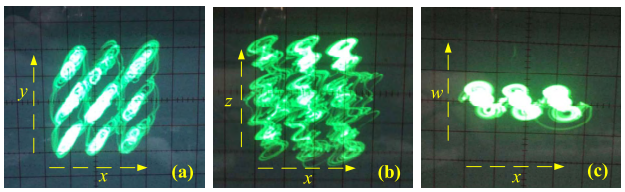

FIGURE 32. Test results of the three-attractor period 3 × 3 × 3 scroll chaotic integrated circuit, where $x = y = z = w = 1V/div$. (a) $x - y$ plane projection; (b) $x - z$ plane projection; (c) $x - w$ plane projection.

In-Line Package (DIP). This form of encapsulation is easy to implement the connection between the chip and discrete components on the breadboard.

By adding bias and external power supply in corresponding position, the double-attractor period and three-attractor period $3 \times 3 \times 3$ scroll chaotic phase portraits can be observed in analog oscilloscope, which are shown in Fig.31 and Fig.32. Therefore, the correctness of the designed chaotic circuit is verified.

D. COMPARISON OF RELATED CHAOTIC CIRCUITS

Table 3 shows the comparison between the implementation scheme of the chaotic circuit in this paper and several reported chaotic circuits. From Table 3, the multi-attractor period multi-scroll chaotic system proposed in this paper can generate new attractor forms, and the new current signal scheme is used to implement its chaotic circuit based on high-performance CMOS CCCII with electronic tunability. In addition, the chaotic circuit in this paper does not contain any passive resistor, which is easy to integrate and has the advantages of low supply voltage. For this new chaotic circuit, simulation and hardware testing are performed. These characteristics reflect the advanced and innovative nature of the work done in this paper.

VI. CONCLUSION

A new multi-attractor period multi-scroll chaotic system is proposed in this paper, and the dynamic characteristics of this proposed chaotic system are analyzed in detail. A current mode device CCCII which possesses wide intrinsic resistance tunable and dynamic input range is also designed to realize the novel multi-attractor period multi-scroll chaotic system. The performances of the CCCII are simulated in cadence based on *GlobalFoundries*' $0.18\mu m$ CMOS process. Unlike available chaotic circuits, the chaotic circuit in this paper is composed of CMOS CCCIIs and four capacitors without any passive resistor, in addition, only current-signals are used as state variables in our chaotic circuit. Because the functional devices in the chaotic circuit are composed of tunable CCCIIs, the value of the active resistance, the slope and saturation value of the saturation circuit are adjustable even after chip fabrication. Therefore, the new chaotic circuit can be adjusted by external bias after chip fabrication to generate chaos. Experimental results show that it is feasible to realize chaos completely using current-signals as state variables. The actual chip test results show the feasibility of this scheme, and this is of great significance to further study the current mode complex multi-scroll chaotic systems and chaotic integrated circuits.

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XIN ZHANG was born in Xiangtan, Hunan, China, in 1989. He received the M.S. degree in information and communication engineering from the College of Computer Science and Electronic Engineering, Hunan University, Changsha, China, in 2014, where he is currently pursuing the Ph.D. degree. His research interests mainly include current-mode circuit design, complex multi-scroll chaotic system and chaotic circuit design, and analog integrated circuit design.

CHUNHUA WANG was born in Yongzhou, China, in 1963. He received the B.S. degree from Hengyang Normal University, Hengyang, China, the M.S. degree from the Physics Department, Zhengzhou University, Zhengzhou, China, and the Ph.D. degree from the Beijing University of Technology, Beijing, China. He is currently a Professor and a Doctoral Supervisor with Hunan University, Changsha, China. His research interests include current-mode circuit design, RFIC design, wireless communication, chaotic system and circuit design, and chaos synchronization and encryption.