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Design and Hardware Implementation Considerations of Modified Multilevel Cascaded H-Bridge Inverter for Photovoltaic System

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ABSTRACT Inverters are an essential part in many applications including photovoltaic generation. With the increasing penetration of renewable energy sources, the drive for efficient inverters is gaining more and more momentum. In this paper, output power quality, power loss, implementation complexity, cost, and relative advantages of the popular cascaded multilevel H-bridge inverter and a modified version of it are explored. An optimal number of levels and the optimal switching frequency for such inverters are investigated, and a five-level architecture is chosen considering the trade-offs. This inverter is driven by level shifted in-phase disposition pulse width modulation technique to reduce harmonics, which is chosen through deliberate testing of other advanced disposition pulse width modulation techniques. To reduce the harmonics further, the application of filters is investigated, and an LC filter is applied which provided appreciable results. This system is tested in MATLAB/Simulink and then implemented in hardware after design and testing in Proteus ISIS. The general cascaded multilevel H-bridge inverter design is also implemented in hardware to demonstrate a novel low-cost MOSFET driver build for this study. The hardware setups use MOSFETs as switching devices and low-cost ATmega microcontrollers for generating the switching pulses via level shifted in-phase disposition pulse width modulation. This implementation substantiated the effectiveness of the proposed design.

INDEX TERMS Inverter, multilevel inverter, cascaded H-bridge, modified cascaded H-bridge, advanced PWM techniques, MOSFET driving technique, level shifted in-phase disposition pulse width modulation.

LIST OF ABBREVIATIONS

AC	Alternating Current
APOD	Alternative Phase Opposition Disposition
BJT	Bipolar Junction Transistor
CHB	Cascaded H-bridge
DC	Direct Current
DSP	Digital Signal Processor
EV	Electric Vehicle
FPGA	Field Programmable Gate Array
IDE	Integrated Development Environment
LS-IPD	Level Shifted In-Phase Disposition
MIPS	Mega Instruction Cycles Per Second
MLI	Multilevel Inverter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
PD	Phase Disposition
POD	Phase Opposition Disposition
PSO	Particle Swarm Optimization
PV	Photovoltaic
PWM	Pulse Width Modulation
RES	Renewable Energy Sources
THD	Total Harmonic Distortion

I. INTRODUCTION

Renewable energy sources (RES) are getting ever-important with the current drive towards sustainable and environment-friendly power generation techniques. In this ongoing revolution, solar photovoltaic (PV) generation plays a huge part. Recent revolutionary developments in this technology have risen to a level where they can now compete with coal as an affordable power source. But PV systems require components other than the photovoltaic cells themselves. In a power system where alternating current (AC) underpins the transmission and distribution system, the direct current (DC)-generating PV systems require inverters to put their produce in the grid; and thus, to enhance the PV system efficiency, improving the inverters is crucial. Inverters are power electronic devices consisting of a number of switching elements that, when controlled through proper switching sequences, can produce AC output from a DC input. This arrangement obviously raises some complications in the form of losses at the switches, complexity regarding switching each individual device, the added hassle of using switching devices rated high enough to withstand the required output, associated cost etc. These also lead to the question of inverter efficiency, as that contributes significantly while determining the efficiency of a PV system. Different inverter architectures are therefore conceived to increase the efficiency, multilevel inverter (MLI) being one of them. MLI produces an AC output by using multiple levels of DC, and the number of levels it can generate determines the smoothness of the output. It offers certain benefits over other designs [1]–[3], and its variants are thus widely employed [4]. In this paper, the popular [5]–[8] cascaded H-bridge architecture of multilevel inverter is adopted, as it requires less components when compared to other MLI topologies. Here, the general construction of cascaded H-bridge MLI is further modified to attain a 5-level output for single phase usage with less number of switching elements compared to the 8 switches required in the general design. Moreover, to reduce the total harmonic distortion (THD) in the output, the switching pulses are generated via an advanced pulse width modulation (PWM) technique – chosen through comparing its performance with other similar methods. A filter is then applied at the inverter output to further reduce the THD. The optimal system obtained through this procedure is then implemented in hardware to observe real-word responses. Additionally, the relation of THD with changing inverter levels and switching frequencies are investigated, where 7-level inverter, and 6 kHz switching frequency are found as the ones producing the least THD. However, 5-level design is chosen here as it offers both less THD and less circuit complexity.

The significance of this inverter type can be perceived just from the amount of work done in this topic in recent times. Balikci et al proposed a 3-phase 5-level inverter which employed 6 switches, and used sinusoidal PWM technique for switching. It was aimed for STATCOM application, and was implemented in hardware using digital signal processor (DSP) TMS320F28335 as the controller [4]. A similar topology for both symmetric (equal DC voltage for all the bridges) and asymmetric (unequal DC voltages) operations was presented in [9]. Lezana *et al.* [10] presented a single-phase inverter design with 6 switches per inverter cell. Two of those switches had a different rating than the other four. An 11-level inverter with 14 switches was presented by Babaei *et al.* [11], which was implemented in hardware with IGBTs as the switching elements. 4 switches in this design had to withstand 400 Volts, while the rest faced 200 Volts – thus making the system requiring switches of two different ratings. The switching in their work was conducted through an Atmel 89C52 microcontroller, and isolation at the switches was achieved by optocouplers. According to [12], this design was an improvement on the work done in [13], which was further refined in [14] – where the design was validated through a 125-level single phase converter. Hinago et al presented a way to create the voltage source as a combination of individual battery cells connected in series to obtain multiple voltage levels with reduced switching elements through intelligent connection modifications of the cells. Capacitors and other DC sources could also be used in their topology, and this strategy could be employed for grid-connected PV systems [15]. Single phase MLI's, interfaced with grid-connected PV systems, were presented in [16]–[18]. Another topology proposed by Gupta and Jain [19] reduced the required number of switches to 6 by altering the DC source polarities as required. Their method was demonstrated through a 5-level single phase inverter. Kangarlu *et al.* [20] presented a scalable symmetric inverter architecture with reduced switching elements. This topology did not require isolated DC sources, and was tested for a 15-level inverter prototype – which employed IGBTs with internal anti-parallel diodes, and Atmel 89C52 microcontroller for generating the switching signals. Kangarlu and Babaei [12] proposed a reduced switch architecture, which used switches of low ratings, and achieved desired performance by cross connecting the switches. This strategy was tested on an 11-level inverter. Similar reduced switch MLI architectures were presented in [21–[25]. These reduced switched MLI's have the following advantages - less component count, cost effectiveness, and less space occupancy [26]. In [27], a boost inverter following the cascaded H-bridge multilevel inverter (MLI) architecture was presented which omitted the use of inductors, and used capacitors as voltage sources with a single DC source. This design employed 6 switches for getting a 5-level output, and this three-phase inverter was intended for electric vehicle (EV) application. It was implemented in hardware using MOSFETs rated at 180 Amperes and 100 Volts; the controller was implemented in an Altera field programmable gate array (FPGA, device: FLEX 10K). A similar topology for a single phase MLI was presented in [28].

Other than these, Busarello *et al.* [29] presented a small-signal model for analyzing the output of single phase asymmetric cascaded H-bridge MLI. A cascaded MLI-based STATCOM with DC voltages controlled by

control system employing small-signal model was presented in [30]. Khounjahan et al proposed capacitor switched architecture to produce a workable MLI using only a single DC source. They used level shifted sinusoidal pulse width modulation (LS-SPWM) technique to drive their proposed 9-level converter, which they also implemented in hardware. Grid connected PV system was listed as a potential application for their system [31]. Control technique of cascaded H-bridge converter to mitigate unbalanced voltage sags in grid-connected PV by means of reactive and active power injection is presented by Tafti *et al.* [32]. Sajadi *et al.* [33] introduced a method of elimination of selective harmonics in an asymmetric 3-phase cascaded H-bridge inverter intended for STATCOM application. They also implemented their model in hardware, particle swarm optimization (PSO) was used here for switching. A different approach to reduce certain harmonics is presented by Moeini *et al.* [34], where they used current as reference, and compensated current harmonics. This method is verified through hardware implementation as well. Baidya et al proposed a multistep model predictive control for cascaded H-bridge inverters which monitors the references of the control input alongside the current references tracked in traditional single-step techniques. They also used fast sphere decoding algorithm to reduce the computational load of their proposed method [35]. Huang and Huang [36] presented a PWM technique based on feedforward proportional carrier to control a single phase cascaded H-bridge MLI, which was also tested in hardware. Wang *et al.* [37], presented a modified version of phase disposition PWM technique for driving a symmetric MLI, which achieved a THD of 4.88%. Biswas and Khan [38] presented a phase shifted carrier PWM for switching a grid-connected MLI. An improved PWM carrier for PWM was proposed earlier by Podder *et al.* [39]. They also presented a modified 11-level H-bride MLI architecture in [40].

This work expanded on these works by investigating the optimum number of levels (adopting a 5-level reduced switch topology with 6 switches), testing several PWM switching techniques on it and choosing the one with the best performance, and then testing different filters to use in the obtained system to reduce the output THD further. The optimum inverter system obtained through MATLAB/Simulink simulation is then designed in Proteus ISIS for hardware implementation, and implemented using MOSFETs as switches and ATmega2560 microcontrollers. This implementation technique rests in sharp contrast with previous works in the literature in that it uses low cost microcontrollers instead of costly DSP and FPGAs. Though these two devices provide real time response, they have a high cost – and thus cannot be used in mass-produced inverters. Microcontrollers, on the other hand, offer significantly lower cost at the expense of slightly higher latency. But that is negligible and does not affect inverter performance. The general 5-level inverter is implemented as well. Outputs from these hardware are then compared against each other as well as the simulation results, and the discrepancies found are analyzed.

The rest of the paper is organized as follows: section II presents the theoretical background of the multilevel inverters, the PWM switching technique used, reason of using PWM instead of general switching sequences, and filters. The proposed MLI with integrated photo voltaic system is presented in section III. Section IV presents the simulation studies conducted on the modified CHB with different switching strategies. The hardware implementation of the modified and the general 5-level CHB inverter designs are presented in section V. Section VI presents the analysis of the power losses in the conventional MLI and proposed MLI. Section VII provides a discussion of the overall study while presenting a potential use case of the proposed modified inverter in grid-connected PV systems. Finally, the conclusions are drawn in section VII.

II. BACKGROUND

A. CHB MULTILEVEL INVERTER

The primary function of an inverter is to convert DC input voltage into AC output voltage. This AC output can be maintained at a constant amplitude and frequency, or both of them can be varied. Inverter outputs are not generally ideal sine waves, a trait caused mainly by the presence of harmonics which are generated primarily from the nonlinear behavior of the ferromagnetic cores of electrical machines, and from nonlinear behavior of semiconductor devices used in the inverters. However, with high-speed power semiconductor devices and proper switching techniques, the amount of harmonic content in inverter output can be substantially reduced. The cascaded H-bridge inverter type adopted in this work falls into the multilevel voltage source inverter type, and requires multiple DC sources to produce the AC output. Multilevel inverters are an easy way to produce a near-sinusoidal output from DC input. Fig. 1 shows the working principle behind producing a sinusoidal voltage in multilevel inverters using multiple DC voltage levels. There are few methods for calculating fundamental switching time. We used the half height method for the following figures [1]. Through proper switching mechanism, different DC levels are made available at the output for different time periods which produces a near-sinusoidal output. If a single DC source, V_s is used in such an inverter with m number of levels, then the voltage for each level, E_s can be expressed as:

$$E_s = \frac{V_s}{m-1} \tag{1}$$

Switching angle is important for inverter systems as it helps to reduce the harmonic in the output voltage or current. For fundamental Switching frequency, the switching angle calculation method can be calculated using the following method described in the paper [1]

1. Equal Phase Method

$$\alpha_i = i\left(\frac{180^\circ}{m}\right) \tag{2}$$

where $i = 1, 2, \ldots .(m-1)/2$

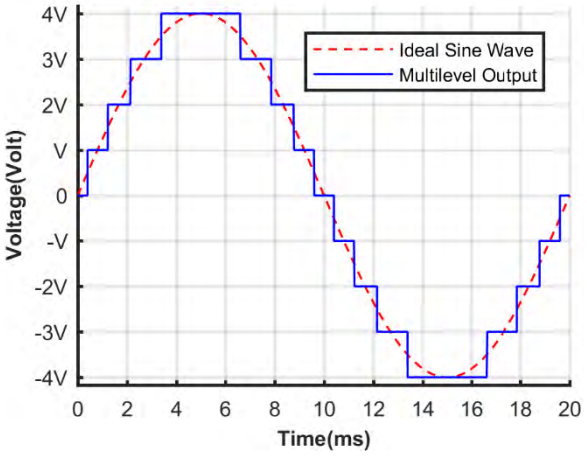


FIGURE 1. Principle of producing sinusoidal output in multilevel inverters from multiple DC voltage levels. Permitting different DC levels available at the output for different time periods produces a near-sinusoidal output.

2. Half Equal Phase Metho

$$\alpha_i = i\left(\frac{180^\circ}{m+1}\right) \tag{3}$$

where $i = 1, 2, \ldots .(m-1)/2$

3. Half Height Method

$$\alpha_i = \sin^{-1}\left(\frac{2i-1}{m-1}\right) \tag{4}$$

where $i = 1, 2, \ldots .(m-1)/2$

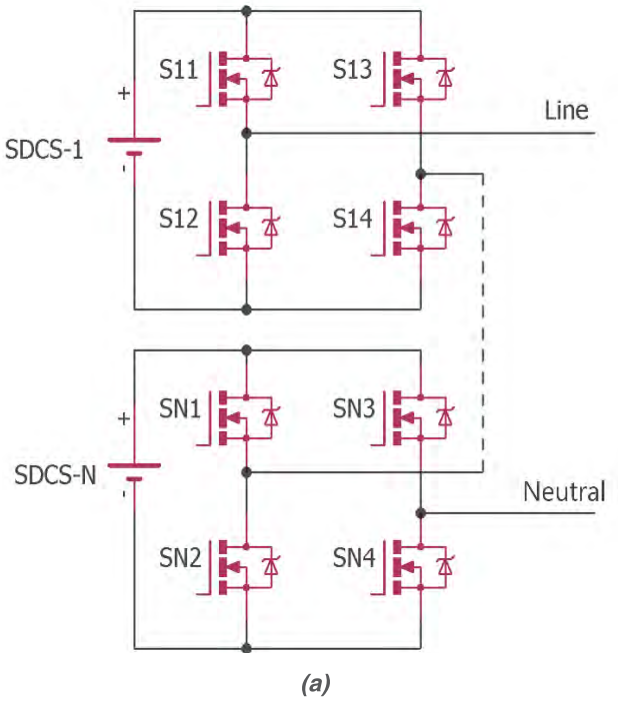
4. Feed Forward metho

$$\alpha_i = \frac{\sin^{-1}(\frac{2i-1}{m-1})}{2} \tag{5}$$

where $i = 1, 2, \ldots .(m-1)/2$

General structure of multilevel inverter is presented in Fig. 2a, with the modified structure used in this paper in Fig. 2b.

Multilevel inverters are modular and simple in design [41], [42], can be used in high voltage and high power applications [12], and their configuration allows to produce a higher voltage without requiring components of high ratings, as the multilevel architecture distributes the total device stress among the individual components [43], [44]. This way, insulated-gate bipolar transistors (IGBT) rated at 3.3 kV can be used for inverters rated for 10 kV DC link voltage. Switching losses also decrease significantly – a 5 level inverter can reduce losses by 60% for rated load. With increased number of inverter levels, the THD in the output decreases, thus the signal quality gets better [12]. Therefore, these inverters also allow the use of smaller output filters along with less common node currents. The effect of increased levels in decreasing THD is shown in Fig. 3, where THDs for multilevel inverters with 10 kHz switching frequency and an LC filter are visualized. It can be seen that THD reduces significantly till 7-level, and then the decreasing rate deteriorates – indicating the necessity of choosing an optimal number of levels, which



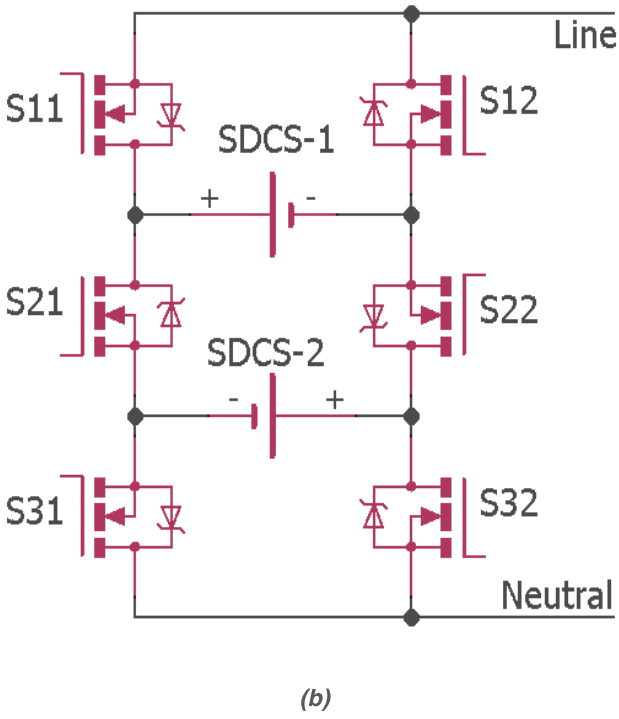


FIGURE 2. (a) General structure of multilevel inverter. Each 4-switch block represents an H-bridge, each equipped with its own DC source. (b) Modified 5 level inverter configuration: this one uses 6 switches instead of the 8 required in the general structure.

was also stated in [45]. Increasing levels also increases the complexity, thus defining the underlying rules to determine the trade-off between THD and level number.

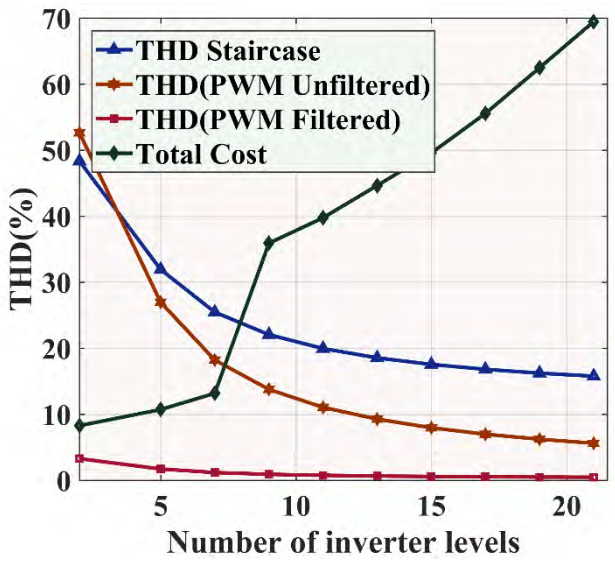


FIGURE 3. Decrease in THD with increasing inverter levels. THD reduces significantly till 7-level, and then the decreasing rate deteriorates.

With increased number of levels, each switch experiences less amount of voltage, and therefore faces less stress [44], [46]–[48]. Multilevel inverters are also capable of generating utility-rated voltages and can work as an alternative to transformers: a 26 level inverter can generate 220 Volts [49], [50]. For PV systems, these inverters also have multiple DC links, which allows independent maximum power point tracking (MPPT) and voltage control in each PV string. Because of that, when mismatch happens between the strings because of a multitude of factors i.e. aging of panels, unequal solar irradiation, cell-type mismatch, and dust on panel surface, the efficiency of the whole system can be better than other converter topologies [50]. But with increased number of switches, conduction loss, complexity, circuit size, cost, and area needed for installation increase, while decreasing the efficiency and reliability [12], [51]. Harmonics in output also reduces with increased number of voltage levels. These features make this inverter design very favorable [52]. The multilevel converter types requiring single DC source (i.e. diode clamped multilevel inverter, and flying capacitors multilevel inverter) have certain disadvantages: the diode clamped type needs a large number of diodes with high inverter levels, and is inconvenient for controlling the flow of real power of the individual converters in setups with multiple converters; the flying capacitor type also requires a large number of capacitors for higher levels which makes the device bulky and expensive, and its control mechanism can be extremely clunky while switching frequency and losses rise during transmitting real power [52]. For producing a 9 level output, the diode clamped multilevel inverter needs 16 power switches, 56 clamping diode and 8 main DC bus capacitance. The capacitor clamped inverter requires 16 switches, 56 clamping capacitors, and 8 main DC bus capacitances to produce a 9-level output. On the other hand, the cascaded inverter configuration can achieve the same voltage levels with less number of components (only 16 switches needed to produce a 9-level output), its packaging can be optimized with proper circuit design, and it offers soft-switching which reduces switching losses and thus device stresses [52]. This structure also offers switching redundancy for inner voltage levels, less susceptibility to electrical shock and short circuit (due to the isolated DC sources), multiple switching opportunity, automatic voltage sharing, less dv/dt stress, switching redundancy, and more reliability when driven with advanced PWM techniques [47], [50], [53]. Because of these, cascaded multilevel inverter with H-bridge topology is chosen for the purpose of this work. This inverter's only shortcoming is that it requires isolated DC sources; but in PV generation, there generally exists multiple isolated DC sources [19] – which makes this device the perfect choice for such applications. This inverter configuration can be of two types, symmetric and asymmetric. The symmetric configuration uses DC sources with the same ratings at each bridge for the multiple source system, while the asymmetric one uses different rated sources [54]. The asymmetric configuration has varied DC voltage ratios, and thus needs different rated semiconductor devices for handling the various switching frequencies and DC blocking voltages – some of which can demand high ratings, and thus negating one of the original features of MLI (using low-rated elements for high-rated device) [12], [54]. They also cause additional difficulties in determining switching angles caused by the asymmetry in selective harmonic elimination equations [55]. Therefore, in this paper, the symmetric architecture is used. In a symmetric cascaded H-bridge multilevel inverter, all the DC sources are connected in an H-bridge formation. For N number of DC sources, this inverter output voltage V_n can be expressed as:

$$V_n = \sum_{H=1}^{N} V_H = \sum_{H=1}^{N} V_{dc}(S_{H1} - S_{H2}) \tag{6}$$

The symmetric cascaded H-bridge MLI can produce an AC output having $2n+1$ voltage levels with n number of H-bridges [11], [54]. Each H-bridge traditionally requires 4 switches, and thus, such a 5-level inverter will generally need 8 switches. In this work, a modified architecture with 6 switches along with the general CHB with 8 switches is presented.

Conduction loss, switching loss, and total harmonic distortion (THD) are the performance parameters that determine the quality of an inverter. Conduction loss results from the collision of electrons with other carriers. Switching loss occurs while turning on a switching device. If expressed by E_T, the actual switching loss can be determined by:

$$E_T = E_{TS} \frac{I_m \sin(\omega t)}{I_c} \frac{V_s}{V_{ce}} \tag{7}$$

where E_{TS} is the sum of switching energy loss of the transistors and the diodes, V_{ce} and I_c are the DC bus voltage and current respectively, V_s is the DC source voltage, I_m is the maximum current, ω is the angular frequency, and t is time.

THD indicates how close a waveform's shape is to that of its fundamental component. It can be expressed as:

$$THD = \frac{\sqrt{\sum_{n=2,3,\ldots}^{\infty} V_n^2}}{V_1} \tag{8}$$

where V_1 is the root mean square (rms) value of the fundamental component of the output voltage of the inverter, and V_n represents harmonic component of n-th order. The 2nd order harmonic is particularly hard to remove, and makes proper timing during switching crucial. In order to get around that, advanced pulse width modulation (PWM) techniques are used in this work to reduce the lower order harmonics in the inverter output.

B. SWITCHING SEQUENCES FOR THE PROPOSED MULTILEVEL INVERTER

In this paper, both general switching sequences and PWM switching are implemented in cascaded modified H-bridge MLI. If the general switching sequences are used, the MOSFETs used as the switching devices toggle between on and off at a frequency of 50 Hz (frequency of the residential supply). But for PWM switching, this frequency becomes more than 1 kHz. Therefore, switching loss for the switching sequences is insignificant as compared to the switching loss for PWM switching. However, PWM follows ideal sinusoidal wave closely, which results in less THD in the inverter output. In the case of using switching sequences, discrete staircase sinewaves or quantized sinewaves are generated, thus the output does not follow ideal sinusoidal shape, producing a higher THD.

5-level output can be generated using the modified cascaded H-bridge configuration (shown in Fig. 2b). In this configuration, two H-bridges are connected in such a way that it can generate 5-level output with reduced number of switches. There are 6 switches in this modified circuit rather than the 8 switches required in the general CHB configuration. The general switching sequence for this architecture to produce 5 voltage levels at the output are shown in Table 1. From Fig. 4, where the operation of the modified CHB inverter by switching sequences is shown, it can be seen that for any case, two-thirds of the total MOSFETs conduct. For the cases of +V and −V outputs, two MOSFETs, and one body diode conducts. For +2V and −2V outputs, 3 MOSFETs conduct. Therefore, it is evident that the modified H-bridge configuration reduces switching and conduction losses as it uses less switching elements to produce the same outputs as the conventional design. But, in this design, body diodes conduct for two voltage levels – which affects signal quality and efficiency. These phenomena are demonstrated in the next section using simulation results and outputs from hardware implementation. The output voltage generated by the modified 5-level inverter using the switching sequences is shown in Fig. 5.

TABLE 1. Switching sequences for modified 5-level cascaded H-bridge inverter.

S11	S12	S21	S22	S31	S32	V_{out}
0	0	0	0	0	0	0
1	0	0	1	0	0	+V
1	0	0	1	1	0	+2V
0	1	1	0	0	0	-V
0	1	1	0	0	1	-2V

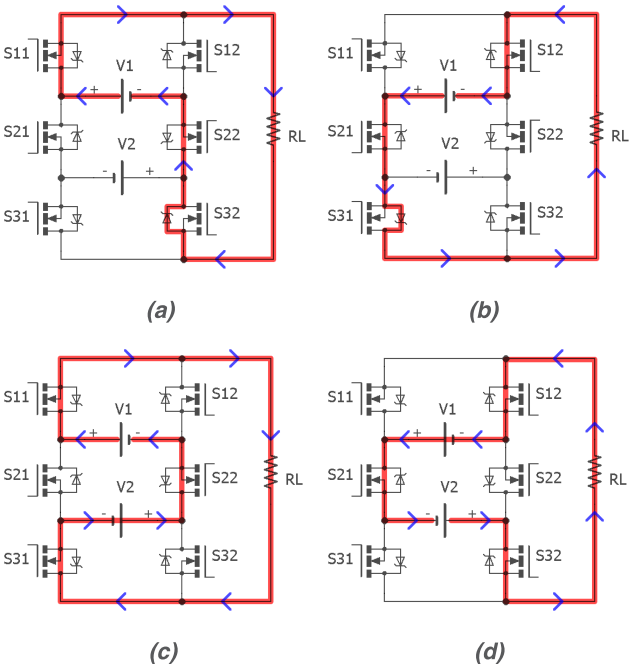


FIGURE 4. Generation of four distinct voltage levels in the modified 5-level cascaded H-bridge multilevel inverter, when operated by switching sequences shown in Table 1. (a) +V. (b) −V. (c) +2V. (d) −2V.

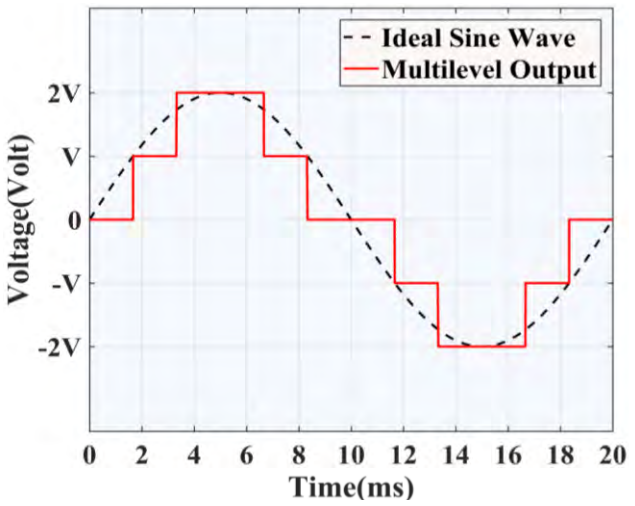


FIGURE 5. Output voltage generated by the general 5-level modified cascaded H-bridge multilevel inverter, when operated by switching sequences shown in Table 1 based on equation (3).

C. MULTILEVEL PWM TECHNIQUES

The problem of using the switching sequences is that they produce a lot of harmonics. To overcome that,

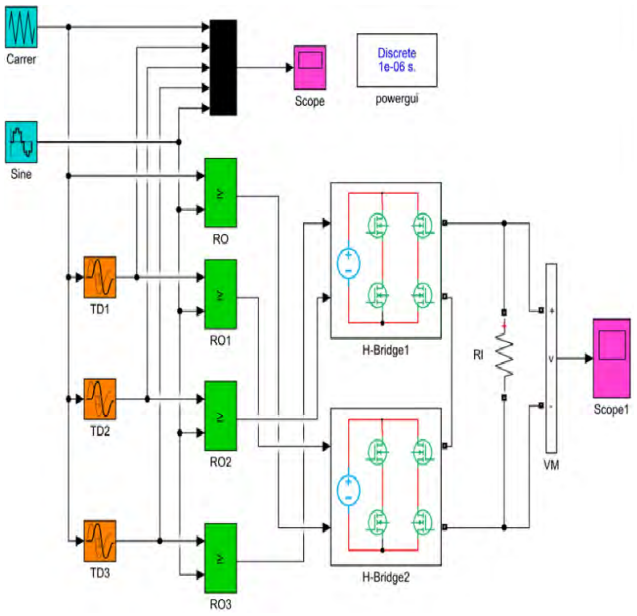


FIGURE 6. Conventional 5-level inverter using 4 phase shifted carrier waves where the shift between two consecutive carriers is 90 degrees.

PWM techniques can be used instead of switching sequences to produce sine waves with better quality – which resembles the ideal sine wave more closely. There are several PWM techniques that can be applied for operating multilevel inverters. These techniques are basically of two types: level shifted pulse width modulation (LS-PWM), and phase shifted pulse width modulation (PS-PWM). There are different schemes to implement the carriers: in-phase disposition (IPD), phase opposite disposition (POD), alternate phase opposite disposition (APOD), and phase shifted carrier (PSC). Different types of these carrier schemes are show in Fig. 8. In this paper, level shifted in-phase disposition (LS-IPD) PWM is used.

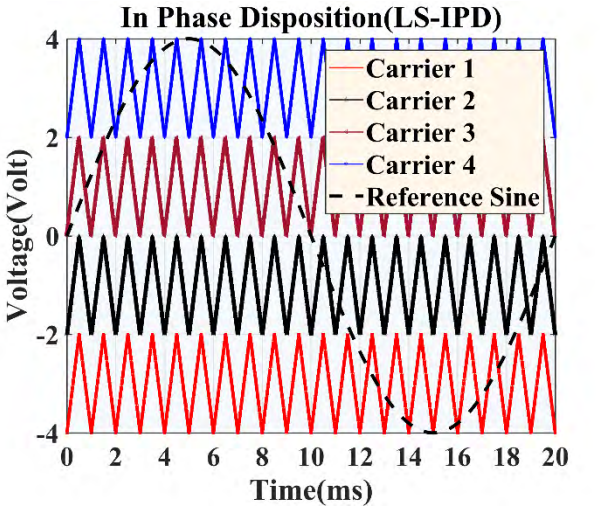
In general, for n-level inverter (n-1) phase shifted carrier signals are required. The phase shift between carriers are governed by the following equation

$$\phi = \frac{180^\circ}{m} \tag{9}$$

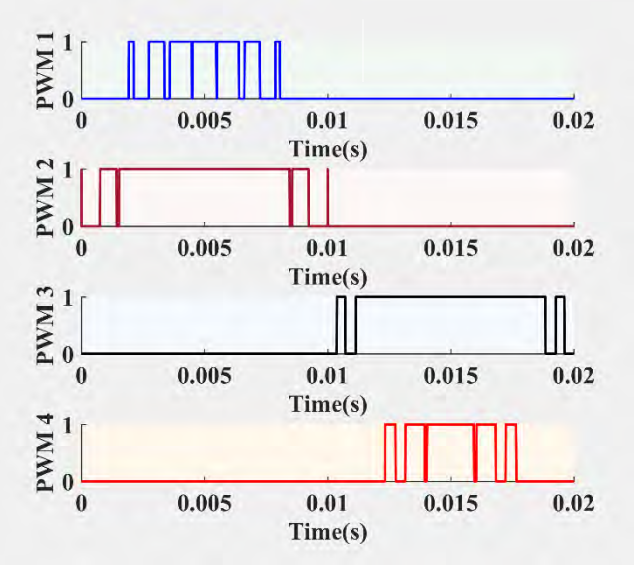
where m is the number of h-bridge used in a multi-level inverter. For 5-level inverter driver by phase shifted carrier, 4 phase shifted carrier waves are required and the phase shift between two consecutive carriers is 90 degrees as shown in Fig. 6. The switching patterns generated from the LS-IPD PWM technique are shown in Fig. 7. The four triangular waveforms are compared with a sinusoidal reference in each case to generate switching signals. The colors of the PWM signals in Fig. 7b indicate the carriers they are generated from, which are shown in Fig. 7a.

D. FILTERS

Even after adopting the harmonic-reducing multilevel structure, there exists some harmonics in the output – resulting from the high switching frequency. A filter is thus required to



(a)



(b)

FIGURE 7. (a) LS-IPD PWM technique, and (b) generated PWM signals. The colors of the PWM signals indicate the carriers they are generated from. When the voltage of a carrier falls below the reference sine wave, the corresponding PWM signal turns on; if the voltage of the carrier rises above the reference, then the PWM signal is turned off.

reduce the harmonic content of the output. Generally, a filter with low cut-off frequency and high attenuation at switching frequency is suitable for this purpose. High attenuation at switching frequency is required because most of the dominating harmonics are created due to the switching. But due to filtering, some power loss also occurs and the magnitude of the fundamental voltage drops. Different types of filters such as L-filter, LC-filter, or LCL-filter can be employed. Here, L indicates inductor and C means capacitor (the names come from the circuit elements used to construct the filters). The L-filter only needs inductor but provides the worst performance among the proposed three. On the other hand, the LCL-filter has the best theoretical performance but introduces

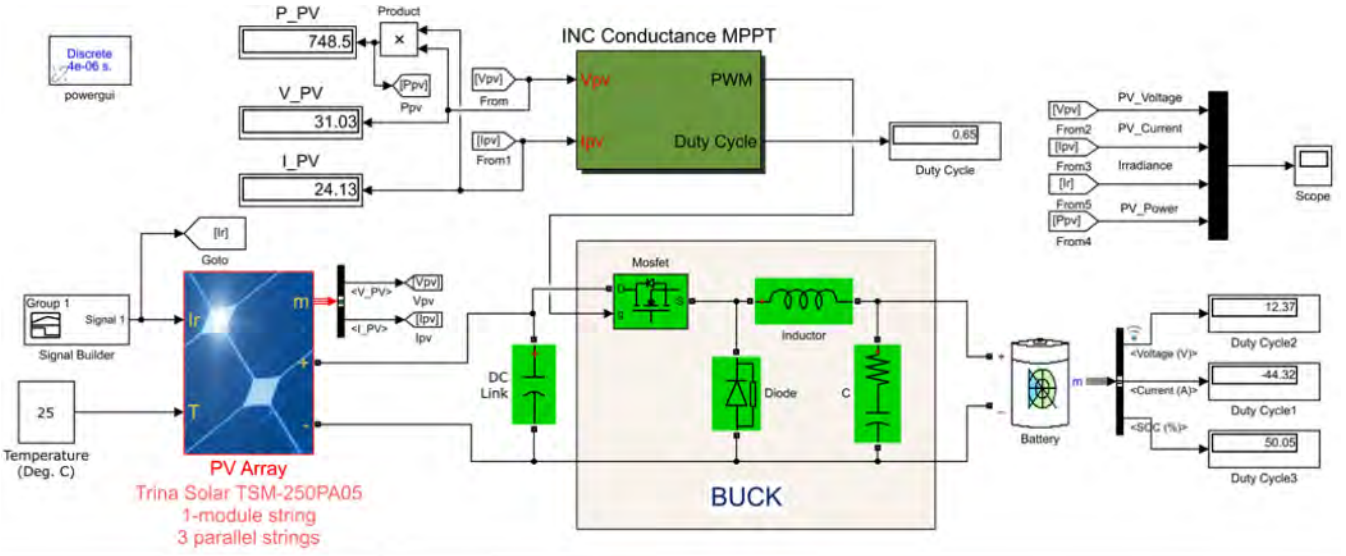


FIGURE 8. Block diagram of the proposed MLI integrated with photo voltaic system using MPPT method along with an energy storage battery and three parallel arrays.

challenges such as increased complexity and cost when implemented at a hardware level. Therefore, the LC-filter is the best choice to be used for inverter application when considering the trade-off between performance and implementation complexity. For increased switching frequency of an inverter, as THD decreases in the output, the filter size and cost also decreases.

III. PROPOSED MLI INTEGRATED WITH PHOTO VOLTAIC SYSTEM

In the proposed multilevel inverter system, the storage battery is charged using solar PV. Maximum Power Point Tracking (MPPT) method is used to extract the maximum power from solar panel. The incremental conductance algorithms was used along with a buck converter in the proposed system to charge the battery at daytime. For the simulation, three parallel Trina Solar TMS-250PA05 panels were used. Each panel produces 249.86W at standard condition (25-degree Celsius temperature and 1000W/m^2 irradiance condition).The block diagram of the entire system is shown in Fig. 8.

The incremental algorithm used in this proposed system is a very popular algorithm because of its higher accuracy in a rapidly changing environment and is represented in Fig. 9. Here the number of step sizes of the converter duty cycle is automatically tuned. The PV array output voltage and current at time k are V (k) and I (k), respectively. dV and dI are the change in the output voltage and current, respectively, for time k-1 to k. The duty cycle (step size) depends on dV and dI. When dI/dV = -I/V or dI = 0, the duty cycle (step size) remains unchanged. Otherwise, it either increases or decreases. The output voltage and current are updated in accordance with the change in the duty cycle.

At maximum power point (MPP), the 3 PV panels can generate up to 749.58W. Fig. 10 shows the output power at different irradiance conditions at 25 degrees Celsius. From the figure, it is evident that the incremental conductance algorithm is extracting the 748.5W power from the aforementioned PV panels which are operating at a capacity of 99.86%. In this case, the switching, conduction, and other losses are not considered.

IV. SIMULATION

In this section, simulations on CHBs having levels up to 21 are conducted to investigate how output THD changes with change in levels. This is done for both the switching sequences and the PWM switching. It is found out from the simulations that changes in THD become insignificant from level 7 onwards. Therefore, the 5-level architecture is chosen as it consumes less cost with favorable THD values. 5-level CHB is simulated in both the general and the modified form for switching frequencies ranging from 1 kHz to 10 kHz to find out THD values with and without filter.

A. SWITCHING SEQUENCES SIMULATION

In this section, multilevel inverters are simulated using just the general switching sequences. One of the Simulink models used in this section- namely, the model of 9-level inverter- is shown in Fig. 11. For higher levels than this, such as 21 level, the number of H-bridges and control signals increase. In this method, control signals switch the MOSFETs in such a fashion that connects or disconnects the voltage sources of the bridge one after another, thus the output signal becomes time varying AC. The output signal obtained through this process looks like a staircase sine wave. In Fig. 12 and 13, the output waveforms for 9-level and 21-level inverters are shown.

As can be seen from these figures, the outputs obtained by using the switching sequences have staircase waveform, and thus the THD of the output signal is significantly high.

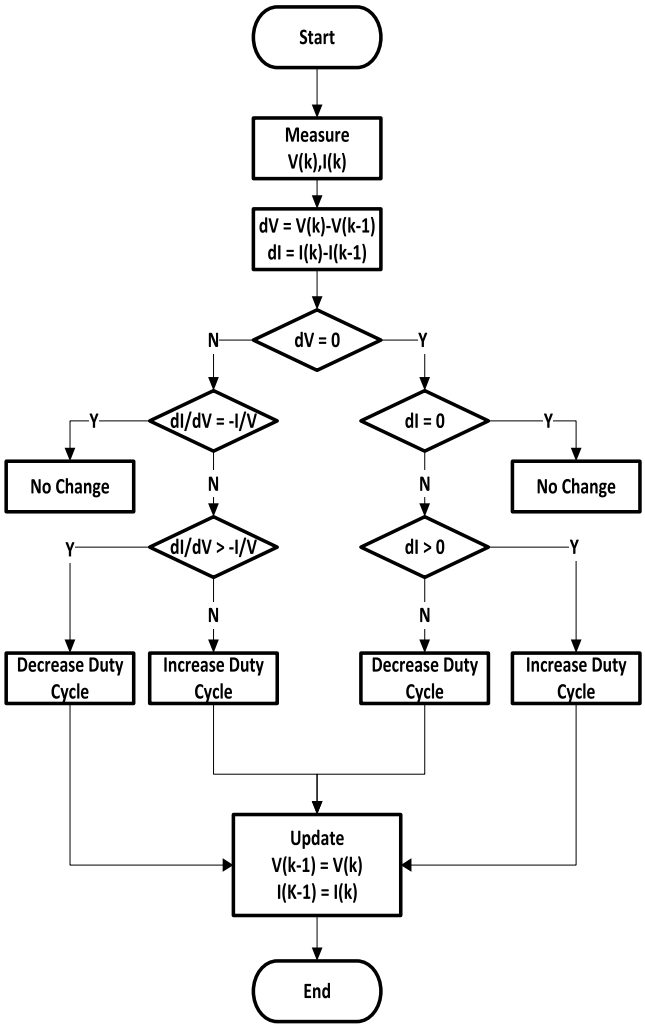


FIGURE 9. Incremental conductance algorithm used in the proposed system to automatically update the step size of the converter duty cycle.

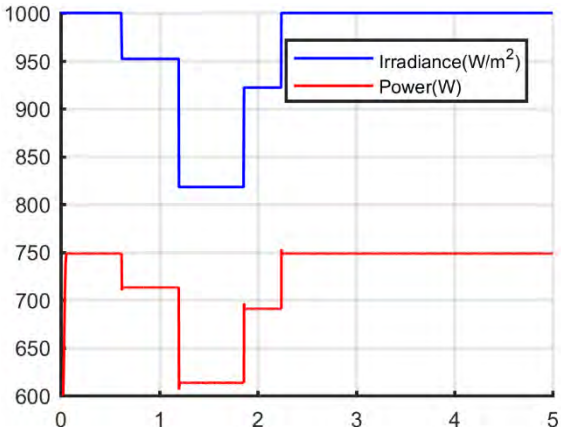


FIGURE 10. Output power of the PV panels for different irradiance conditions at 25 degrees Celsius.

From Fig. 14, it can be observed that the THD varies from 48% for a 2-level inverter to 15% for a 21-level inverter. For a 21-level inverter, the total number of DC sources needed

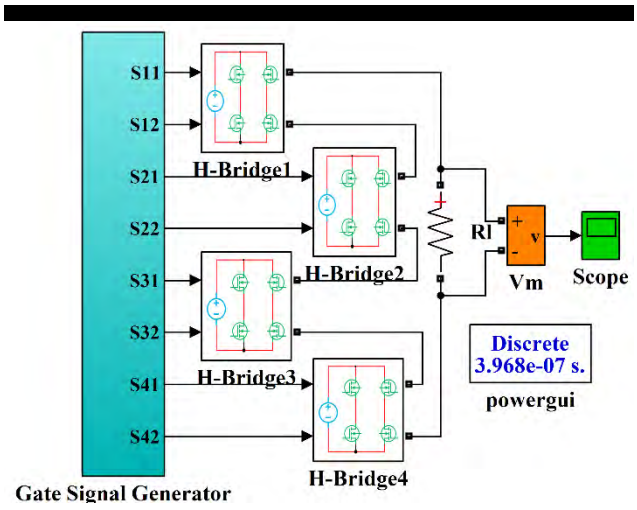


FIGURE 11. Simulink model of a 9-level CHB inverter. It needs 4 H-bridges and 8 control signals. These numbers will increase for increased inverter levels.

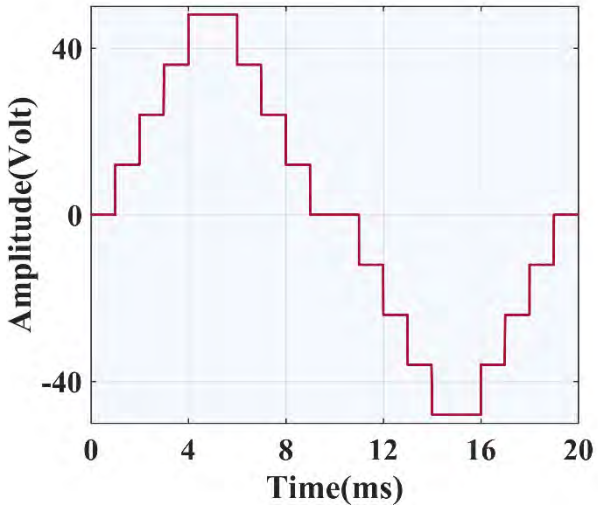


FIGURE 12. Output of a 9-level CHB inverter operated by switching sequences.

is 10. As a result, this inverter can generate sine wave with a peak of 120 V from standalone solar and storage setup, without any transformer or batteries connected in series – all the while maintaining a THD of 15%. The best part of using the switching sequences is that the switching loss is significantly low because of the MOSFETs being switched at 50 Hz only.

B. PWM SWITCHING SIMULATION

The least THD that is obtained is 15% and it comes from using the switching sequences in the 21-level multilevel inverter. However, this value does falls above the maximum THD allowable in the grid [56]. Therefore, an advanced PWM technique is now adopted in this study to reduce the amount of THD. Previously, two types of advanced PWM techniques- namely, level shifted PWM (LS-PWM) and phase

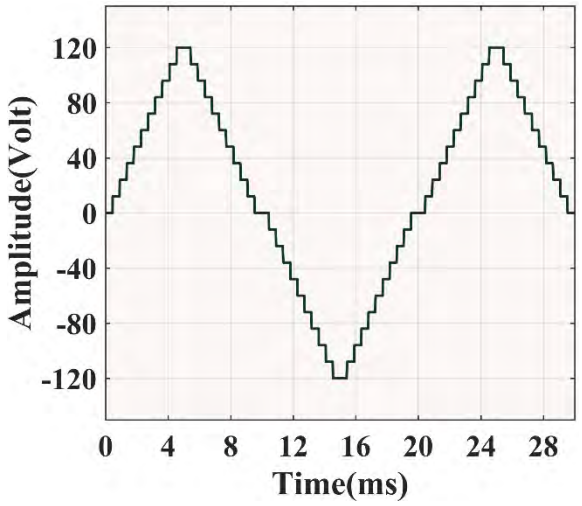


FIGURE 13. Output of a 21-level CHB inverter operated by switching sequences. The increase in levels enabled the output to become more identical to the ideal sinusoidal form as compared to the 9-level output shown in Fig. 12.

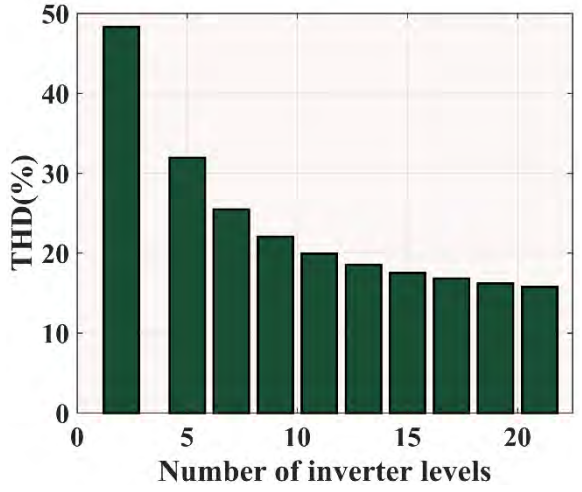


FIGURE 14. Comparison of THD (%) of 2–21 level inverters operated by switching sequences. The trend of reduction in THD with increased levels flattens out from level-9 onwards.

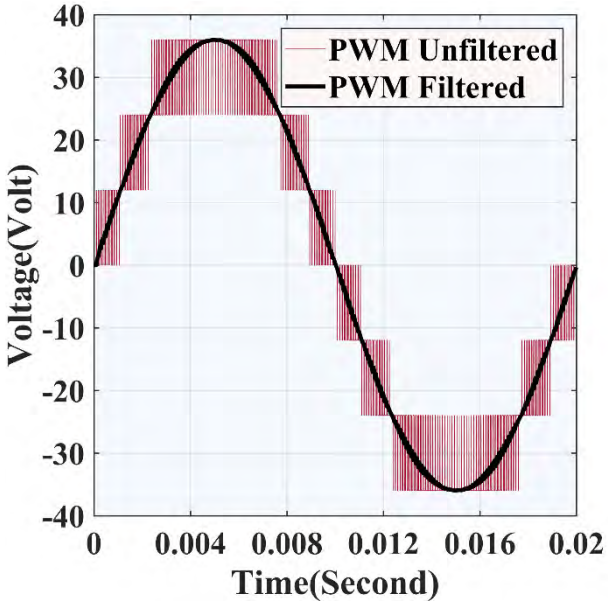


FIGURE 15. Output of a 7-level CHB inverter operated by PWM switching.

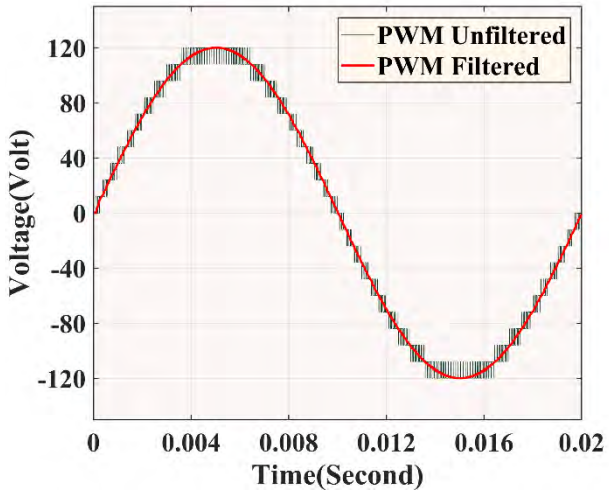


FIGURE 16. Output of 21-level CHB inverter operated by PWM switching. The increase in levels enabled this output to become more identical to the ideal sinusoidal waveform as compared to the 7-level output shown in Fig. 15.

shifted PWM (PS-PWM)- are mentioned. In this subsection, basically LS-PWM is used. LS-PWM can be of two types based on carrier scheme, such as in phase disposition (IPD), and opposite phase disposition (OPD). LS-IPD PWM method is used here to simulate inverters of different levels ranging from 5 to 21. The Simulink model for this simulation is similar to the one shown in Fig. 11, except for a filter block. The simulated output graphs for 5-level, 7-level, and 21-level inverter are shown in Fig. 15 and Fig. 16. From Fig. 15, it is clear that the 21-level inverter produces 120 V peak to peak, which can produce utility-scale pure sine wave of US Standard (single phase residential voltage is 110 in the United States) from 12 V separated DC source, without using transformer to change the amplitude modulation index.

From the simulations conducted in this section, the THDs for the inverters with different levels are figured out. The switching frequency was 10 kHz for all the inverters. The unfiltered THD value here varies from 52% to 5% for 2-level inverters on one end of the spectrum and 21-level inverters on the other (shown in Fig. 17). But, if this output is filtered, the THD values reduce significantly (shown in Fig. 18). With filtering, the THD varies from 3.27 to 0.046- for 2-21 level inverters- switched by LS-IPD PWM. With such low values of THD, it is possible to obtain pure sine wave at the output, which is required in sensitive power electronics-based applications. It is also worth noticing that the THD values differ very little from 12-level onwards.

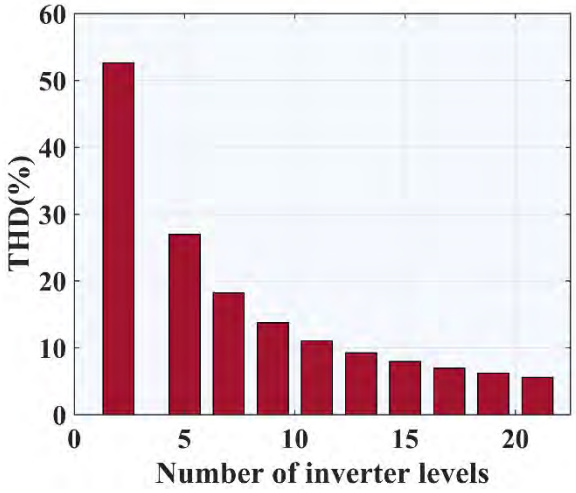


FIGURE 17. Comparison of THD (%) of 2–21 level inverters operated with PWM switching. The trend of reduction in THD with increased levels slows down from level 12 onwards.

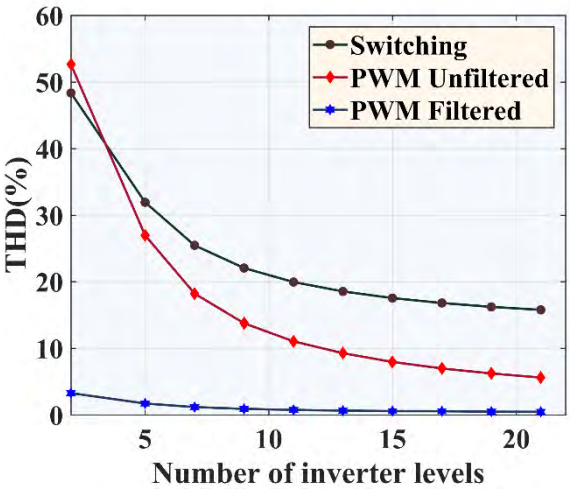


FIGURE 19. Change in THD (%) for switching sequences, PWM unfiltered, and PWM filtered cases for inverters with levels from 2 to 21. Change of THD is insignificant with increase in level from level 7 onwards.

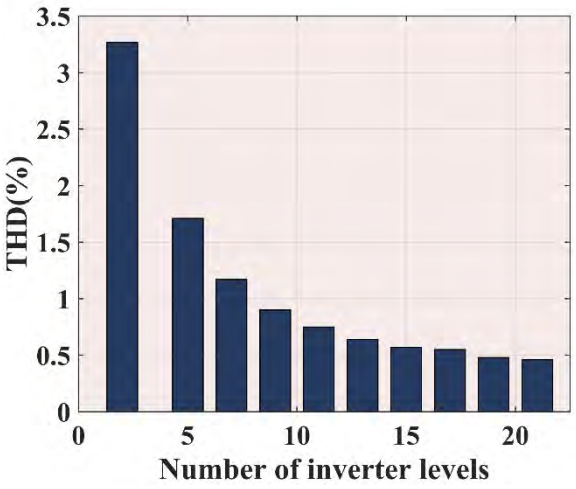


FIGURE 18. Comparison of THD (%) in filtered output of 2–21 level inverters operated with PWM switching. The THD reduces drastically for each inverter after filtering.

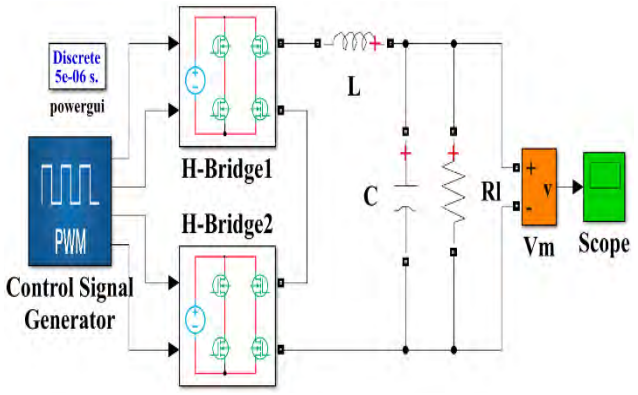


FIGURE 20. Simulink model of a 5-level general cascaded H-bridge inverter with LC filter. This design requires 2 H-bridges and 8 switches.

C. SUMMARY OF THE THD STUDY

Combining all the THD values obtained from the simulations conducted so far, Fig. 19 is prepared to compare the THD values for the 3 cases- namely, switching sequences, PWM unfiltered, and PWM filtered- for inverters with levels ranging from 2 to 21. From this figure, it is evident that change in THD becomes insignificant with increase in level from level 7 onwards, for all the three switching scenarios simulated. As higher-level inverters increase circuit complexities as well as cost, level 7 is the cutoff recommended for hardware implementation of multilevel inverter. If the hardware implementation of inverters having up to 7 levels is considered, the circuitry involved is not that complex as 3 cascaded H-bridges with 6 gate drive signals are required. Therefore, any low-end microcontroller can handle the required calculation complexity.

D. 5-LEVEL INVERTER

In this subsection, a 5-level inverter is experimented on for different carrier frequencies. In this study, both the general cascaded H-bridge and the modified cascaded H-bridge configurations are worked on, which are shown in Fig. 20 and Fig. 21, respectively. The component values used for these simulations are shown in Table 3. The 5-level inverter needs 2 H-brides and 8 switches in total, whereas the modified CHB needs only 6 switches. Both of these configurations have their own advantages and disadvantages, as discussed earlier. Major advantages of using the modified CHB are reduction of cost for switching devices by 25%, and decreased conduction loss across the switches. Switching loss is the dominant loss among all types of losses in power electronics systems, and it increases with increase in the switching frequency.

Keeping the parameters same for both configurations (as shown in Table 2), the output voltage shapes for two different switching frequencies are shown in Fig. 22 (for 2 kHz) and Fig. 23 (for 6 kHz). From these figures, it is clear that the

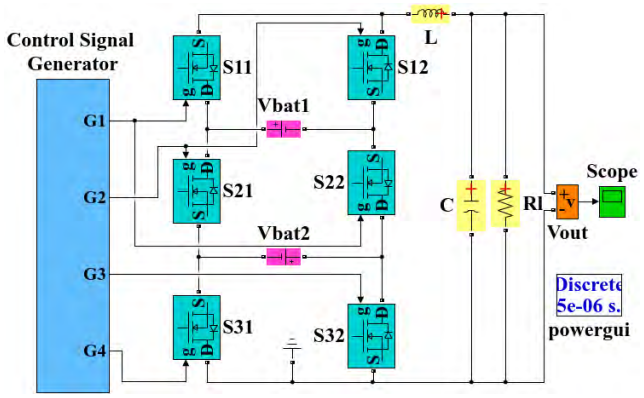


FIGURE 21. Simulink model of a 5-level modified cascaded H-bridge inverter with LC filter. This design requires 6 switches, which is 2 less than the general design.

TABLE 2. Component values used in simulating the 5-level cascaded H-bridge inverter models.

Symbol	Standard Value	Range of Variation
S11	MOSFET	N/A
S12	MOSFET	N/A
S21	MOSFET	N/A
S22	MOSFET	N/A
S31	MOSFET	N/A
S32	MOSFET	N/A
Vbat1	12V	10V-14V
Vbat2	12V	10-14V
L		1mH-10mH
C	$5\mu F$	$5\mu F - 10\mu F$
R_{load}	24Ω	$1\Omega - 50\Omega$

N/A: Not applicable

general CHB signal quality is better than the modified CHB signal quality. This is because in the modified CHB configuration, non-linearity is introduced from the diode conductions required for generating +V and −V voltage levels (as shown in Fig. 4a and Fig. 4b).

E. SIGNAL QUALITY COMPARISON FOR GENERAL AND MODIFIED CHB INVERTERS

For designing the filter (which is to be added for reducing the THD value), the resonance frequencies for each switching frequency need to be calculated. In order to do that, a general method to determine the L and C values is adopted here. The filter's resonance frequency is governed by the following equation:

$$10F_m \leq F_r \leq \frac{F_{sw}}{2} \tag{10}$$

The probable maximum and minimum values of resonance frequency are calculated using the following equation:

$$F_r = \frac{F_r(\min.) + F_r(\max.)}{2} \tag{11}$$

where, $F_r(\min.) = 10F_m$ and $F_r(\max.) = \frac{F_{sw}}{2}$. F_m is the output voltage frequency which is 50 Hz, F_{sw} is the switching frequency, and F_r is the low-pass filter cut-off frequency.

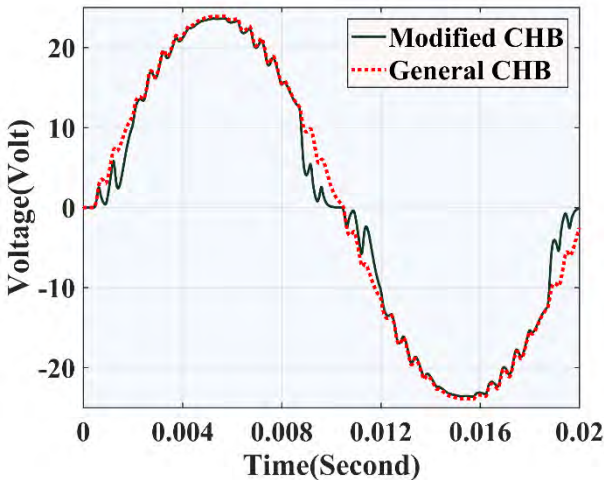


FIGURE 22. Outputs of 5-level general and modified CHB at 2 kHz switching frequency. The general CHB signal quality is better than the modified CHB signal quality because of the presence of non-linearity in the modified design.

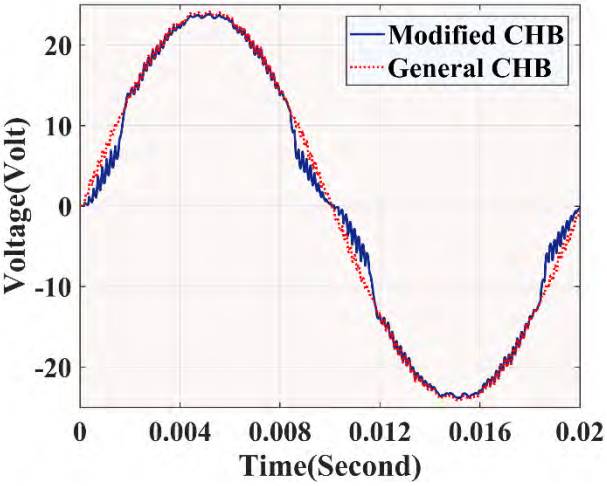


FIGURE 23. Outputs of 5-level general and modified CHB at 6 kHz switching frequency. The general CHB signal quality is better than the modified CHB signal quality because of the presence of non-linearity in the modified design.

Using equation (12), the LC filter is designed for the different frequencies ranging from 1 kHz to 30 kHz with 1 kHz intervals:

$$F_r = \frac{1}{2\pi\sqrt{LC}} \tag{12}$$

where, L and C represent the values of inductor and capacitor respectively. The values of filter elements calculated according to these equations for different switching frequencies are showed in Table 3. The output voltage of the modified CHB for 4 kHz PWM switching frquency, with and without using a filter, is shown in Fig. 24(a). From this figure, it is evident that adding a filter reduces the THD. The current waveform of the modified CHB for 4 kHz PWM switching frquency without using a filter is shown in Fig. 24(b).

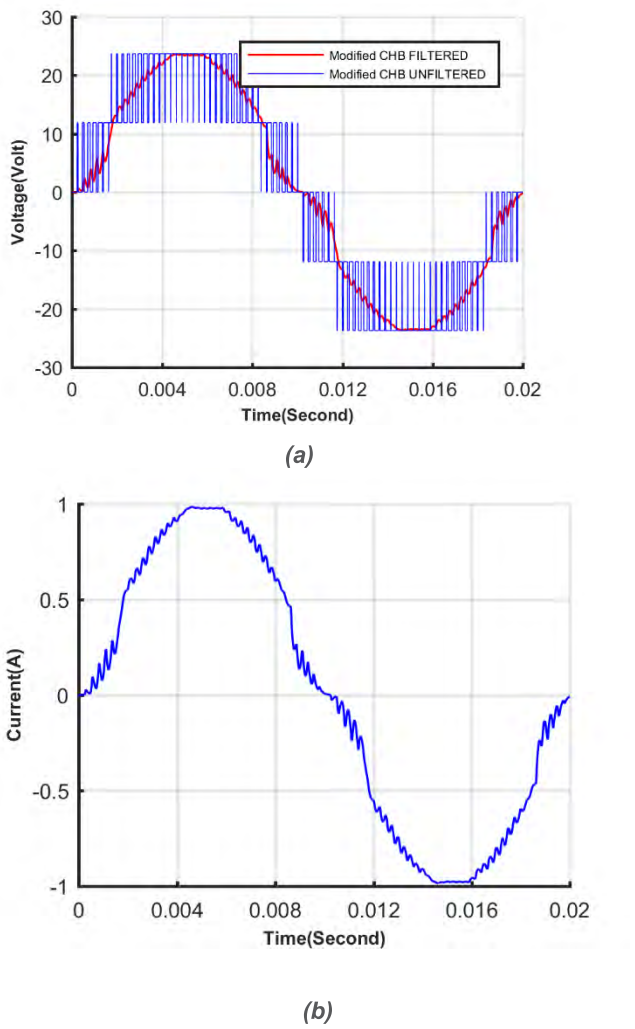


FIGURE 24. (a) The filtered and unfiltered output voltage of the modified CHB for 4 kHz PWM switching frequency, and (b) the filtered output current of the modified CHB for 4 kHz PWM switching frequency.

TABLE 3. Filter element value calculation for different switching frequencies.

F_{sw}	F_r(min)	F_r(max)	F_r	C (F)	L (H)
1000	500	500	500	5.00E-06	2.03E-02
2000	500	1000	750	5.00E-06	9.01E-03
3000	500	1500	1000	5.00E-06	5.07E-03
4000	500	2000	1250	5.00E-06	3.24E-03
5000	500	2500	1500	5.00E-06	2.25E-03
6000	500	3000	1750	5.00E-06	1.65E-03
7000	500	3500	2000	5.00E-06	1.27E-03
8000	500	4000	2250	5.00E-06	1.00E-03
9000	500	4500	2500	5.00E-06	8.11E-04
10000	500	5000	2750	5.00E-06	6.70E-04
20000	500	10000	5250	5.00E-06	1.84E-04
30000	500	15000	7750	5.00E-06	8.43E-05

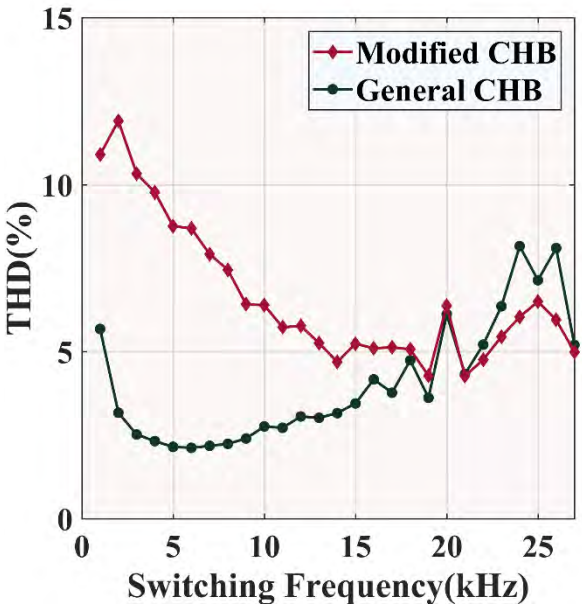


FIGURE 25. Comparison of THD for general CHB and modified CHB inverters at different switching frequencies. THD is less in the general design for up to 22 kHz.

Using the calculated values, the systems for both general CHB and modified CHB configurations are simulated. THD comparison of these two cases are shown in Fig. 25. From this figure, it is evident that THD is much less for the general CHB configuration than for the modified CHB configuration – which indicates that the general CHB configuration can generate better quality sinusoidal signal. The reason behind this is the much greater non-linearity in the modified CHB configuration – resulting from body diode conduction required for generating a few voltage levels. From Fig. 25, it is also evident that the minimum THD for the general CHB configuration occurs for 6 kHz. From this observation, it can be assumed that 6 kHz is the suitable operating frequency for the general CHB configuration.

V. HARDWARE IMPLEMENTATION

So far, inverters with different levels for a wide range of switching frequency are simulated. In this section, 5-level CHB inverter for both general CHB and modified CHB configurations are implemented in hardware. Also, both switching sequences and advanced PWM switching techniques are employed. The outputs obtained from the hardware devices are then compared with the simulated results. For the convenience of demonstration, this section is divided into the following two subsections.

A. MODIFIED 5-LEVEL CHB INVERTER WITH SWITCHING SEQUENCES

Hardware using the switching sequences for operating the MOSFETs is the simplest implementation of multilevel inverter, as generating the control signals is not challenging. The main challenge of the modified CHB configuration is driving the gates of the MOSFETs. The hardware prototype is simulated in Proteus ISIS 7.1. For turning on/off a MOSFET,

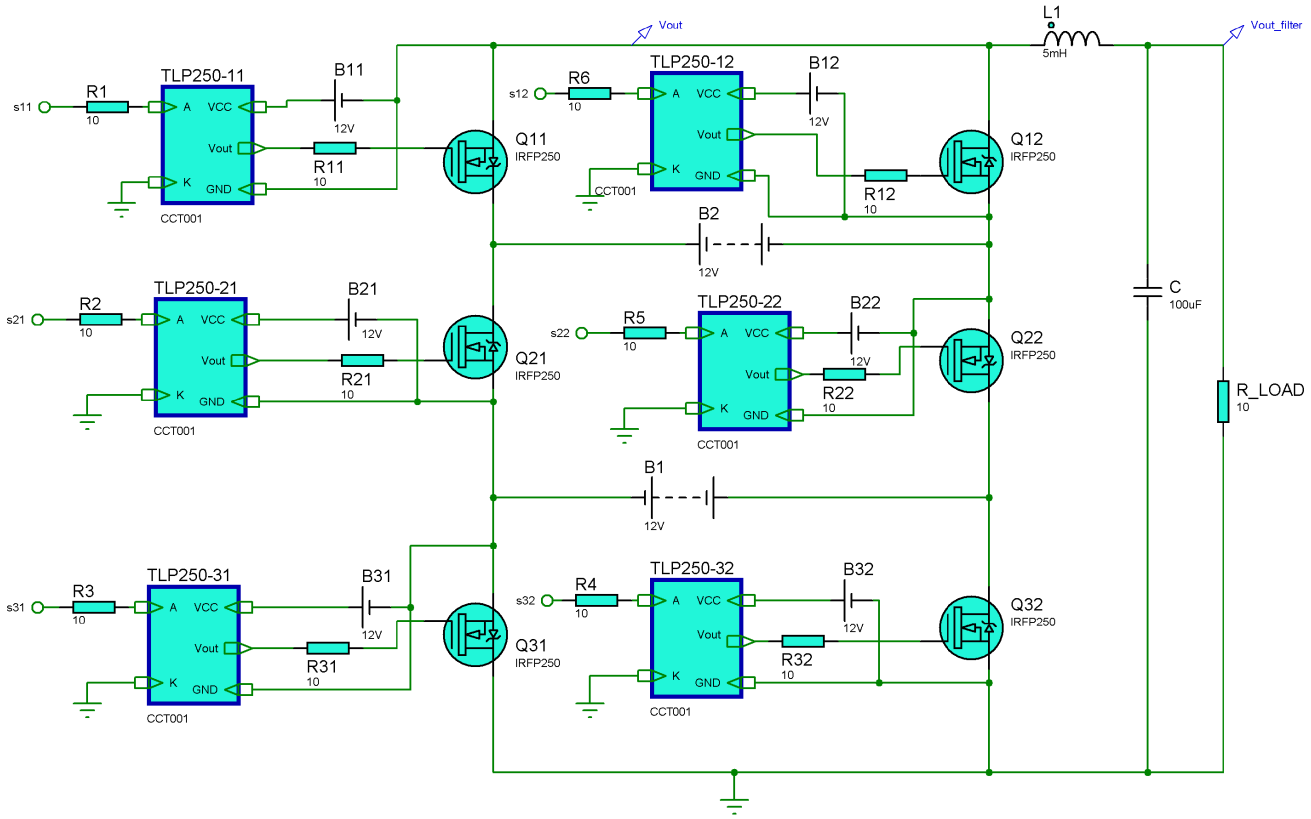


FIGURE 26. Driving mechanism of a 5-level modified CHB inverter driven by switching sequences, designed in Proteus for simulation.

voltage greater than threshold voltage has to be applied across the gate and the source. With careful observation of the modified CHB configuration in Fig. 21, it can be seen that the sources of the MOSFETs are not similar to the ones of the general H-bridge configuration. These sources are oriented in different points, and thus the modified configuration cannot be driven by the bootstrap mechanism [57]. There are two driving mechanisms that suit this configuration: gate drive transformer, and isolated DC source with optocoupler.

Optocouplers are chosen to build the driving mechanism in this paper. It can be seen from the Proteus simulation that separate DC sources are used for driving each MOSFET. This is impractical, and not an economic way to drive the MOSFETs. This technique is optimized for PWM switching, which is shown in Fig. 26. Using this configuration, all the MOSFETs and the microcontroller can be driven with only one DC source, which is labeled in Fig. 27 as $V_{control}$. The hardware setup of a 5-level modified CHB inverter driven by switching sequences, and the corresponding output are shown in Fig. 27 and Fig. 28, respectively. The output signal produced from this implemented hardware is consistent with the simulation results obtained in section III.A.

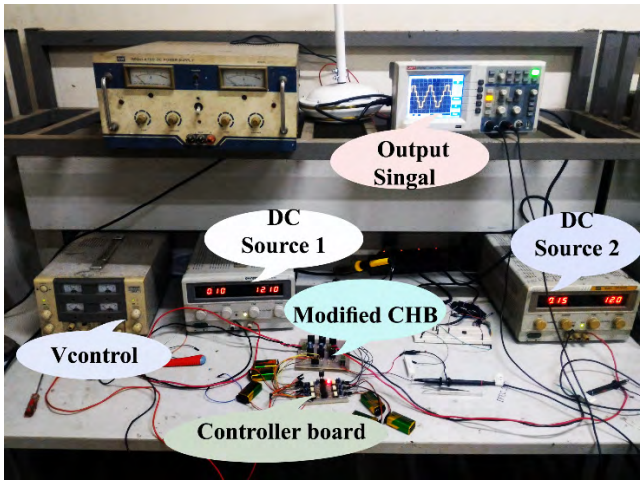


FIGURE 27. Hardware setup of a 5-level modified CHB inverter driven by switching sequences.

B. MODIFIED 5-LEVEL CHB INVERTER WITH ADVANCED PWM SWITCHING

As discussed earlier in sections II and III, because of the harmonic content in the inverter output obtained by using switching sequences, PWM is used to reduce the THD. In this stage of hardware implementation, this PWM technique is implemented to drive the proposed single phase inverter circuit. Similar to the simulation, four carrier frequencies are compared with a reference sinusoidal wave to generate four signals to drive the MOSFETs. For these four switching signals, two 16-bit timers are required in the microcontroller.

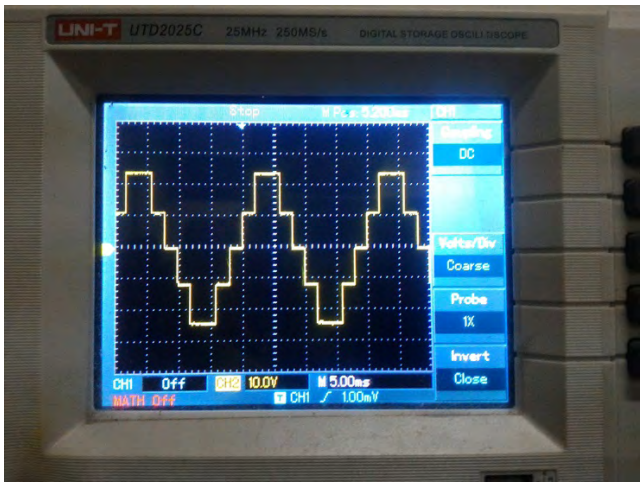


FIGURE 28. Output of the 5-level modified CHB inverter driven by switching sequences. It shows the staircase pattern of outputs obtained by switching sequences, as seen in the simulations.

An ATmega2560 is used in this stage, which has four 16-bit timers – thus meeting the design requirements [58]. A major problem that surfaced in this stage is the generation of pulse value on-the-fly. The microcontroller used is an 8-bit one, and its maximum operating speed is 16 MHz, which means it can handle only 16 mega instruction cycles per second (MIPS) – which barred it from calculating the pulse width for each sample on the fly. To overcome this impediment, it is decided to pre-calculate the PWM of each sample, and thus two look-up tables are prepared calculating the pulse width of different PWM techniques using MATLAB and Simulink.

ATmega2560 has four timers available, with three PWM channels at each timer. Timer 1 and timer 3 are used in this hardware setup for PWM generation, using two of each of these timers' available PWM channels. To operate the microcontroller, certain registers need to be configured as instructed by the datasheet [58]. For the desired operation, timer counter registers ICR1 and ICR3 are used for defining PWM frequency for timer 1 and timer 3. For defining pulse width, OCR1A and OCR1B registers are used for the two channels of timer 1, while configuring OCR3A and OCR3B registers served the purpose for the two channels of timer 3. The algorithm for generating the PWM signals from the microcontroller is shown in Fig. 29. If the PWM frequency is considered 4 kHz, the total number of samples for 50 Hz sinusoidal wave is 80. For this scenario, the value of N in the figure is 80, and n represents the index variable for the PWM samples.

Because of the reduced number of switches in the proposed inverter architecture, a few challenges arise while implementing it in hardware which are absent in the case of a conventional CHB multilevel inverter. In the conventional design, the MOSFETs can be driven using bootstrap driving mechanism. But for the design with reduced switches, this is not possible. MOSFETs can only be turned on when the gate pulse is provided with respect to the source terminal.

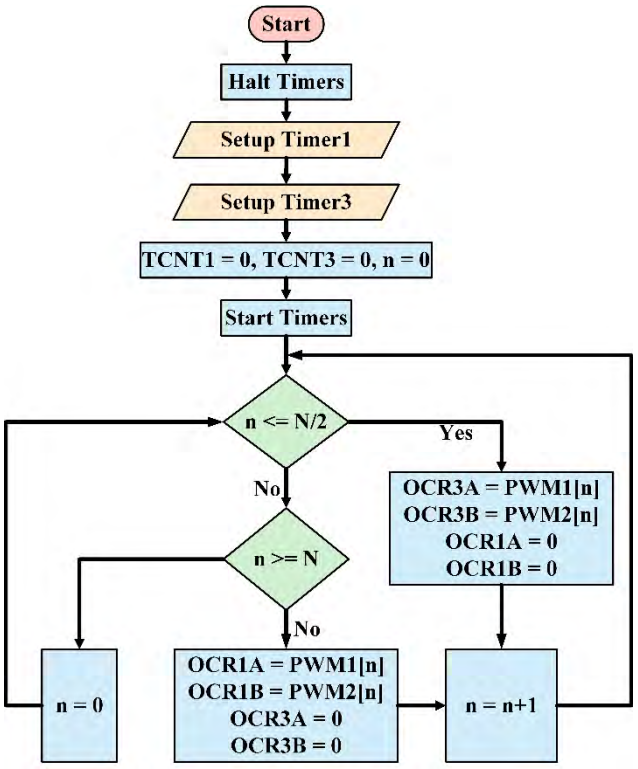


FIGURE 29. Algorithm to operate ATmega2560 to generate PWM signals to drive the proposed inverter. Timer counter registers ICR1 and ICR3 are used for defining PWM frequency for timer 1 and timer 3. For defining pulse width, OCR1A and OCR1B PWM pulse width registers are used for the two channels of timer 1, while configuring OCR3A and OCR3B registers served the purpose for channels 1 and 2 of timer 3.

The proposed inverter, with MOSFET control mechanism is shown in Fig. 30. From this figure, it can be seen that isolated DC-DC converter modules are required for each MOSFET gate driving mechanism, which is not required in the case of a conventional CHB configuration. These isolated DC-DC converters power up totem-pole drive optocouplers, which receive signals from the microcontroller, and this mechanism drives the MOSFETs to produce the multilevel output. Fig. 31 shows the whole inverter system in hardware, while Fig. 32 shows the output of this system for 4 kHz switching frequency. This output is much closer to the ideal sinusoidal shape as compared to the one obtained by switching sequences in the previous subsection (shown in Fig. 28). Table 4 lists the components used in the hardware circuit.

C. GENERAL 5-LEVEL CHB INVERTER

Simulation results have indicated that signal quality of the general cascaded H-bridge inverter is better than that of the modified configuration. Therefore, in this subsection, the general CHB is implemented and tested in hardware. These hardware setups are shown in the Fig. 33 and Fig. 34. For the general 5-level CHB implementation, two H-bridges are needed, which are shown in the figures as two separate modules. The design adopted in this paper is completely modular, including the driver circuit and the H-bridge.

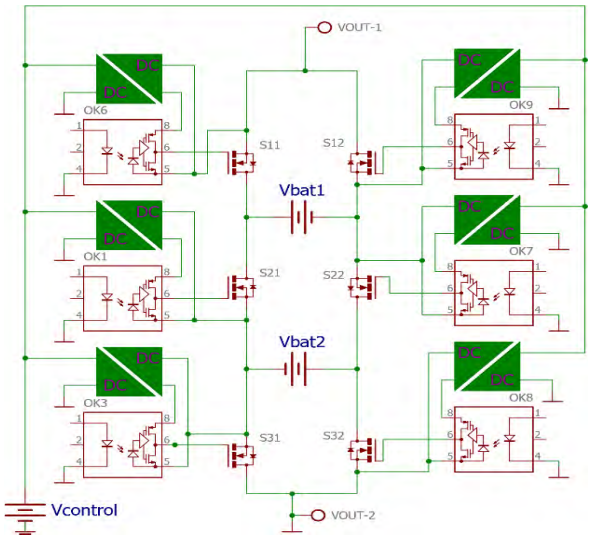


FIGURE 30. Proposed inverter with MOSFET control mechanism. Isolated DC-DC converter modules are needed for each MOSFET gate driving mechanism, which are powered up by totem-pole drive optocouplers, and they receive signals from the microcontroller.

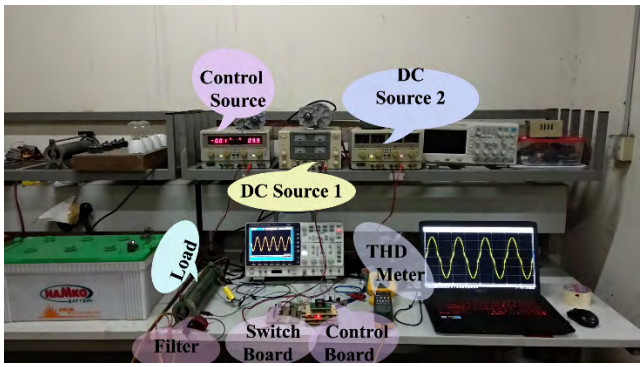


FIGURE 31. Complete hardware setup for the proposed modified 5-level CHB inverter.

The motivation behind this modular architecture is to construct inverters with any required number of levels. A single module includes 2 half-bridge drivers, and 1 H-bridge, as shown in Fig. 34. The output graphs, seen in the oscilloscopes in Fig. 33 and Fig. 34, imitate the graphs obtained in the simulations very closely. In this hardware setup, incandescent lamps rated for the grid voltage (220 V) are driven using a step-up transformer.

The microcontroller used for this general CHB implementation is the same one employed for the modified CHB, which is ATmega2560. A very low cost MOSFET driver is introduced in this section compared to the previous mechanisms used in this paper. It is achieved by designing an isolated MOSFET driver by modifying the existing non-isolated integrated circuit (IC), which reduces the cost of driving the MOSFETs by a considerable margin. Non-isolated half bridge driver IR-2111 is used for this MOSFET driver. IR2111 is a half-bridge driver. It can drive low side and high side MOSFETs [59]. But when two H-bridges are driven using IR2111 MOSFET driver, it shorts the grounds of two isolated sources: SDCS-1 and SDCS-N (shown in Fig. 33). Therefore, the traditional non-isolated MOSFET driver is modified into isolated MOSFET driver using simple optocouplers OK1 and OK2, as shown in Fig. 35. Fig. 36 shows the disassembled circuit to provide a better idea of the circuit blocks. Table 5 shows the THD values obtained from this setup for different switching frequencies. The highest frequency, 4 kHz, generated the least THD, as expected.

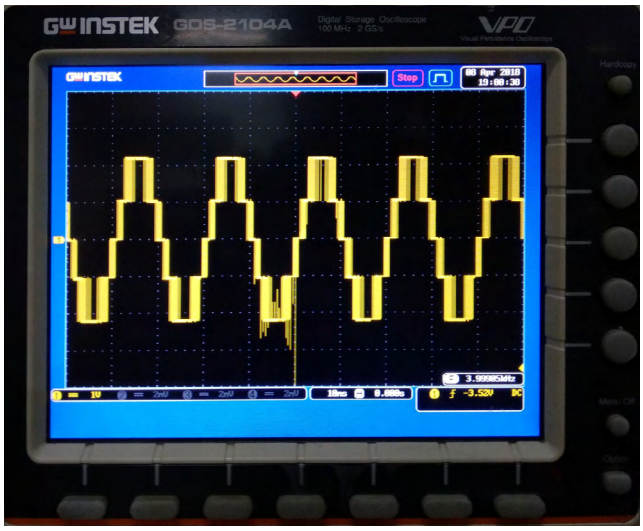


FIGURE 32. The output of the proposed 5-level multilevel CHB inverter with 4 kHz PWM switching frequency, implemented in hardware.

TABLE 4. Hardware components Used to Implement the Proposed 5-Level Multilevel CHB Inverter.

Symbol	Name	Ratings	Used value
S11	MOSFET(IRFP250)		
S21	MOSFET(IRFP250)		
S31	MOSFET(IRFP250)		
S12	MOSFET(IRFP250)		
S22	MOSFET(IRFP250)		
S32	MOSFET(IRFP250)		
R1,R2,R3,R4,R5,R6	Resistor	0.25W	10k
R7, R8, R9, R10, R11, R12	Resistor	0.25W	10
C1, C2	Capacitor		1000 uF
Ok1, OK2, OK3, Ok4, OK5, OK6	Optocoupler		TLP250
U1	Microcontroller		Atmega2560
DC1,DC2,DC3,DC4, DC5,Dc6	Isolated DC-DC Converter Module		

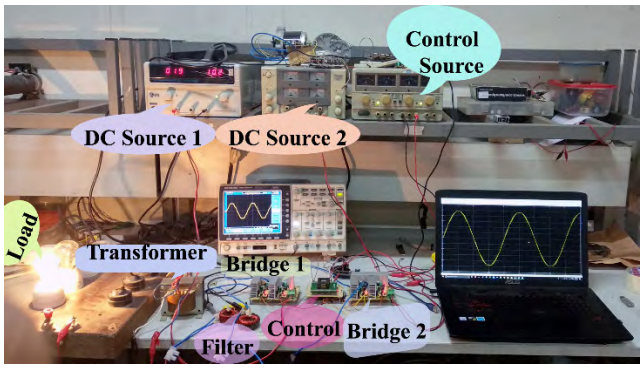


FIGURE 33. Hardware setup of a general 5-level CHB inverter, with incandescent lamps rated for the grid voltage (220 V) as loads.

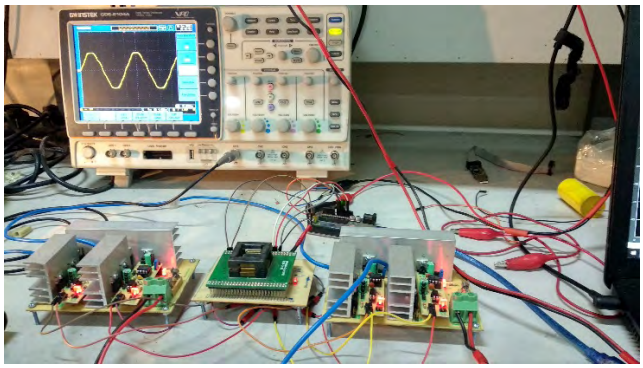


FIGURE 34. Filtered output of the general 5-level CHB inverter implemented in hardware.

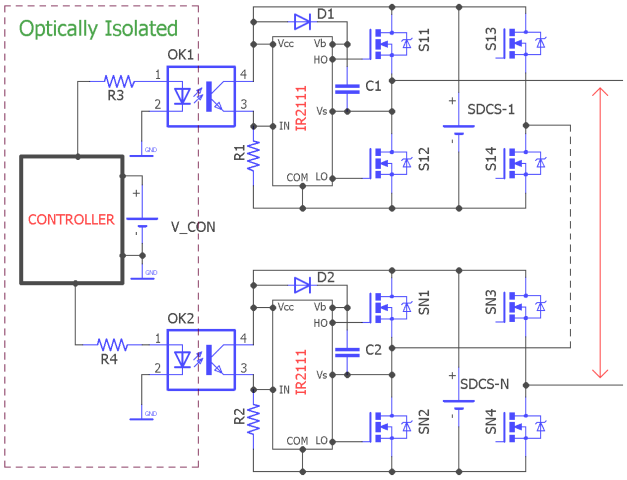


FIGURE 35. Isolated MOSFET driver for driving the general CHB inverter, designed by modifying the IR2111 MOSFET driver with added optocouplers OK1 and OK2.

VI. ANALYSIS OF POWER LOSSES

Power loss analysis is a must for cost optimization and also for cooling system design of an MLI. In an MLI system, the total power loss is the sum of the losses occurring in MOSFET and diode. Two types of power loss occur in a MOSFET – the switching loss and the conduction loss.

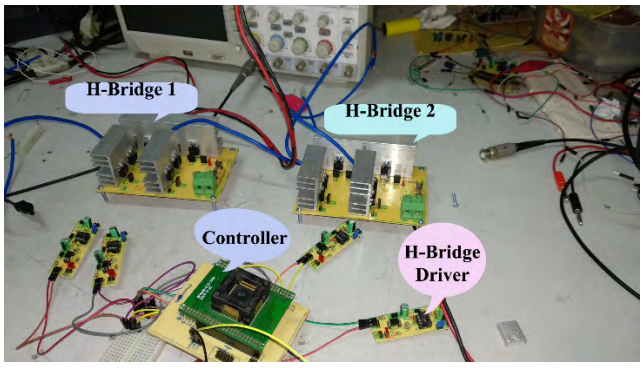


FIGURE 36. Disassembled circuit of the general 5-level CHB inverter, showing the building blocks.

TABLE 5. THD values obtained from the hardware setup of a general 5-level CHB inverter for different switching frequencies.

Switching Frequency	THD
2 kHz	9.2%
3 kHz	8.01%
4 kHz	5.08%

On the other hand, overall diode power loss consists of the conduction loss, the switching loss, and the reverse leakage loss. The switching loss is more dominant at high switching frequencies, whereas the conduction loss is more dominant at lower frequencies. As the number of levels of MLI increases, the number of switches increases and thus the switching loss increases.

A. POWER LOSS IN THE MOSFET

The conduction loss and the switching loss occurring in the MOSFET are denoted by $P_{conduction}$ and $P_{switching}$ respectively. Thus the overall power loss in the MOSFET is

$$P_{loss} = P_{conduction} + P_{switching} \tag{13}$$

The conduction loss and the switching loss are calculated using equations (14) (15), respectively.

$$P_{conduction} = I_D^2.Rds\,(hot)\,.D \tag{14}$$

$$P_{switching} = \frac{V.I_D}{2}.\left(T_{on} + T_{off}\right).F_{Sw} + C_{oss}.V^2.F_{sw} \tag{15}$$

Here, duty cycle, switching frequency, and MOSFET output capacitance is denoted by D, F_{sw}, and C_{oss}, respectively. We used IRF3205 MOSFET for H Bridge and the switching frequency is 4 kHz. The different symbols used in equation (13), (14), (15), their corresponding names, and values are presented in Table 6.

The power losses occurring in each MOSFET are presented in Table 7.

B. POWER LOSS IN THE DIODE

The conduction loss, switching loss and reverse leakage loss occurring in the diode are denoted by $P_{conduction}$, $P_{switching}$

TABLE 6. Table of parameter values of MOSFET.

Symbol	Name	Value
R_{ds}	Drain to source resistance	$8.0m\Omega$
T_{on}	Turn on time	14nS
T_{off}	Turn off time	50nS
C_{oss}	Output capacitance	781pF
F_{sw}	Switching frequency	4 kHz
D	Duty cycle	0.5
I_D	Drain current	1A
V	Forward voltage	12V

TABLE 7. Different power losses in MOSFET.

$Pconduction$	$4mW$
$P_{switching}$	$1.986mW$
P_{loss}	$5.986mW$

TABLE 8. Table of parameter values of diode.

Symbol	Name	Value
D	Duty cycle	0.5
V_f	Forward voltage Drop	$1.3V$
I_r	Reverse Leakage Current	$250\ \mu A$
V_r	Reverse Voltage	$12V$
T_{rr}	Reverse Recovery Time	$104ns$(max)
F_{sw}	Switching Frequency	4 kHz
I_f	Max Forward Current	1
I_{rrm}	Max Recovery Current	$2.067A$

and $P_{reverse}$, respectively. Then the overall power loss in the diode is

$$P_{loss} = P_{conduction} + P_{reverse} + P_{switching} \tag{16}$$

The conduction loss, the reverse leakage loss, and the switching loss are calculated using the following equations.

$$P_{conduction} = I_f.V_f.D \tag{17}$$

$$P_{reverse} = I_r.V_r.(1-D) \tag{18}$$

$$P_{switching} = \frac{T_{rr}.I_{rrm}.V_r.F_{sw}}{2} \tag{19}$$

TABLE 9. Different power losses in diode.

$P_{conduction}$	650 mW
$P_{reverse}$	$0.0015W$
$P_{switching}$	$0.00516W$
P_{loss}	656.66 mW

TABLE 10. Modified CHB loss calculation.

Level	Diode Conduction	MOSFET Conduction	Per Cycle Conduction (%)	Losses (mW)
+V	1	2	16	106.97
-V	1	2	16	106.97
+2V	0	3	34	6.1057
-2V	0	3	34	6.1057
Total Losses				226.1514

TABLE 11. CHB loss calculation.

Level	Diode Conduction	MOSFET Conduction	Per Cycle Conduction (%)	Losses (mW)
+V	0	4	16	3.831
-V	0	4	16	3.831
+2V	0	4	34	8.141
-2V	0	4	34	8.141
Total Losses				23.944

The different symbols used in equation (16), (17), (18), (19), their corresponding names, and values are presented in Table 8.

The power losses occurring in each diode are presented in Table 9

Now the total loss calculation for CHB and modified CHB are presented in Table 10 and Table 11, respectively.

VII. RESULTS AND DISCUSSIONS

From the MATLAB simulations, the effectiveness of filters to improve the inverter output quality by reducing THD has become obvious. The LC filter used in this work has managed to reduce THD by as much as 13.75% for a switching frequency of 2 kHz generated from PWM. The output obtained from the hardware clearly resembles the simulation results. The primary reason of the little irregularities appeared is the switching losses of the transistors. Also, the source voltage has not been constant all the time. Harmonics are generated due to the switching frequency, and to reduce that, filter is introduced. But as the harmonics contain a portion of signal

TABLE 12. Comparison between CHB and modified CHB inverters.

Subject	CHB	Modified CHB
Implementation Complexity	Mild	Moderate
Gate Drive Complexity	Mild	Moderate
Filter Requirement	Mild	Mild
Conduction Loss	Mild	Moderate
Efficiency	Moderate	Mild
Gate Drive Cost	Mild	Moderate
Total Switch for 5 Level	8	6
Switching Device Cost	Moderate	Mild
THD	Mild	Moderate
Nonlinearity	Mild	Moderate

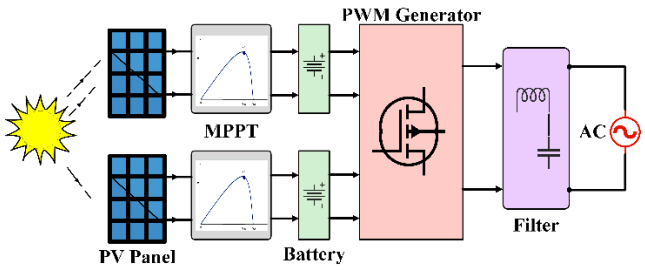


FIGURE 37. Application of the proposed 5-level inverter in grid-connected photovoltaic systems. The two PV panels store their outputs at the batteries, which act as the isolated DC sources. The DC power is converted to AC for the grid through the inverter system comprised of the power electronics switches, PWM generator, and the LC filter.

power, the quality of the signal degrades due to the filtering of harmonic content. A filter also offers some attenuation at some specific frequency. Due to this attenuation, the fundamental voltage magnitude degrades. In hardware, a resistive load is used for simplicity. Deviation of the output will be much higher if inductive or capacitive loads are used. For this hardware implementation, the values for the filter components cannot be changed unlike the simulation. Therefore, the same filter is used for all the hardware implementations. The simulations also show decrease in THD with increased switching frequency, and 6 kHz is identified as the optimum frequency for switching. However, in hardware, switching frequency up to 5 kHz is attained. The hardware results shown in Table 5 also conforms to the fact that THD decreases significantly for increase in the switching frequency. To summarize the contrast between the general and the modified CHB inverters, Table 7 is presented below:

An application of the proposed modified 5-level CHB inverter is shown in Fig. 37. Here, the two PV panels serve as the isolated DC sources required for CHB inverter operation. Their generation is controlled by a maximum power point tracking (MPPT) system, and the electrical energy generated is stored in batteries. Using these batteries as isolated DC sources, the inverter system – which is comprised of the power electronics switches, PWM generator, and the LC filter – supplies AC power to the grid.

VIII. CONCLUSION

In this work, a single phase modified 5-level symmetric cascaded multilevel H-bridge (CHB) inverter with 6 switches has been presented. This reduction in switches has reduced the cost, complexity, area requirement, and losses, while improving efficiency. The CHB architecture has been chosen over other designs because of its unique advantages. These benefits of CHB- namely, the optimum number of levels in the CHB, and the optimum switching frequency – have been investigated thoroughly. A 7-level CHB with 6 kHz switching frequency has appeared as the best performing system in this study. However, this performance has been achieved for unfiltered outputs. In this paper, an LC filter has been used to reduce THD in the output significantly. When this filter is used, both 5-level and 7-level CHBs have demonstrated almost equal THD levels. Thus the less complex, and hence more practical, 5-level design has been chosen. Also, advanced PWM techniques have been investigated to determine their effectiveness in reducing the THD, and level shifted in-phase disposition PWM technique has been selected to be used in the proposed system as it has provided the best performance. Because of the use of PWM switching, the switching frequency has also been much higher than 7 kHz – which has increased the switching losses, but the resulting reduction in THD has immensely improved the inverter performance. As a result, the increased switching losses can be safely neglected. After obtaining satisfactory simulation results in MATLAB/Simulink, this system has been designed and tested in Proteus for hardware implementation, and then implemented in hardware using MOSFETs and ATmega microcontrollers. The hardware outputs have deviated a bit from the simulation results, and the use of transformers to aid in measurement has been identified as the reason. A use-case of the proposed inverter has also been presented. Future expansion of this work can focus on applying this design in real-life standalone and/or grid-connected PV system.

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